HY11P32
Datasheet
8-Bit RISC-Like Mixed Signal Microcontroller
Embedded 4x12 LCD Driver
18-Bit ΣΔADC

Table of Content

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1. Features

- 8-bit RISC, 46 instructions included.
- Operating voltage range: 2.2V to 3.6V, operation temperature range: -40℃~85℃.
- External Crystal Oscillator and Internal High Precision RC Oscillator, 6 CPU clock rates enable users to have the most power-saving plan.
  - Active Mode 300uA@2MHz
  - Standby Mode 3uA@28KHz
  - Sleep Mode 1uA
- 2K Word OTP (One Time Programmable) Type Program Memory, 128 Byte Data Memory
- Brownout detector and Watch dog Timer, prevents CPU from Crash.
- 18-bit fully differential input Sigma-Delta Analog-to-Digital Converter (A/D)
  - Built-in PGA (Programmable Gain Amplifier) 1/4x、1/2x、1x. …128x，10 input signal gain selection.
  - Built-in Input zero point adjustment can increase measurement range according to different application.
- 1.0V internal analog circuit common ground that equips with Push-Pull drive ability to provide sensor driving voltage.
- LVD low voltage detection function has 14 steps of voltage detection configuration and external input voltage detection function.
- Analog voltage source, VDDA equips with 10mA low dropout regulator function
- 4x12 LCD Driver
  - 1/4 Duty, 1/3 Bias
  - Built-in Charge Pump regulated circuit, providing 4 LCD Bias voltage
- 8-bit Timer A
- Built-in EPROM (BIE)
- Support 6 stack level

.

2. Pin Definition

2.1 PIN Diagram LQFP44

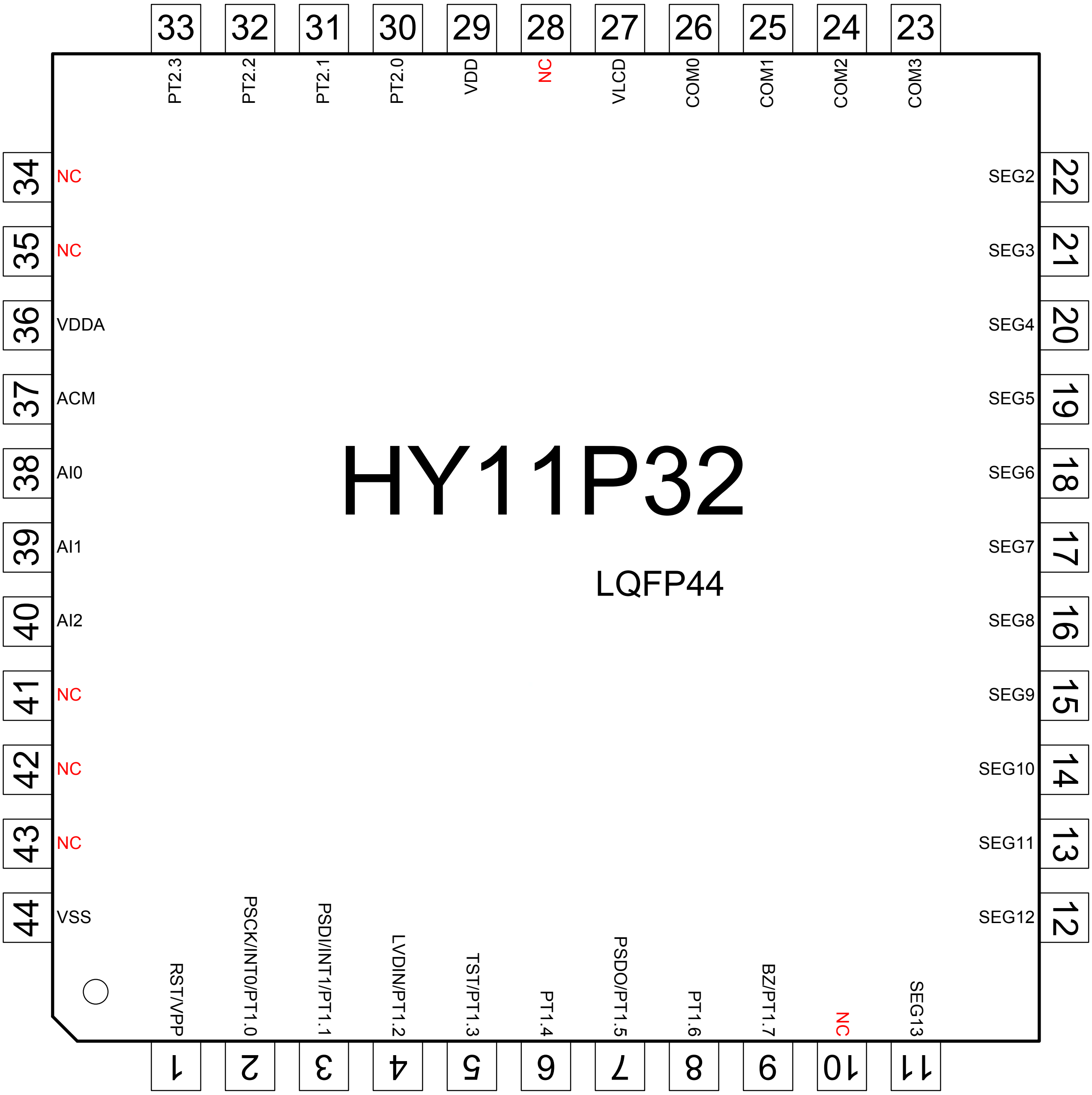


Figure 2-1 HY11P32 LQFP44 Pin Diagram

Note 1：VPP and RST use the same pin. Input voltage cannot exceed 5.8V when not programming EPROM.

Note 2：TST and PT1.3 use the same pin. Input voltage cannot exceed Vdd+0.3V while operating.

Note 3：If PT1.3 is not configured as external pin button, it can help to enhance the anti-interference ability.

2.2 PIN Diagram LQFP48

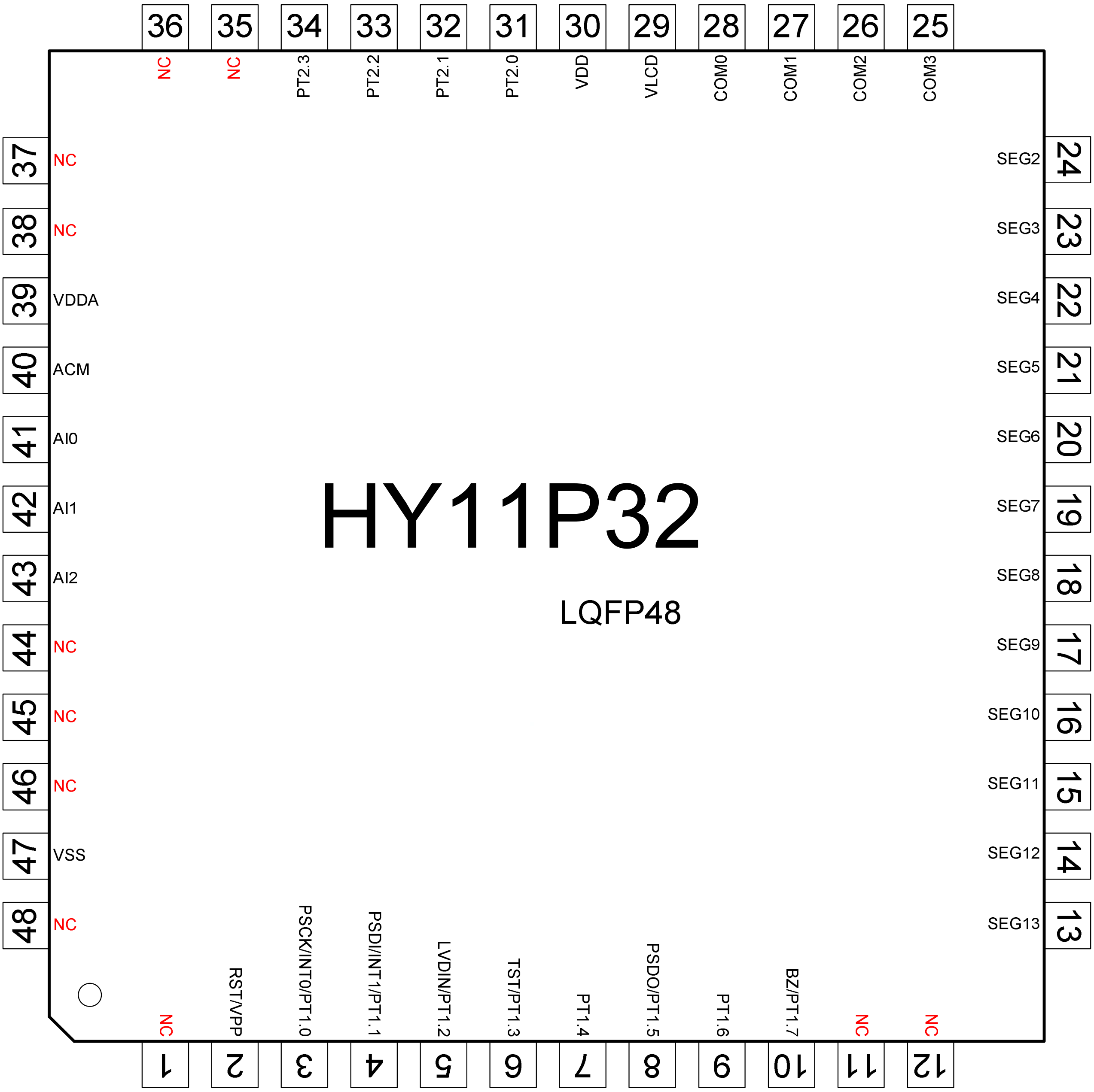


Figure 2-1 HY11P32 LQFP48 Pin Diagram

Note 1：VPP and RST use the same pin. Input voltage cannot exceed 5.8V when not programming EPROM.

Note 2：TST and PT1.3 use the same pin. Input voltage cannot exceed Vdd+0.3V while operating.

Note 3：If PT1.3 is not configured as external pin button, it can help to enhance the anti-interference ability.

2.3 LQFP44 Pinout I/O Description

"I/O" input/output, "I" input, "O" output, "S" Smith Trigger, "C" CMOS features compatible input/output, "P" power supply, "A" analog channel

NO.	Pin Name	Pin Characteristic		Description
		Pin Type	Buffer Type	
1	RST/VPP			
	RST	I	S	Reset IC
	VPP	P	P	EPROM programming voltage input
2	PT1.0/INT0/PSCK			
	PT1.0	I	S	Digital input
	INT0	I	S	Interrupt input INT0
	PSCK	I	S	OTP programming interface SCK
3	PT1.1/INT1/PSDI			
	PT1.1	I	S	Digital input
	INT1	I	S	Interrupt input INT0
	PSDI	I	S	OTP programming interface SDI
4	PT1.2/LVDIN			
	PT1.2	I	S	Digital input
	LVDIN	A	A	LVD external signal input pin
5	PT1.3/TST			
	PT1.3	I	S	Digital input
	TST	I	S	Test Mode input pin (invalid)
6	PT1.4	I/O	S	Digital I/O
7	PT1.5/PSDO			
	PT1.5	I/O	S	Digital I/O
	PSDO	O	C	OTP programming interface SDO
8	PT1.6	I/O	S	Digital I/O
9	PT1.7/BZ			
	PT1.7	I/O	S	Digital I/O
	BZ	O	C	Buzzer output
10	NC	-	-	Unused
11	SEG13	O	A	Segment output for LCD
12	SEG12	O	A	Segment output for LCD
13	SEG11	O	A	Segment output for LCD
14	SEG10	O	A	Segment output for LCD
15	SEG9	O	A	Segment output for LCD
16	SEG8	O	A	Segment output for LCD

17	SEG7	O	A	Segment output for LCD
18	SEG6	O	A	Segment output for LCD
19	SEG5	O	A	Segment output for LCD
20	SEG4	O	A	Segment output for LCD
21	SEG3	O	A	Segment output for LCD
22	SEG2	O	A	Segment output for LCD
23	COM3	O	A	COM segment output for LDO
24	COM2	O	A	COM segment output for LDO
25	COM1	O	A	COM segment output for LDO
26	COM0	O	A	COM segment output for LDO
27	VLCD	P	P	Power supply for LCD
28	NC	-	-	Unused
29	VDD	P	P	Power supply for IC operation
30	PT2.0	I/O	S	Digital I/O
31	PT2.1	I/O	S	Digital I/O
32	PT2.2	I/O	C	Digital I/O
33	PT2.3	I/O	S	Digital I/O
34	NC	-	-	Unused
35	NC	-	-	Unused
36	VDDA	P	P	Regulator output, analog circuit voltage source
37	ACM	P	P	Internal analog circuit common ground pin
38	AI0	A	A	Analog input channel
39	AI1	A	A	Analog input channel
40	AI2	A	A	Analog input channel
41	NC	-	-	Unused
42	NC	-	-	Unused
43	NC	-	-	Unused
44	VSS	P	P	Grounding pin for IC operation voltage

Table 2-1 Pin Definition and Function Description

3. Application Circuit

3.1 Bridge Sensor I

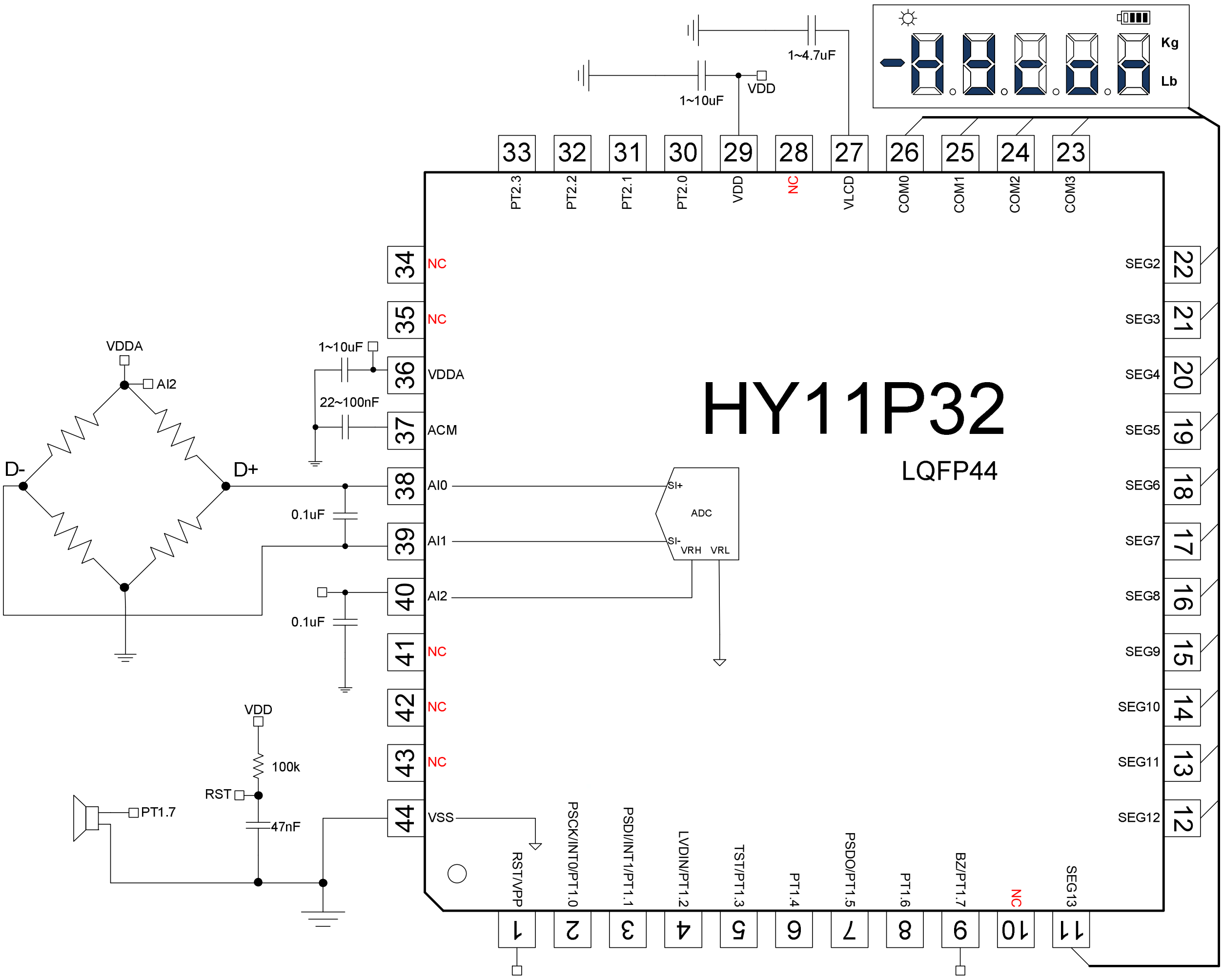


Figure 3-1 Bridge Sensor Application Circuit

Note 1：DCSET[2:0] can conduct bias adjustment of Load Cell zero point voltage address

4. Function Outline

4.1 Internal Block Diagram

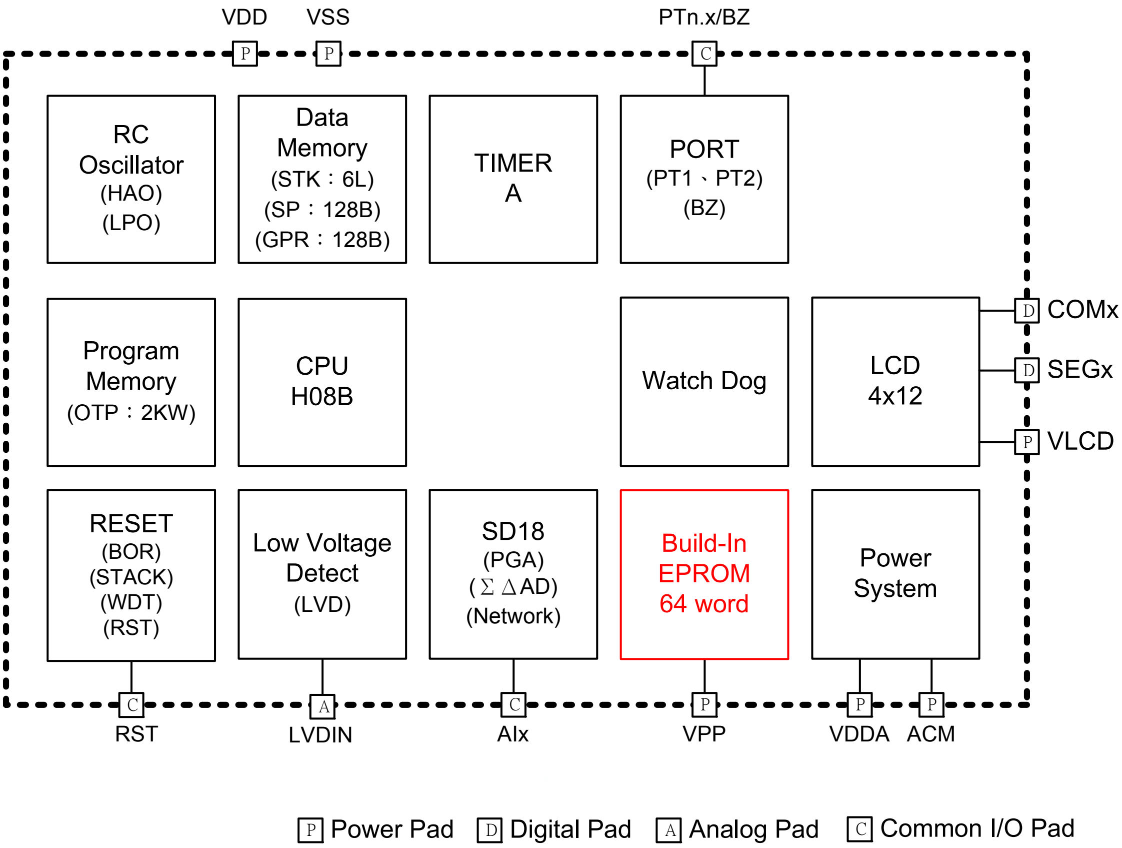


Figure 4-1 HY11P32 Internal Block Diagram

4.2 Related Description and Supporting Documents

IC Function Related Operating Instruction

DS-HY11P32-Vxx	HY11P32 Datasheet
UG-HY11S14-Vxx	HY11Pxx Series Users' Manual
APD-CORE003-Vxx	H08B Instruction Description

Development Tool Related Operating Instruction

APD-HYIDE006-Vxx	HY11xxx Series Development Tool Software Instruction Manual
APD-HYIDE005-Vxx	HY11xxx Series Development Tool Hardware Instruction Manual
APD-OTP001-Vxx	OTP Products Programming Pin Manual
	Product Production Related Operating Instruction
APD-HYIDE004-Vxx	HY1xxxx Series Production Line Specialized Programmer Manual
BDI-HY11P32-Vxx	HY11P32 Individual Product Die Bonding Information

4.3 SD18 Network

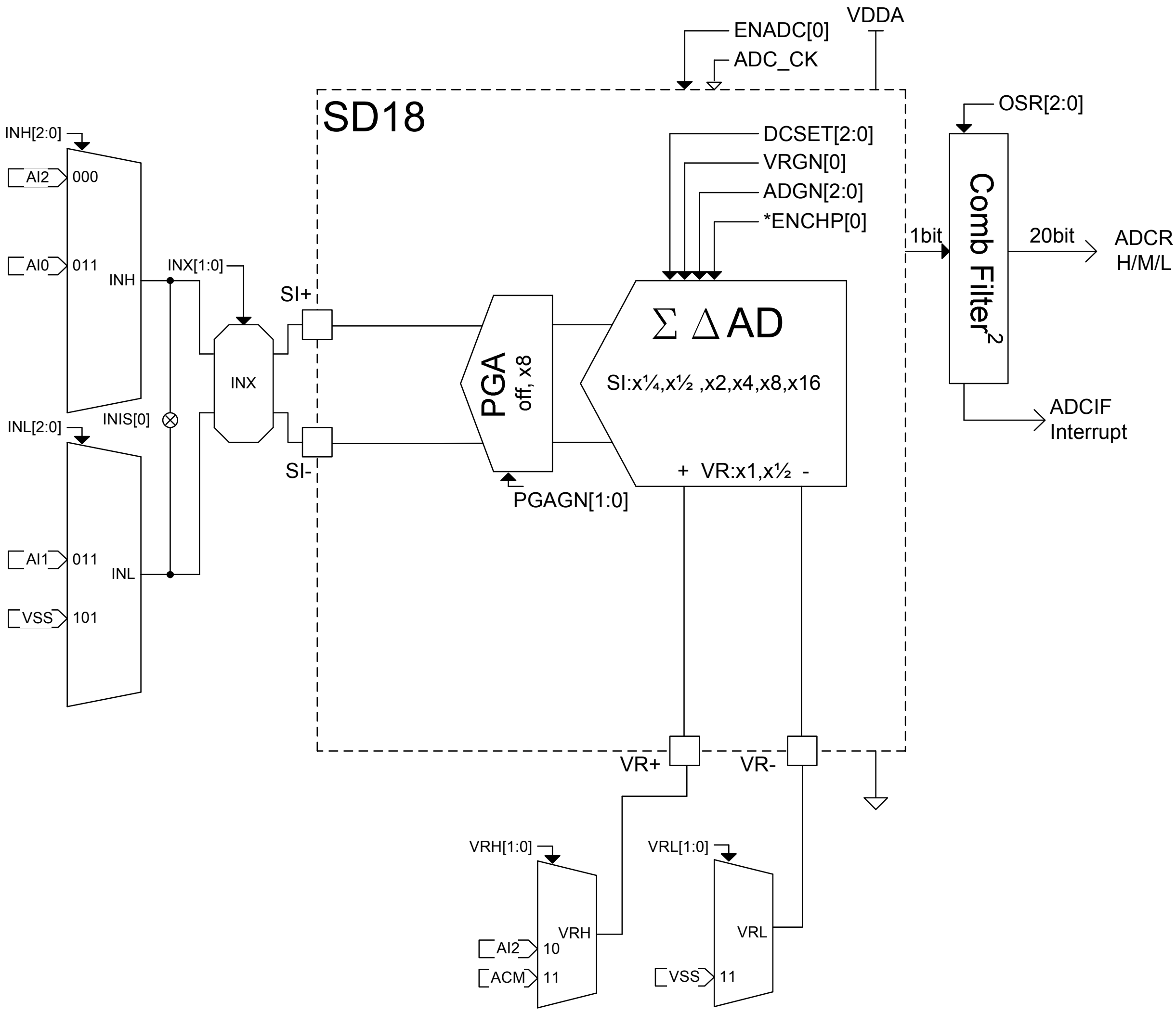


Figure 4-2 SD18 Network

5. Register List

Register File Summary for H08B

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1
"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	File Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A-RESET	i-RESET	R/W
00H	INDF0	Contents of FSR0 to address data memory -value of FSR0 not changed								N/A	N/A	*,*,*,*,*,*,*,*
10H	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18H	STKPTR	STKFL	STKUN	STKOV			STKPRT[2:0]			000. .000	000. .000	r,rw0,rw0,- -,r,r,r
1AH	PCLATH						PC[10]	PC[9]	PC[8]	.... .000	.... .000	-,-,-,- -,*,*,*
1BH	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	*,*,*,*,*,*,*,*
1CH	BIECTRL					VPP_HIGH		BIEWR	BIERD	1000 d000	1000 d000	-,-,-,- *,r0,*,*
1EH	BIEPTRL	0	0	BIE_ADDR[5:0]						0000 0000	0000 0000	w0,w0,*,*,*,*,*,*
1FH	BIEDH	BIE_DATA[15:8]								xxxx xxxx	xxxx xxxx	*,*,*,*,*,*,*,*
20H	BIEDL	BIE_DATA[7:0]								xxxx xxxx	xxxx xxxx	*,*,*,*,*,*,*,*
23H	INTE1	GIE	ADCIE			TMAIE	WDTIE	E1IE	E0IE	0000 0000	0000 0000	*,*,r0,r0 *,*,*,*
26H	INTF1		ADCIF			TMAIF	WDTIF	E1IF	E0IF	.000 0000	.000 0000	-,*,r0,r0 *,*,*,*
29H	WREG	Working Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
2BH	STATUS				C				Z	xxxx xxxx	xxxx xxxx	-,-,-,* -,-,-,*
2CH	Pstatus	PD	TO	IDLEB	BOR		SKERR			000d xxxx	000d xxxx	rw0,rw0,rw0,rw0 x,x,x,x
2DH	LVDCN		LVDFG	LVD	LVDON	**VLDX[3:0]**				x000 0000	x000 0000	x,*,r,r *,*,*,*
30H	PWRCN	ENVDDA	**VDDAX[1:0]=11**		ENACM					0xx0 xxxx	0xx0 xxxx	*,r,r,* x,x,x,x
31H	MCKCN1	ADCS[2:0]			ADCCK			ENXT=0	ENHAO	0000 0001	0000 0001	*,*,*,* r0,r0,r0,*
32H	MCKCN2			**LSCK=0**	**HSCK=0**	**HSS[1:0]=00**		CPUCK[1:0]		..00 0000	..00 0000	r0,r0,r0,r0 r0,r0,*,*
33H	MCKCN3	LCDS[2:0]				PERCK	BZS[2:0]			000. 0000	000. 0000	*,*,*,r0 *,*,*,*
39H	ADCRH	ADC conversion memory HighByte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3AH	ADCRM	ADC conversion memory Middle Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3BH	ADCRL	ADC conversion memory Low Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r0,r0,r0,r0
3CH	ADCCN1	ENADC		ENCHP	**PGAGN[1:0]=00 or 11**		ADGN[2:0]			0000 0000	0000 0000	*,r0,*,* *,*,*,*
3DH	ADCCN2			INBUF=0	VRBUF=0	VREGN	DCSET[2:0]			0000 0000	0000 0000	r0,r0,r0,r0 *,*,*,*
3EH	ADCCN3	OSR[2:0]								0000 0000	0000 0000	*,*,*,r0 r0,r0,r0,r0
3FH	AINET1	**INH[2:0]=XX0 or XX1(AI2 or AI0)**			**INL[2:0]=0XX or 1XX(AI1 or VSS)**			INIS		xx00 xx0x	xx00 xx0x	x,x,*,* x,x,*,x
40H	AINET2		**VRH[1:0]=X0 or X1(AI2 or ACM)**		INX[1:0]		**VRL[1:0]=11(VSS)**			xx00 0xxx	xx00 0xxx	x,x,*,* *,x,x,x
41H	TMACN	ENTMA	TMACK	TMAS[1:0]		ENWDT	WDTS[2:0]			0000 0000	0000 0000	*,*,*,* w1,*,*,*
42H	TMAR	TimerA data register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
52H	LCDCN1	ENLCD	LCDPR	VLCDX[1:0]		LCDBF	**LCDBI[1:0]=10**			0000 0xxx	0000 0xxx	*,*,*,* *,x,x,x
53H	LCDCN2	LCDBL	**LCDMX[1:0]=11**							0xxx xxxx	0xxx xxxx	*,x,x,x x,x,x,x
54H	LCD0	Segment SEG2@[3:0] and SEG3@[7:4] data register of LCD0								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
55H	LCD1	Segment SEG4@[3:0] and SEG5@[7:4] data register of LCD1								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
56H	LCD2	Segment SEG6@[3:0] and SEG7@[7:4] data register of LCD2								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
57H	LCD3	Segment SEG8@[3:0] and SEG9@[7:4] data register of LCD3								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
58H	LCD4	Segment SEG10@[3:0] and SEG11@[7:4] data register of LCD4								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
59H	LCD5	Segment SEG12@[3:0] and SEG13@[7:4] data register of LCD5								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
6DH	PT1	PT1.7	PT1.6	PT1.5	PT1.4	PT1.3	PT1.2	PT1.1	PT1.0	xxxx xxxx	uuuu uuuu	*,*,*,* r,r,r,r
6EH	TRISC1	TC1.7	TC1.6	TC1.5	TC1.4					0000 0000	0000 0000	*,*,*,* r0,r0,r0,r0
70H	PT1PU	PU1.7	PU1.6	PU1.5	PU1.4	PU1.3	PU1.2	PU1.1	PU1.0	0000 0000	0000 0000	*,*,*,*,*,*,*,*
71H	PT1M1					INTEG1[1:0]		INTEG0[1:0]		0000 0000	0000 0000	r0,r0,r0,r0 *,*,*,*
72H	PT1M2		PM1.7[0]							0000 0000	0000 0000	r0,*,r0,r0 r0,r0,r0,r0
74H	PT2					PT2.3	PT2.2	PT2.1	PT2.0	 xxxx	.... uuuu	x,x,x,x *,*,*,*
75H	TRISC2					TC2.3	TC2.2	TC2.1	TC2.0	 0000	 0000	x,x,x,x *,*,*,*
77H	PT2PU					PU2.3	PU2.2	PU2.1	PU2.0	 0000	 0000	x,x,x,x *,*,*,*
80H ~ FFH		GENERAL PURPOSE REGISTER @ 128Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*

Figure 5-1 HY11P32 Register List

6. Electrical Characteristics

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at V_{DD} to V_{SS} . . . . −0.2 V to 4.0 V

Voltage applied to any pin (see Note 1) . . . . −0.2 V to V_{DD} + 0.3 V

Voltage applied to RST/VPP pin . . . . −0.2 V to 6.9 V

Voltage applied to TST/PT1.3 pin (see Note 1) . . . . −0.2 V to V_{DD} + 1 V

Diode current at any device terminal . . . . ±2 mA

Storage temperature, Tstg: (unprogrammed device) . . . . −55℃ to 150℃

(programmed device) . . . . −40℃ to 85℃

Total power dissipation. 0.5w

Maximum output current sink by any PORT1 to PORT2 I/O pin. 25mA

6.1 Recommended Operating Conditions

T_A = -40℃ ~ 85℃,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{DD}	Supply Voltage	All digital peripherals and CPU	2.2		3.6	V
		Analog peripherals	2.4		3.6	
V_{SS}	Supply Voltage		0		0	

6.2 Internal RC Oscillator

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1	1.6	2.0	2.4	MHz
LPO	Low Power Oscillator frequency	V_{DD} supply voltage be enable LPO	22	28	35	KHz

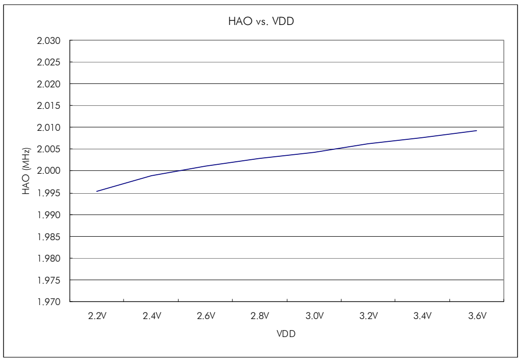


Figure 6.2-1 HAO vs. VDD

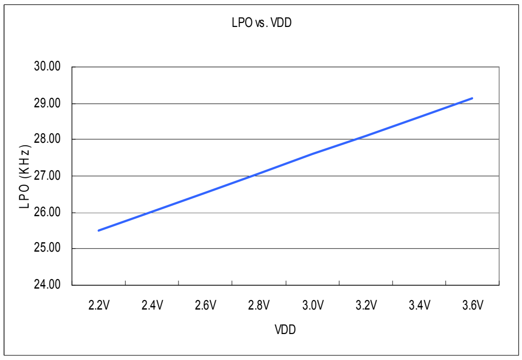


Figure 6.2-2 LPO vs. VDD

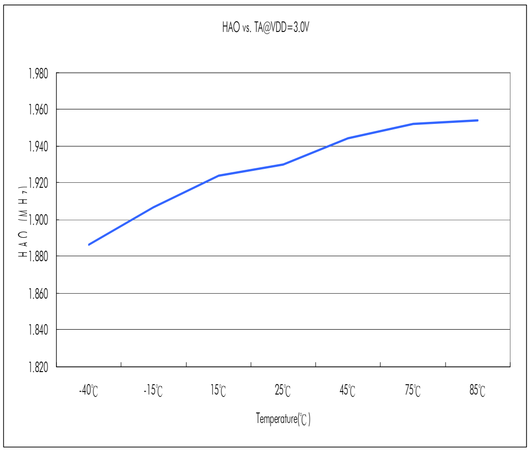


Figure 6.2-3 HAO vs. Temperature

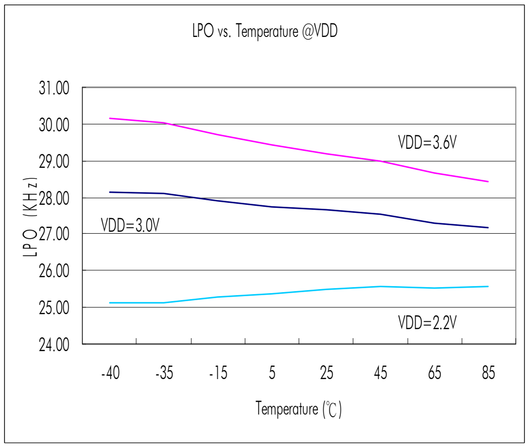


Figure 6.2-4 LPO vs. Temperature

6.3 Supply Current into VDD Excluding Peripherals Current

T_A = 25℃, V_{DD} = 3.0V, OSC_LPO = 28KHz, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 2MHz		0.28	0.55	mA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 1MHz		0.165	0.3	mA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		1.65	3	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.65	1.2	uA

OSC_HAO：Internal High Accuracy Oscillator frequency.

CPU_CK：CPU core work frequency.

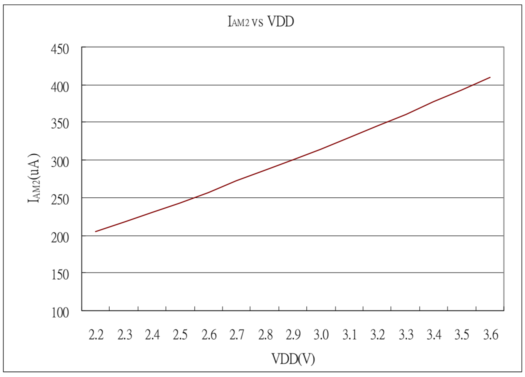


Figure 6.3-1 I_{AM2} vs. VDD

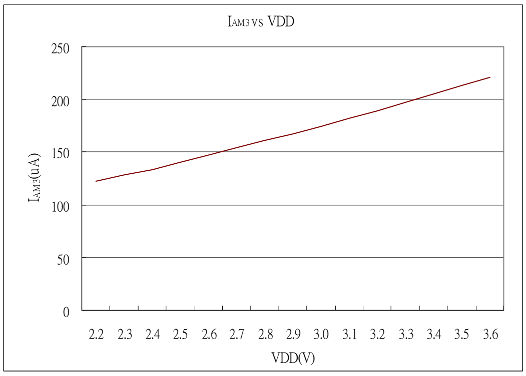


Figure 6.3-2 I_{AM3} vs. VDD

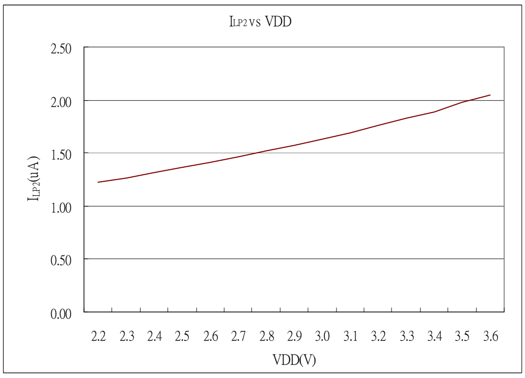


Figure 6.3-3 I_{LP2} vs. VDD

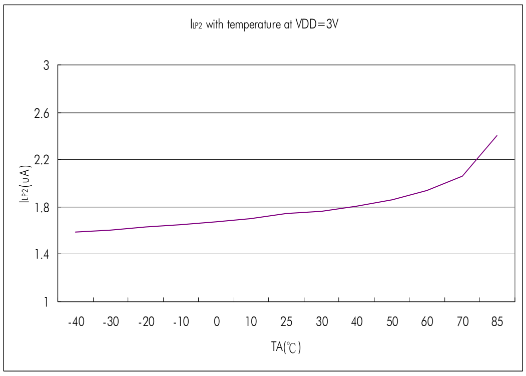


Figure 6.3-4 I_{LP2} vs. Temperature

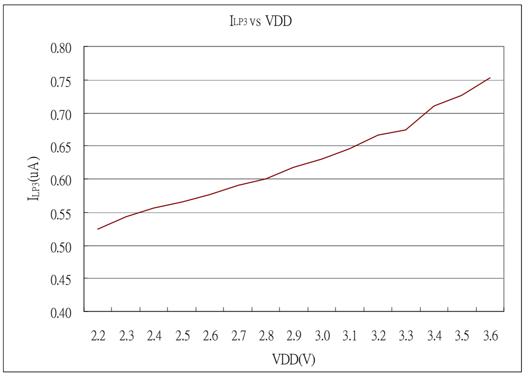


Figure 6.3-5 I_{LP3} vs. VDD

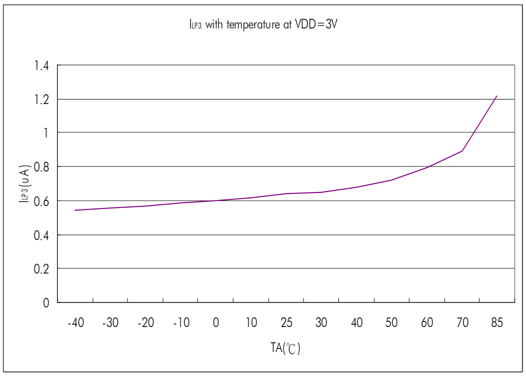


Figure 6.3-6 I_{LP3} vs. Temperature

6.4 Port1~2

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				2.1	V
V_{IL}	Low-Level input voltage		0.9			V
V_{hys}	Input Voltage hysteresis(VIH - VIL)			0.8		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance			180		kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	I_{OH}=10mA	V_{DD} -0.3			V
V_{OL}	Low-level output voltage	I_{OL}=-10mA			VSS +0.3	V

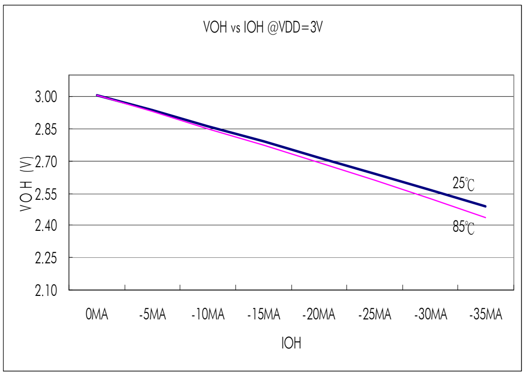


Figure 6.4-1 V_{OH} vs. I_{OH} @VDD=3.0V

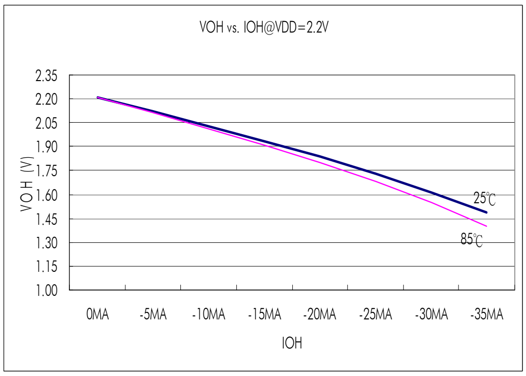


Figure 6.4-2 V_{OH} vs. I_{OH} @VDD=2.2V

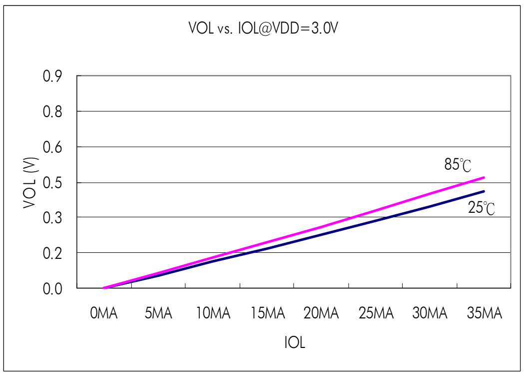


Figure 6.4-3 V_{OL} vs. I_{OL}@VDD=3.0V

Figure 6.4-4 V_{OL} vs. I_{OL}@VDD=2.2V

6.5 Reset (Brownout, External RST pin, Low Voltage Detect)

T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
BOR	Pulse length needed to accepted reset internally, $t_{d\text{-}LVR}$		2			us
	V_{DD} Start Voltage to accepted reset internally (L➔H),V_{LVR}		1.6	1.85	2.1	V
	Hysteresis, $V_{HYS\text{-}LVR}$			70		mV
RST	Pulse length needed as RST/VPP pin to accepted reset internally, $t_{d\text{-}RST}$		2			us
	Input Voltage to accepted reset internally		0.9			V
	Hysteresis, $V_{HYS\text{-}RST}$			0.8		V
LVD	Operation current, I_{LVD}			10	15	uA
	External input voltage to compare reference voltage			1.2		V
	Compare reference voltage temperature drift	T_A = -40℃ ~ 85 ℃		100		ppm/℃
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1110b			3.3		V
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1101b			3.2		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1100b			3.1		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1011b			3.0		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1010b			2.9		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1001b			2.8		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1000b			2.7		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0111b			2.6		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0110b			2.5		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0101b			2.4		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0100b			2.3		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0011b			2.2		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0010b			2.1		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0001b			2.0		

BOR：Brownout Reset

LVR：Low Voltage Reset of BOR

LVD：Low Voltage Detect

RST：External Reset pin

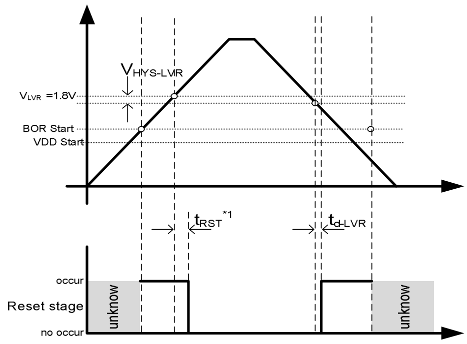


Figure6.5-1 BOR reset diagram

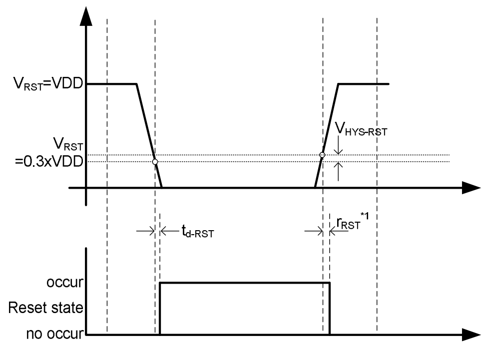


Figure6.5-2 RST reset diagram

[*1] r_{RST} : Please see BOR Introduce of HY11Pxx series User's Guide (UG-HY11S14-Vxx).

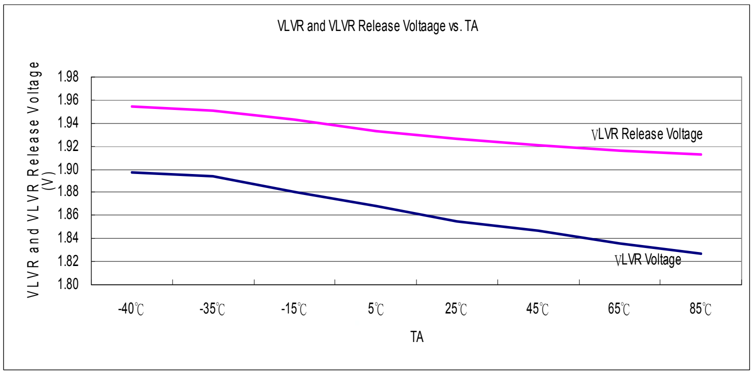


Figure6.5-3 LVR vs. Temperature

6.6 Power System

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
VDDA	VDDA operation current, I_{VDDA}	I_L = 0mA	VDDAX[1:0]=00b		22		uA
	Select VDDA output voltage	I_L = 0.1mA, VDD≧VDDA+0.2V	VDDAX [1:0]=11b		2.4		V
	Dropout voltage	I_L = 10mA	VDDAX [1:0]=11b		180		mV
	Temperature drift	VDDAX [1:0]=11b	T_A=-40℃~85℃		50		ppm/℃
	V_{DD} Voltage drift	I_L = 0.1mA	V_{DD}=2.5V~3.6V		±0.2		%/V
ACM	ACM operation current, I_{ACM}	I_L = 0mA			20		uA
	Output voltage ,V_{ACM}	ENACM[0]=1	I_L = 0uA		1.0		V
	Output voltage with Load		I_L = ±200uA	0.98		1.02	V_{ACM}
	Temperature drift	ENACM[0]=1, I_L = 10uA	T_A=-40℃~85℃		50		ppm/℃
	VDDA Voltage drift				100		uV/V

VDDA：Adjust Voltage Regulator

ACM：Analog Common Mode Voltage

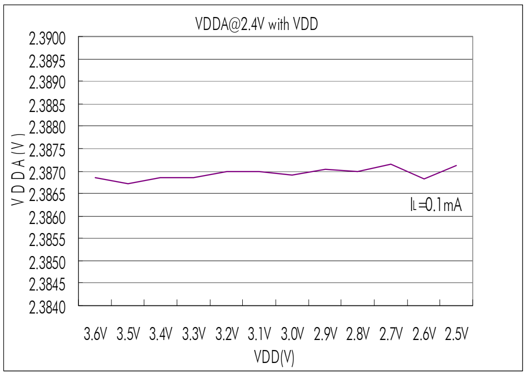


Figure6.6-1 VDDA IL=0.1mA vs. VDD

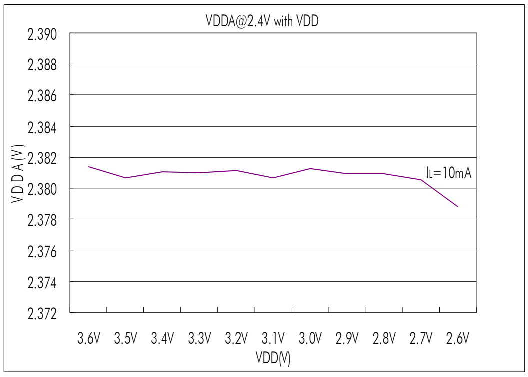


Figure6.6-3 VDDA IL=10mA vs. VDD

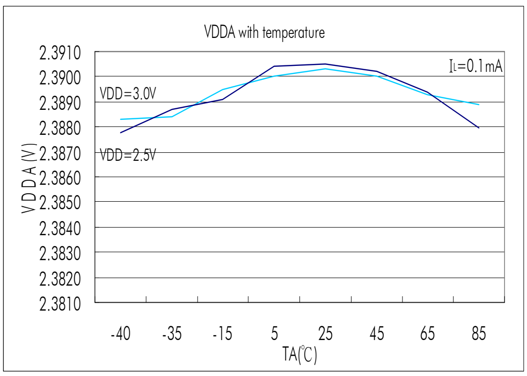


Figure6.6-2 VDDA IL=0.1mA vs. Temperature

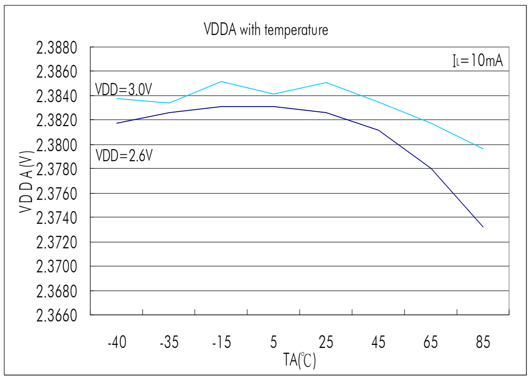


Figure6.6-4 VDDA IL=10mA vs. Temperature

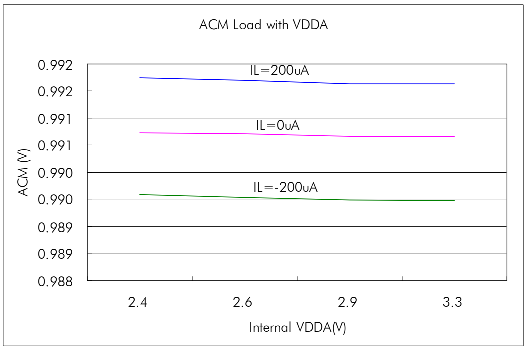


Figure 6.6-5 ACM Load vs. VDDA

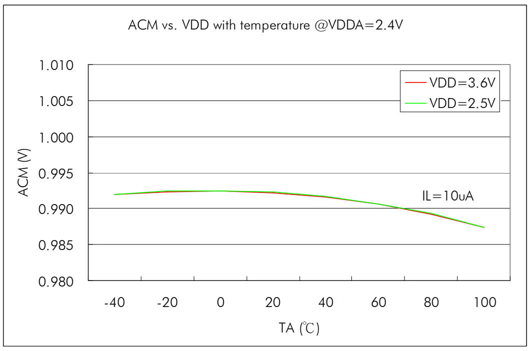


Figure 6.6-6 ACM vs. Temperature

6.7 LCD

T_A = 25℃, V_{DD} = 3.0V, C_{VLCD} =4.7uF,unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
I_{LCD}	Operation supply current without output buffer.(all segment turn on)	LCDPR[0]=1	V_{DD} = 2.2V		20		uA
			V_{DD} = 3.0V				
VLCD	Supply Voltage at VLCD pin	LCDPR[0]=0		2.2		3.6	V
	Embedded Charge Pump output voltage at VLCD pin	V_{DD} = 2.2V, LCDPR[0]=1, C_{VLCD} =4.7uF	VLCDX[1:0]=11b	2.295	2.55	2.805	V
			VLCDX[1:0]=10b	2.52	2.8	3.08	
			VLCDX[1:0]=01b	2.745	3.05	3.355	
			VLCDX[1:0]=00b	2.97	3.3	3.63	
Z_{LCD}	Output impedance with LCD buffer	f_{LCD} =128Hz,VLCD=3.05V			10		kΩ

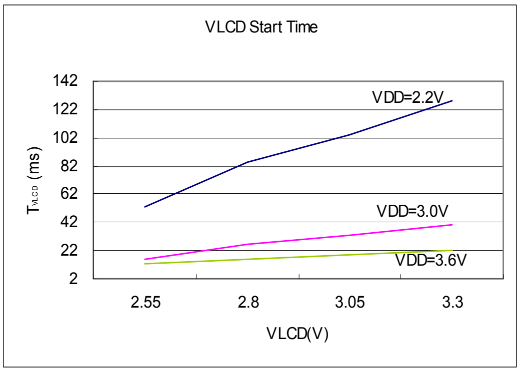


Figure 6.7-1 LCD Start Time

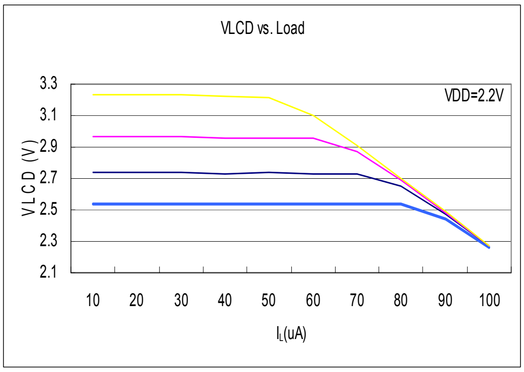


Figure 6.7-2 VLCD vs. I_L @VDD=2.2V

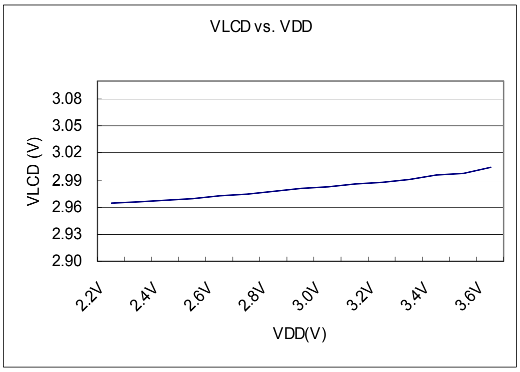


Figure 6.7-3 VLCD vs. VDD

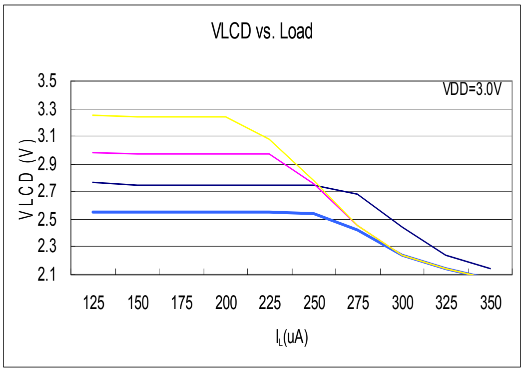


Figure 6.7-4 VLCD vs. I_L @VDD=3.0V

6.8 SD18, Power Supply and Recommended Operating Conditions

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{SD18}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
f_{SD18}	Modulator sample frequency, ADC_CK			25	250	300	KHz
	Over Sample Ratio, OSR			256		32768	
I_{SD18}	Operation supply current without PGA	ENADC[0]=1 INBUF[0]=0,VRBUF[0]=0	GAIN =4, ADC_CK=250KHz		120		uA

6.8.1 PGA, Power Supply and Recommended Operating Conditions

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{PGA}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
I_{PGA}	Operation supply current	PGAGN[1:0]=<11>			320		uA
G_{PGA}	Gain temperature drift	T_A = -40℃~ 85℃	GAIN=128		15		ppm/℃

6.8.2 SD18, PerformanceⅡ(fSD18=250KHz)

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.9V,V_{VR}=1.0V,GAIN=1 without PGA, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
INL	Integral Nonlinearity(INL)	VDDA=2.4V,V_{VR}=1.0V,ΔSI=±200mV VDDA=2.4V,V_{VR}=1.0V,ΔSI=±450mV			±0.003	±0.01	%FSR
	No Missing Codes[3]	ADC_CK=250KHz,OSR[2:0]=010b		19			Bits
G_{SD18}	Temperature drift **Gain 1~x16 (INBUF[0]=0b,)**	INBUF[0]=0b,VRBUF[0]=0b	T_A = -40℃~ 85℃		10		ppm/℃
E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper without PGA	ΔAI=0V ΔVR=0.9V DCSET[2:0]=<000> *ΔAI is external short	Gain=2			1	%FSR
	Offset error temperature drift with chopper without PGA		GAIN=1		2		uV/℃
			GAIN=2		1		uV/℃
			GAIN=4		0.5		uV/℃
			GAIN=16		0.15		uV/℃
CM_{SD18}	Common-mode rejection	V_{CM}=0.7V to 1.7V, V_{VR}=1.0V,without PGA	V_{SI}=0V, GAIN=1		90		dB
		V_{CM}=0.7V to 1.7V, V_{VR}=1.0V, without PGA	V_{SI}=0V, GAIN=16		75		dB

PSRR	DC power supply rejection	VDDA=3.0V,ΔVDDA=±100mV, V_{VR}=1.0V, V_{SI}=1.2V,V_{SI-}=1.2V,	GAIN=1 PGA=off	75	dB
			GAIN=16 PGA=8		

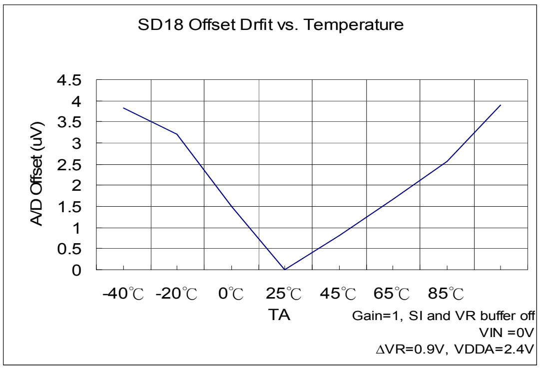


Figure 6.8-1(a) SD18 Offset Temperature Drift

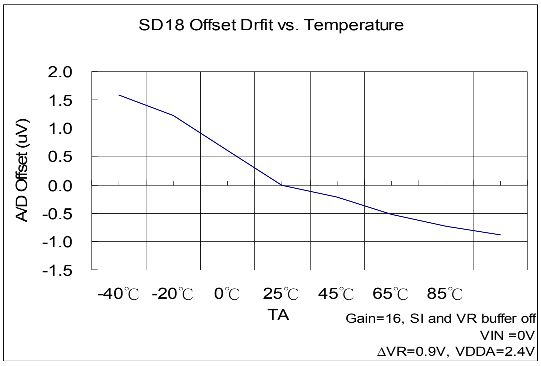


Figure 6.8-1(b) SD18 Offset Temperature Drift

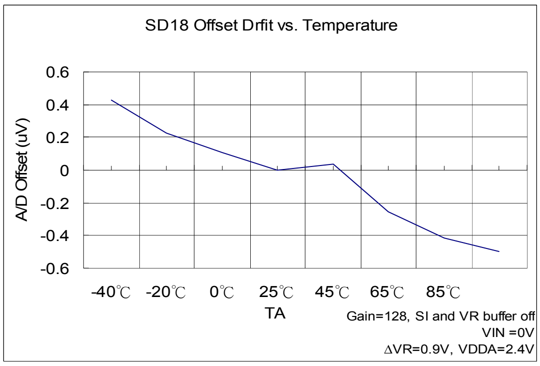


Figure 6.8-1(c) SD18 Offset Temperature Drift

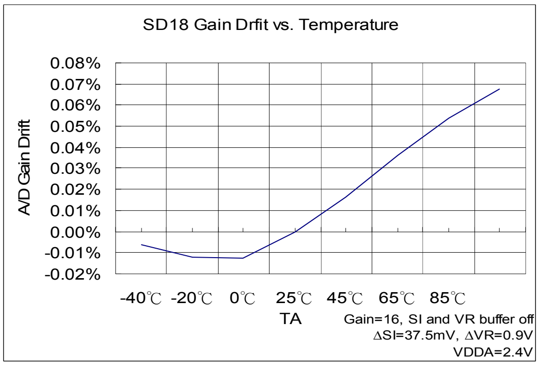


Figure 6.8-2(a) SD18 Gain Drift with Temperature

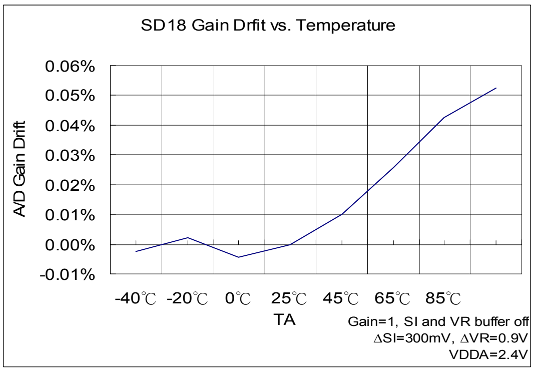


Figure 6.8-2(b) SD18 Gain Drift with Temperature

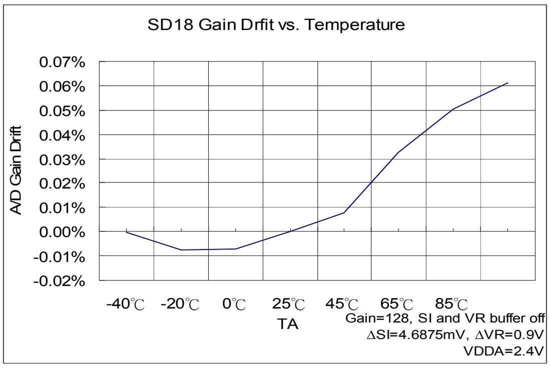


Figure 6.8-2(c) SD18 Gain Drift with Temperature

6.8.3 SD18 Noise Performance

T_A = 25℃, V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

HY11P32 provides important input noise specification that aims at SD18. Table6.8-3(a) and Table6.8-3(b) lists out the relations of typical noise specification, Gain, Output rate, and maximum input voltage of single end. Test condition configuration and external input signal short, voltage reference: 1.2V and 1024 records were sampled.

ENOB(RMS) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V

Max. Vin(mV) =0.9*VREF [1]	OSR					256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					977	488	244	122	61	31	15	8
	Gain	=	PGA	×	ADGN								
±2400	0.25	=	1	×	0.25	16.14	17.41	18.04	18.47	18.80	19.06	19.23	19.31
±2160	0.5	=	1	×	0.5	16.15	17.41	18.03	18.42	18.75	19.13	19.24	19.30
±1080	1	=	1	×	1	16.12	17.35	17.98	18.37	18.74	19.02	19.24	19.34
±540	2	=	1	×	2	16.06	17.18	17.80	18.20	18.64	18.98	19.17	19.32
±270	4	=	1	×	4	15.97	16.97	17.57	17.98	18.44	18.79	19.05	19.20
±135	8	=	1	×	8	15.79	16.66	17.20	17.70	18.16	18.50	18.85	19.10
±68	16	=	1	×	16	15.53	16.30	16.79	17.36	17.79	18.26	18.60	18.87
±8	128	=	8	×	16	13.84	14.35	14.87	15.33	15.85	16.38	16.85	17.28

(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).

Table6.8-3(a) SD18 ENOB Table

RMS Noise(uV) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V

Max. Vin(mV) =0.9*VREF	OSR					256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					977	488	244	122	61	31	15	8
	Gain	=	PGA	×	ADGN								
±2400	0.25	=	1	×	0.25	133.39	55.79	35.80	26.52	21.22	17.56	15.68	14.77
±2160	0.5	=	1	×	0.5	66.41	27.72	18.10	13.82	11.01	8.37	7.75	7.45
±1080	1	=	1	×	1	33.93	14.45	9.32	7.11	5.51	4.53	3.88	3.62
±540	2	=	1	×	2	17.68	8.15	5.28	4.00	2.96	2.32	2.04	1.84
±270	4	=	1	×	4	9.42	4.69	3.10	2.34	1.69	1.32	1.11	1.00
±135	8	=	1	×	8	5.33	2.91	2.00	1.41	1.03	0.81	0.64	0.54
±68	16	=	1	×	16	3.17	1.87	1.33	0.90	0.66	0.48	0.38	0.31
±8	128	=	8	×	16	1.28	0.90	0.63	0.46	0.32	0.22	0.16	0.12

Table6.8-3(b) SD18 RMS Noise Table

The RMS noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$\text{ENOB(RMS)} = \ln\left(\frac{\text{FSR}}{\text{RMS Noise}}\right) \Big/ \ln(2)$$

$$\text{RMS Noise} = \left(2 \times \text{VREF} \times \sqrt{\sum_{k=1}^{1024} (\text{ADO}[k] - \text{Average})^2}\right) \Big/ 2^{23}$$

Where FSR (Full - Scale Range) = 2 × VREF/Gain.

$$\text{Average} = \frac{\sum_{k=1}^{1024} (\text{ADO}[k])}{1024}$$

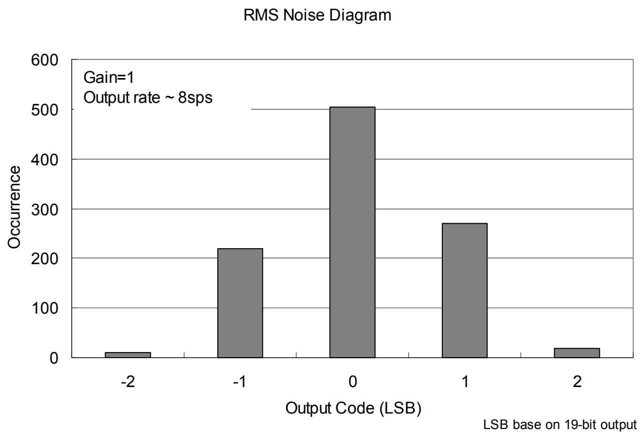


Figure 6.8-3(a) RMS Noise Diagram

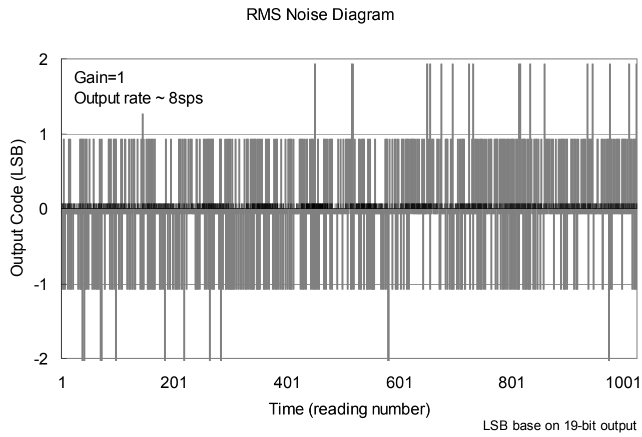


Figure 6.8-3(b) Output Code Diagram

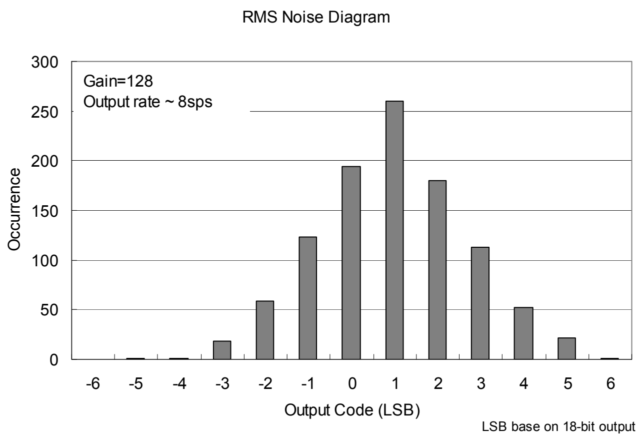


Figure 6.8-3(c) RMS Noise Diagram

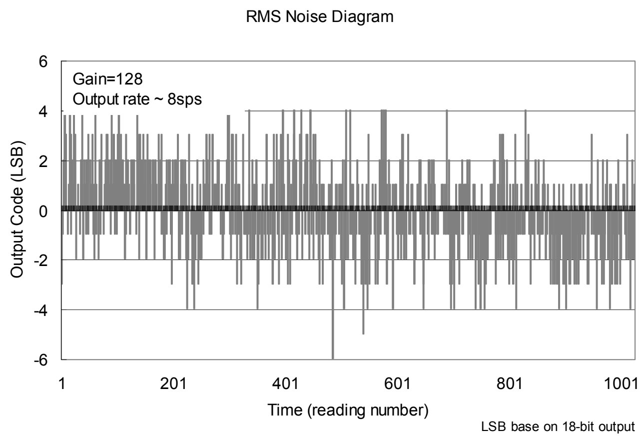


Figure 6.8-3(d) Output Code Diagram

6.9 Built-in EPROM (BIE)

T_A = 25℃, V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{BIE}	Supply Voltage			6.0	6.5	V
I_{BIE}	Operation supply current			5		mA
V_{SS}	Supply Voltage			0		V

7. Ordering Information

Device No.[1]	Package Type	Pins	Package Drawing		Code[2]	Shipment Packing Type	Unit Q'ty	Material Composition	MSL[3]
HY11P32-D000	Die	-	D	000	000	-	250	Green[4]	-
HY11P32-L044	LQFP	44	L	044	000	Tray	160	Green[4]	MSL-3
HY11P32-L048	LQFP	48	L	048	000	Tray	250	Green[4]	MSL-3

[1] **Device No.: Model No. – Package Type Description – Code** (Blank Code/ Standard/ Customized Programming Code)

Ex: Your customized programming code is 008 and you require die shipment.
The device No. will be HY11P32-D000-008.

Ex: You request blank code in die package.
The device No. will be HY11P32-D000.

Ex: You request blank code in LQFP 44 package.
The device No. will be HY11P32-L044.
And please clearly indicate the shipment packing type when placing orders.

Ex: Your customized programming code is 009 and you require products in LQFP 48 package.
The device No. will be HY11P32-L048-009.
And please clearly indicate the shipment packing type when placing orders.

[2] **Code:**

"001"~ "999" is standard or customized programming code. Blank code does not have these numbers.

[3] **MSL:**

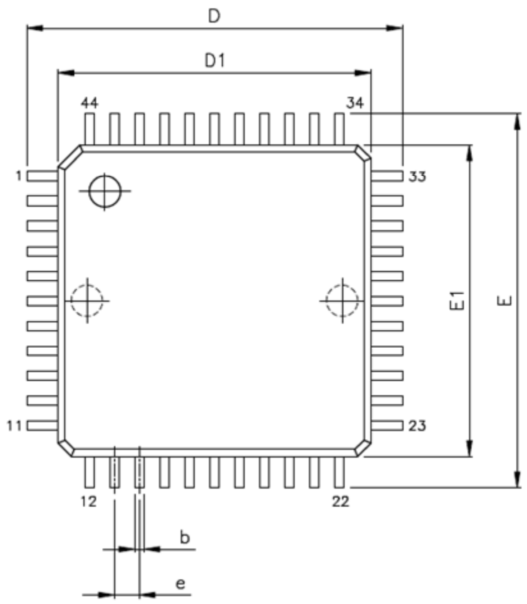
The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

[4] **Green (RoHS & no Cl/Br):**

HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br/Cl<0.1%)

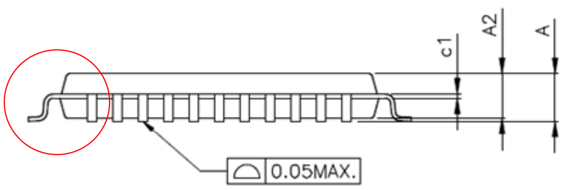
8. Package Information

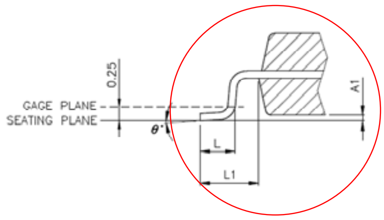
8.1 LQFP44(L044)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

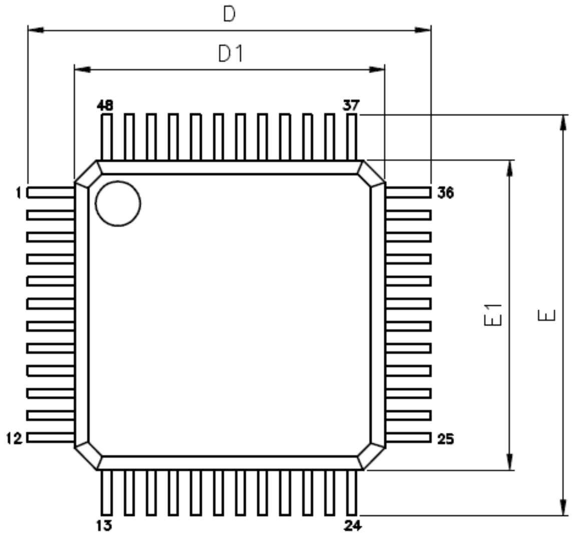
SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
c1	0.09	—	0.16
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.80 BSC		
b	0.30	0.37	0.45
L	0.45	0.60	0.75
L1	1.00 REF		
θ°	0°	3.5°	7°





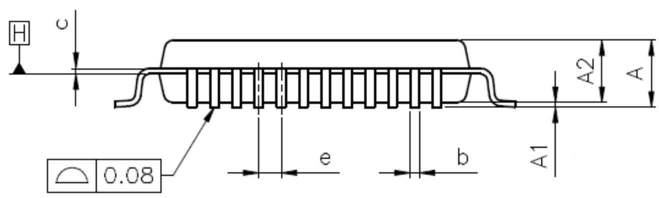
JEDEC MS-026 compliant

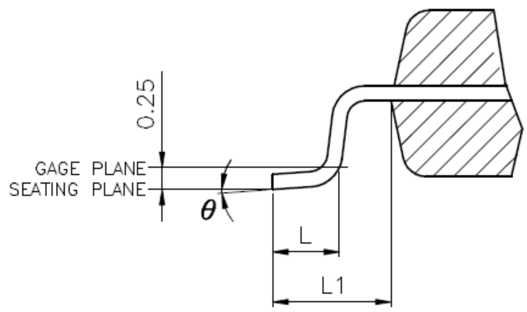
8.2 LQFP48(L048)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°





JEDEC MS-026 compliant

9. Revision Record

Major differences are stated thereinafter:

Version	Page	Revision Summary
V03	ALL	First edition
V08	1	Title Revised
	6	Add in LVDIN function of PT1.2
	7	Add in LVDIN function of PT1.2
	9	Add in LVDIN function of PT1.2
	10	Revise the content of block diagram, WDT reset is 00H
	11	Add in Chapter 4.3 SD18 Network
	12	Revise register list, add in LVDIN function of PT1.2
	14	HAO spec revised, 2MHz±20%
	17	Add in LVDIN function of PT1.2
	23	Revise Figure 6.8 content and order
V12	5	Revise Chapter 1 Features Content
	11	Revise Figure 4.1 and 4.2 Development Tool Related Operating Instruction serial numbers
	14	Revise Chapter 6 Electrical Characteristics Content
	20	Revise Power System Temperature Drift Spec
	25~26	Add in Chapter 6.8.3 SD18 Noise Performance
	28	Chapter 7 Ordering information revision