HY11P12
Datasheet

8-Bit RISC-like Mixed Signal Microcontroller
Embedded 4x12 LCD Driver
18-Bit ΣΔADC

Table of Contents

Attention:

1、 HYCON Technology Corp. reserves the right to change the content of this datasheet without further notice. For most up-to-date information, please constantly visit our website: http://www.hycontek.com .

2、 HYCON Technology Corp. is not responsible for problems caused by figures or application circuits narrated herein whose related industrial properties belong to third parties.

3、 Specifications of any HYCON Technology Corp. products detailed or contained herein stipulate the performance, characteristics, and functions of the specified products in the independent state. We does not guarantee of the performance, characteristics, and functions of the specified products as placed in the customer's products or equipment. Constant and sufficient verification and evaluation is highly advised.

4、 Please note the operating conditions of input voltage, output voltage and load current and ensure the IC internal power consumption does not exceed that of package tolerance. HYCON Technology Corp. assumes no responsibility for equipment failures that resulted from using products at values that exceed, even momentarily, rated values listed in products specifications of HYCON products specified herein.

5、 Notwithstanding this product has built-in ESD protection circuit, please do not exert excessive static electricity to protection circuit.

6、 Products specified or contained herein cannot be employed in applications which require extremely high levels of reliability, such as device or equipment affecting the human body, health/medical equipments, security systems, or any apparatus installed in aircrafts and other vehicles.

7、 Despite the fact that HYCON Technology Corp. endeavors to enhance product quality as well as reliability in every possible way, failure or malfunction of semiconductor products may happen. Hence, users are strongly recommended to comply with safety design including redundancy and fire-precaution equipments to prevent any accidents and fires that may follow.

8、 Use of the information described herein for other purposes and/or reproduction or copying without the permission of HYCON Technology Corp. is strictly prohibited.

1. Features

- 8-bit RISC, 46 instructions included.
- Operating voltage range: 2.0V to 3.6V, operation temperature range: -40℃~85℃.
- External Crystal Oscillator and Internal High Precision RC Oscillator, 6 CPU clock rates enable users to have the most power-saving plan.
  - Active Mode 300uA@2MHz
  - Standby Mode 3uA@28KHz
  - Sleep Mode 1uA
- 2K Word OTP (One Time Programmable) Type program memory, 128 Byte Data Memory.
- Brownout detector and Watch dog Timer, prevents CPU from Crash.
- 18-bit fully differential input Sigma-Delta Analog-to-Digital Converter (A/D)
  - Built-in PGA (Programmable Gain Amplifier) 1/4x、1/2x、1x. …128x，10 input signal gain selection.
  - Built-in Input zero point adjustment can increase measurement range according to different application.
  - Built-in high impedance input buffer (Not suitable for 4x or upwards input gain).
  - Built-in absolute temperature sensor
- 1.0V internal analog circuit common ground that equips with Push-Pull drive ability to provide sensor driving voltage.
- LVD low voltage detection function has 14 steps of voltage detection configuration and external input voltage detection function.
- VDDA can select 4 different output voltage that equips with 10mA low dropout regulator function.
- 4x12 LCD driver
  - Static、1/2、1/3、1/4 Duty and 1/3 Bias Programmable Option.
  - Built-in Charge Pump regulated circuit, providing 4 LCD Bias voltage.
- 8-bit Timer A
- Support 6 stack level

2. Pin Definition

2.1. Pin Diagram LQFP44

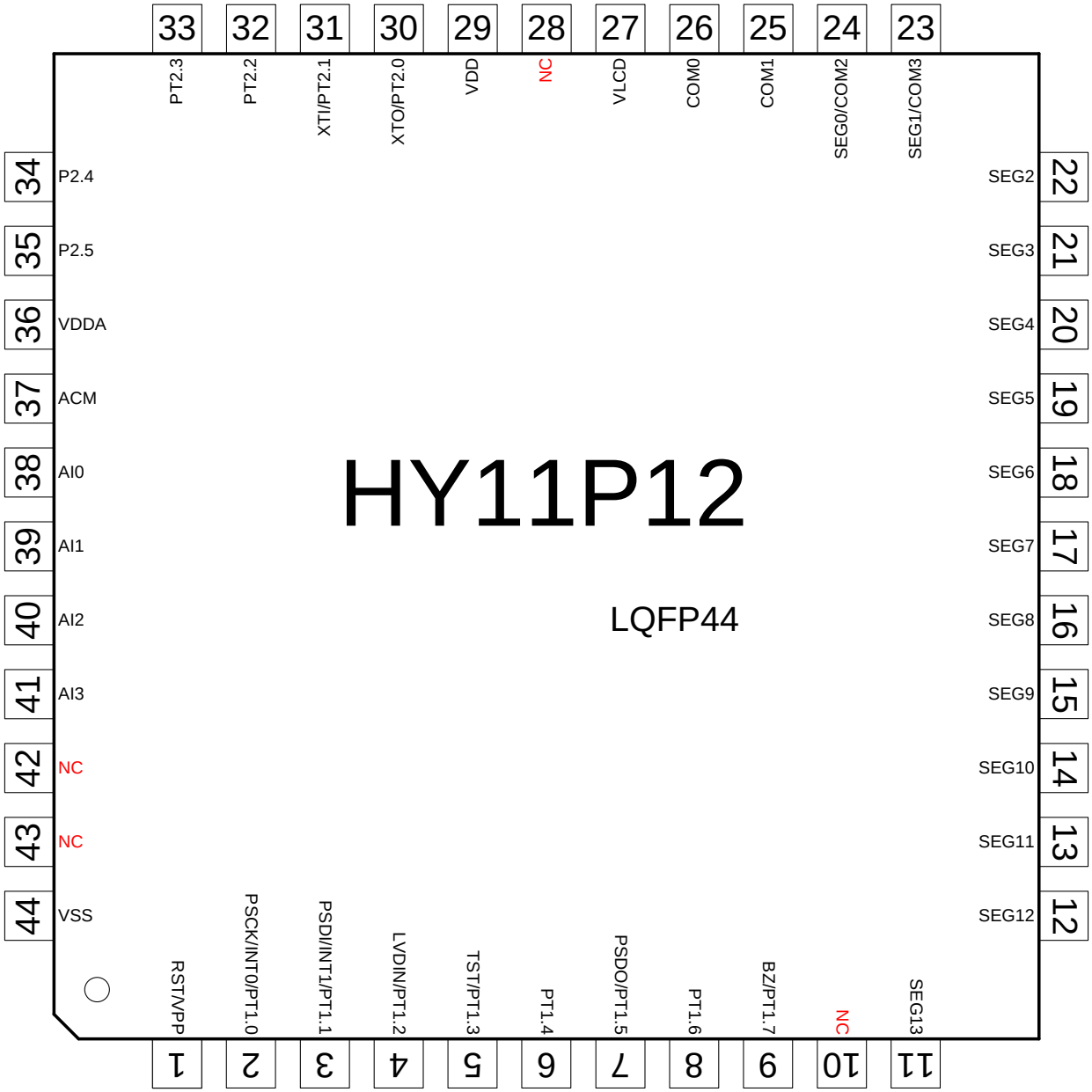


Figure 2-1 HY11P12 LQFP44 Pin Diagram

Note 1：VPP and RST use the same pin. Input voltage cannot exceed 5.8V when not programming EPROM.

Note 2：TST and PT1.3 use the same pin. Input voltage cannot exceed Vdd+0.3V while operating.

Note 3：If PT1.3 is not configured as external pin button, it can help to enhance the anti-interference ability.

2.2. Pin Diagram LQFP48

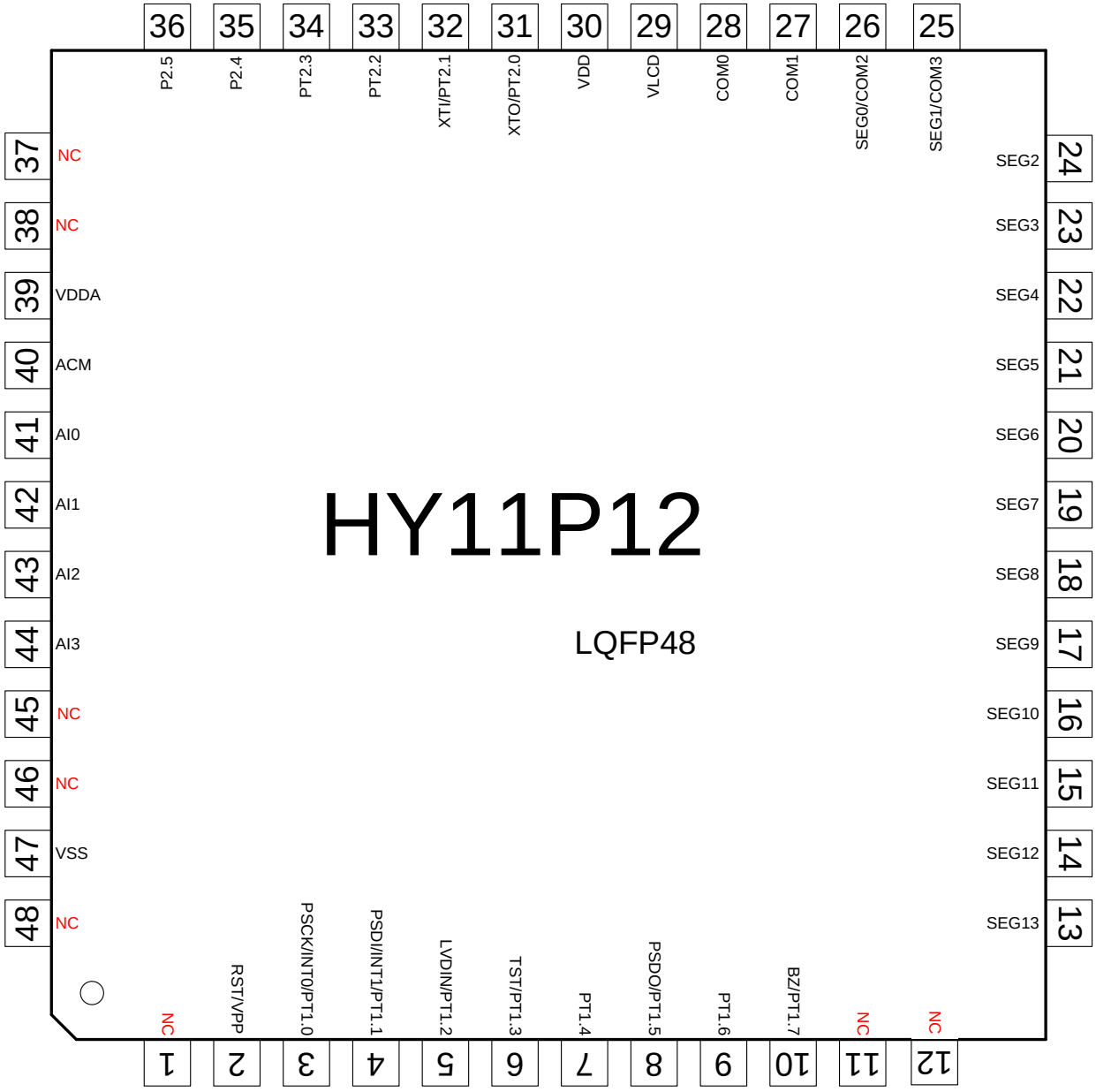


Figure 2-2 HY11P12 LQFP48 Pin Diagram

Note 1：VPP and RST use the same pin. Input voltage cannot exceed 5.8V when not programming EPROM.

Note 2：TST and PT1.3 use the same pin. Input voltage cannot exceed Vdd+0.3V while operating.

Note 3：If PT1.3 is not configured as external pin button, it can help to enhance the anti-interference ability.

2.3. Pin Diagram QFN48

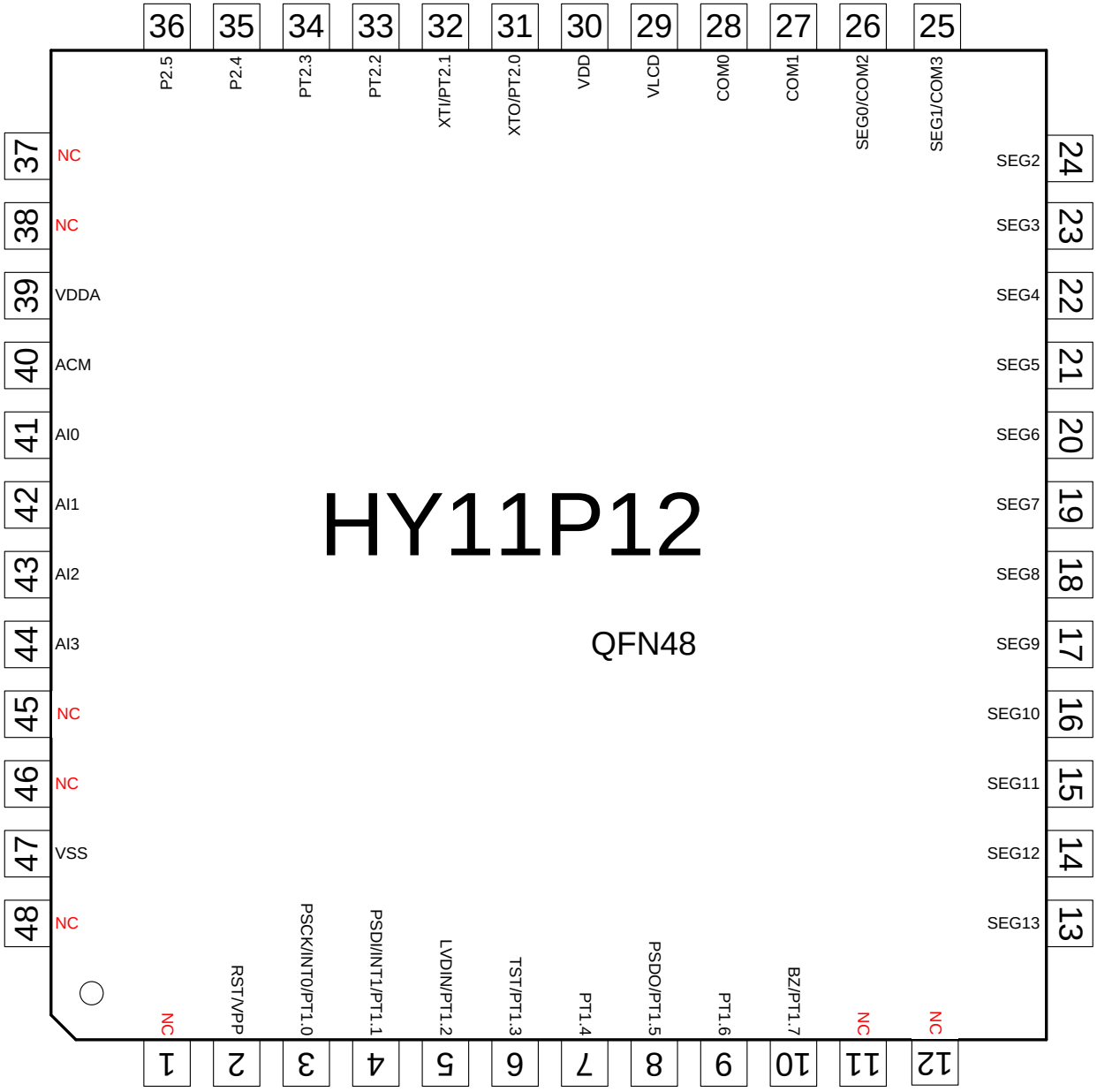


Figure 2-3 HY11P12 QFN48 Pin Diagram

Note 1：VPP and RST use the same pin. Input voltage cannot exceed 5.8V when not programming EPROM.

Note 2：TST and PT1.3 use the same pin. Input voltage cannot exceed Vdd+0.3V while operating.

Note 3：If PT1.3 is not configured as external pin button, it can help to enhance the anti-interference ability.

2.4. LQFP44 Pinout I/O Description

"I/O" input/output, "I" input, "O" output, "S" Smith Trigger, "C" CMOS features compatible input/output, "P" power supply, "A" analog channel

NO.	Pin Name	Pin characteristic		Description
		Pin Type	Buffer Type	
1	RST/VPP			
	RST	I	S	Reset IC
	VPP	P	P	EPROM programming voltage input
2	PT1.0/INT0/PSCK			
	PT1.0	I	S	Digital input
	INT0	I	S	Interrupt input INT0
	PSCK	I	S	OTP programming interface SCK
3	PT1.1/INT1/PSDI			
	PT1.1	I	S	Digital input
	INT1	I	S	Interrupt input INT1
	PSDI	I	S	OTP programming interface SDI
4	PT1.2/LVDIN			
	PT1.2	I	S	Digital input
	LVDIN	A	A	LVD external signal input interface
5	PT1.3/TST			
	PT1.3	I	S	Digital input
	TST	I	S	Test Mode input pin (invalid)
6	PT1.4	I/O	S	Digital output
7	PT1.5/PSDO			
	PT1.5	I/O	S	Digital output
	PSDO	O	C	OTP programming interface SDO
8	PT1.6	I/O	S	Digital input/output
9	PT1.7/BZ			
	PT1.7	I/O	S	Digital I/O
	BZ	O	C	Buzzer output
10	NC	-	-	Unused
11	SEG13	O	A	Segment output for LCD
12	SEG12	O	A	Segment output for LCD
13	SEG11	O	A	Segment output for LCD
14	SEG10	O	A	Segment output for LCD
15	SEG9	O	A	Segment output for LCD

16	SEG8	O	A	Segment output for LCD
17	SEG7	O	A	Segment output for LCD
18	SEG6	O	A	Segment output for LCD
19	SEG5	O	A	Segment output for LCD
20	SEG4	O	A	Segment output for LCD
21	SEG3	O	A	Segment output for LCD
22	SEG2	O	A	Segment output for LCD
23	COM3/SEG1	O	A	COM/segment output for LCD
24	COM2/SEG0	O	A	COM/segment output for LCD
25	COM1	O	A	COM output for LCD
26	COM0	O	A	COM output for LCD
27	VLCD	P	P	Power supply for LCD
28	NC	-	-	Unused
29	VDD	P	P	Power supply for IC operation
30	PT2.0/XTO PT2.0 XTO	 I/O A	 S A	 Digital I/O External oscillator output
31	PT2.1/XTI PT2.1 XTI	 I/O A	 S A	 Digital I/O External oscillator input
32	PT2.2	I/O	C	Digital I/O
33	PT2.3	I/O	S	Digital I/O
34	PT2.4	I/O	S	Digital I/O
35	PT2.5	I/O	S	Digital I/O
36	VDDA	P	P	Regulator output, analog circuit voltage source
37	ACM	P	P	Internal analog circuit common ground pin
38	AI0	A	A	Analog channel pin
39	AI1	A	A	Analog channel pin
40	AI2	A	A	Analog channel pin
41	AI3	A	A	Analog channel pin
42	NC	-	-	Unused
43	NC	-	-	Unused
44	VSS	P	P	Grounding pin for IC operation voltage

Table 2-1 Pin Definition and Function Description

2.5. LQFP48/QFN48 Pinout I/O Description

"I/O" input/output, "I" input, "O" output, "S" Smith Trigger, "C" CMOS features compatible input/output, "P" power supply, "A" analog channel

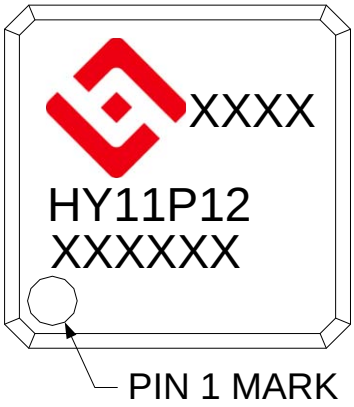
NO.	Pin Name	Pin Characteristic		Description
		Pin Type	Buffer Type	
1	NC	-	-	Unused
2	RST/VPP			
	RST	I	S	Reset IC
	VPP	P	P	EPROM programming voltage input
3	PT1.0/INT0/PSCK			
	PT1.0	I	S	Digital input
	INT0	I	S	Interrupt input INT0
	PSCK	I	S	OTP programming interface SCK
4	PT1.1/INT1/PSDI			
	PT1.1	I	S	Digital input
	INT1	I	S	Interrupt input INT1
	PSDI	I	S	OTP programming interface SDI
5	PT1.2/LVDIN			
	PT1.2	I	S	Digital input
	LVDIN	A	A	LVD external signal input interface
6	PT1.3/TST			
	PT1.3	I	S	Digital input
	TST	I	S	Test Mode input pin (invalid)
7	PT1.4	I/O	S	Digital input/output
8	PT1.5/PSDO			
	PT1.5	I/O	S	Digital I/O
	PSDO	O	C	OTP programming interface SDO
9	PT1.6	I/O	S	Digital input/output
10	PT1.7/BZ			
	PT1.7	I/O	S	Digital I/O
	BZ	O	C	Buzzer output
11	NC	-	-	Unused
12	NC	-	-	Unused
13	SEG13	O	A	Segment output for LCD
14	SEG12	O	A	Segment output for LCD

15	SEG11	O	A	Segment output for LCD
16	SEG10	O	A	Segment output for LCD
17	SEG9	O	A	Segment output for LCD
18	SEG8	O	A	Segment output for LCD
19	SEG7	O	A	Segment output for LCD
20	SEG6	O	A	Segment output for LCD
21	SEG5	O	A	Segment output for LCD
22	SEG4	O	A	Segment output for LCD
23	SEG3	O	A	Segment output for LCD
24	SEG2	O	A	Segment output for LCD
25	COM3/SEG1	O	A	COM/segment output for LCD
26	COM2/SEG0	O	A	COM/segment output for LCD
27	COM1	O	A	COM output for LCD
28	COM0	O	A	COM output for LCD
29	VLCD	P	P	Power supply for LCD
30	VDD	P	P	Power supply for IC operation
31	PT2.0/XTO PT2.0 XTO	 I/O A	 S A	 Digital I/O External oscillator output
32	PT2.1/XTI PT2.1 XTI	 I/O A	 S A	 Digital I/O External oscillator input
33	PT2.2	I/O	C	Digital input/output
34	PT2.3	I/O	S	Digital input/output
35	PT2.4	I/O	S	Digital input/output
36	PT2.5	I/O	S	Digital input/output
37	NC	-	-	Unused
38	NC	-	-	Unused
39	VDDA	P	P	Regulator output, analog circuit voltage source
40	ACM	P	P	Internal analog circuit common ground pin
41	AI0	A	A	Analog channel pin
42	AI1	A	A	Analog channel pin
43	AI2	A	A	Analog channel pin
44	AI3	A	A	Analog channel pin
45	NC	-	-	Unused

46	NC	-	-	Unused
47	VSS	P	P	Grounding pin for IC operation voltage
48	NC	-	-	Unused

Table 2-2 LQFP48/QFN48 Pin Definition and Function Description

2.5.1. LQFP package marker information

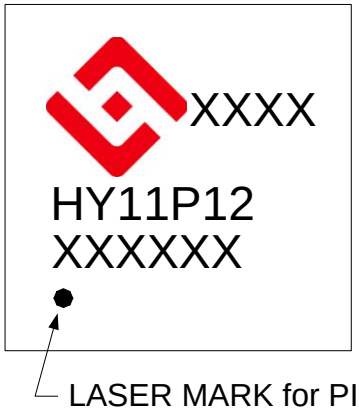


→ HYCON's Logo + Traceability code

→ Product Name : HY11P12

→ Product Lot No.

2.5.2. QFN package marker information



→ HYCON's Logo + Traceability code

→ Product Name : HY11P12

→ Product Lot No.

3. Application Circuit

3.1. Bridge Sensor I

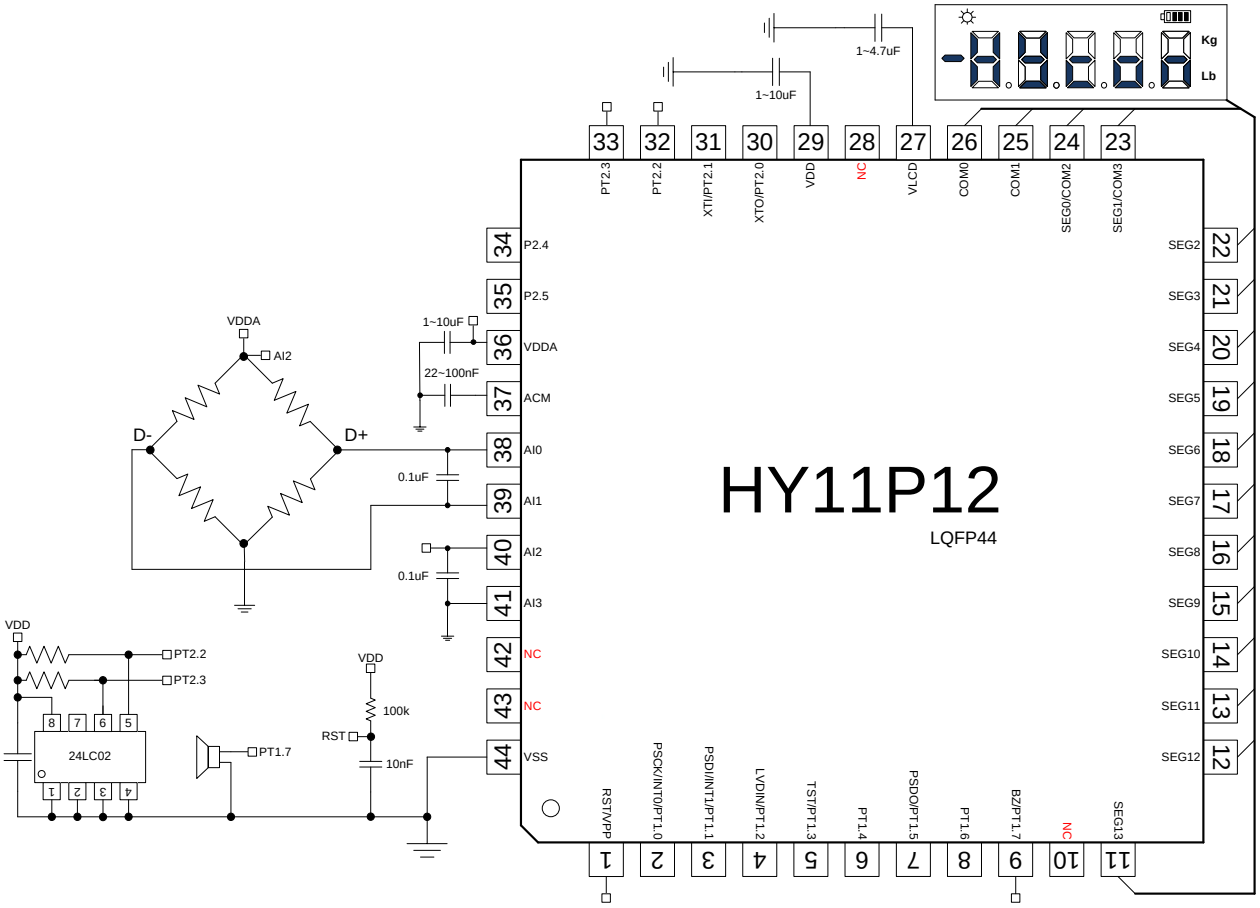


Figure 3-1 Bridge Sensor Application Circuit

Note 1：DCSET[2:0] can conduct bias adjustment of Load Cell zero point voltage address

3.2. Bridge Sensor II

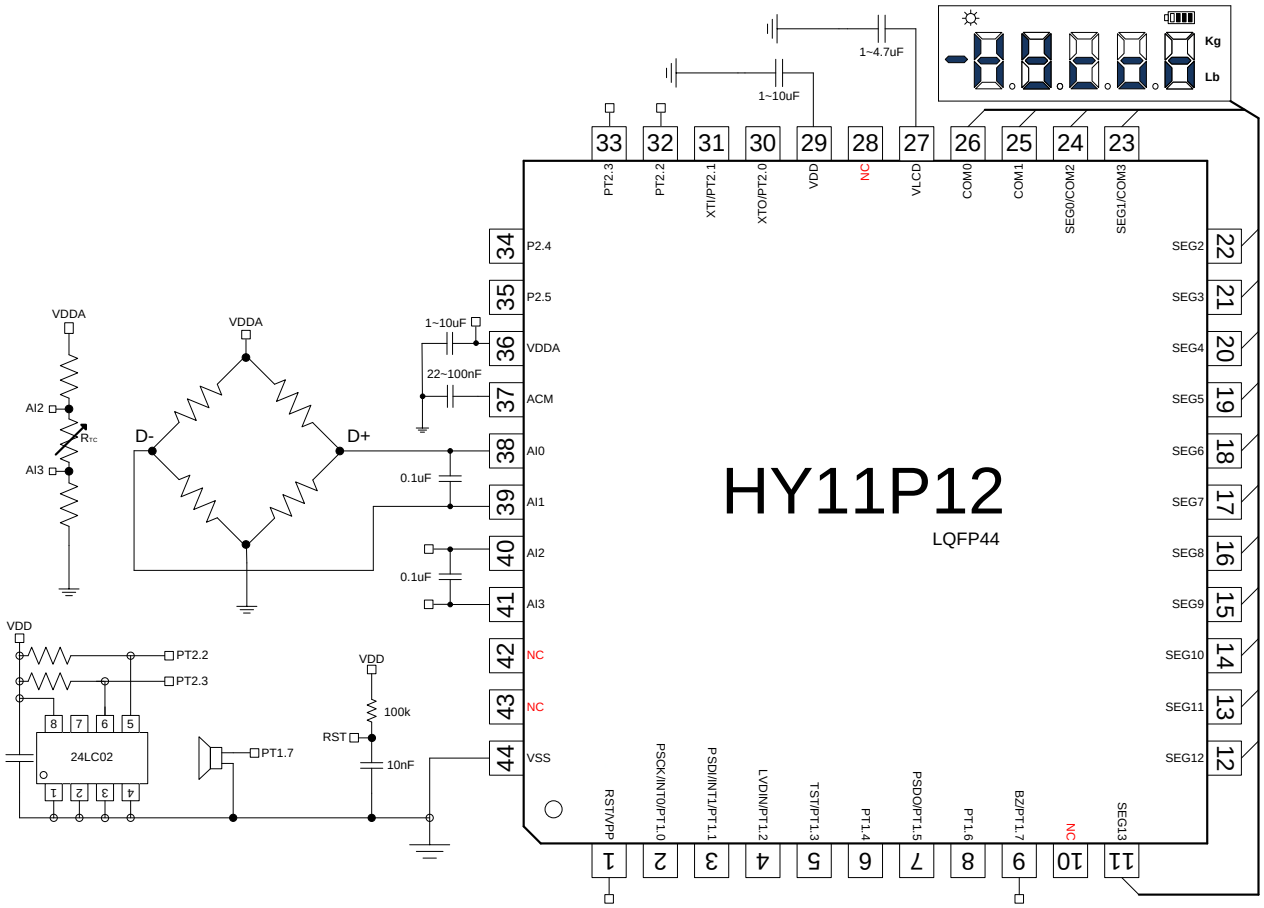


Figure 3-2 Application Circuit of Temperature Compensation Bridge Sensor

Note 1：Using external reference voltage to design temperature compensation resistor NTC basic circuit

Note 2：DCSET [2:0] can conduct bias adjustment of Load Cell zero point voltage address

4. Function Outline

4.1. Internal Block Diagram

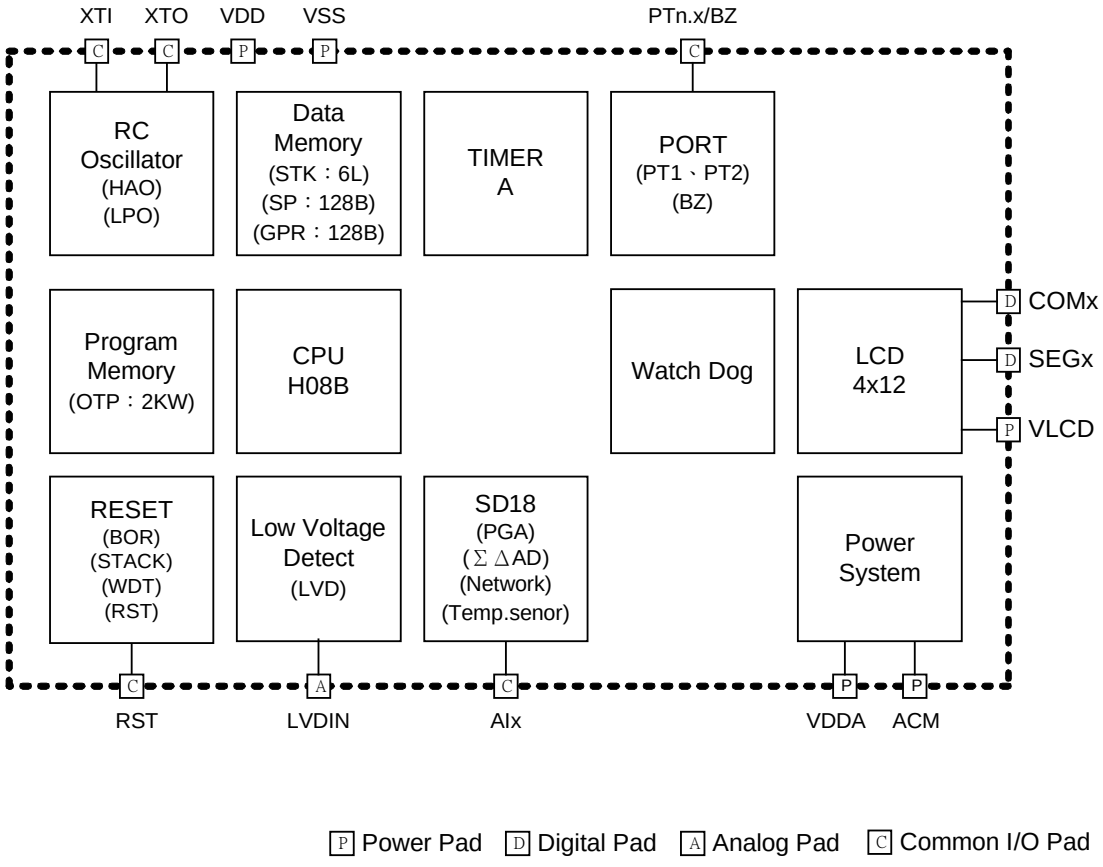


Figure 4-1 HY11P12 Internal Block Diagram

4.2. Related Description and Supporting Documents

IC Function Related Operating Instruction

DS-HY11P12-Vxx	HY11P12 Data Sheet
UG-HY11S14-Vxx	HY11P Series Users' Manual
APD-CORE003-Vxx	H08B Instruction Description

Development Tool Related Operating Instruction

APD-HYIDE006-Vxx	HY11xxx Series Development Tool Software Instruction Manual
APD-HYIDE005-Vxx	HY11xxx Series Development Tool Hardware Instruction Manual
APD-OTP001-Vxx	OTP Products Programming Pin Manual

Product Production Related Operating Instruction

APD-HYIDE004-Vxx	HY1xxxx Series Production Line Specialized Programmer Manual
BDI-HY11P12-Vxx	HY11P12 Individual Product Die Bonding Information

4.3. SD18 Network

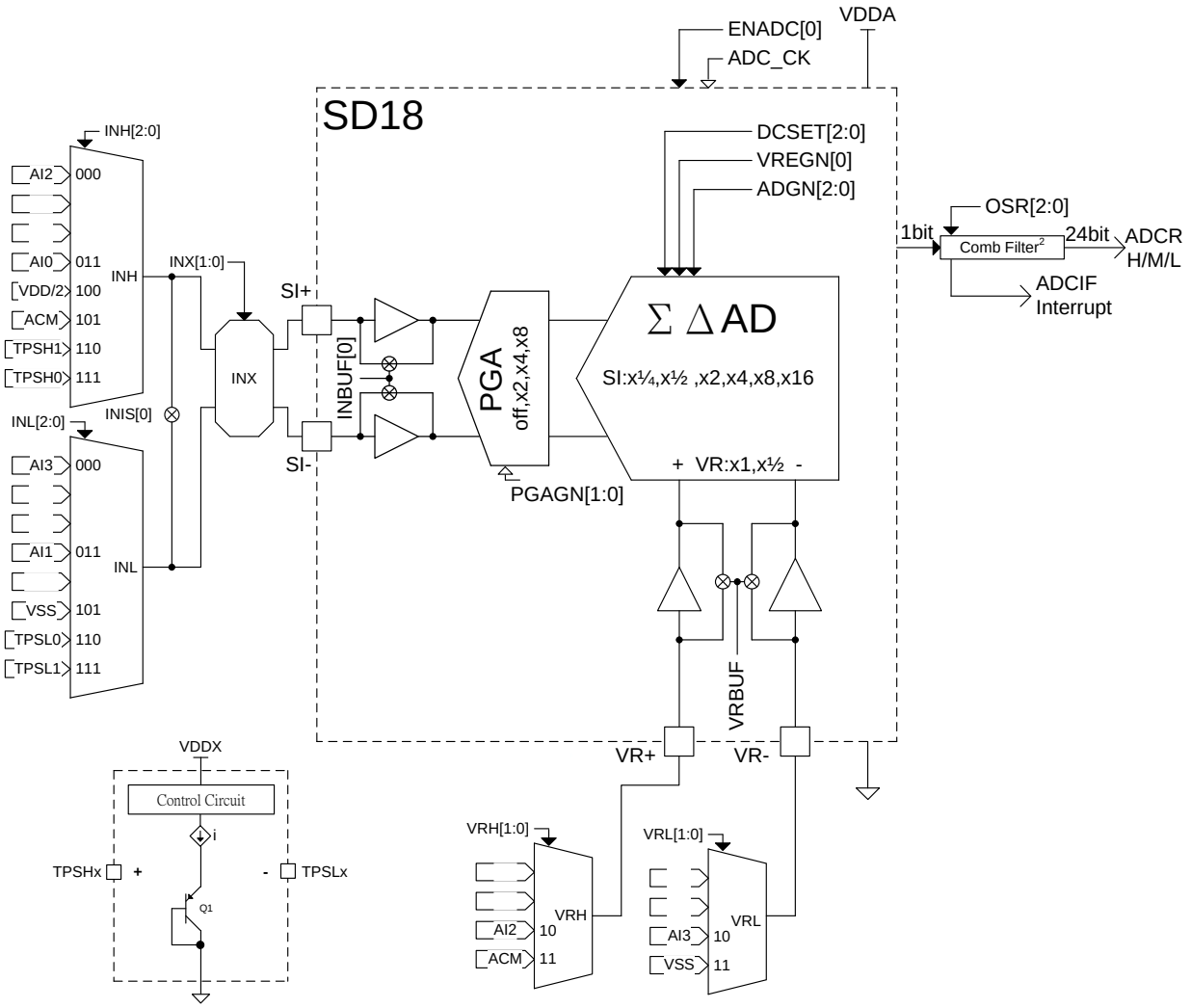


Figure 4-2 SD18 Network

5. Register List

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1												
"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition												
Address	**File Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**A-RESET**	**i-RESET**	**R/W**
00H	INDF0	Contents of FSR0 to address data memory value of FSR0 not changed								N/A	N/A	*,*,*,*,*,*,*,*
05H	INDF1	Contents of FSR1 to address data memory value of FSR0 not changed								N/A	N/A	*,*,*,*,*,*,*,*
10H	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
12H	FSR1L	Indirect Data Memory Address Pointer 1 Low Byte,FSR1[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18H	STKPTR	STKFL	STKUN	STKOV			STKPRT[2:0]			000. .000	000. .000	r,rw0,rw0,- -,r,r,r
1AH	PCLATH						PC[10]	PC[9]	PC[8]	.... .000	.... .000	-,-,-,- -,*,*
1BH	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	*,*,*,*,*,*,*,*
23H	INTE1	GIE	ADCIE			TMAIE	WDTIE	E1IE	E0IE	00.. 0000	00.. 0000	*,*,-,- *,*,*,*
26H	INTF1		ADCIF			TMAIF	WDTIF	E1IF	E0IF	.0.. 0000	.0.. 0000	-,*,-,- *,*,*,*
29H	WREG	Working Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
2BH	STATUS				C				Z	...x ...x	...u ...u	-,-,-,* -,-,-,*
2CH	PSTATUS	PD	TO	IDLEB	BOR		SKERR			000d .0..	uduu .d..	rw0,rw0,rw0,rw0 -,rw0,-,-
2DH	LVDCN		LVDFG	LVD	LVDON	VLDX[3:0]				.000 0000	.000 uuuu	-,*,r,r *,*,*,*
30H	PWRCN	ENVDDA	VDDAX[1:0]		ENACM					0000	0000	*,*,*,* -,-,-,-
31H	MCKCN1	ADCS[2:0]			ADCCK	XTHSP	XTSP	ENXT	ENHAO	0000 0001	0000 0001	*,*,*,*,*,*,*,*
32H	MCKCN2			LSCK	HSCK	HSS[1:0]		CPUCK[1:0]		..00 0000	..00 0000	-,-,*,*,*,*,*,*
33H	MCKCN3	LCDS[2:0]				PERCK	BZS[2:0]			000. 0000	000. 0000	*,*,*,- *,*,*,*
39H	ADCRH	ADC conversion memory HighByte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3AH	ADCRM	ADC conversion memory Middle Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3BH	ADCRL	ADC conversion memory Low Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3CH	ADCCN1	ENADC	ENHIGN	ENCHP	PGAGN[1:0]		ADGN[2:0]			0000 0000	0000 0000	*,*,*,*,*,*,*,*
3DH	ADCCN2			INBUF	VRBUF	VREGN	DCSET[2:0]			..00 0000	..00 0000	-,-,*,*,*,*,*,*
3EH	ADCCN3	OSR[2:0]								000.	000.	*,*,*,- -,-,-,-
3FH	AINET1	INH[2:0]			INL[2:0]			INIS		0000 000.	0000 000.	*,*,*,*,*,*,*,-
40H	AINET2		VRH[1:0]		INX[1:0]		VRL[1:0]			.000 000.	.000 000.	-,*,*,*,*,*,*,-
41H	TMACN	ENTMA	TMACK	TMAS[1:0]		ENWDT	WDTS[2:0]			0000 0000	0000 0000	*,*,*,* w1,*,*,*
42H	TMAR	TimerA data register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
52H	LCDCN1	ENLCD	LCDPR	VLCDX[1:0]		LCDBF	LCDBI[1:0]			0000 000.	0000 000.	*,*,*,*,*,*,*,-
53H	LCDCN2	LCDBL	LCDMX[1:0]							000.	000.	*,*,*,- -,-,-,-
54H	LCD0	Segment SEG2@[3:0] and SEG3@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
55H	LCD1	Segment SEG4@[3:0] and SEG5@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
56H	LCD2	Segment SEG6@[3:0] and SEG7@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
57H	LCD3	Segment SEG8@[3:0] and SEG9@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
58H	LCD4	Segment SEG10@[3:0] and SEG11@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
59H	LCD5	Segment SEG12@[3:0] and SEG13@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
6DH	PT1	PT1.7	PT1.6	PT1.5	PT1.4	PT1.3	PT1.2	PT1.1	PT1.0	xxxx xxxx	uuuu uuuu	*,*,*,* r,r,r,r
6EH	TRISC1	TC1.7	TC1.6	TC1.5	TC1.4					0000	0000	*,*,*,* -,-,-,-
6FH	PT1DA						DA1.2			.... .0..	.... .0..	-,-,-,- -,*,-,-
70H	PT1PU	PU1.7	PU1.6	PU1.5	PU1.4	PU1.3	PU1.2	PU1.1	PU1.0	0000 0000	0000 0000	*,*,*,*,*,*,*,*
71H	PT1M1					INTEG1[1:0]		INTEG0[1:0]		 0000	 0000	-,-,-,- *,*,*,*
72H	PT1M2		PM1.7[0]							.0..	.0..	-,*,-,- -,-,-,-
74H	PT2			PT2.5	PT2.4	PT2.3	PT2.2	PT2.1	PT2.0	..xx xxxx	..uu uuuu	-,-,*,*,*,*,*,*
75H	TRISC2			TC2.5	TC2.4	TC2.3	TC2.2	TC2.1	TC2.0	..00 0000	..00 0000	-,-,*,*,*,*,*,*
77H	PT2PU			PU2.5	PU2.4	PU2.3	PU2.2	PU2.1	PU2.0	..00 0000	..00 0000	-,-,*,*,*,*,*,*
80H ~ FFH	GPR0	General Purpose Register as 128Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*

Figure 5-1 HY11P12 Register List

6. Electrical Characteristics

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at V_{DD} to V_{SS} . . . . . −0.2 V to 4.0 V

Voltage applied to any pin (see Note 1) . . . . . −0.2 V to V_{DD} + 0.3 V

Voltage applied to RST/VPP pin . . . . . −0.2 V to 6.9 V

Voltage applied to TST/PT1.3 pin (see Note 1) . . . . . −0.2 V to V_{DD} + 1 V

Diode current at any device terminal . . . . . ±2 mA

Storage temperature, Tstg: (unprogrammed device) . . . . . −55℃ to 150℃

(programmed device) . . . . . −40℃ to 85℃

Total power dissipation. 0.5w

Maximum output current sink by any PORT1 to PORT3 I/O pin. 25mA

6.1. Recommended operating conditions

T_A = -40℃ ~ 85℃, unless otherwise noted

Sym.	Parameter		Test Conditions		Min.	Typ.	Max.	unit
V_{DD}	Supply Voltage		All digital peripherals and CPU		2.2		3.6	V
			Analog peripherals		2.4		3.6	
V_{SS}	Supply Voltage				0		0	
XT	External Oscillator Frequency	Watch crystal	V_{DD} = 2.2V, ENXT[0]=1	XTSP[0]=0, XTHSP[0]=0	32.768K			Hz
		Ceramic resonator		XTSP[0]=1, XTHSP[0]=0	450K		8M	
		Crystal		XTSP[0]=1, XTHSP[0]=0	1M		8M	

6.2. Internal RC Oscillator

T_A = 25℃ ,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1	1.8	2.0	2.2	MHz
LPO	Low Power Oscillator frequency	V_{DD} supply voltage be enable LPO	22	28	35	KHz

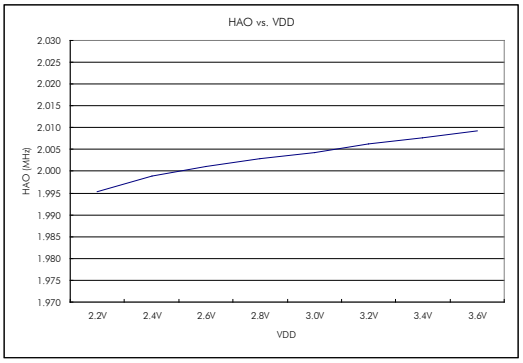


Figure 6.2-1 HAO vs. VDD

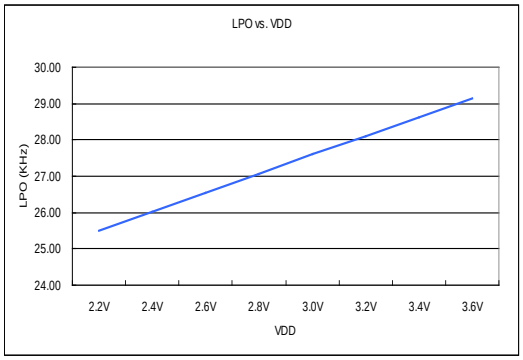


Figure 6.2-2 LPO vs. VDD

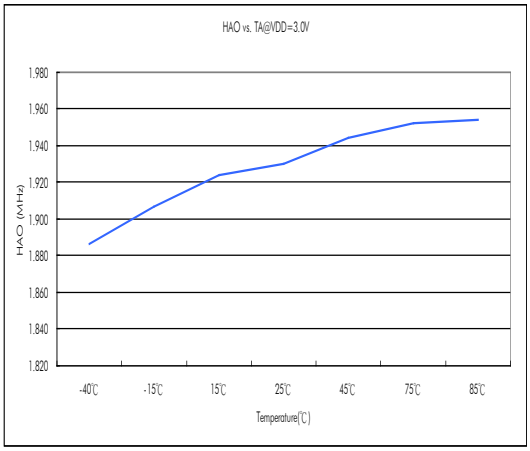


Figure 6.2-3 HAO vs. Temperature

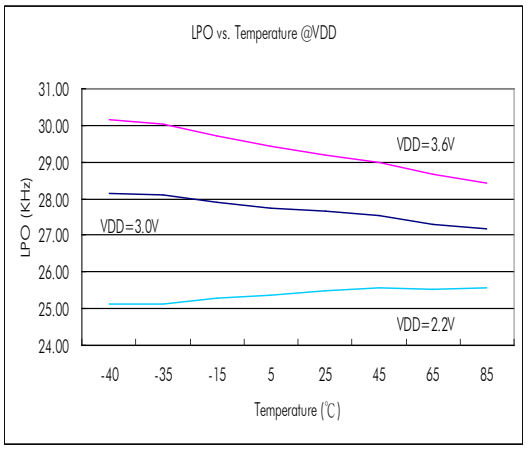


Figure 6.2-4 LPO vs. Temperature

6.3. Supply current into VDD excluding peripherals current

T_A = 25℃,V_{DD} = 3.0V,OSC_LPO = 28KHz, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM1}	Active mode 1	OSC_CY = 8MHz, OSC_HAO = off, CPU_CK = 8MHz		1	2	mA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 2MHz		0.28	0.55	mA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 1MHz		0.165	0.3	mA
I_{LP1}	Low Power 1	OSC_CY = 32768Hz, OSC_HAO = off, CPU_CK = 16384Hz		7	12	uA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		1.65	3	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.65	1.2	uA

OSC_CY：External Oscillator frequency.

OSC_HAO：Internal High Accuracy Oscillator frequency.

CPU_CK：CPU core work frequency.

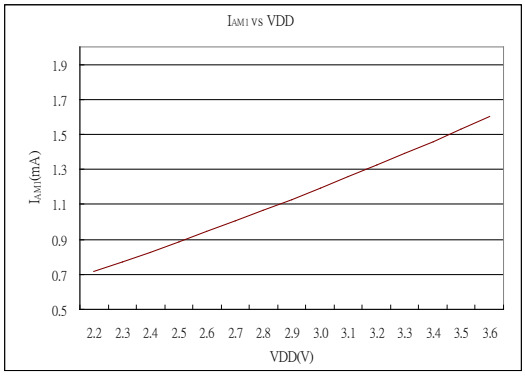


Figure 6.3-1 I_{AM1} vs. VDD

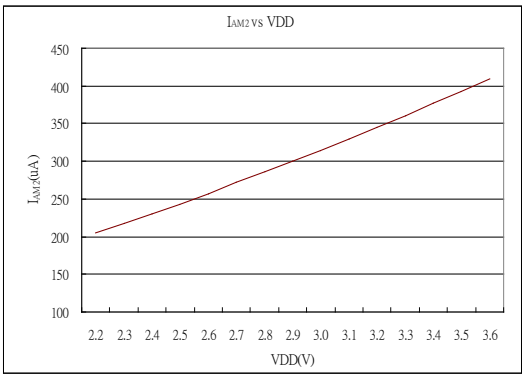


Figure 6.3-2 I_{AM2} vs. VDD

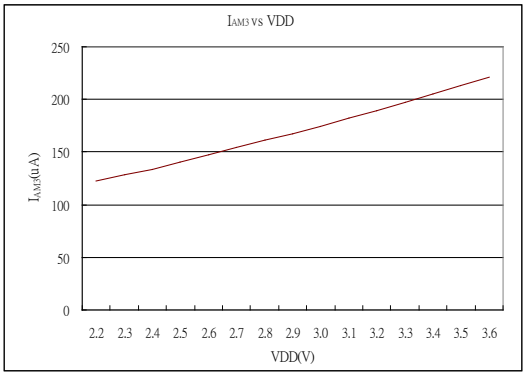


Figure 6.3-3 I_{AM3} vs. VDD

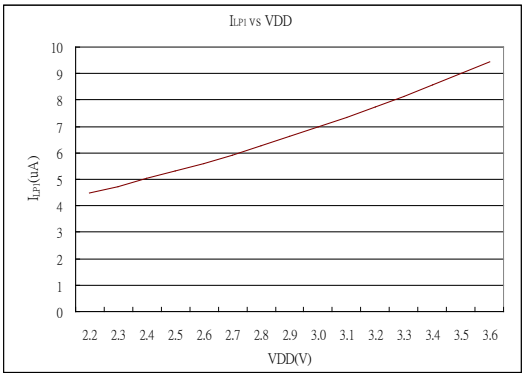


Figure 6.3-4 I_{LP1} vs. VDD

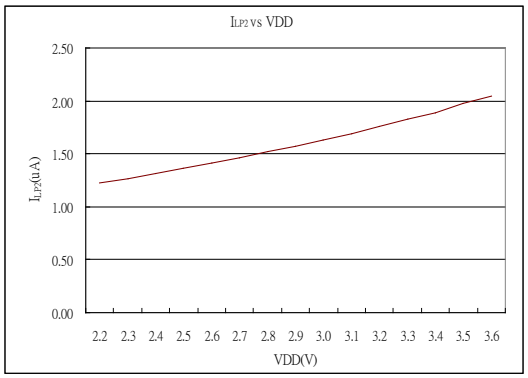


Figure 6.3-5 I_{LP2} vs. VDD

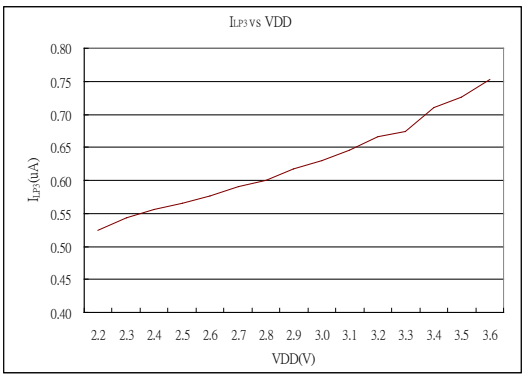


Figure 6.3-6 I_{LP3} vs. VDD

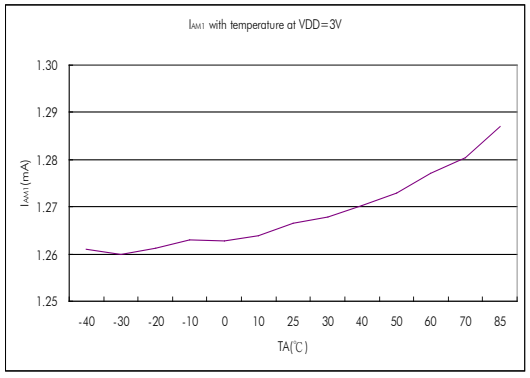


Figure 6.3-7 I_{AM1} vs. Temperature

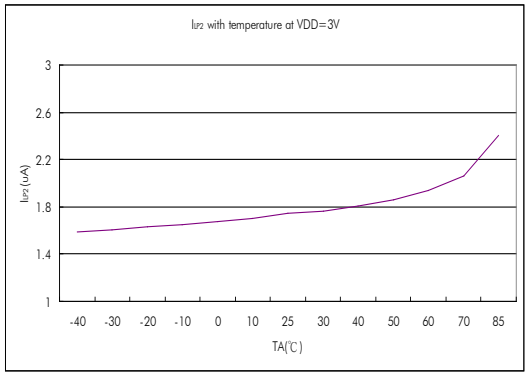


Figure 6.3-8 I_{LP2} vs. Temperature

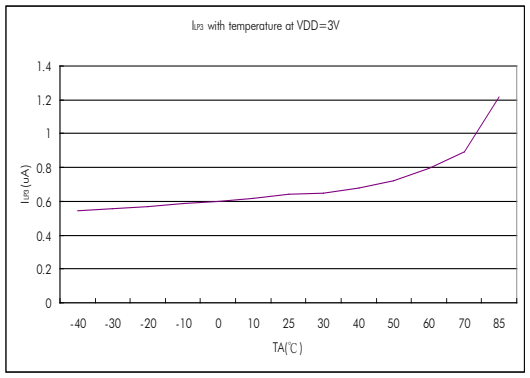


Figure 6.3-9 I_{LP3} vs. Temperature

6.4. Port1~2

T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				2.1	V
V_{IL}	Low-Level input voltage		0.9			
V_{hys}	Input Voltage hysteresis(VIH - VIL)			0.8		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance			180		kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	I_{OH}=10mA	V_{DD} -0.3			V
V_{OL}	Low-level output voltage	I_{OL}=-10mA			VSS +0.3	

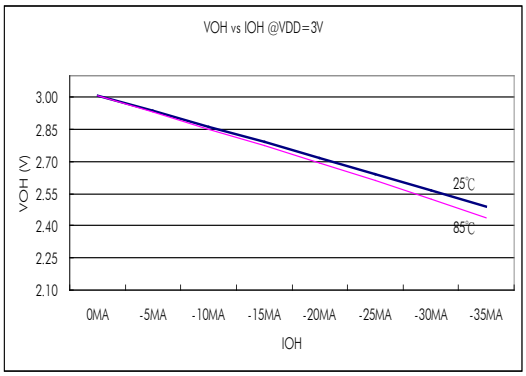


Figure 6.4-1 V_{OH} vs. I_{OH} @VDD=3.0V

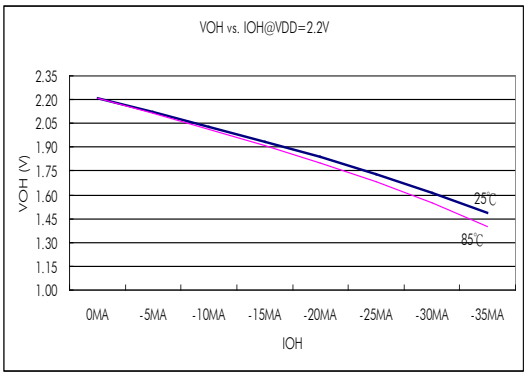


Figure 6.4-2 V_{OH} vs. I_{OH} @VDD=2.2V

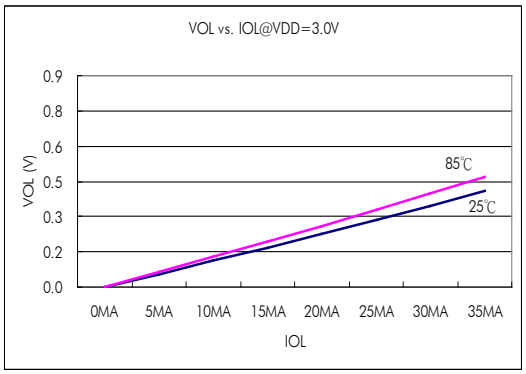


Figure 6.4-3 V_{OL} vs. I_{OL}@VDD=3.0V

Figure 6.4-4 V_{OL} vs. I_{OL}@VDD=2.2V

6.5. Reset (Brownout, External RST pin, Low Voltage Detect)

T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
BOR	Pulse length needed to accepted reset internally, t_{d-LVR}		2			us
	V_{DD} Start Voltage to accepted reset internally (L➔H),V_{LVR}		1.6	1.85	2.1	V
	Hysteresis, $V_{HYS-LVR}$			70		mV
RST	Pulse length needed as RST/VPP pin to accepted reset internally, t_{d-RST}		2			us
	Input Voltage to accepted reset internally		0.9			V
	Hysteresis, $V_{HYS-RST}$			0.8		V
LVD	Operation current, I_{LVD}			10	15	uA
	External input voltage to compare reference voltage			1.2		V
	Compare reference voltage temperature drift	T_A = -40℃ ~ 85 ℃		100		ppm/℃
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1110b			3.3		V
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1101b			3.2		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1100b			3.1		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1011b			3.0		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1010b			2.9		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1001b			2.8		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1000b			2.7		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0111b			2.6		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0110b			2.5		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0101b			2.4		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0100b			2.3		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0011b			2.2		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0010b			2.1		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0001b			2.0		

BOR：Brownout Reset

LVR：Low Voltage Reset of BOR

LVD：Low Voltage Detect

RST：External Reset pin

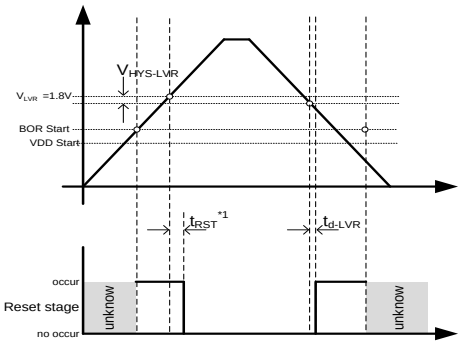


Figure6.5-1 BOR reset diagram

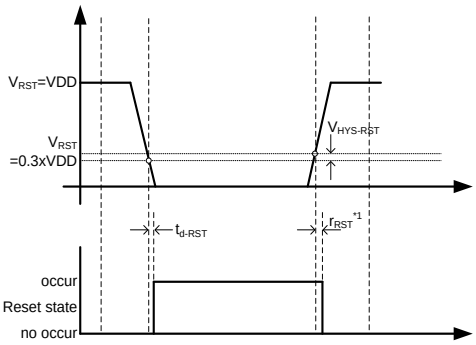


Figure6.5-2 RST reset diagram

*1 r_{RST} ：Please see BOR Introduce of HY11Pxx series User's Guide (UG-HY11S14-Vxx).

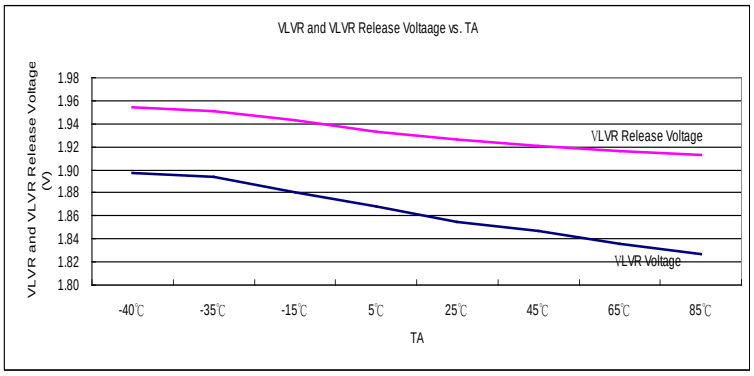


Figure 6.5-3 LVR vs. Temperature

6.6. Power System

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
VDDA	VDDA operation current, I_{VDDA}	I_L = 0mA	VDDAX[1:0]=00b		22		uA
	Select VDDA output voltage	I_L = 0.1mA, VDD≧VDDA+0.2V	VDDAX [1:0]=00b		3.3		V
			VDDAX [1:0]=01b		2.9		V
			VDDAX [1:0]=10b		2.6		V
			VDDAX [1:0]=11b		2.4		V
	Dropout voltage	I_L = 10mA	VDDAX [1:0]=00b		135		mV
			VDDAX [1:0]=01b		150		mV
			VDDAX [1:0]=10b		165		mV
			VDDAX [1:0]=11b		180		mV
	Temperature drift	VDDAX [1:0]=11b	T_A=-40℃~85℃		50		ppm/℃
	V_{DD} Voltage drift	I_L = 0.1mA	V_{DD}=2.5V~3.6V		±0.2		%/V
ACM	ACM operation current, I_{ACM}	I_L = 0mA			20		uA
	Output voltage ,V_{ACM}	ENACM[0]=1	I_L = 0uA		1.0		V
	Output voltage with Load		I_L = ±200uA	0.98		1.02	V_{ACM}
	Temperature drift	ENACM[0]=1, I_L = 10uA	T_A=-40℃~85℃		50		ppm/℃
	VDDA Voltage drift				100		uV/V
VDDA：Adjust Voltage Regulator ACM：Analog Common Mode Voltage							

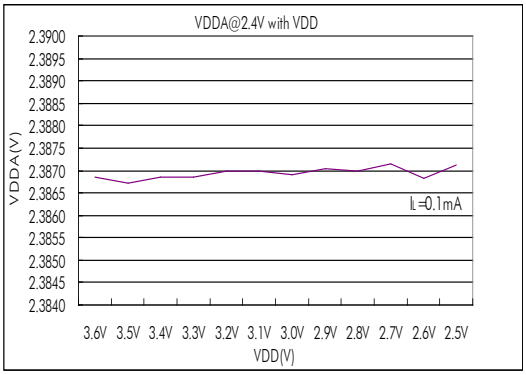


Figure 6.6-1 VDDA IL=0.1mA vs. VDD

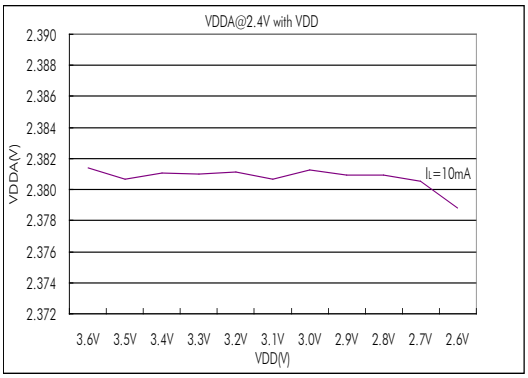


Figure 6.6-2 VDDA IL=10mA vs. VDD

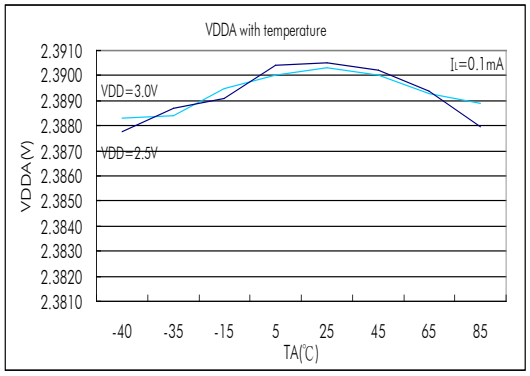


Figure 6.6-3 VDDA I_L=0.1mA vs. Temperature

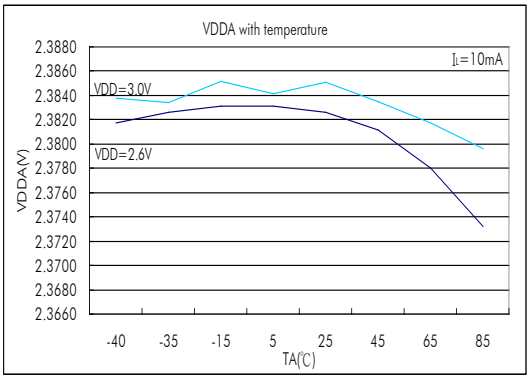


Figure 6.6-4 VDDA I_L=10mA vs. Temperature

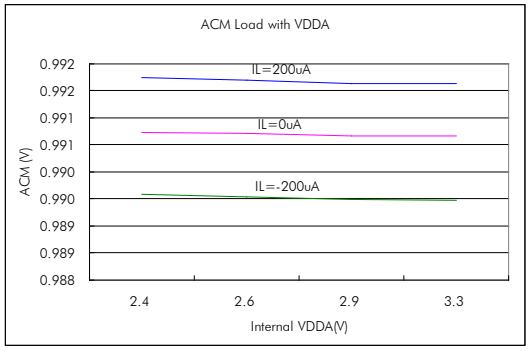


Figure 6.6-5 ACM Load vs. VDDA

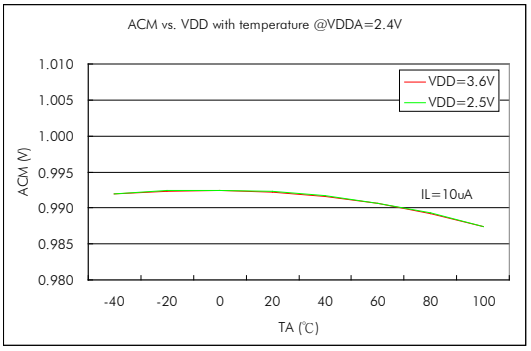


Figure 6.6-6 ACM vs. Temperature

6.7. LCD

T_A = 25℃,V_{DD} = 3.0V, C_{VLCD} =4.7uF, unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
I_{LCD}	Operation supply current without output buffer.(all segment turn on)	LCDPR[0]=1	V_{DD} = 2.2V		10		uA
			V_{DD} = 3.0V				
VLCD	Supply Voltage at VLCD pin	LCDPR[0]=0		2.2		3.6	V
	Embedded Charge Pump output voltage at VLCD pin	V_{DD} = 2.2V, LCDPR[0]=1, C_{VLCD} =4.7uF	VLCDX[1:0]=11b	2.295	2.55	2.805	V
			VLCDX[1:0]=10b	2.52	2.8	3.08	
			VLCDX[1:0]=01b	2.745	3.05	3.355	
			VLCDX[1:0]=00b	2.97	3.3	3.63	
Z_{LCD}	Output impedance with LCD buffer	f_{LCD} =128Hz,VLCD=3.05V			10		kΩ

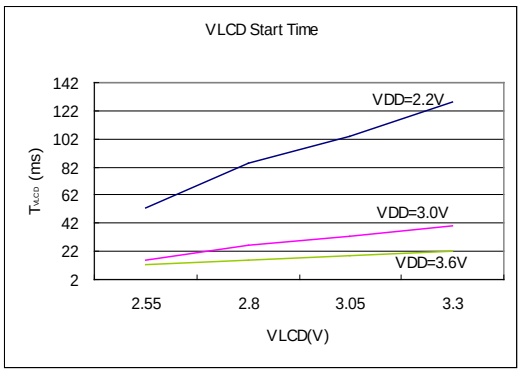


Figure 6.7-1 LCD start time

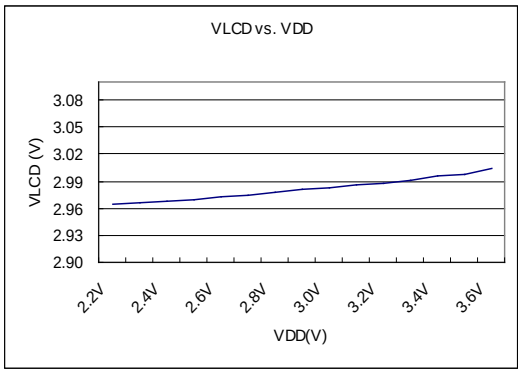


Figure 6.7-2 VLCD vs. VDD

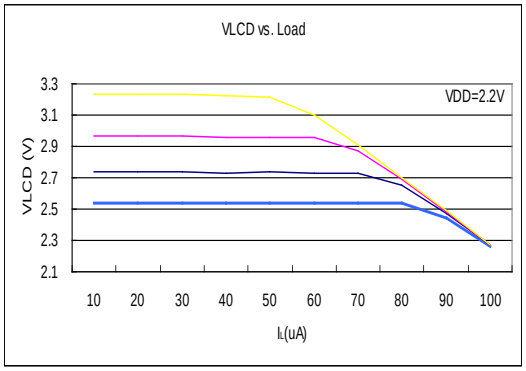


Figure 6.7-3 VLCD vs. I_L @VDD=2.2V

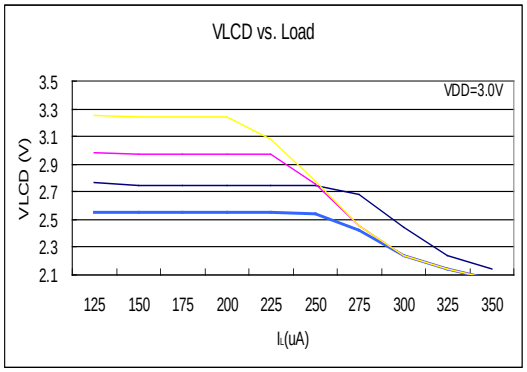


Figure 6.7-4 VLCD vs. I_L @VDD=3.0V

6.8. SD18, Power Supply and Recommended Operating Conditions

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{SD18}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
f_{SD18}	Modulator sample frequency, ADC_CK			25	250	300	KHz
	Over Sample Ratio, OSR			256		32768	
I_{SD18}	Operation supply current without PGA	ENADC[0]=1 INBUF[0]=1,VRBUF[0]=0	GAIN =4, ADC_CK=250KHz		168		uA
		ENADC[0]=1 INBUF[0]=0,VRBUF[0]=1			150		
		ENADC[0]=1 INBUF[0]=0,VRBUF[0]=0			120		

6.8.1. PGA, Power Supply and Recommended Operating Conditions

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{PGA}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
I_{PGA}	Operation supply current	PGAGN[1:0]=<01>or<1x>			320		uA
G_{PGA}	Gain temperature drift	T_A = -40℃~ 85℃	GAIN=128		5		ppm/℃

6.8.2. SD18, Performance II (fSD18=250KHz)

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.9V,V_{VR}=1.0V,GAIN=1 without PGA, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
INL	Integral Nonlinearity(INL)	VDDA=2.4V,V_{VR}=1.0V,ΔSI=±200mV			±0.003	±0.01	%FSR
		VDDA=2.4V,V_{VR}=1.0V,ΔSI=±450mV					
	No Missing Codes[3]	ADC_CK=250KHz,OSR[2:0]=010b		23			Bits
G_{SD18}	Temperature drift **Gain 1~x16 (INBUF[0]=0b,)** **Gain 1~x4 (INBUF[0]=1b,)**	INBUF[0]=0b,VRBUF[0]=0b	T_A = -40℃~85℃		2		ppm/℃
		INBUF[0]=1b,VRBUF[0]=0b					
		INBUF[0]=0b,VRBUF[0]=1b					
		INBUF[0]=1b,VRBUF[0]=1b					
E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper and Buffer(INBUF,VRBUF) without PGA	ΔAI=0V ΔVR=0.9V DCSET[2:0]=<000> *ΔAI is external short	Gain=2			1	%FSR
	Offset error of Full Scale Rang input voltage range with Chopper without PGA and Buffer(INBUF,VRBUF)		Gain=2			1	
	Offset temperature drift with chopper without PGA and Buffer (INBUF,VRBUF).		GAIN=1		2		uV/℃
			GAIN=2		1		
			GAIN=4		0.5		
			GAIN=16		0.15		
	Offset temperature drift with chopper and Buffer (INBUF,VRBUF) without PGA.		GAIN=1		2		
			GAIN=2		1		
			GAIN=4		0.5		
	Offset temperature drift with chopper without Buffer (INBUF,VRBUF).		GAIN=128		0.02		
CM_{SD18}	Common-mode rejection	V_{CM}=0.7V to 1.7V, V_{VR}=1.0V,without PGA	V_{SI}=0V, GAIN=1		90		dB
		V_{CM}=0.7V to 1.7V, V_{VR}=1.0V, without PGA	V_{SI}=0V, GAIN=16		75		
PSRR	DC power supply rejection	VDDA=3.0V,ΔVDDA=±100mV, V_{VR}=1.0V, V_{SI}=1.2V,V_{SI-}=1.2V,	GAIN=1 PGA=off		75		dB
			GAIN=16 PGA=8				

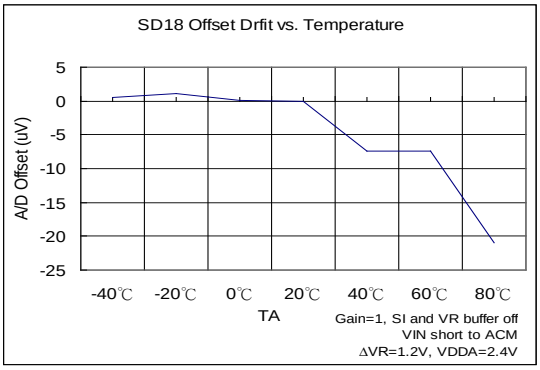


Figure 6.8-1(a) SD18 Offset Temperature Drift

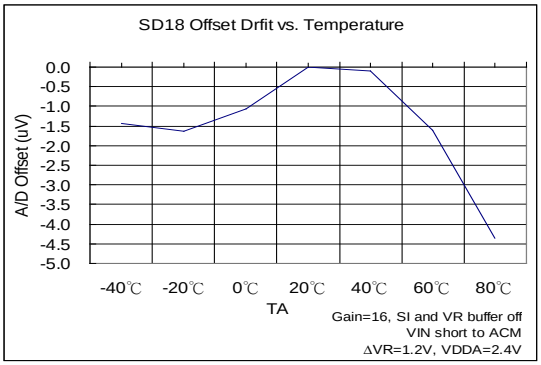


Figure 6.8-1(b) SD18 Offset Temperature Drift

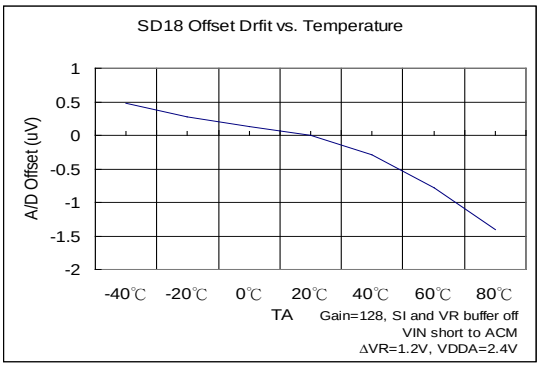


Figure 6.8-1(c) SD18 Offset Temperature Drift

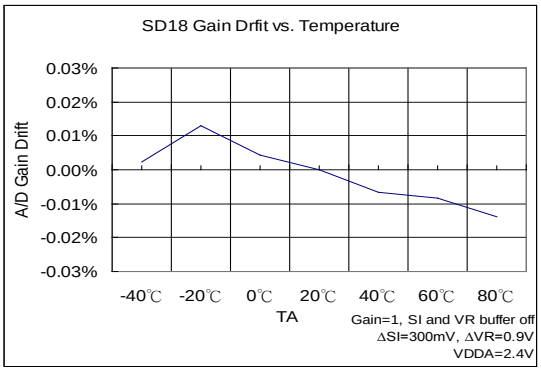


Figure 6.8-2(a) SD18 Gain Drift with Temperature

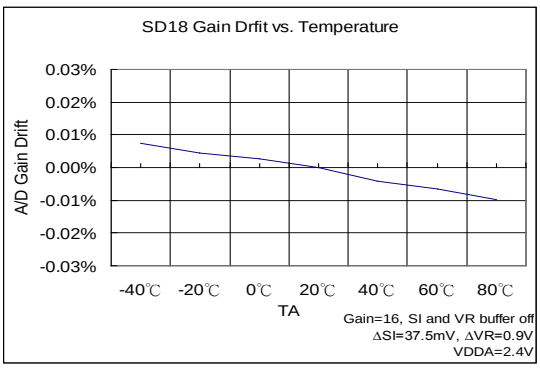


Figure 6.8-2(b) SD18 Gain Drift with Temperature

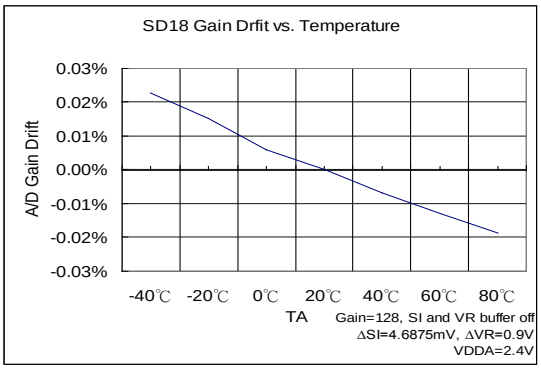


Figure 6.8-2(c) SD18 Gain Drift with Temperature

6.8.3. SD18, Temperature Sensor

T_A = 25℃,V_{DD} = 3.0V, VDDA=3.3V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
TC_S	Sensor temperature drift	ΔVR=2.4V,VRGN[0]=1,		178		uV/℃
KT	Absolute Temperature Scale 0°K	INBUF[0]=1		-289		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~85℃		±2		℃

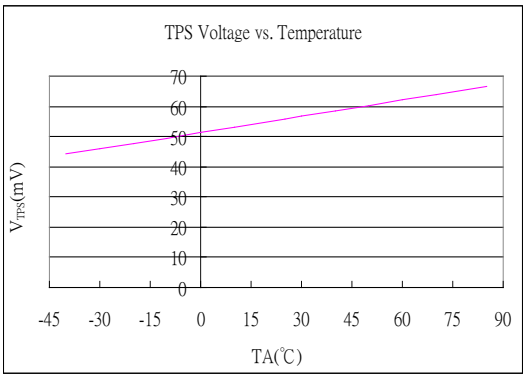


Figure 6.8-3 TPS Output Voltage vs. Temperature Drift

6.8.4. SD18 Noise Performance

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

HY11P12 provides important input noise specification that aims at SD18. Table6.8-4(a) and Table6.8-4(b) lists out the relations of typical noise specification, Gain, Output rate, and maximum input voltage of single end. Test condition configuration and external input signal short, voltage reference: 1.2V and 1024 records were sampled.

ENOB(RMS) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V													
Max. Vin(mV) =0.9*VREF (1)	**OSR**					**256**	**512**	**1024**	**2048**	**4096**	**8192**	**16384**	**32768**
	Output rate(HZ)					**977**	**488**	**244**	**122**	**61**	**31**	**15**	**8**
	Gain	**=**	**PGA**	**×**	**ADGN**								
±2400	**0.25**	**=**	**1**	**×**	**0.25**	16.3	17.4	17.9	18.5	19.0	19.5	20.0	20.4
±2160	**0.5**	**=**	**1**	**×**	**0.5**	16.3	17.3	17.9	18.4	18.9	19.4	19.8	20.2
±1080	**1**	**=**	**1**	**×**	**1**	16.2	17.2	17.8	18.3	18.8	19.3	19.7	20.1
±540	**2**	**=**	**1**	**×**	**2**	16.1	17.1	17.6	18.2	18.7	19.2	19.6	20.0
±270	**4**	**=**	**1**	**×**	**4**	16.0	16.9	17.5	18.0	18.5	18.9	19.4	19.8
±135	**8**	**=**	**1**	**×**	**8**	15.9	16.6	17.2	17.7	18.2	18.7	19.2	19.6
±68	**16**	**=**	**1**	**×**	**16**	15.6	16.3	16.8	17.3	17.7	18.3	18.8	19.3
±34	**32**	**=**	**2**	**×**	**16**	14.8	15.3	15.9	16.4	16.9	17.4	17.8	18.3
±17	**64**	**=**	**4**	**×**	**16**	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0
±8	**128**	**=**	**8**	**×**	**16**	14.0	14.6	15.1	15.6	16.0	16.6	17.0	17.5

(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).

Table6.8-4(a) SD18 ENOB Table

RMS Noise(uV) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V													
Max. Vin(mV) =0.9*VREF	**OSR**					**256**	**512**	**1024**	**2048**	**4096**	**8192**	**16384**	**32768**
	Output rate(HZ)					**977**	**488**	**244**	**122**	**61**	**31**	**15**	**8**
	Gain	**=**	**PGA**	**×**	**ADGN**								
±2400	**0.25**	**=**	**1**	**×**	**0.25**	121.08	57.40	38.74	26.66	18.39	13.21	9.49	6.98
±2160	**0.5**	**=**	**1**	**×**	**0.5**	61.63	29.23	19.21	13.51	9.78	7.02	5.12	3.91
±1080	**1**	**=**	**1**	**×**	**1**	32.21	15.70	10.25	7.31	5.19	3.77	2.80	2.13
±540	**2**	**=**	**1**	**×**	**2**	16.59	8.54	5.91	4.06	2.86	2.06	1.48	1.12
±270	**4**	**=**	**1**	**×**	**4**	9.00	4.84	3.33	2.37	1.67	1.19	0.87	0.65
±135	**8**	**=**	**1**	**×**	**8**	5.04	2.97	2.02	1.44	1.01	0.73	0.51	0.39
±68	**16**	**=**	**1**	**×**	**16**	3.03	1.84	1.29	0.92	0.70	0.46	0.33	0.24
±34	**32**	**=**	**2**	**×**	**16**	2.61	1.81	1.27	0.89	0.62	0.45	0.32	0.23
±17	**64**	**=**	**4**	**×**	**16**	1.66	1.13	0.80	0.56	0.41	0.29	0.20	0.14
±8	**128**	**=**	**8**	**×**	**16**	1.13	0.77	0.55	0.38	0.28	0.19	0.14	0.10

Table6.8-4(b) SD18 RMS Noise Table

The RMS noise is referred to the input. The Effective Number of Bits (ENOB (RMS Bit)) is defined as :

$$\text{ENOB(RMS)} = \ln\left(\frac{\text{FSR}}{\text{RMS Noise}}\right) \Big/ \ln(2)$$

$$\text{RMS Noise} = \left(2 \times \text{VREF} \times \sqrt{\sum_{k=1}^{1024}(\text{ADO}[k] - \text{Average})^2}\right) \Big/ 2^{23}$$

$$\text{Where FSR (Full - Scale Range)} = 2 \times \text{VREF/Gain.}$$

$$\text{Average} = \frac{\sum_{k=1}^{1024}(\text{ADO}[k])}{1024}$$

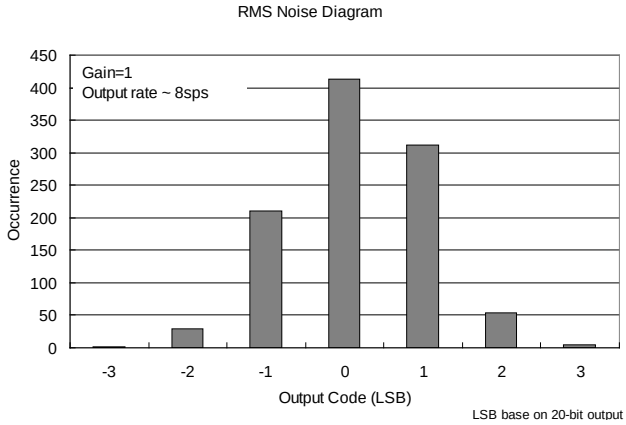


Figure 6.8-4(a) RMS Noise Diagram

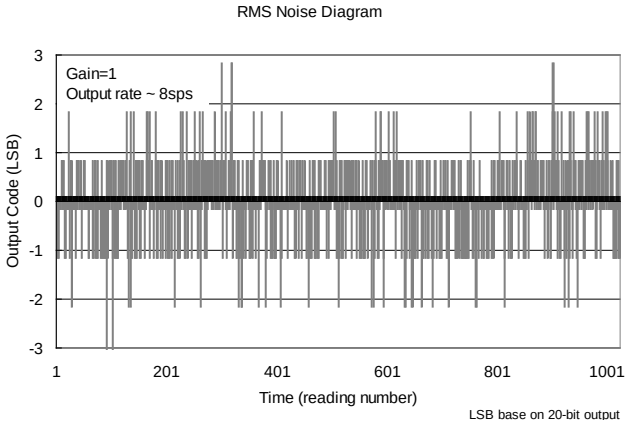


Figure 6.8-4(b) Output Code Diagram

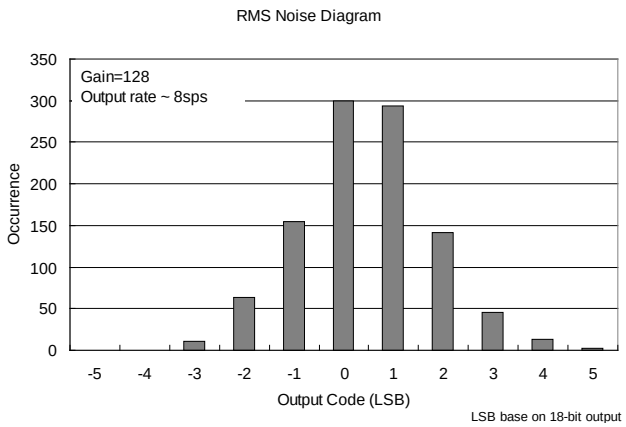


Figure 6.8-4(c) RMS Noise Diagram

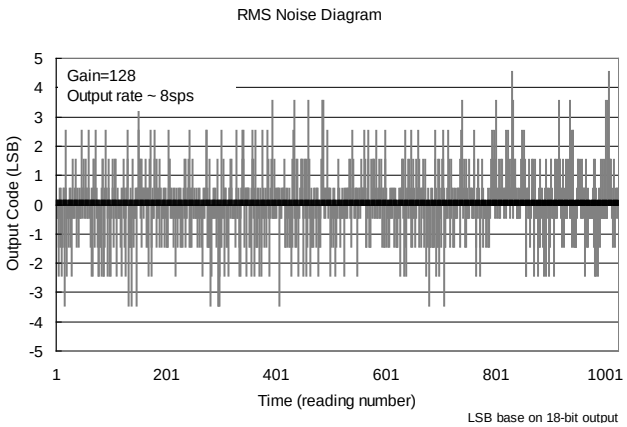


Figure 6.8-4(d) Output Code Diagram

7. Ordering Information

Device No.[1]	Package Type	Pins	Package Drawing		Code[2]	Shipment Packing Type	Unit Q'ty	Material Composition	MSL[3]
HY11P12-D000	Die	-	D	000	000	-	200	Green[4]	-
HY11P12-L044	LQFP	44	L	044	000	Tray	160	Green[4]	MSL-3
HY11P12-L048	LQFP	48	L	048	000	Tray	250	Green[4]	MSL-3
HY11P12-N048	QFN	48	N	048	000	Tape & Reel	3000	Green[4]	MSL-3

[1] **Device No.: Model No. – Package Type Description – Code** (Blank Code/ Standard/ Customized Programming Code)

Ex: Your customized programming code is 008 and you require die shipment.
The device No. will be HY11P12-D000-008.

Ex: You request blank code in die package.
The device No. will be HY11P12-D000.

Ex: You request blank code in LQFP 44 package.
The device No. will be HY11P12-L044.
And please clearly indicate the shipment packing type when placing orders.

Ex: Your customized programming code is 009 and you require products in LQFP 48 package.
The device No. will be HY11P12-L048-009.
And please clearly indicate the shipment packing type when placing orders.

[2] **Code:**

"001"~ "999" is standard or customized programming code. Blank code does not have these numbers.

[3] **MSL:**

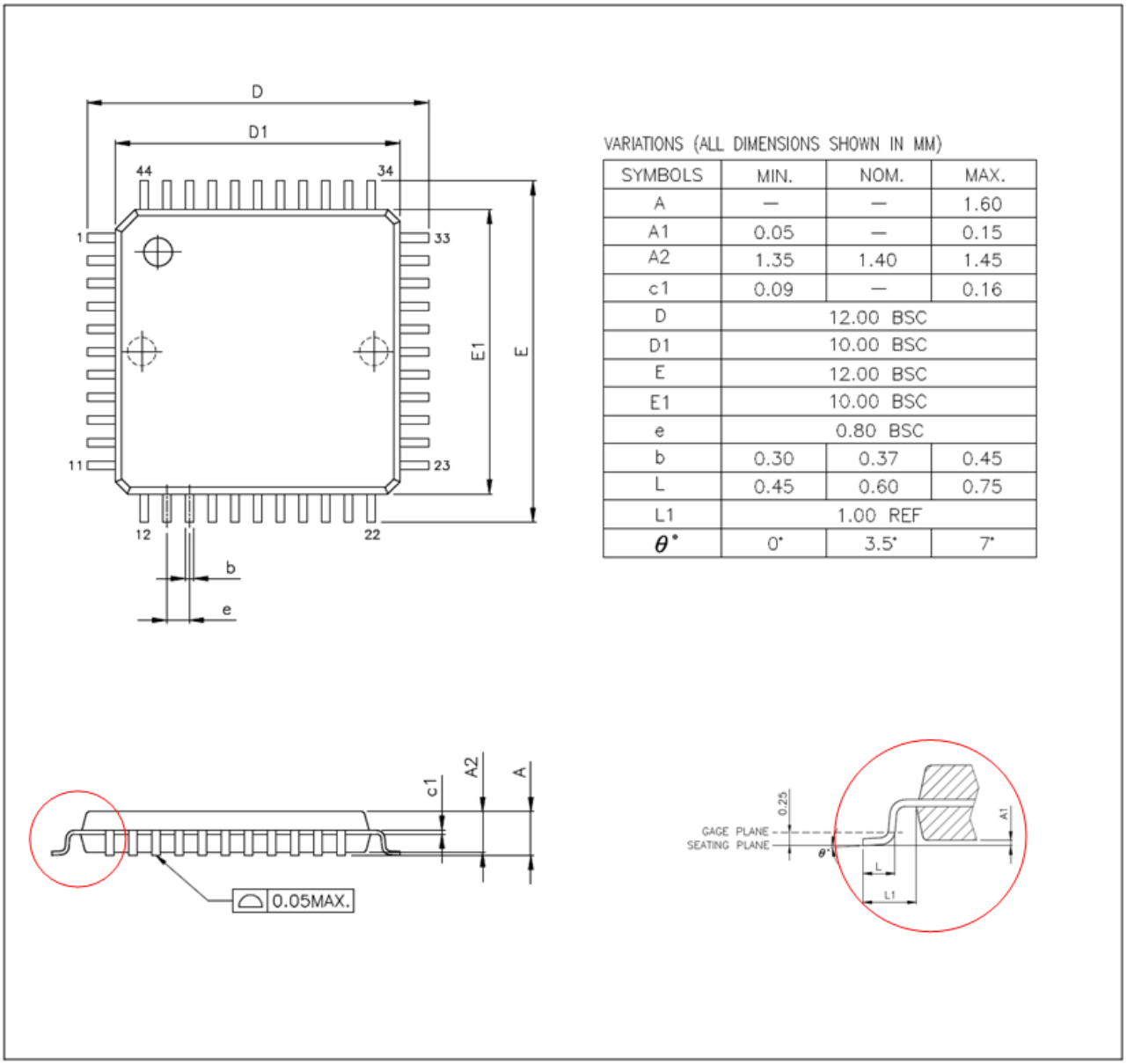
The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

[4] **Green (RoHS & no Cl/Br):**

HYCON products are Green products that are compliant with RoHS directive, SVHC under REACH and Halogen free.

8. Package Information

8.1. LQFP44(L044)

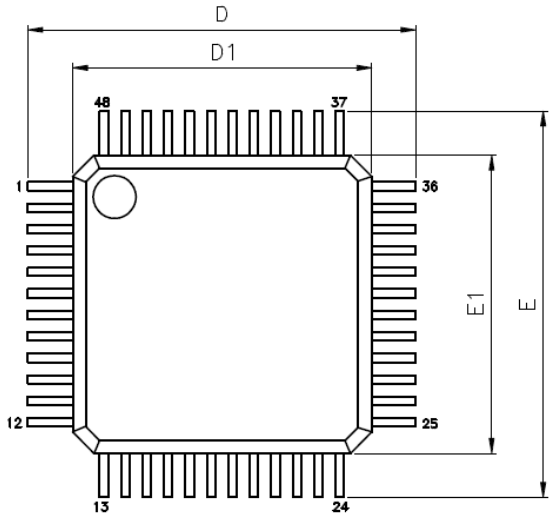


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
c1	0.09	—	0.16
D		12.00 BSC	
D1		10.00 BSC	
E		12.00 BSC	
E1		10.00 BSC	
e		0.80 BSC	
b	0.30	0.37	0.45
L	0.45	0.60	0.75
L1		1.00 REF	
θ°	0°	3.5°	7°

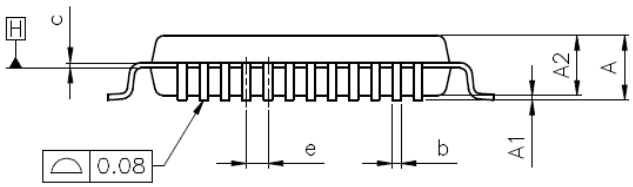
JEDEC MS-026 compliant

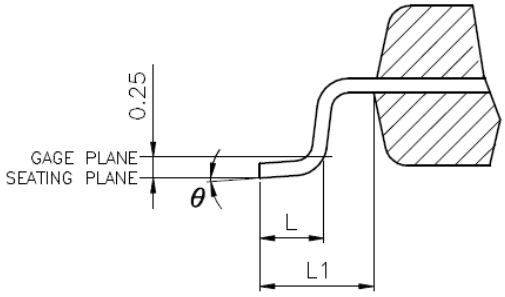
8.2. LQFP48(L048)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

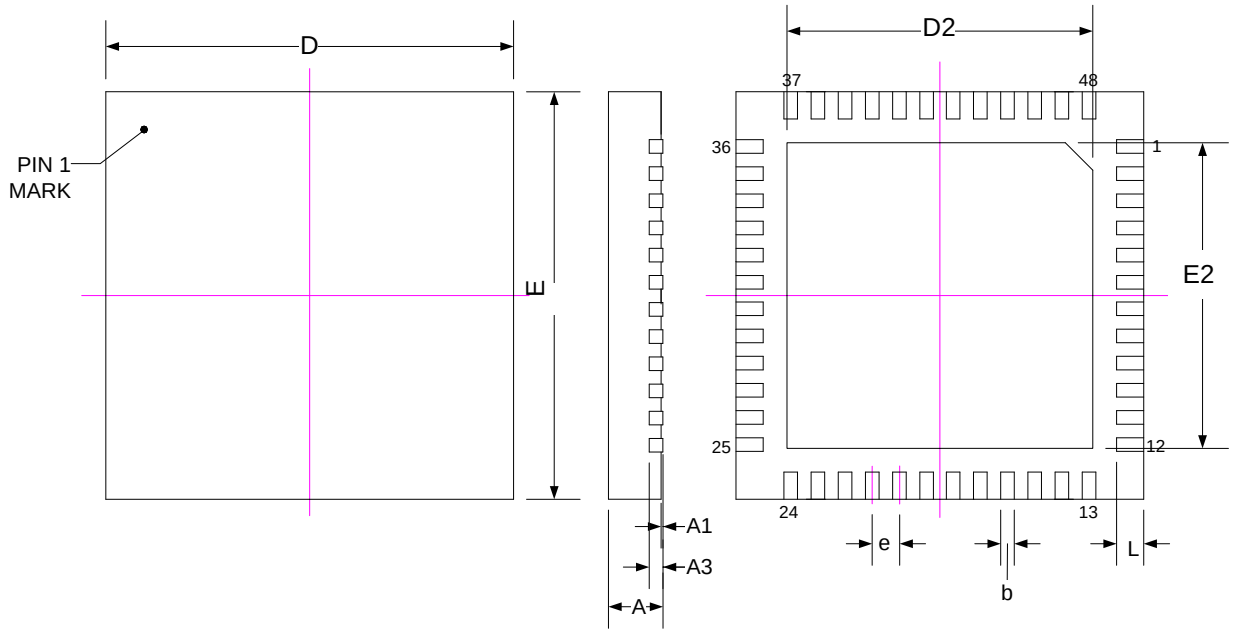




JEDEC MS-026 compliant

8.3. QFN48(N048)

8.3.1. Package Dimensions



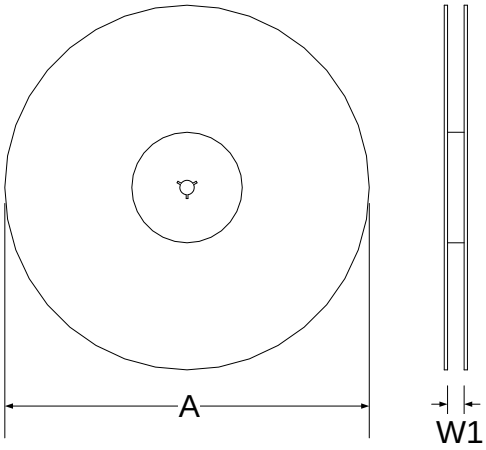
SYMBOLS	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.15	0.20	0.25
D		6.00 BSC	
E		6.00 BSC	
D2	4.40	4.50	4.55
E2	4.40	4.50	4.55
L	0.35	0.40	0.45
e		0.40 BSC	

Note: All dimensions refer to JEDEC OUTLINE MO-220.

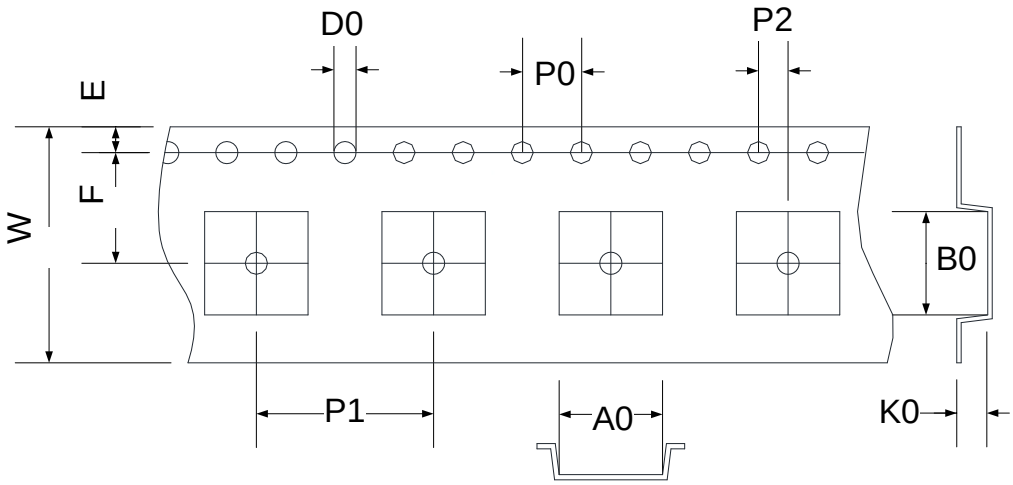
8.3.2. Tape & Reel Information

8.3.2.1. Reel Dimensions –Type1

Unit : mm



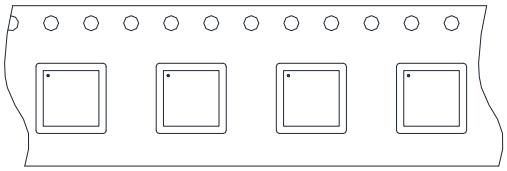
8.3.2.2. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	16.5	6.30	6.30	1.10	4.00	12.00	2.00	1.75	7.50	1.50	16.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

8.3.2.3. Pin1 direction



9. Revision Record

The following describes the major changes made to the document, excluding the punctuation and font changes.

Version	Page	Revision Summary
V03	ALL	First edition
V06		With reference to documentation: DS-HY11P12-V06_TC
	4	Features revision
	6~7	Table 2-1 Pin Definition and Function Description revision
	8~9	Chapter 4 Application circuit revision
	10	Chapter 5 Register List revision
	14	Chapter 6.3 Supply Current content revision
	17	Chapter 6.5 Reset content revision
	19	Chapter 6.6 Power System content revision
	20	Figure 6.6-5, Figure 6.6-6 ACM Chart revision
	22~24	Chapter 6.8 content revision
V07	11	Chapter 5 Register List revision
V09	1	Title revision
	4	Delete 1/2 bias feature
	5	Pin Diagram revision, add in LVDIN pin , add in Note 3
	8~9	Chapter 3 Application circuit revision, add in LVDIN pin and RC circuit of RST
	10	Add in LVDIN pin of the internal block diagram
V12	4	Revise Chapter 1 Features
	9	Revise Figure 3-2
	11	Add in Chapter 4.3 ADC Network
	13	Revise Chapter 6 Electrical Characteristics Content
	20	Revise Power System temperature drift spec
	22	Revise I_{LCD} spec
	27~28	Add in Chapter 6.8.4 SD18 Noise Performance
V14	6	Add in LQFP48 pin diagram
	11	Revise Development Tool Related Operating Instruction serial numbers
	12	Revise Figure 4-2 INH/INL
	30	Add in ordering information
	32	Add in package information
V15	7	Add in QFN48 pin diagram
	10~12	Add in LQFP48/QFN48 pinout I/O description
	34	Add in ordering information

	37	Add in package information
V16	14	Update Package marker information
	36	Update Green (RoHS & no Cl/Br)
	40	Update Tape & Reel Information