



HY16F188

Datasheet

High Precision Mixed-Signal Controller
Embedded 65nV Resolution ADC
32-bit Low Power MCU
64K Byte Flash ROM

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1. Features

Digital Circuit

- 32-bit MCU 1T Andes Core N801
- C Compiler & User Friendly Development Tools
- 2.2V to 3.6V operational voltage.
- -40 to 85°C operational environment
- Low power operation:
 - MCU: 350uA/MIPS@3.3V
 - Low speed mode: 10uA@35KHz/2&3.3V
 - Sleep mode: 2.5uA@3.3V
- 64K Byte Flash ROM
- 8K Byte SRAM
- 16-bit PWM controller
- I2C/SPI/ UART communication Hardware IP
- RTC Hardware IP
- Low voltage detection/BOR circuit
- Programmable Digital I/O Ports

Analog Circuit

- An ultra low noise 24-bit SD ADC
 - Down to 65nVrms input refer noise
 - Conversion rate up to 350KSPS
 - Input amplification gain up to 128
 - Operation voltage 2.4V to 3.6V
- External High Speed Oscillator Max 16MHz
- External Low Speed Oscillator Mode 32768Hz
- Internal High Speed Oscillator Max 20MHz
- Internal Low Speed Oscillator 35KHz
- Power management
 - Charge Pump regulation
 - Build-in selectable VDDA voltage LDO
 - 1.2V Band gap reference output
- A 8-bit resistor ladders can be used as 8-bit DAC
 - Programmable potentiometer
 - Monotonic guarantee
- A rail-to-rail operation amplifier
 - CMOS input, 1MHz bandwidth
 - Can use as comparator
- Multi-function Analog Comparator
 - Support touch key

2. Pin Definition

2.1 HY16F188 Series Pin Introduction

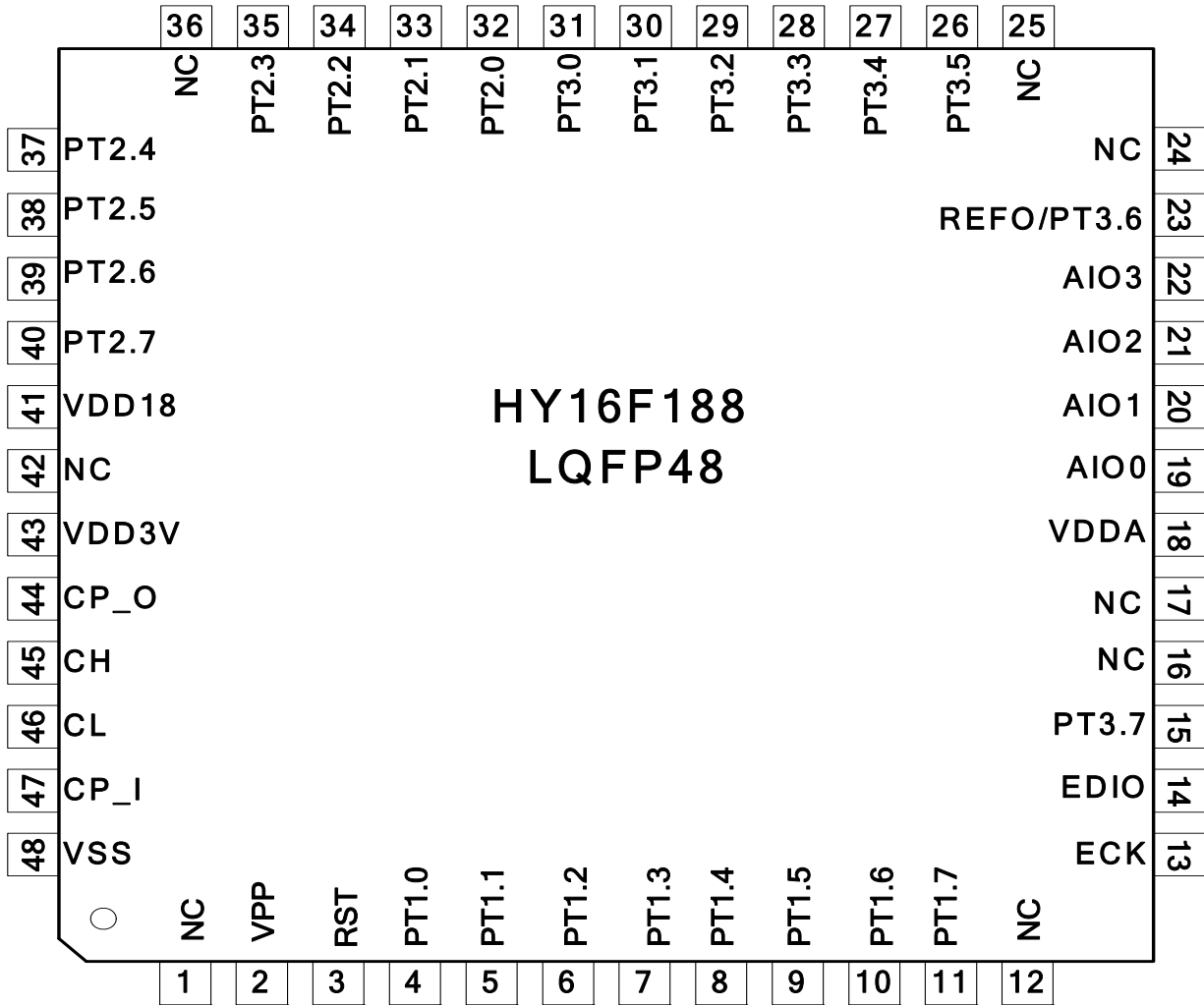


Figure 2-1 HY16F188 LQFP48 Pin Diagram

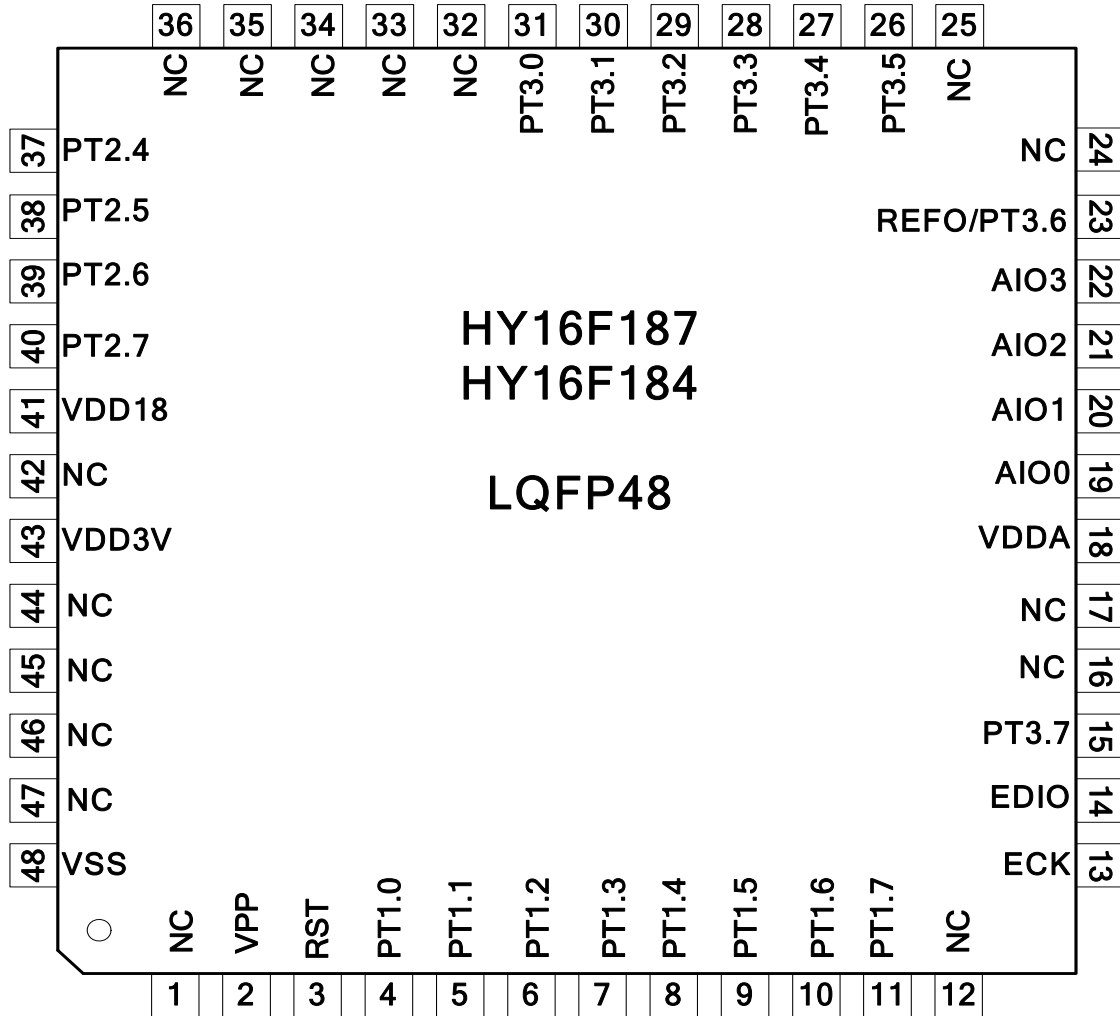


Figure 2-2 HY16F187/184 LQFP48 Pin Diagram

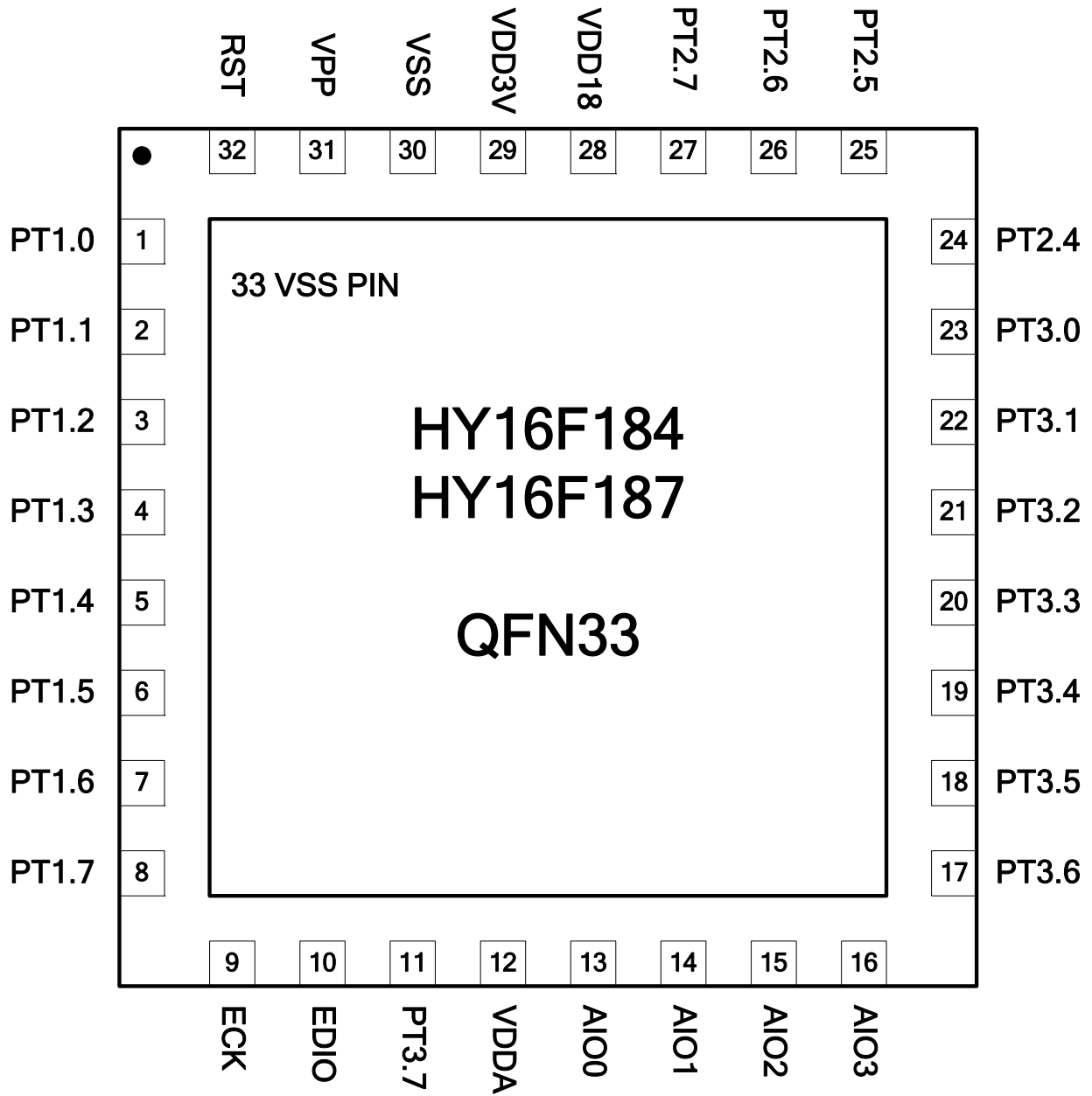


Figure 2-3 HY16F187/184 QFN33 Pin Diagram

2.2 Pin Name List

2.2.1 HY16F188 LQFP48

PIN	TYPE ⁽¹⁾	NAME	DESCRIPTION
1	NC	NC	Not connect
2	PI	VPP	Reserve (can't connect to any pin)
3	I	RST	Reset IC PIN
4	IO	PT1.0	Digital Input/ Output PIN
	AI	CH1	Comparator Analog Input PIN
	I	INT1.0	Interrupt Source INT1.0
	O	PWM0_1	PWM0_1 Output PIN
	I	CS_1	SPI Communication Interface PIN CS_1
	IO	TX_1	EUART Communication Interface PIN TX_1
	I	TCI1_1	Timer C Capture Module PIN TCI1_1
	IO	SCL_1	I2C Communication Interface PIN SCL_1
5	IO	PT1.1	Digital Input/ Output PIN
	AI	CH2	Comparator Analog Input PIN
	I	INT1.1	Interrupt Source INT1.1
	O	PWM1_1	PWM1_1 Output PIN
	I	CK_1	SPI Communication Interface PIN CK_1
	I	RX_1	EUART Communication Interface PIN RX_1
	I	TCI2_1	Timer C Capture Module PIN TCI2_1
	IO	SDA_1	I2C Communication Interface PIN SDA_1
6	IO	PT1.2	Digital Input/ Output PIN
	AI	CH3	Comparator Analog Input PIN
	I	INT1.2	Interrupt Source INT1.2
	O	PWM0_2	PWM0_2 Output PIN
	I	MISO_1	SPI Communication Interface PIN MISO_1
	IO	TX_2	EUART Communication Interface PIN TX_2
	I	TCI1_2	Timer C Capture Module PIN TCI1_2
	IO	SCL_2	I2C Communication Interface PIN SCL_2
7	IO	PT1.3	Digital Input/ Output PIN
	AI	CL1	Comparator Analog Input PIN
	I	INT1.3	Interrupt Source INT1.3
	O	PWM1_2	PWM1_2 Output PIN
	O	MOSI_1	SPI Communication Interface MOSI_1
	I	RX_2	EUART Communication Interface RX_2
	I	TCI2_2	Timer C Capture Module PIN TCI2_2
	IO	SDA_2	I2C Communication Interface PIN SDA_2
8	IO	PT1.4	Digital Input/ Output PIN
	AI	CL2	Comparator Analog Input PIN
	I	INT1.4	Interrupt Source INT1.4
	O	PWM0_3	PWM0_3 Output PIN
	I	CS_2	SPI Communication Interface CS_2
	IO	TX_3	EUART Communication Interface TX_2
	I	TCI1_3	Timer C Capture Module PIN TCI1_3
	IO	SCL_3	I2C Communication Interface PIN SCL_3

PIN	TYPE ⁽¹⁾	NAME	DESCRIPTION	
9	IO	PT1.5	Digital Input/ Output PIN	
	AI	CL3	Comparator Analog Input PIN	
	I	INT1.5	Interrupt Source INT1.5	
	O	PWM1_3	PWM1_3 Output PIN	
	I	CK_2	SPI Communication Interface PIN CK_2	
	I	RX_3	EUART Communication Interface PIN RX_3	
	I	TCI2_3	Timer C Capture Module PIN TCI2_3	
10	IO	SDA_3	I2C Communication Interface PIN SDA_3	
	IO	PT1.6	Digital Input/Output PIN	
	AI	CL4	Comparator Analog Input PIN	
	I	INT1.6	Interrupt Source INT1.6	
	O	PWM0_4	PWM0_4 Output PIN	
	I	MISO_2	SPI Communication Interface PIN MISO_2	
	IO	TX_4	EUART Communication Interface PIN TX_4	
11	I	TCI1_4	Timer C Capture Module PIN TCI1_4	
	IO	SCL_4	I2C Communication Interface PIN SCL_4	
	IO	PT1.7	Digital Input/ Output PIN	
	AO	CMPO1	Comparator Analog Output PIN	
	I	INT1.7	Interrupt Source INT1.7	
	O	PWM1_4	PWM1_4 Output PIN	
	O	MOSI_2	SPI Communication Interface PIN MOSI_2	
12	I	RX_4	EUART Communication Interface PIN RX_4	
	I	TCI2_4	Timer C Capture Module PIN TCI2_4	
	IO	SDA_4	I2C Communication Interface PIN SDA_4	
	12	NC	NC	Not Connect
	13	I	ECK	Embedded Debug Module (EDM) Clock Input PIN
	14	IO	EDIO	Embedded Debug Module (EDM) Data Input/ Output PIN
	15	IO	PT3.7	Digital Input/ Output PIN
AO		OPO1	RAIL-TO-RAIL OPAMP Output PIN	
16	NC	NC	Not Connect	
17	NC	NC	Not Connect	
18	PIO	VDDA	Analog Power Supply, LDO Output, or Analog Power Input	
19	AI	AIO0	Analog Input Signal Port 0	
20	AI	AIO1	Analog Input Signal Port 1	
21	AI	AIO2	Analog Input Signal Port 2	
22	AI	AIO3	Analog Input Signal Port 3	
23	IO	PT3.6	Digital Input/ Output PIN	
	PIO	REFO	Analog Reference Voltage	
24	NC	NC	Not Connect	
25	NC	NC	Not Connect	
26	IO	PT3.5	Digital Input/ Output PIN	
	AI	AIO7	Analog Input Signal Port 7	
27	IO	PT3.4	Digital Input/ Output PIN	
	AI	AIO6	Analog Input Signal Port 6	
28	IO	PT3.3	Digital Input/ Output PIN	
	AI	AIO5	Analog Input Signal Port 5	

PIN	TYPE ⁽¹⁾	NAME	DESCRIPTION
29	IO	PT3.2	Digital Input/ Output PIN
	AI	AIO4	Analog input signal port 4
30	IO	PT3.1	Digital Input/ Output PIN
	DO	OPOD2	RAIL-TO-RAIL OPAMP Output
	AO	DAO	8-bit Resistance Ladders Output pin
31	IO	PT3.0	Digital Input/ Output PIN
	DO	OPOD1	RAIL-TO-RAIL OPAMP Output
32	IO	PT2.0	Digital Input/Output PIN
	I	INT2.0	Interrupt Source INT 2.0
	O	PWM0_5	PWM0_5 Output PIN
	I	CS_3	SPI Communication Interface PIN CS_3
	IO	TX_5	EUART Communication Interface PIN TX_5
	I	TCI1_5	Timer C Capture Module PIN TCI1_5
	IO	SCL_5	I2C Communication Interface PIN SCL_5
33	IO	PT2.1	Digital Input/ Output PIN
	I	INT2.1	Interrupt Source INT 2.1
	O	PWM1_5	PWM1_5 Output PIN
	I	CK_3	SPI Communication Interface PIN CK_3
	I	RX_5	EUART Communication Interface PIN RX_5
	I	TCI2_5	Timer C Capture Module PIN TCI2_5
	IO	SDA_5	I2C Communication Interface PIN SDA_5
34	IO	PT2.2	Digital Input/Output PIN
	I	INT2.2	Interrupt Source INT 2.2
	O	PWM0_6	PWM0_6 Output PIN
	I	MISO_3	SPI Communication Interface PIN MISO_3
	IO	TX_6	EUART Communication Interface PIN TX_6
	IO	SCL_6	I2C Communication Interface PIN SCL_6
35	IO	PT2.3	Digital Input/ Output PIN
	I	INT2.3	Interrupt Source INT 2.3
	O	PWM1_6	PWM1_6 Output PIN
	O	MOSI_3	SPI Communication Interface PIN MOSI_3
	I	RX_6	EUART Communication Interface PIN RX_6
	I	TCI2_6	Timer C Capture Module PIN TCI2_6
	IO	SDA_6	I2C Communication Interface PIN SDA_6
36	NC	NC	Not connect
37	IO	PT2.4	Digital Input/Output PIN
	XI	LS_XIN	LS_XIN
	I	INT2.4	Interrupt Source INT 2.4
	O	PWM0_7	PWM0_7 Output PIN
	I	CS_4	SPI Communication Interface PIN CS_4
	IO	TX_7	EUART Communication Interface PIN TX_7
	IO	SCL_7	I2C Communication Interface PIN SCL_7

PIN	TYPE ⁽¹⁾	NAME	DESCRIPTION
38	IO	PT2.5	Digital Input/ Output PIN
	XO	LS_XOUT	LS_XOUT
	I	INT2.5	Interrupt Source INT 2.5
	O	PWM1_7	PWM1_7 Output PIN
	I	CK_4	SPI Communication Interface PIN CK_4
	I	RX_7	EUART Communication Interface PIN RX_7
	I	TCI2_7	Timer C Capture Module PIN TCI2_7
	IO	SDA_7	I2C Communication Interface PIN SDA_7
39	IO	PT2.6	Digital Input/Output PIN
	XI	HS_XIN	HS_XIN
	I	INT2.6	Interrupt Source INT 2.6
	O	PWM0_8	PWM0_8 Output PIN
	I	MISO_4	SPI Communication Interface PIN MISO_4
	IO	TX_8	EUART Communication Interface PIN TX_7
	IO	SCL_8	I2C Communication Interface PIN SCL_8
40	IO	PT2.7	Digital Input/ Output PIN
	XO	HS_XOUT	HS_XOUT
	I	INT2.7	Interrupt Source INT 2.7
	O	PWM1_8	PWM1_8 Output PIN
	O	MOSI_4	SPI Communication Interface PIN MOSI_4
	I	RX_8	EUART Communication Interface PIN RX_8
	I	TCI2_8	Timer C Capture Module PIN TCI2_8
	IO	SDA_8	I2C Communication Interface PIN SDA_8
41	PO	VDD18	Digital Power Supply. LDO Output 1.8V
42	NC	NC	Not connect
43	PI	VDD3V	Power Input For System
44	PO	CP_O	Charge Pump 3V Out
45	PIO	CH	Charge Pump Capacitor High Voltage Plate
46	PIO	CL	Charge Pump Capacitor Low Voltage Plate
47	PI	CP_I	Charge Pump Power Input
48	P	VSS	Power Ground Pad

Table 2-1 HY16F188 LQFP48 Pin Definition and Function description

(1)TYPE Definition :

- I = Digital Input
- O = Digital Output
- OD = Open-drain Output
- AI = Analog Input
- AO = Analog Output
- P = Power Connection

2.2.2 HY16F187/184 LQFP48

PIN	TYPE ⁽¹⁾	NAME	DESCRIPTION
1	NC	NC	Not connect
2	PI	VPP	Reserve (can't connect to any pin)
3	I	RST	Reset IC PIN
4	IO	PT1.0	Digital Input/ Output PIN
	AI	CH1	Comparator Analog Input PIN
	I	INT1.0	Interrupt Source INT1.0
	O	PWM0_1	PWM0_1 Output PIN
	I	CS_1	SPI Communication Interface PIN CS_1
	IO	TX_1	EUART Communication Interface PIN TX_1
	I	TCI1_1	Timer C Capture Module PIN TCI1_1
	IO	SCL_1	I2C Communication Interface PIN SCL_1
5	IO	PT1.1	Digital Input/ Output PIN
	AI	CH2	Comparator Analog Input PIN
	I	INT1.1	Interrupt Source INT1.1
	O	PWM1_1	PWM1_1 Output PIN
	I	CK_1	SPI Communication Interface PIN CK_1
	I	RX_1	EUART Communication Interface PIN RX_1
	I	TCI2_1	Timer C Capture Module PIN TCI2_1
	IO	SDA_1	I2C Communication Interface PIN SDA_1
6	IO	PT1.2	Digital Input/ Output PIN
	AI	CH3	Comparator Analog Input PIN
	I	INT1.2	Interrupt Source INT1.2
	O	PWM0_2	PWM0_2 Output PIN
	I	MISO_1	SPI Communication Interface PIN MISO_1
	IO	TX_2	EUART Communication Interface PIN TX_2
	I	TCI1_2	Timer C Capture Module PIN TCI1_2
	IO	SCL_2	I2C Communication Interface PIN SCL_2
7	IO	PT1.3	Digital Input/ Output PIN
	AI	CL1	Comparator Analog Input PIN
	I	INT1.3	Interrupt Source INT1.3
	O	PWM1_2	PWM1_2 Output PIN
	O	MOSI_1	SPI Communication Interface MOSI_1
	I	RX_2	EUART Communication Interface RX_2
	I	TCI2_2	Timer C Capture Module PIN TC12_2
	IO	SDA_2	I2C Communication Interface PIN SDA_2
8	IO	PT1.4	Digital Input/ Output PIN
	AI	CL2	Comparator Analog Input PIN
	I	INT1.4	Interrupt Source INT1.4
	O	PWM0_3	PWM0_3 Output PIN
	I	CS_2	SPI Communication Interface CS_2
	IO	TX_3	EUART Communication Interface TX_2
	I	TCI1_3	Timer C Capture Module PIN TCI1_3
	IO	SCL_3	I2C Communication Interface PIN SCL_3

PIN	TYPE ⁽¹⁾	NAME	DESCRIPTION
9	IO	PT1.5	Digital Input/ Output PIN
	AI	CL3	Comparator Analog Input PIN
	I	INT1.5	Interrupt Source INT1.5
	O	PWM1_3	PWM1_3 Output PIN
	I	CK_2	SPI Communication Interface PIN CK_2
	I	RX_3	EUART Communication Interface PIN RX_3
	I	TCI2_3	Timer C Capture Module PIN TCI2_3
	IO	SDA_3	I2C Communication Interface PIN SDA_3
10	IO	PT1.6	Digital Input/Output PIN
	AI	CL4	Comparator Analog Input PIN
	I	INT1.6	Interrupt Source INT1.6
	O	PWM0_4	PWM0_4 Output PIN
	I	MISO_2	SPI Communication Interface PIN MISO_2
	IO	TX_4	EUART Communication Interface PIN TX_4
	I	TCI1_4	Timer C Capture Module PIN TCI1_4
	IO	SCL_4	I2C Communication Interface PIN SCL_4
11	IO	PT1.7	Digital Input/ Output PIN
	AO	CMPO1	Comparator Analog Output PIN
	I	INT1.7	Interrupt Source INT1.7
	O	PWM1_4	PWM1_4 Output PIN
	O	MOSI_2	SPI Communication Interface PIN MOSI_2
	I	RX_4	EUART Communication Interface PIN RX_4
	I	TCI2_4	Timer C Capture Module PIN TCI2_4
	IO	SDA_4	I2C Communication Interface PIN SDA_4
12	NC	NC	Not Connect
13	I	ECK	Embedded Debug Module (EDM) Clock Input PIN
14	IO	EDIO	Embedded Debug Module (EDM) Data Input/ Output PIN
15	IO	PT3.7	Digital Input/ Output PIN
	AO	OPOD1	RAIL-TO-RAIL OPAMP Output PIN
16	NC	NC	Not Connect
17	NC	NC	Not Connect
18	PIO	VDDA	Analog Power Supply, LDO Output, or Analog Power Input
19	AI	AIO0	Analog Input Signal Port 0
20	AI	AIO1	Analog Input Signal Port 1
21	AI	AIO2	Analog Input Signal Port 2
22	AI	AIO3	Analog Input Signal Port 3
23	IO	PT3.6	Digital Input/ Output PIN
	PIO	REFO	Analog Reference Voltage
24	NC	NC	Not Connect
25	NC	NC	Not Connect
26	IO	PT3.5	Digital Input/ Output PIN
	AI	AIO7	Analog Input Signal Port 7
27	IO	PT3.4	Digital Input/ Output PIN
	AI	AIO6	Analog Input Signal Port 6
28	IO	PT3.3	Digital Input/ Output PIN
	AI	AIO5	Analog Input Signal Port 5

PIN	TYPE ⁽¹⁾	NAME	DESCRIPTION
29	IO	PT3.2	Digital Input/ Output PIN
	AI	AIO4	Analog input signal port 4
30	IO	PT3.1	Digital Input/ Output PIN
	DO	OPOD2	RAIL-TO-RAIL OPAMP Output
	AO	DAO	8-bit Resistance Ladders Output
31	IO	PT3.0	Digital Input/ Output PIN
	DO	OPOD1	RAIL-TO-RAIL OPAMP Output
32	NC	NC	Not connect
33	NC	NC	Not connect
34	NC	NC	Not connect
35	NC	NC	Not connect
36	NC	NC	Not connect
37	IO	PT2.4	Digital Input/Output PIN
	XI	LS_XIN	LS_XIN
	I	INT2.4	Interrupt Source INT 2.4
	O	PWM0_7	PWM0_7 Output PIN
	I	CS_4	SPI Communication Interface PIN CS_4
	IO	TX_7	EUART Communication Interface PIN TX_7
	I	TCI1_7	Timer C Capture Module PIN TCI1_7
	IO	SCL_7	I2C Communication Interface PIN SCL_7
38	IO	PT2.5	Digital Input/ Output PIN
	XO	LS_XOUT	LS_XOUT
	I	INT2.5	Interrupt Source INT 2.5
	O	PWM1_7	PWM1_7 Output PIN
	I	CK_4	SPI Communication Interface PIN CK_4
	I	RX_7	EUART Communication Interface PIN RX_7
	I	TCI2_7	Timer C Capture Module PIN TCI2_7
	IO	SDA_7	I2C Communication Interface PIN SDA_7
39	IO	PT2.6	Digital Input/Output PIN
	XI	HS_XIN	HS_XIN
	I	INT2.6	Interrupt Source INT 2.6
	O	PWM0_8	PWM0_8 Output PIN
	I	MISO_4	SPI Communication Interface PIN MISO_4
	IO	TX_8	EUART Communication Interface PIN TX_7
	I	TCI1_8	Timer C Capture Module PIN TCI1_8
	IO	SCL_8	I2C Communication Interface PIN SCL_8
40	IO	PT2.7	Digital Input/ Output PIN
	XO	HS_XOUT	HS_XOUT
	I	INT2.7	Interrupt Source INT 2.7
	O	PWM1_8	PWM1_8 Output PIN
	O	MOSI_4	SPI Communication Interface PIN MOSI_4
	I	RX_8	EUART Communication Interface PIN RX_8
	I	TCI2_8	Timer C Capture Module PIN TCI2_8
	IO	SDA_8	I2C Communication Interface PIN SDA_8
41	PO	VDD18	Digital Power Supply. LDO Output 1.8V
42	NC	NC	Not connect
43	PI	VDD3V	Power Input For System
44	NC	NC	Not connect
45	NC	NC	Not connect
46	NC	NC	Not connect
47	NC	NC	Not connect
48	P	VSS	Power Ground Pad

Table 2-2 HY16F187/184 LQFP48 Pin Definition and Function description

2.2.3 HY16F187/184 QFN33

PIN	TYPE ⁽¹⁾	NAME	DESCRIPTION
1	IO	PT1.0	Digital Input/ Output PIN
	AI	CH1	Comparator Analog Input PIN
	I	INT1.0	Interrupt Source INT1.0
	O	PWM0_1	PWM0_1 Output PIN
	I	CS_1	SPI Communication Interface PIN CS_1
	IO	TX_1	EUART Communication Interface PIN TX_1
	I	TCI1_1	Timer C Capture Module PIN TCI1_1
	IO	SCL_1	I2C Communication Interface PIN SCL_1
2	IO	PT1.1	Digital Input/ Output PIN
	AI	CH2	Comparator Analog Input PIN
	I	INT1.1	Interrupt Source INT1.1
	O	PWM1_1	PWM1_1 Output PIN
	I	CK_1	SPI Communication Interface PIN CK_1
	I	RX_1	EUART Communication Interface PIN RX_1
	I	TCI2_1	Timer C Capture Module PIN TCI2_1
	IO	SDA_1	I2C Communication Interface PIN SDA_1
3	IO	PT1.2	Digital Input/ Output PIN
	AI	CH3	Comparator Analog Input PIN
	I	INT1.2	Interrupt Source INT1.2
	O	PWM0_2	PWM0_2 Output PIN
	I	MISO_1	SPI Communication Interface PIN MISO_1
	IO	TX_2	EUART Communication Interface PIN TX_2
	I	TCI1_2	Timer C Capture Module PIN TCI1_2
	IO	SCL_2	I2C Communication Interface PIN SCL_2
4	IO	PT1.3	Digital Input/ Output PIN
	AI	CL1	Comparator Analog Input PIN
	I	INT1.3	Interrupt Source INT1.3
	O	PWM1_2	PWM1_2 Output PIN
	O	MOSI_1	SPI Communication Interface MOSI_1
	I	RX_2	EUART Communication Interface RX_2
	I	TCI2_2	Timer C Capture Module PIN TC12_2
	IO	SDA_2	I2C Communication Interface PIN SDA_2
5	IO	PT1.4	Digital Input/ Output PIN
	AI	CL2	Comparator Analog Input PIN
	I	INT1.4	Interrupt Source INT1.4
	O	PWM0_3	PWM0_3 Output PIN
	I	CS_2	SPI Communication Interface CS_2
	IO	TX_3	EUART Communication Interface TX_2
	I	TCI1_3	Timer C Capture Module PIN TCI1_3
	IO	SCL_3	I2C Communication Interface PIN SCL_3

PIN	TYPE ⁽¹⁾	NAME	DESCRIPTION
6	IO	PT1.5	Digital Input/ Output PIN
	AI	CL3	Comparator Analog Input PIN
	I	INT1.5	Interrupt Source INT1.5
	O	PWM1_3	PWM1_3 Output PIN
	I	CK_2	SPI Communication Interface PIN CK_2
	I	RX_3	EUART Communication Interface PIN RX_3
	I	TCI2_3	Timer C Capture Module PIN TCI2_3
	IO	SDA_3	I2C Communication Interface PIN SDA_3
7	IO	PT1.6	Digital Input/Output PIN
	AI	CL4	Comparator Analog Input PIN
	I	INT1.6	Interrupt Source INT1.6
	O	PWM0_4	PWM0_4 Output PIN
	I	MISO_2	SPI Communication Interface PIN MISO_2
	IO	TX_4	EUART Communication Interface PIN TX_4
	I	TCI1_4	Timer C Capture Module PIN TCI1_4
	IO	SCL_4	I2C Communication Interface PIN SCL_4
8	IO	PT1.7	Digital Input/ Output PIN
	AO	CMPO1	Comparator Analog Output PIN
	I	INT1.7	Interrupt Source INT1.7
	O	PWM1_4	PWM1_4 Output PIN
	O	MOSI_2	SPI Communication Interface PIN MOSI_2
	I	RX_4	EUART Communication Interface PIN RX_4
	I	TCI2_4	Timer C Capture Module PIN TCI2_4
	IO	SDA_4	I2C Communication Interface PIN SDA_4
9	I	ECK	Embedded Debug Module (EDM) Clock Input PIN
10	IO	EDIO	Embedded Debug Module (EDM) Data Input/ Output PIN
11	IO	PT3.7	Digital Input/ Output PIN
	AO	OPO	RAIL-TO-RAIL OPAMP Output PIN
12	PIO	VDDA	Analog Power Supply, LDO Output, or Analog Power Input
13	AI	AIO0	Analog Input Signal Port 0
14	AI	AIO1	Analog Input Signal Port 1
15	AI	AIO2	Analog Input Signal Port 2
16	AI	AIO3	Analog Input Signal Port 3
17	IO	PT3.6	Digital Input/ Output PIN
	PIO	REFO	Analog Reference Voltage
18	IO	PT3.5	Digital Input/ Output PIN
	AI	AIO7	Analog Input Signal Port 7
19	IO	PT3.4	Digital Input/ Output PIN
	AI	AIO6	Analog Input Signal Port 6
20	IO	PT3.3	Digital Input/ Output PIN
	AI	AIO5	Analog Input Signal Port 5

PIN	TYPE ⁽¹⁾	NAME	DESCRIPTION
21	IO	PT3.2	Digital Input/ Output PIN
	AI	AIO4	Analog input signal port 4
22	IO	PT3.1	Digital Input/ Output PIN
	DO	OPOD2	RAIL-TO-RAIL OPAMP Output
	AO	DAO	8-bit Resistance Ladders Output
23	IO	PT3.0	Digital Input/ Output PIN
	DO	OPOD1	RAIL-TO-RAIL OPAMP Output
24	IO	PT2.4	Digital Input/Output PIN
	XI	LS_XIN	LS_XIN
	I	INT2.4	Interrupt Source INT 2.4
	O	PWM0_7	PWM0_7 Output PIN
	I	CS_4	SPI Communication Interface PIN CS_4
	IO	TX_7	EUART Communication Interface PIN TX_7
	I	TCI1_7	Timer C Capture Module PIN TCI1_7
	IO	SCL_7	I2C Communication Interface PIN SCL_7
25	IO	PT2.5	Digital Input/ Output PIN
	XO	LS_XOUT	LS_XOUT
	I	INT2.5	Interrupt Source INT 2.5
	O	PWM1_7	PWM1_7 Output PIN
	I	CK_4	SPI Communication Interface PIN CK_4
	I	RX_7	EUART Communication Interface PIN RX_7
	I	TCI2_7	Timer C Capture Module PIN TCI2_7
	IO	SDA_7	I2C Communication Interface PIN SDA_7
26	IO	PT2.6	Digital Input/Output PIN
	XI	HS_XIN	HS_XIN
	I	INT2.6	Interrupt Source INT 2.6
	O	PWM0_8	PWM0_8 Output PIN
	I	MISO_4	SPI Communication Interface PIN MISO_4
	IO	TX_8	EUART Communication Interface PIN TX_7
	I	TCI1_8	Timer C Capture Module PIN TCI1_8
	IO	SCL_8	I2C Communication Interface PIN SCL_8
27	IO	PT2.7	Digital Input/ Output PIN
	XO	HS_XOUT	HS_XOUT
	I	INT2.7	Interrupt Source INT 2.7
	O	PWM1_8	PWM1_8 Output PIN
	O	MOSI_4	SPI Communication Interface PIN MOSI_4
	I	RX_8	EUART Communication Interface PIN RX_8
	I	TCI2_8	Timer C Capture Module PIN TCI2_8
	IO	SDA_8	I2C Communication Interface PIN SDA_8
28	PO	VDD18	Digital Power Supply. LDO Output 1.8V
29	PI	VDD3V	Power Input For System
30	P	VSS	Power Ground Pad
31	PI	VPP	Reserve (can't connect to any pin)
32	I	RST	Reset IC PIN
33	P	VSS	Power Ground Pad

Table 2-3 HY16F187/184 QFN33 Pin Definition and Function description

2.2.4 Function Priority:

GPIO Port	OSC	Interrupt	Timer C Capture	SPI	IIC	UART	CMP	Analog	Timer B PWM
Priority	0	0	0	1	2	3	4	5	6
PT1.0		INT1.0	TCI1_1	CS_1	SCL_1	TX_1	CH1		PWM0_1
PT1.1		INT1.1	TCI2_1	CK_1	SDA_1	RX_1	CH2		PWM1_1
PT1.2		INT1.2	TCI1_2	MISO_1	SCL_2	TX_2	CH3		PWM0_2
PT1.3		INT1.3	TCI2_2	MOSI_1	SDA_2	RX_2	CL1		PWM1_2
PT1.4		INT1.4	TCI1_3	CS_2	SCL_3	TX_3	CL2		PWM0_3
PT1.5		INT1.5	TCI2_3	CK_2	SDA_3	RX_3	CL3		PWM1_3
PT1.6		INT1.6	TCI1_4	MISO_2	SCL_4	TX_4	CL4		PWM0_4
PT1.7		INT1.7	TCI2_4	MOSI_2	SDA_4	RX_4	CMPO1		PWM1_4
PT2.0		INT2.0	TCI1_5	CS_3	SCL_5	TX_5			PWM0_5
PT2.1		INT2.1	TCI2_5	CK_3	SDA_5	RX_5			PWM1_5
PT2.2		INT2.2	TCI1_6	MISO_3	SCL_6	TX_6			PWM0_6
PT2.3		INT2.3	TCI2_6	MOSI_3	SDA_6	RX_6			PWM1_6
PT2.4	LSXT1	INT2.4	TCI1_7	CS_4	SCL_7	TX_7			PWM0_7
PT2.5	LSXT2	INT2.5	TCI2_7	CK_4	SDA_7	RX_7			PWM1_7
PT2.6	HSXT1	INT2.6	TCI1_8	MISO_4	SCL_8	TX_8			PWM0_8
PT2.7	HSXT2	INT2.7	TCI2_8	MOSI_4	SDA_8	RX_8			PWM1_8
PT3.0							OPOD1		
PT3.1							OPOD2	DAO	
PT3.2								AIO4	
PT3.3								AIO5	
PT3.4								AIO6	
PT3.5								AIO7	
PT3.6								REFO	
PT3.7								OPO	
AIO0								AIO0	
AIO1								AIO1	
AIO2								AIO2	
AIO3								AIO3	

3. Application Circuit

3.1 Bridge Sensor

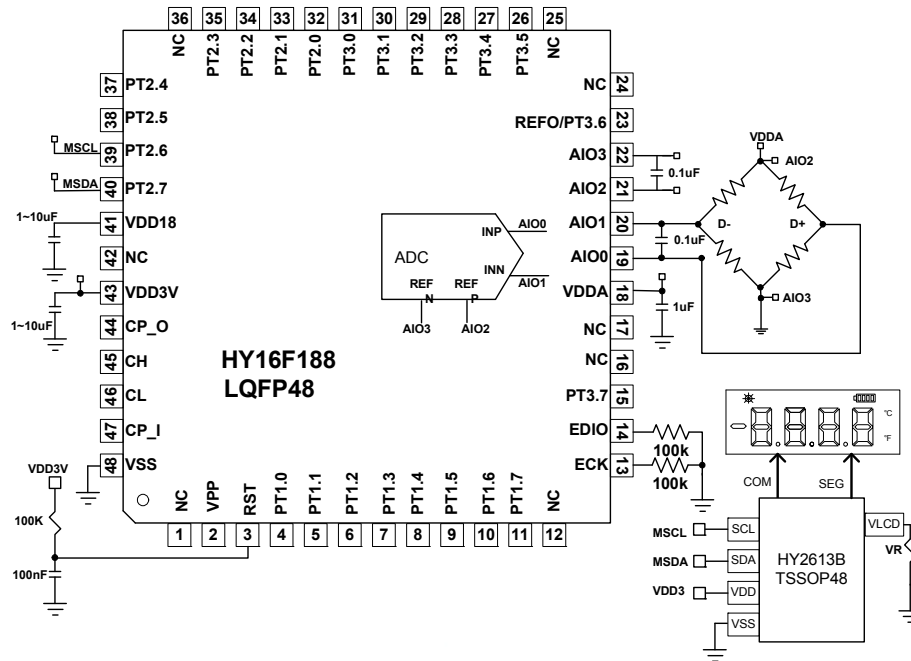


Figure 3-1 Bridge Sensor Circuit

3.3 Electrochemical Sensor

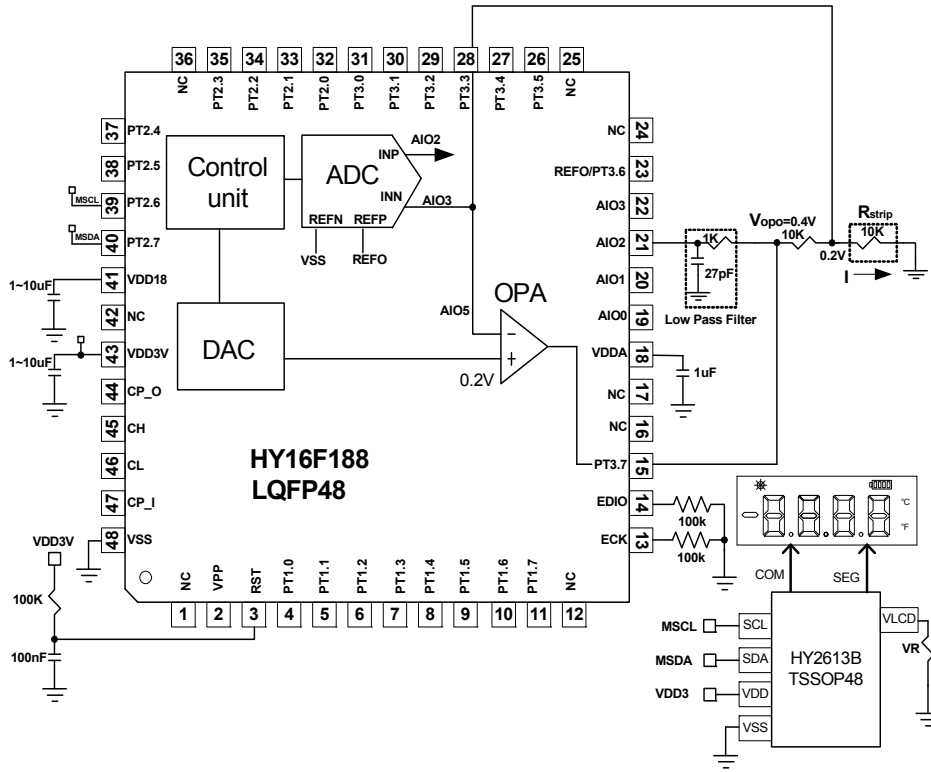


Figure 3-3 Electrochemical Sensor Circuit

3.4 Touch Key Sensor

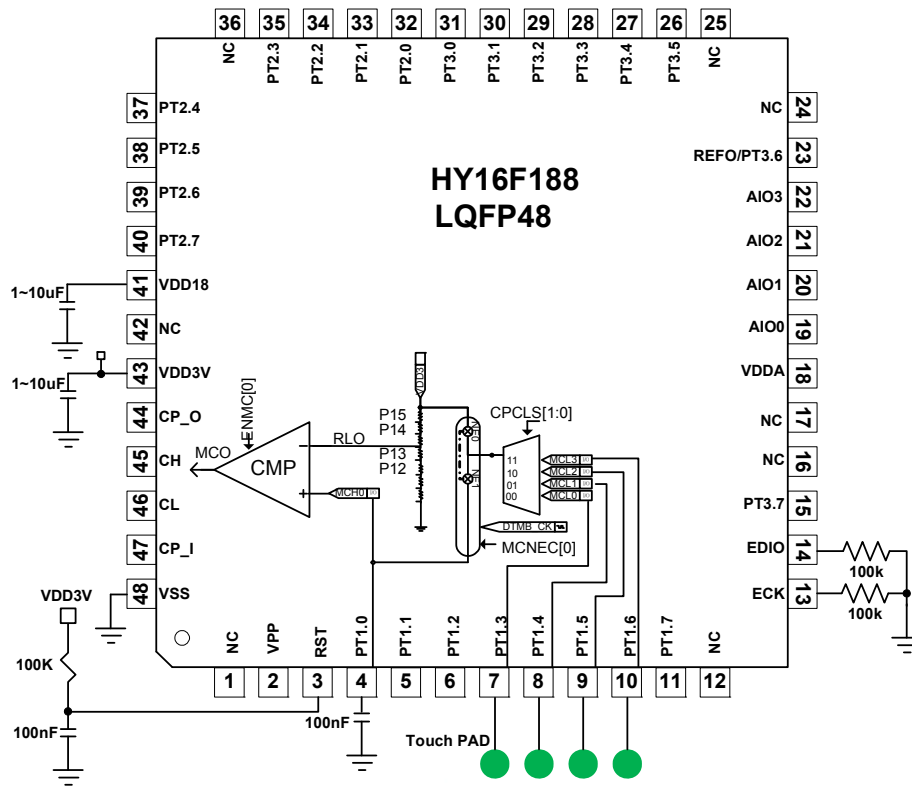


Figure 3-4 Touch Key Sensor Circuit

4. Function Outline

4.1 Internal Block Diagram

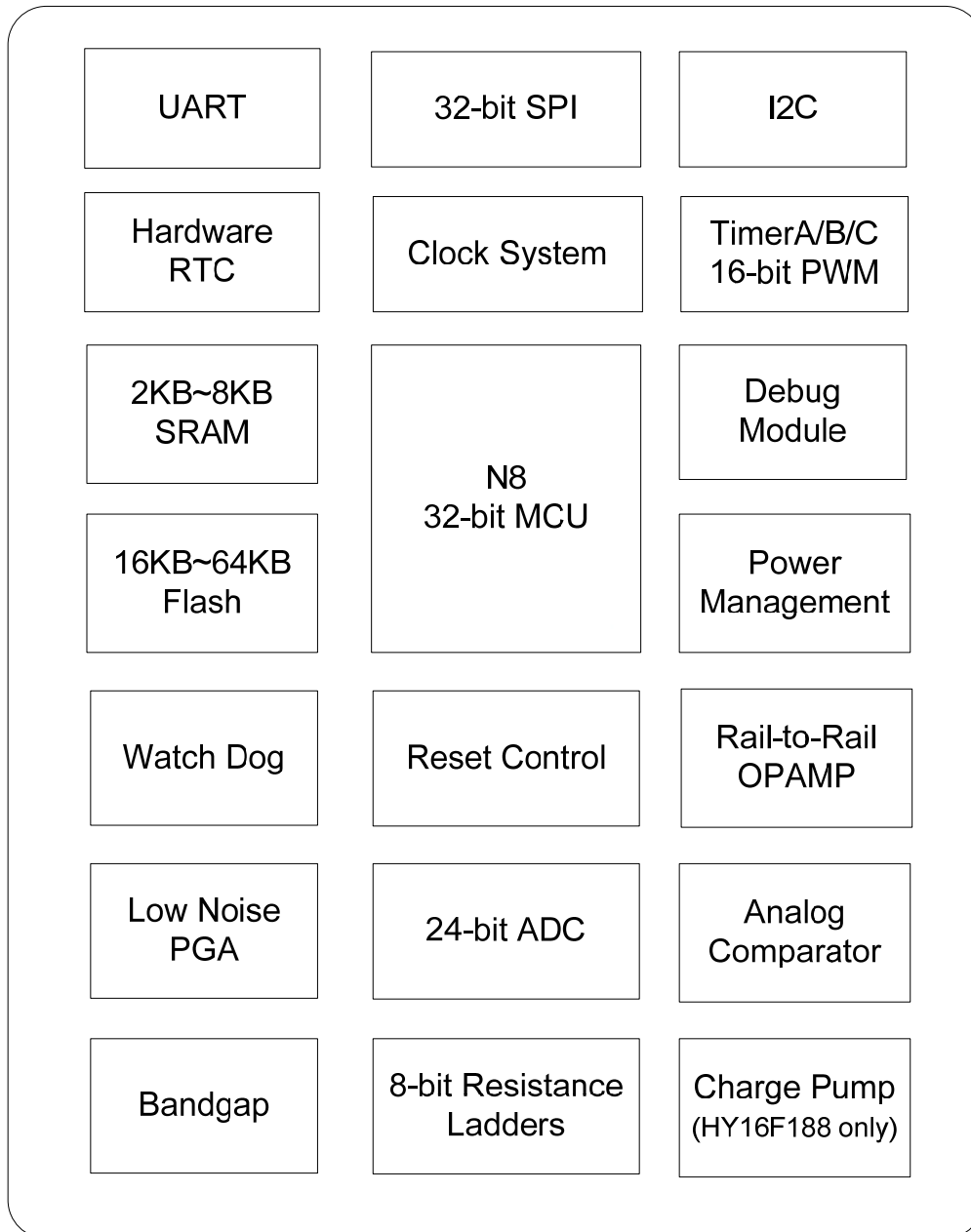


Figure 4-1 Internal Block Diagram

4.2 Building Block Diagram

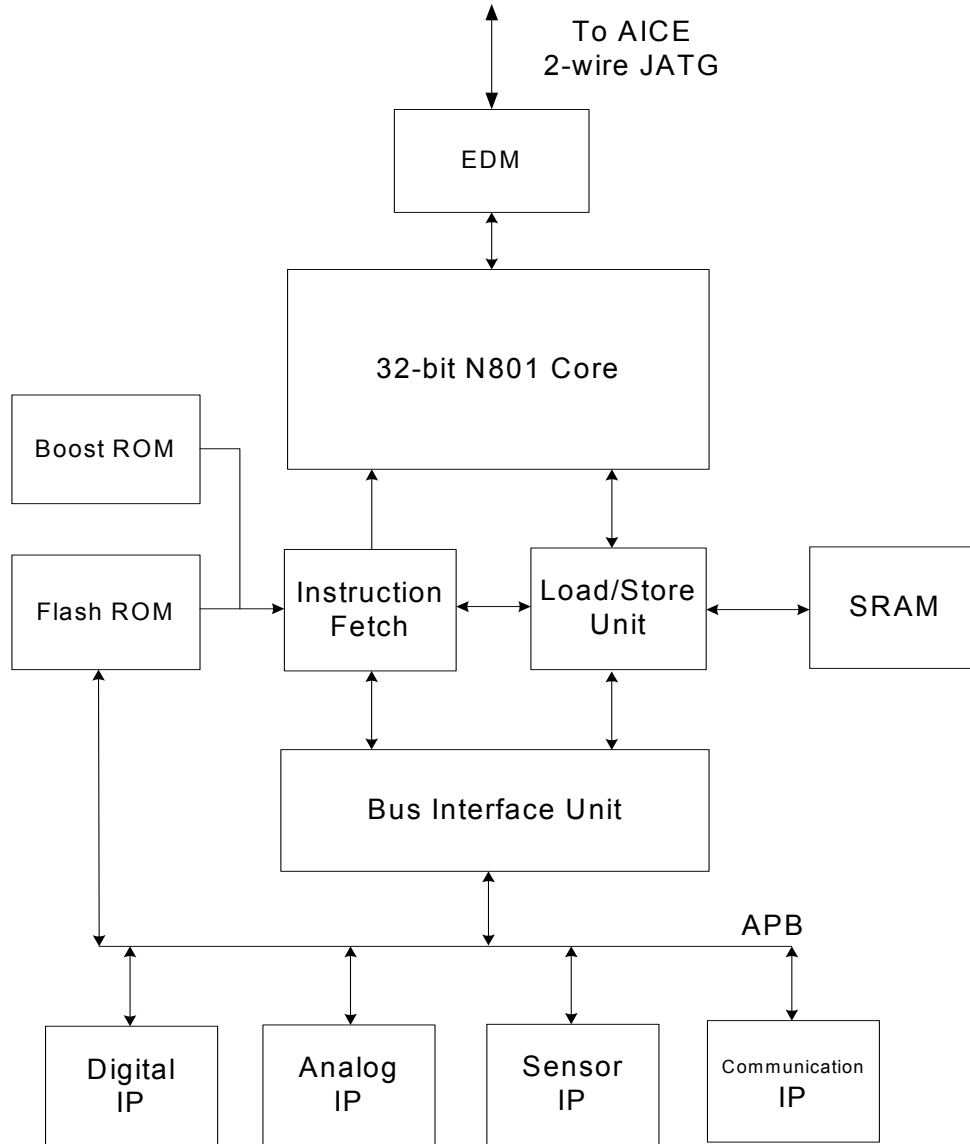
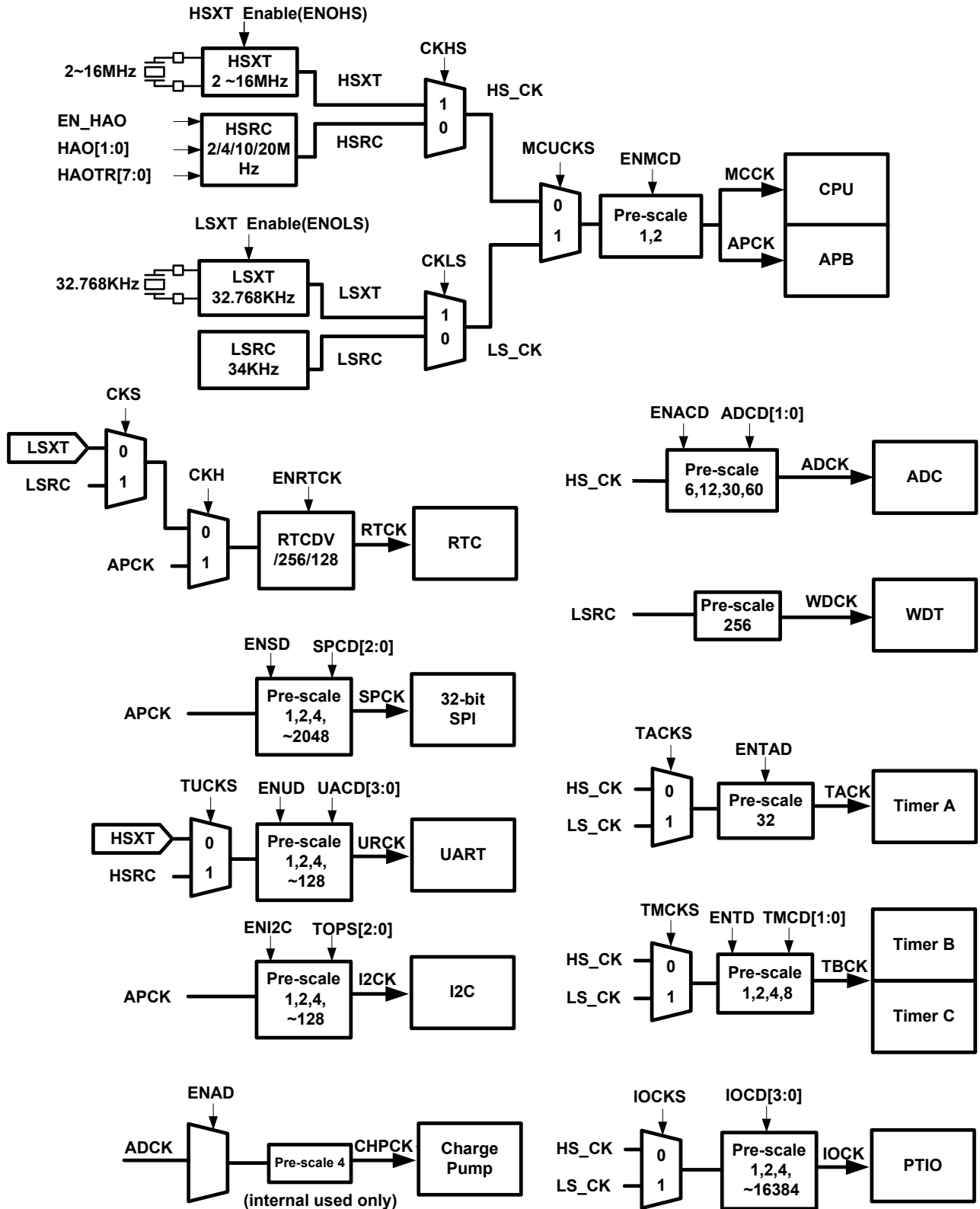


Figure 4-2 Build Block Diagram

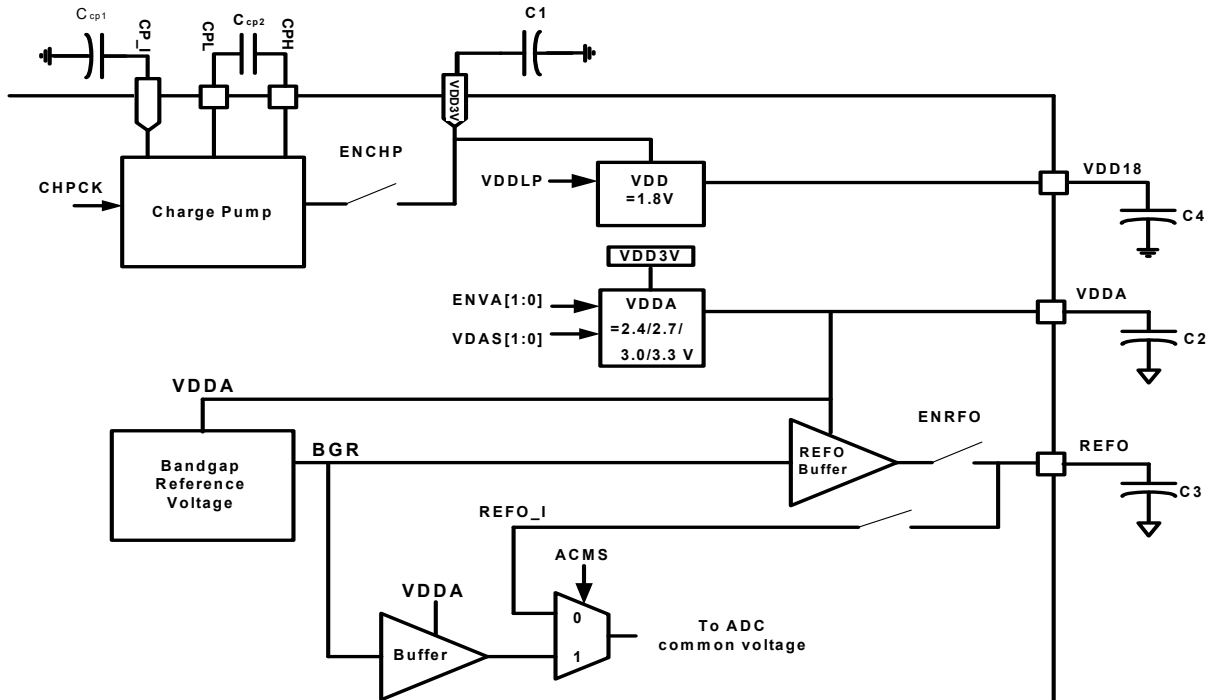
4.3 Supporting Document

NO	File Name	Description
1	UG-HY16F188	HY16F188 User's Manual
2	APD-HY16IDE001	HY16F18x Series IDE Software Manual
3	APD-HY16IDE002	HY16F18x Series IDE Hardware Manual
4	APD-HY16IDE004	HY16F18X C Peripheral Driver Library
5	APD-HY16IDE006	HY16F Series Writer Kit Manual
6	APD-HY16F003	HY16F18X User Manual

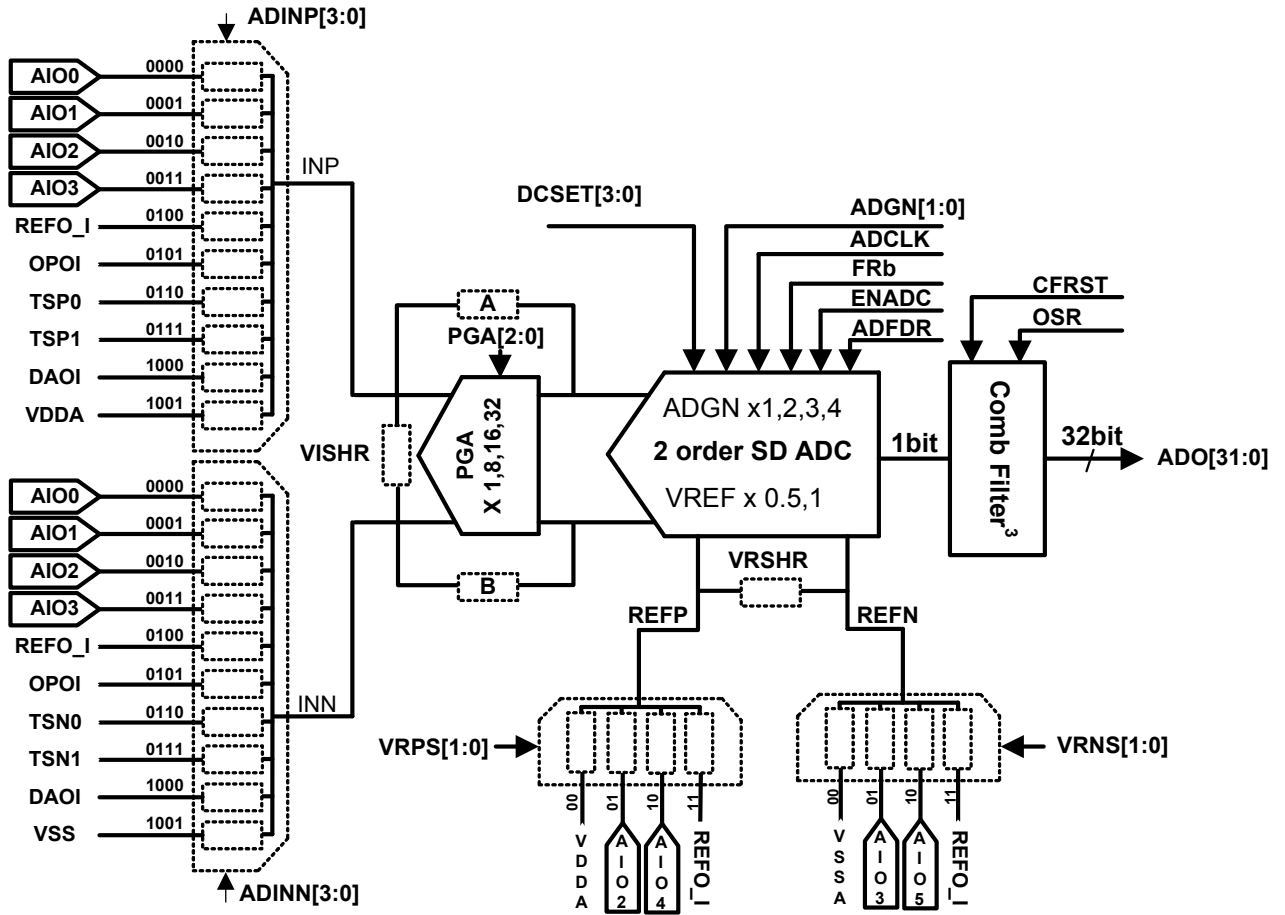
4.4 Clock System Network



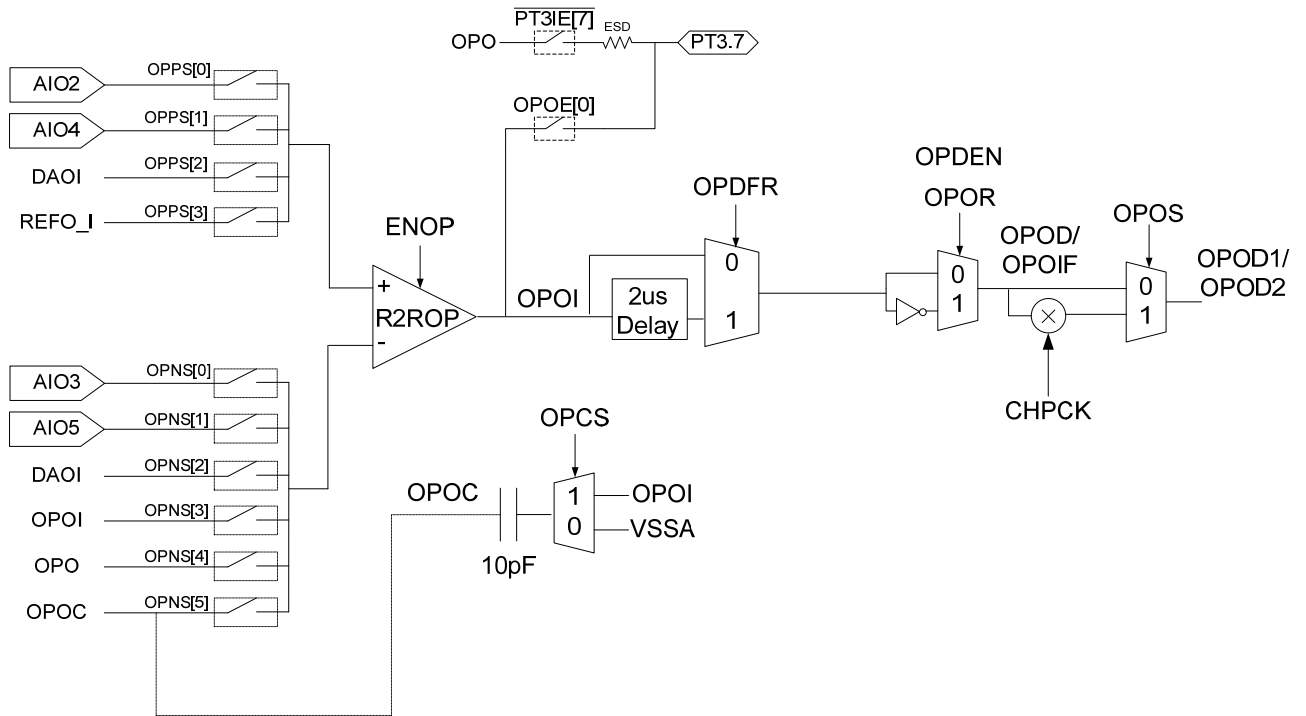
4.5 Power System Network



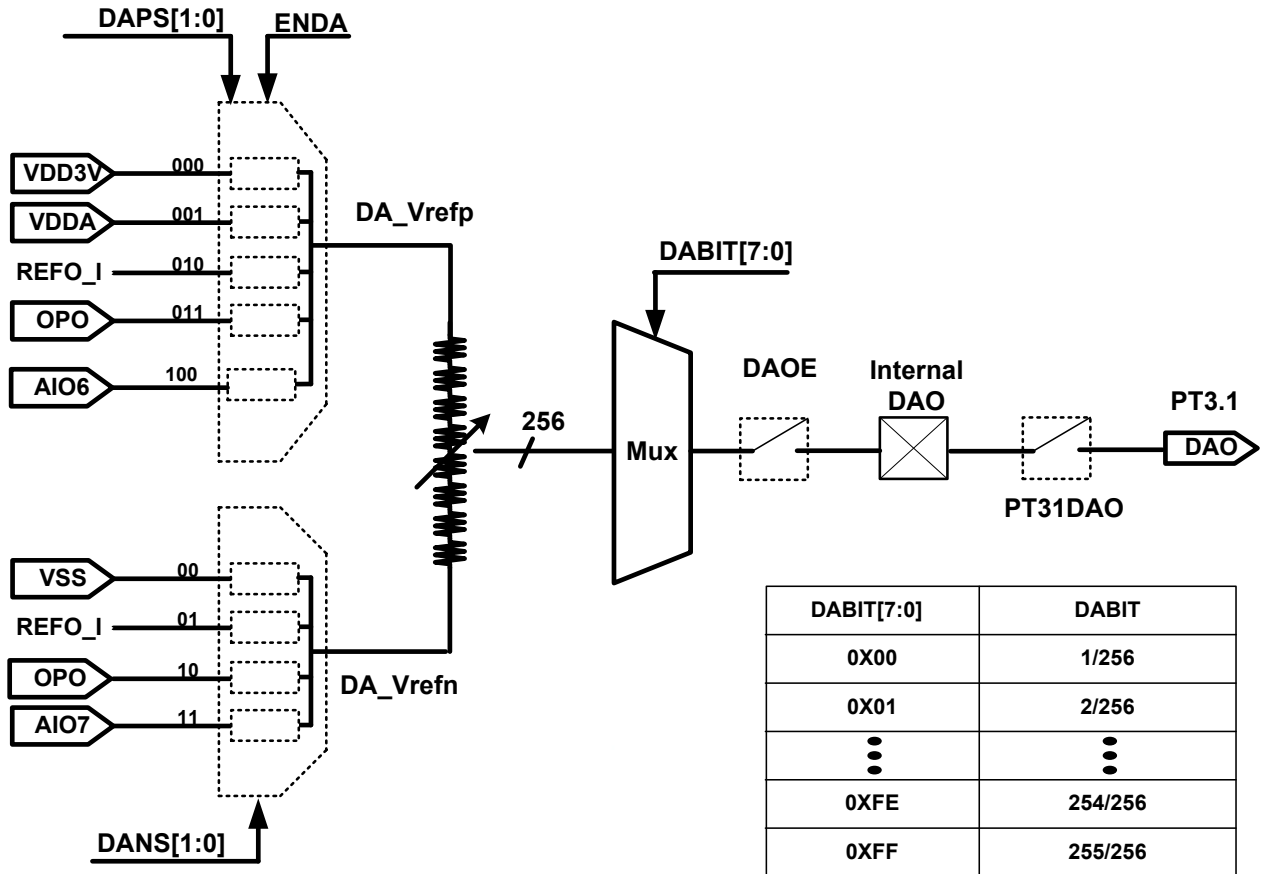
4.6 Σ Δ ADC Network



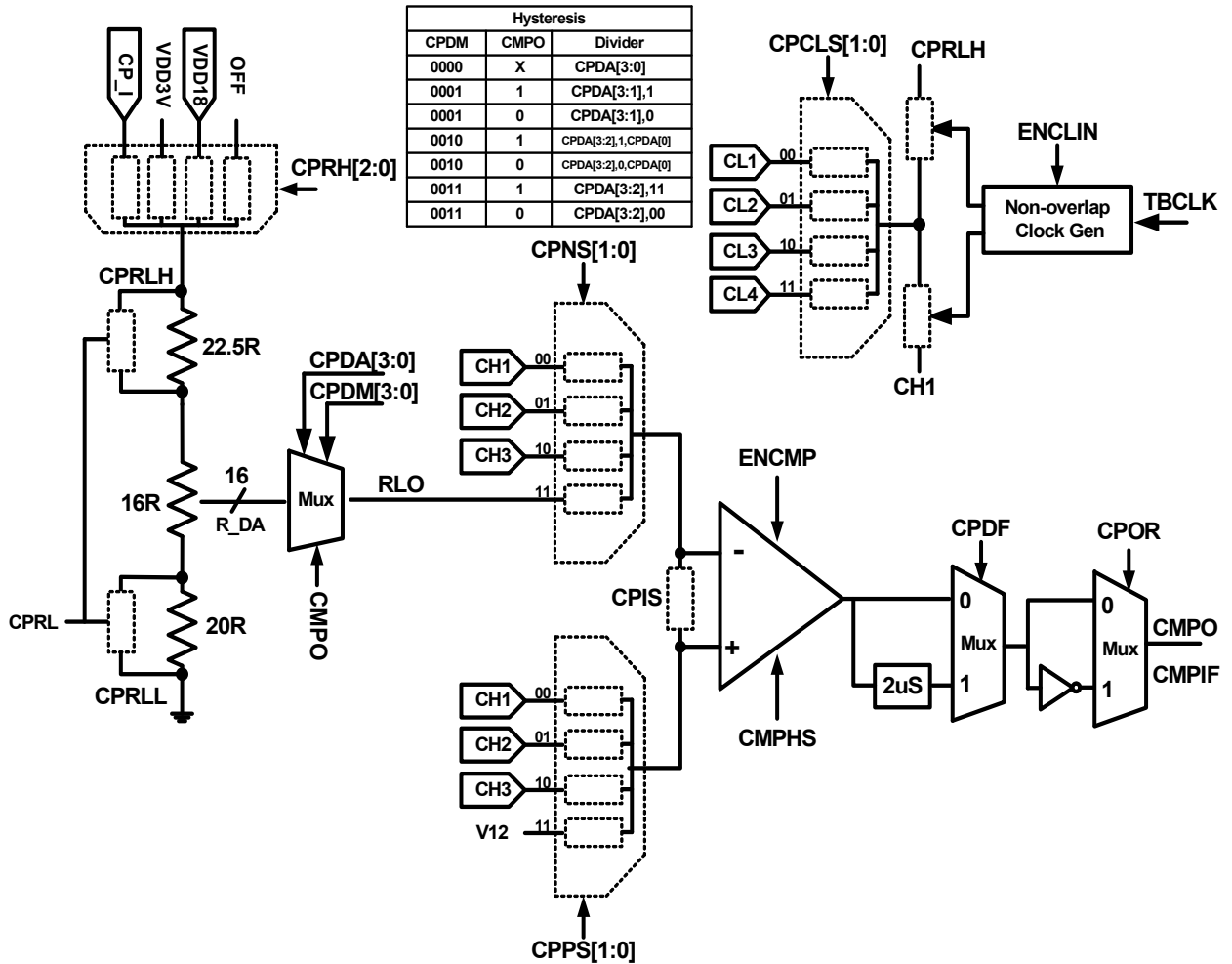
4.7 Rail to Rail OPAMP Network



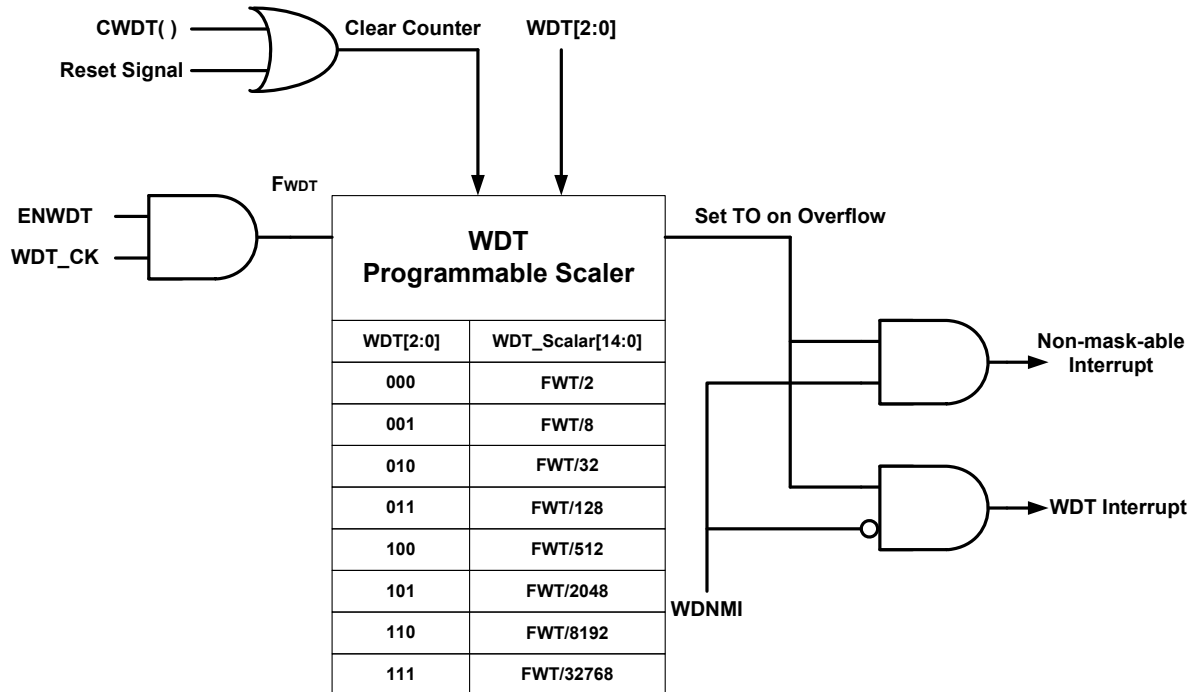
4.8 DAC Network



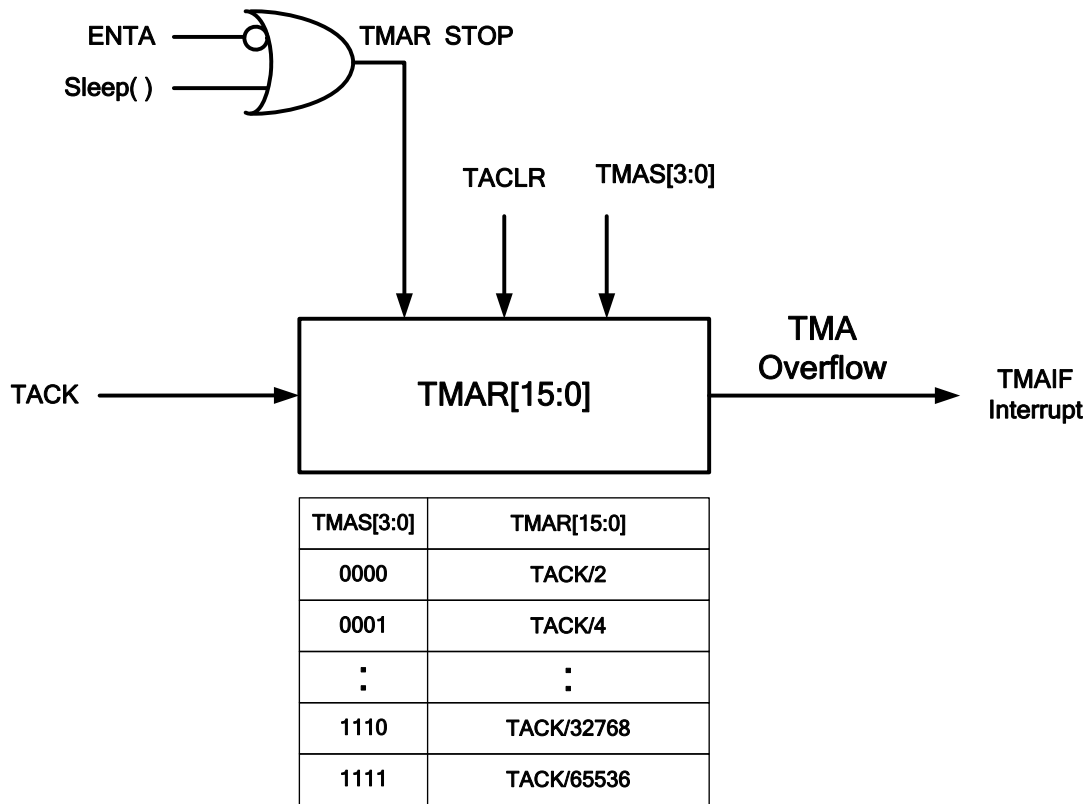
4.9 Analog Comparator Network



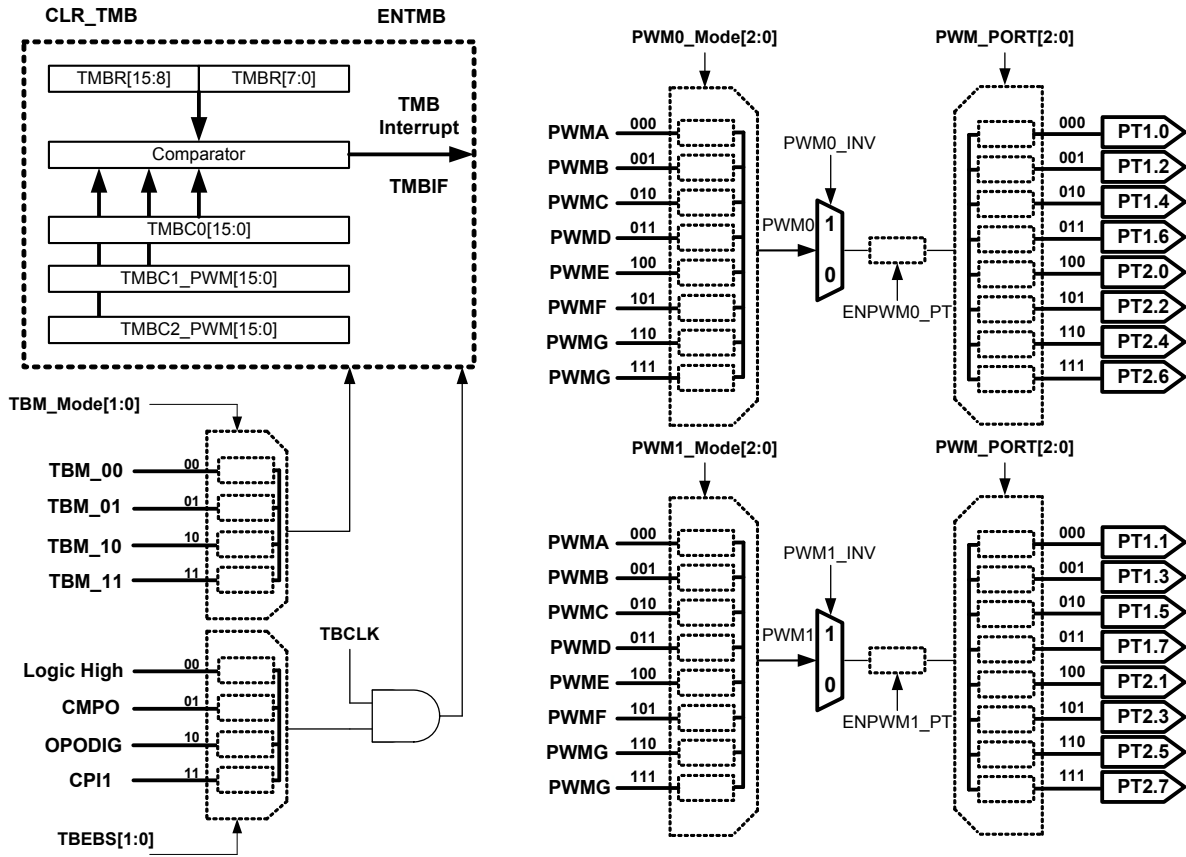
4.10 Watch Dog Timer Network



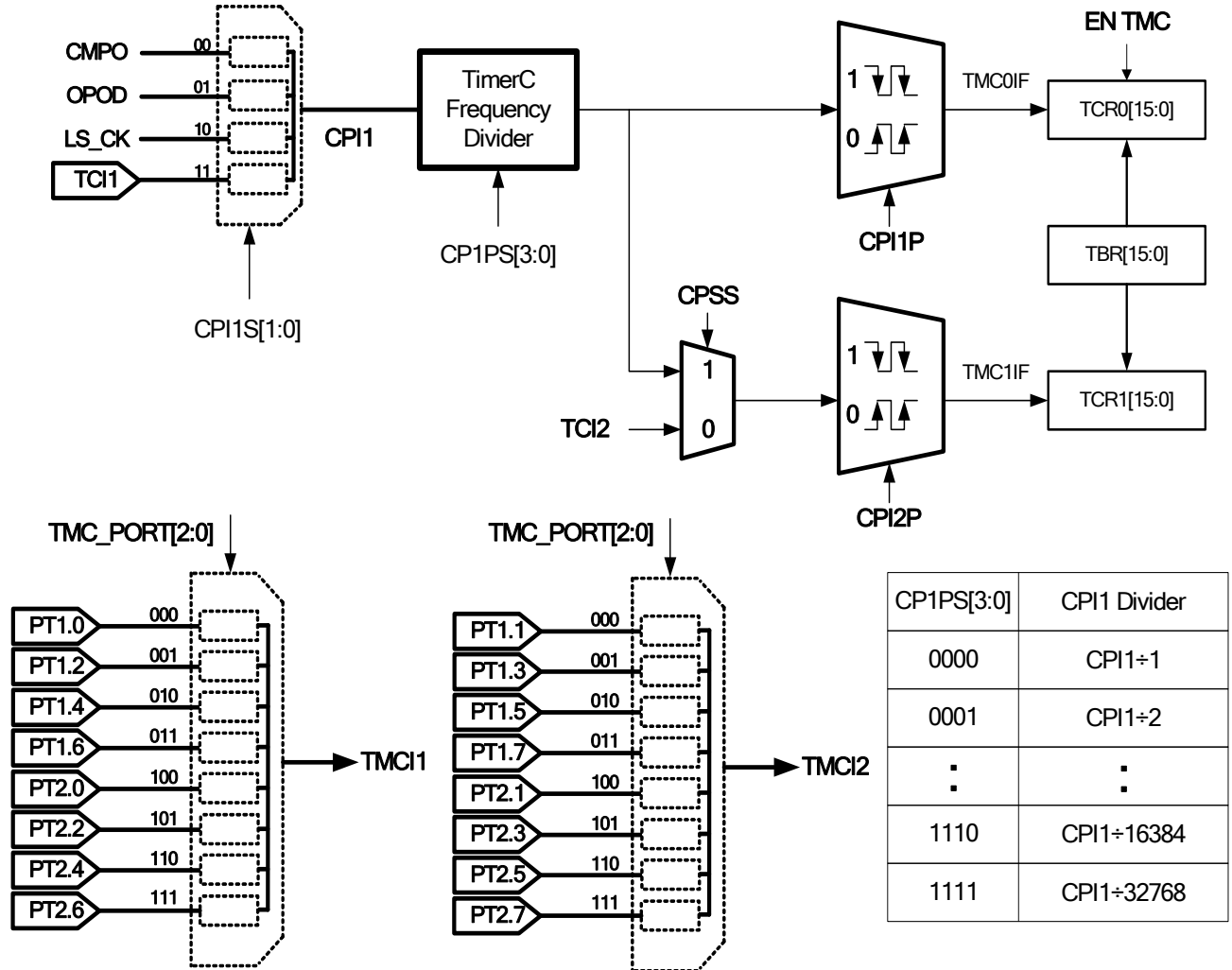
4.11 Timer A Network



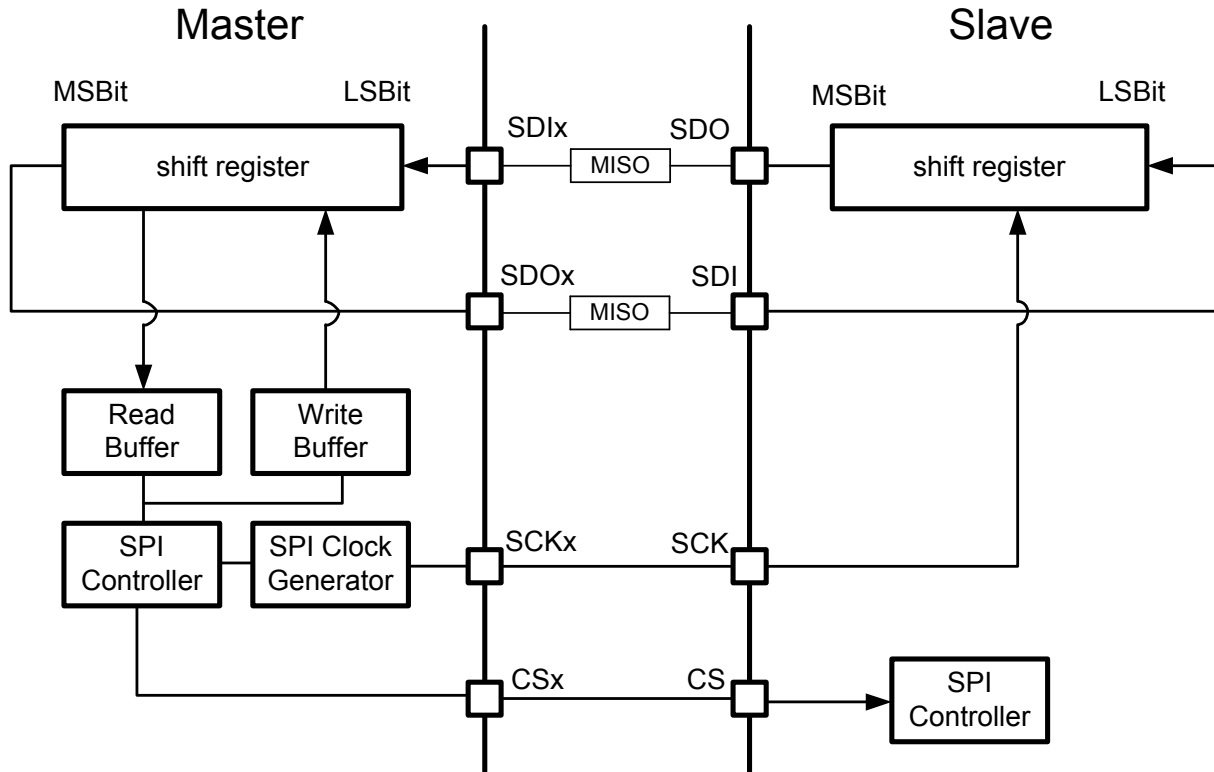
4.12 Timer B Network



4.13 Timer C Network

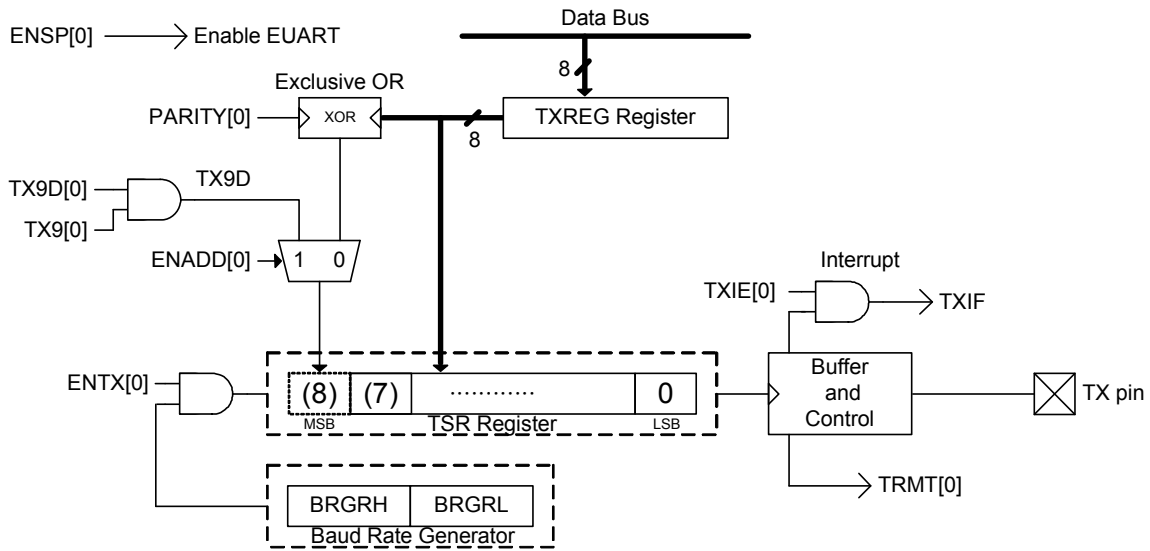


4.14 32-bit SPI Diagram

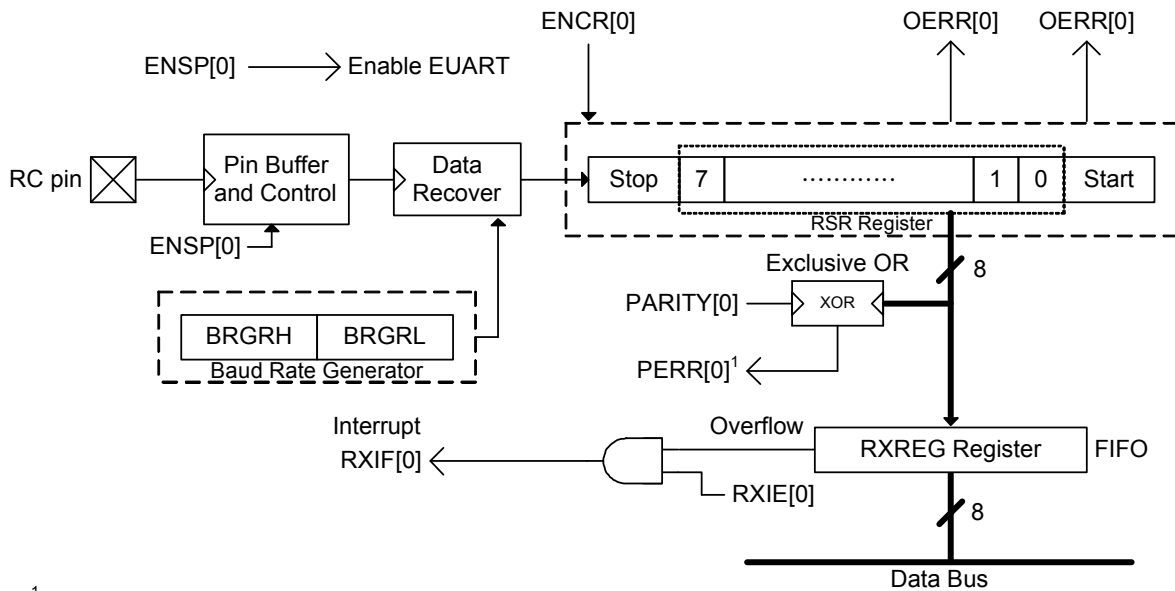


4.15 UART Block Diagram

EUART TRANSMIT BLOCK DIAGRAM

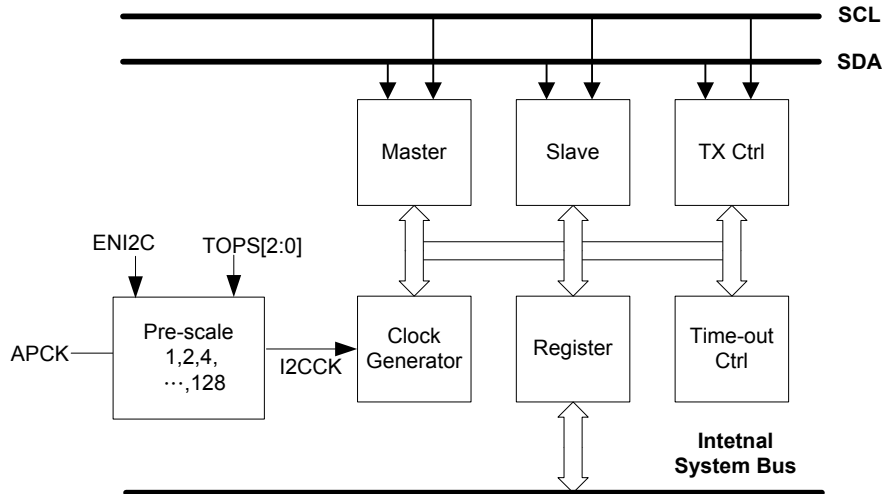


EUART 8-BITS RECEIVE BLOCK DIAGRAM

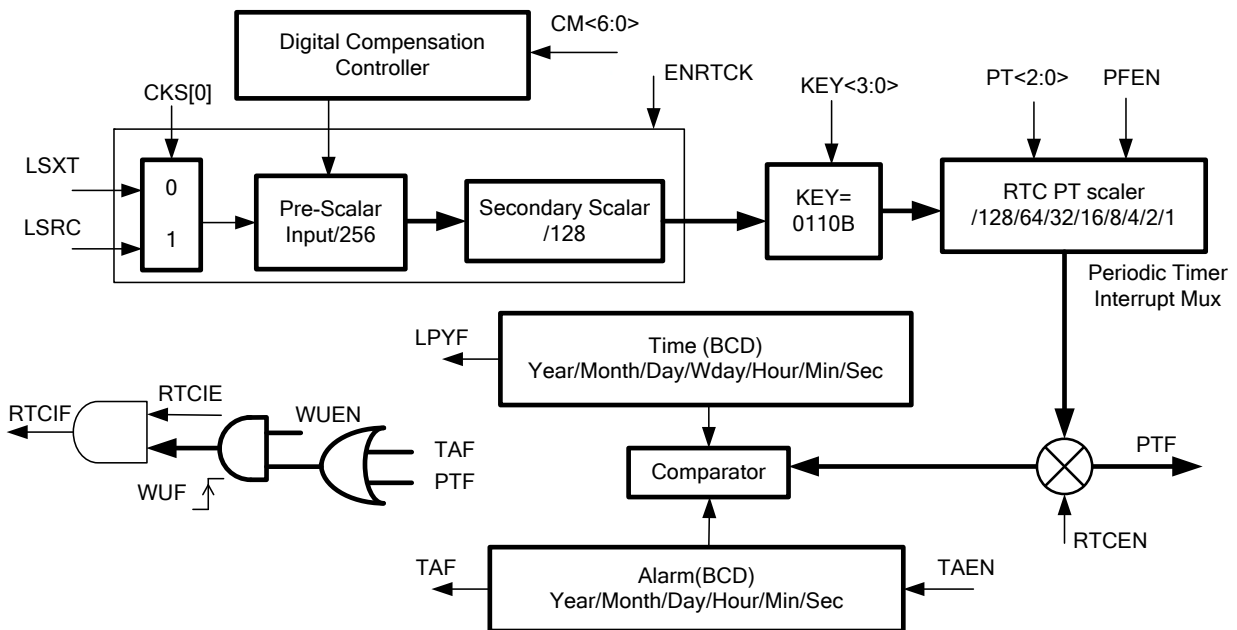


¹Don't care PERR[0] state of 8-bits receive mode

4.16 I2C Block Diagram



4.17 Hardware RTC Block Diagram



5. Ordering Information

5.1 HY16F18X Series Device Number Selection

Device No. ¹	Package Type	Pins	Package Drawing		Code ²	Shipment Packing Type	Unit Q'ty	Material Composition	MSL ³
HY16F188-D000	Die	-	D	000	-	-	200	Green ⁴	-
HY16F188-L048	LQFP	48	L	048	-	Tray	250	Green ⁴	MSL-3
HY16F187-L048	LQFP	48	L	048	-	Tray	250	Green ⁴	MSL-3
HY16F184-L048	LQFP	48	L	048	-	Tray	250	Green ⁴	MSL-3
HY16F187-N033	QFN	33	N	033	-	Tray	490	Green ⁴	MSL-3
HY16F184-N033	QFN	33	N	033	-	Tray	490	Green ⁴	MSL-3

¹ Device No.: Model No. – Package Type Description

HY16F188-L048

IC part
Number IC PKG Type

EX : You request in LQFP 48package.

The device No. will be HY16F188-L048.

And please clearly indicate the shipment packing type when placing orders.

³ MSL:

The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

⁴ Green (RoHS & no Cl/Br):

HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br/Cl<0.1%).

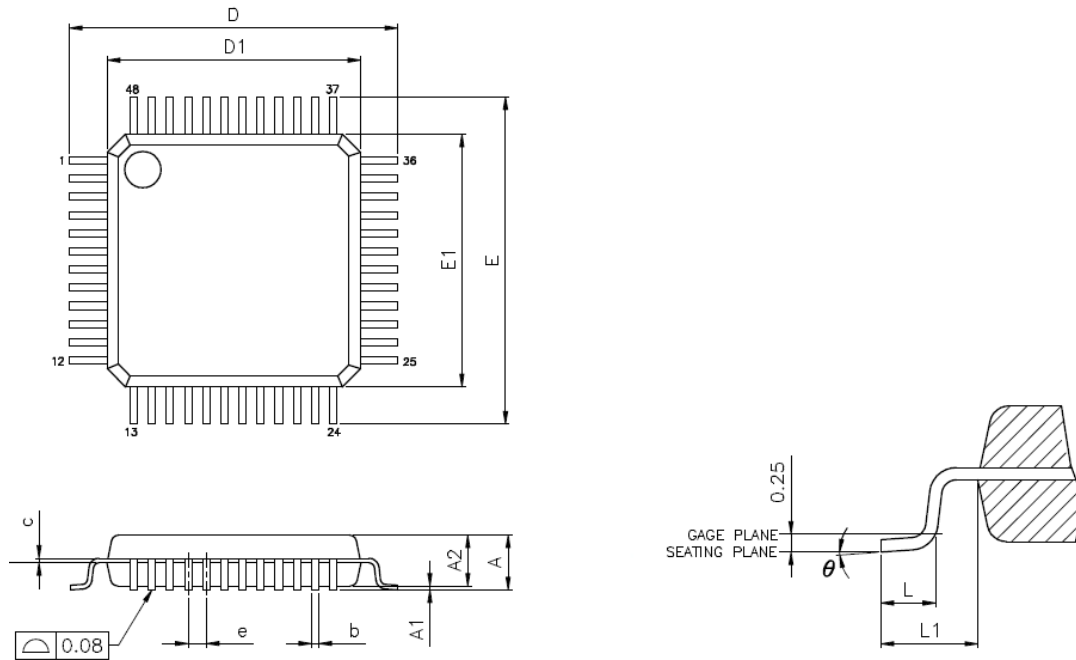
5.2 HY16F18X Series Selection Manual

Part No.	Flash (byte)	SRAM (byte)	24-b ΣADC	UART	32-b SPI	I2C	I/O	PWM	8-bit Resistance Ladders	OPAMP	Comp.	Hardware RTC	Temp. Sensor	Change Pump	Package
HY16F184	16K	2K	4-CH	1	1	1	19	2	8-bit	1	1	1	Y	N	LQFP48
															QFN33
HY16F187	32K	4K	4-CH	1	1	1	19	2	8-bit	1	1	1	Y	N	LQFP48
															QFN33
HY16F188	64K	8K	4-CH	1	1	1	25	2	8-bit	1	1	1	Y	Y	LQFP48

6. Package Information

6.1 LQFP48 PKG Diagram

Package Outline Drawing--- LQFP 7X7 48L Unit: mm



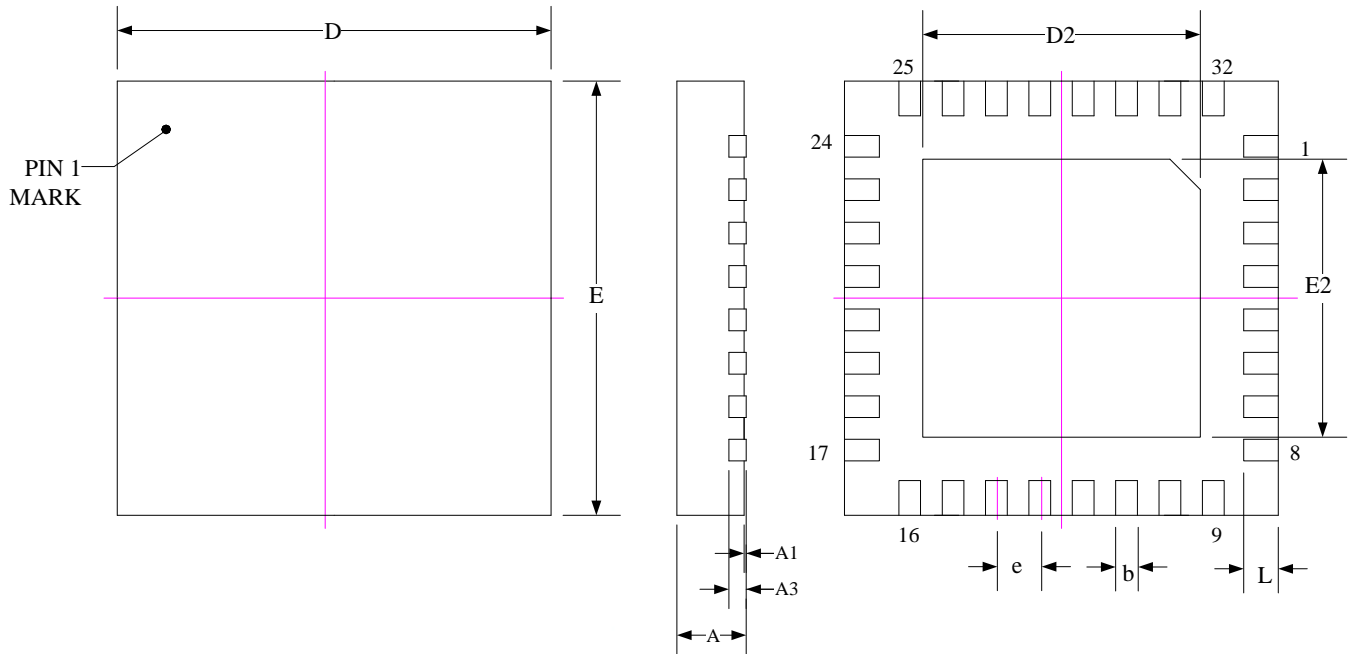
SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Note:

- (1) All dimensions refer to JEDEC OUTLINE MS-026.
- (2) Do not include Mold Flash or Protrusions.

6.2 QFN33 PKG Diagram

Package Outline Drawing--- QFN 5X5 33 Unit: mm
 PIN33=VSS



SYMBOLS	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.18	0.25	0.30
D	5.00 BSC		
E	5.00 BSC		
D2	3.10	3.20	3.30
E2	3.10	3.20	3.30
L	0.35	0.40	0.45
e	0.50 BSC		

Note: All dimensions refer to JEDEC OUTLINE MO-220.

7. Electrical Characteristics

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Parameter	Sym.	Min.	Max.	Unit
Voltage applied at VDD3V to VSS		-0.2	4.0	V
Voltage applied to Pin	V _{in}	-0.2	VDD3V+0.3	V
Diode current @ device terminal		-2	2	mA
Storage Temperature	TST	-55	150	°C
Operating Temperature	T _A	-40	85	°C
Soldering Temperature(10s)			260	°C
Maximum output current sink by any PORT1 to PORT3 I/O PIN			10	mA

7.1 Recommended Operating Conditions

VDD3V=2.2V ~ 3.6V. T_A=-40°C ~85°C, Unless otherwise noted.

Parameter	Sym.	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	VDD3V	Digital Application	2.2		3.6	V
		Digital Analog Application	2.4		3.6	V
Supply Current	I _{LDO+BOR}	VDD3V = 2.2V ~3.6V.	-25%	2.0	+25%	uA
	I _{LDO+BOR+LPO}		-25%	2.5	+25%	
Power-Up Delay	t _{PU,DLY}	Wake up from deep sleep		64		ms

7.2 Clock System

Parameter	Sym.	Test Conditions	Min.	Typ.	Max.	Unit
HSXT	High Speed Crystal Operating Voltage Range	02MHz~04MHz (OHS_HS=0b)	2.2		3.6	V
		04MHz~16MHz (OHS_HS=1b)	2.2		3.6	V
I_HSXT	High Speed Crystal Current	F _{HSXT} = 16MHz		100		uA
F_LSXT	Low Speed Crystal Frequency	VDD3V = 2.2V~3.6V		32.768		KHz
I_LSXT	Low Speed Crystal Current			2		uA
F_HSRC	Internal High Speed Oscillator Frequency	F _{HSRC} = 2MHz Before Trim	-10%	2	+10%	MHz
		F _{HSRC} = 4MHz Before Trim	-10%	4	+10%	MHz
		F _{HSRC} = 10MHz Before Trim	-10%	10	+10%	MHz
		F _{HSRC} = 20MHz Before Trim	-10%	20	+10%	MHz
V_HSRC	Voltage Coefficient	VDD3V = 2.2V ~3.6V	-0.2		+0.2	%
T_HSRC	Temperature Coefficient	-40~85	-1.5		+1.5	%
I_HSRC	Internal High Speed Oscillator Current	F _{HSRC} = 02MHz		20		uA
		F _{HSRC} = 20MHz		60		uA
D_HSRC	Duty OF Internal High Speed Oscillator		40		60	%
WT_HSRC	Wake Up Time	F _{HSRC} = 2MHz		30		us
F_LSRC	Internal Low Speed Oscillator Frequency	VDD3V= 3.0V		33		KHz
V_LSRC	Voltage Coefficient	VDD3V= 2.2V ~3.6V	-2.5		+2.5	%
T_LSRC	Temperature Coefficient	-40~85	-2.5		+2.5	%
I_LSRC	Internal Low Speed Oscillator Current			0.35	0.7	uA
D_LSRC	Duty OF Internal Low Speed Oscillator		40		60	%

7.3 Power Management System

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	
Coarse Band Gap Reference							
01	Operation Voltage		2.2		3.6	V	
	Output Voltage	VDD3V=3.0V	1.05	1.2	1.35	V	
Band Gap Performance							
02	Operation Voltage	VDDA	2.4		3.6	V	
	Output Voltage	VDDA =2.4V	1.15	1.2	1.25	V	
	Temperature Coefficient			50		ppm/°C	
	Startup Time			40		us	
VDDA LDO							
03	Output Voltage Error		-5		5	%	
	Capacitor Loading		22		10,000	nF	
	Settling Time	Capacitor Loading = 100nF 99% OF VDDA		50		us	
	Operation Current	Bias + Band Gap + VDDA LDO		35	50	uA	
	Dropout Voltage	I=10mA		0.2		V	
	Voltage Coefficient	VDD3V= 2.5 ~ 3.6V		0.1		%/V	
	Select VDDA Output Voltage	VDAS=00			2.4		V
		VDAS=01			2.7		V
		VDAS=10			3.0		V
VDAS=11				3.3		V	
Temperature Coefficient	Using BRG VDDA=3.0V		100		ppm/°C		
VDD18 LDO							
04	Output Voltage		1.7	1.8	1.9	V	
	Capacitor Loading		100		10,000	nF	
	Maxim Current	VDD3V= 2.2 ~ 3.6V	10			mA	
	Voltage Coefficient	VDD3V= 2.2 ~ 3.6V		1		%/V	
	Temperature Coefficient			100		ppm/°C	
	Load Regulation	Load = 0.1~10mA		0.1		V/A	
	Dropout Voltage	Load = 10mA		0.2		V	
REFO Buffer							
05	Capacitor Loading		22	100	1000	nF	
	Operation Current			15		uA	
	Input Resistance	Push Pull R		5	20	Ω	
	Output Current	1% Change Voltage	0.25	1		mA	
	Temperature Coefficient	Using BRG VDDA=3.0V		80		ppm/°C	
	Offset Voltage	REFO = 1.2V		±3	±12	mV	
	Voltage coefficient	DC		0.1		%/V	

7.4 Reset Management System

Reset Management System = (Brownout/External RST Pin/Low Voltage Detect)
 Typical values are at TA=25°C and VDD3V= 3.0V. Unless otherwise noted.

Sym.	Parameter Test Conditions	Min.	Typ.	Max.	unit
BOR	Pulse length needed to accepted reset internally, t_{d-LVR}	2			us
	VDD3V Start Voltage to accepted reset internally (L→H), V_{LVR}	1.8	1.95	2.1	V
	Ta=-40°C~85°C	-0.50		+50	mV
	Hysteresis, $V_{HYS-LVR}$	30			mV
POR	Operation Slew Rate	0.1			V/us
	Start Voltage to Accepted Reset	0.6			V

7.5 ΣADC ENOB and RMS Noise

Typical values are at TA=25°C and VDD3V = 3.3V, VDDA=2.4V unless otherwise noted.

HY16F188 provides important input noise specification that aims at ΣADC. Table 7.5-1 and Table 7.5-2 lists out the relations of typical noise specification, Gain, Output rate, and maximum input voltage of single end. Test condition configuration and external input signal short, voltage reference: 1.2V and 1024 records were sampled.

Max. Vin(mV) =0.9*VREF ⁽¹⁾	OSR					32	64	128	256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					10417	5208	2604	1302	651	326	163	81	41	20	10
	Gain	=	PGA	x	ADGN											
±1080	1	=	1	x	1	12.5	15.0	16.6	17.3	17.7	18.1	18.7	19.2	19.6	20.3	20.7
±540	2	=	1	x	2	12.4	14.4	16.3	16.9	17.0	17.4	17.9	19.1	19.3	20.0	20.4
±135	4	=	1	x	4	12.2	14.6	16.1	16.6	16.9	17.2	17.9	18.8	19.4	19.8	20.3
±33.75	32	=	8	x	4	12.2	13.7	15.1	15.6	16.1	16.5	17.0	17.7	18.1	18.6	19.1
±16.875	64	=	16	x	4	12.1	13.8	14.6	15.2	15.6	16.2	16.7	17.2	17.6	18.1	18.5
±11.25	96	=	24	x	4	12.1	13.4	14.4	14.8	15.4	15.9	16.4	16.9	17.4	17.9	18.3
±8.435	128	=	32	x	4	12.0	13.3	14.1	14.7	15.1	15.6	16.1	16.6	17.1	17.6	18.1

(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).

Table 7.5-1ΣADC ENOB Table

Max. Vin(mV) =0.9*VREF	OSR					32	64	128	256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					10417	5208	2604	1302	651	326	163	81	41	20	10
	Gain	=	PGA	x	ADGN											
±1080	1	=	1	x	1	426.3	71.0	23.3	14.56	10.92	8.29	5.72	3.98	2.95	1.89	1.410
±540	2	=	1	x	2	216.6	54.1	14.5	9.93	9.37	7.17	4.77	2.19	1.89	1.12	0.838
±135	4	=	1	x	4	129.5	23.5	8.5	6.04	4.85	4.02	2.46	1.29	0.89	0.65	0.455
±33.75	32	=	8	x	4	15.8	5.5	2.1	1.53	1.07	0.78	0.56	0.36	0.27	0.18	0.135
±16.875	64	=	16	x	4	8.5	2.6	1.5	0.99	0.75	0.51	0.36	0.26	0.19	0.13	0.098
±11.25	96	=	24	x	4	5.9	2.3	1.2	0.85	0.59	0.41	0.30	0.21	0.14	0.10	0.078
±8.435	128	=	32	x	4	4.6	1.9	1.1	0.71	0.52	0.37	0.27	0.19	0.14	0.10	0.068

Table 7.5 -2ΣADC RMS Table

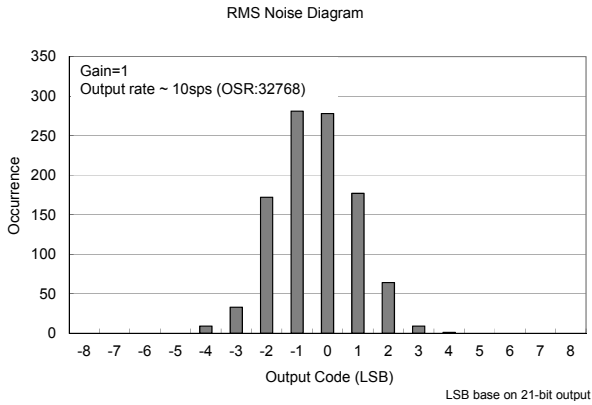


Figure7.5-2(a) RMS Noise Diagram

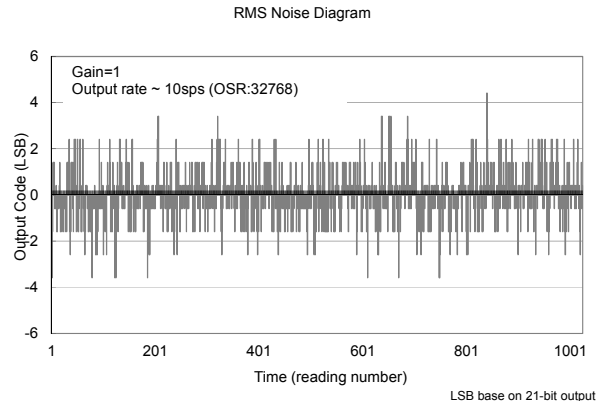


Figure7.5-2(b) Output Code Diagram

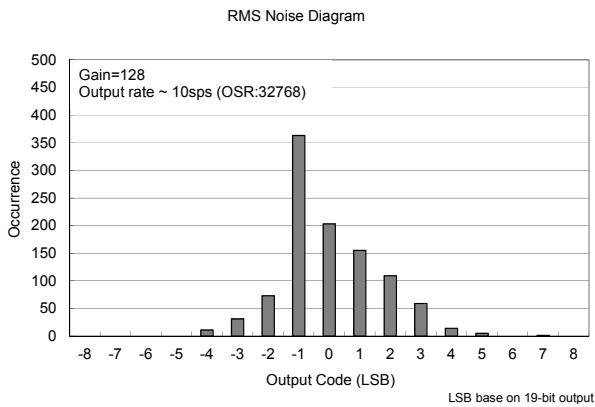


Figure7.5-3(a) RMS Noise Diagram

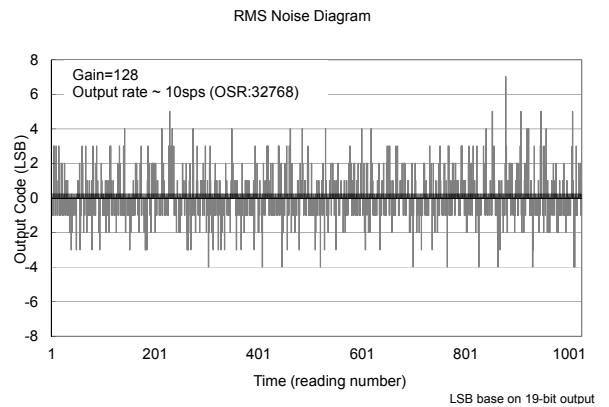


Figure7.5-3(b) Output Code Diagram

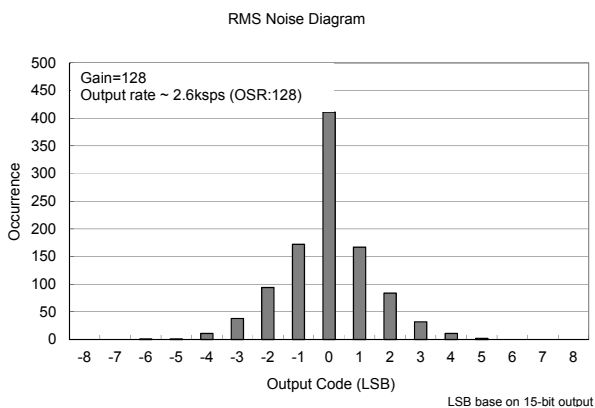


Figure7.5-4(a) RMS Noise Diagram

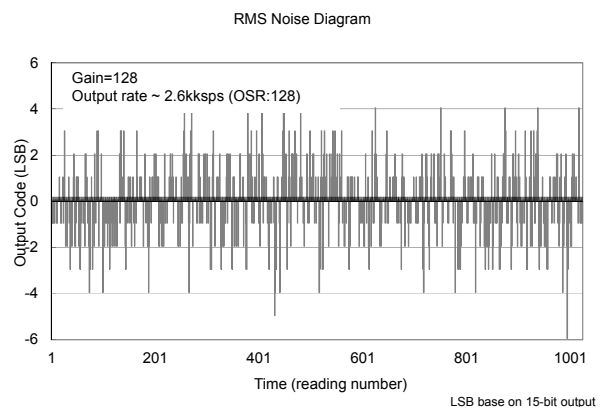


Figure7.5-4(b) Output Code Diagram

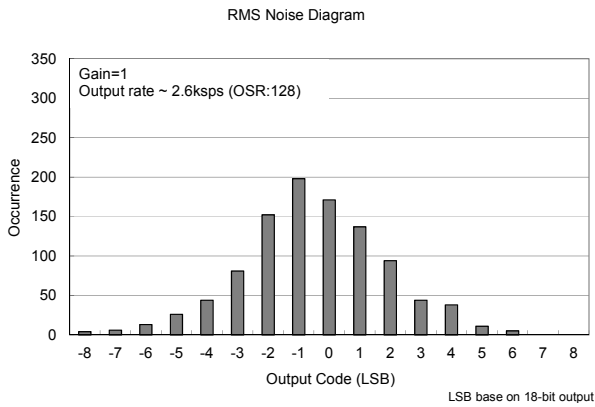


Figure7.5-5(a) RMS Noise Diagram

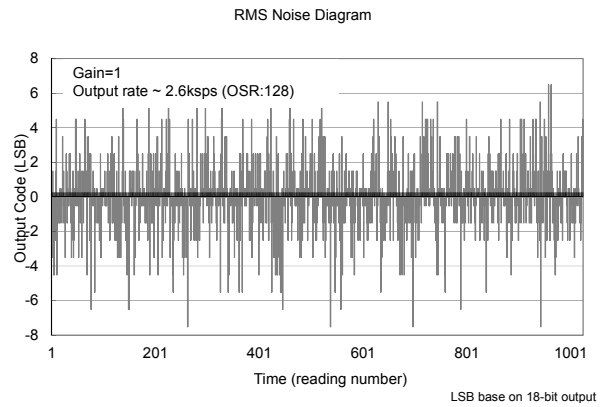


Figure7.5-5(b) Output Code Diagram

7.6 ADC Management System

All specifications at TA = -40°C to +85°C,
VDDA=REFP=3.0V, REFN=VSSA, and Gain=128, unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	
Analog Inputs							
01	Full-Scale Input Voltage (AINP – AINN)		±0.5*VREF/Gain			V	
	Common-Mode Input Range	Gain=1	VSS-0.2	VDDA+0.2		V	
System Performance							
02	Resolution	No Missing Code	24			Bit	
	Data Rate	ADC Clock	ADC Clock/OSR			SPS	
	Digital Filter Settling Time	Full Set	3			Data	
	Integral Nonlinearity(INL)	Differential Input, OSR=32768 End-Point Fit, Gain = 128	15			PPM	
	Gain Drift	Reference Buffer OFF	5			ppm/°C	
	Normal-Mode Rejection	f _N = 50Hz/60Hz ±1Hz, f _{DATA} = 10SPS	HSRC	70			dB
			HSXT	80			dB
	Common-Mode Rejection	@DC, ΔVDDA = 0.1V	80			dB	
	Input-Referred Noise	f _{DATA} = 10SPS	65			nV, rms	
f _{DATA} = 80SPS		140			nV, rms		
Power-Supply Rejection	@ DC, ΔVDDA = 0.1V, ACM=1.2V	80			dB		
Voltage Reference Input							
03	Voltage Reference Input	VREF = REFP – REFN	-0.15V	VDDA+0.15V		V	
	Reference Buffer Range		0.9V	VDDA-0.2		V	
	Reference Buffer Current			30		uA	

7.7 Internal Temperature Sensor

Typical values are at TA=25°C and VDD3V = 3.0V, VDDA=2.4V unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TC _S	Sensor Temperature Drift			178		uV/°C
KT	Absolute Temperature Scale 0°K			-285		°C
TC _{ERR}	One Point Calibrate Error Temperature	Calibration at 25°C , -40°C~85°C		±2		°C

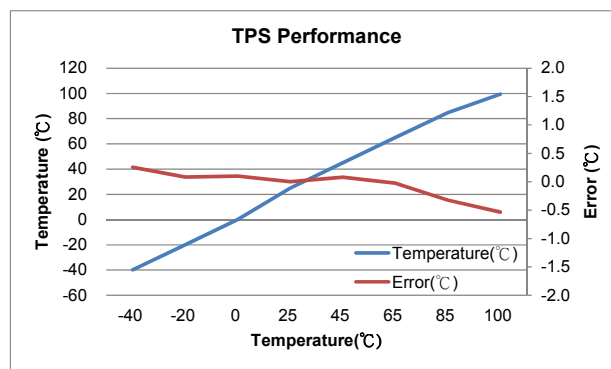


Figure 7.7-1 TPS Performance

7.8 8-bit Resistance Ladders Management System

Typical values are at TA=25°C and VDD3V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Resolution	Monotonic		8		Bit
	Power Supply		2.4		VDD3V	V
VOUT	8-bit Resistance Ladders Output Range		VR-		VR+	V
VREFP	Positive Reference Voltage Range	VREFP > VREFN	0		VDD3V	V
VREFN	Negative Reference Voltage Range		0		VDD3V	V
RON	8-bit Resistance Ladders output switch	VDD3V = 3.0V 0.5V < DA_OP < VDD3V-0.5V			200	Ω
		VDD3V = 3.0V 0.5V > DA_OP, DA_OP > VDD3V-0.5V		10		Ω
RRSW	Reference Voltage Switch	Vrefp = 2.2V, Vrefn=0V, VDD3V =3.0V		15	30	Ω
RLADDER	One LSB Resistance Ladder			600		Ω
INL	Integral Linearity Error	VR+ = 2.4V VR-= 0V		±0.5	±1	LSB
DNL	Differential Linearity Error	VR+ = 2.4V VR-= 0V		±0.5	±1	LSB
EOS	Offset Error	VR+ = 2.4V VR-= 0V			1	LSB

7.9 OPAMP Management System

Typical values are at TA=25°C and VDD3V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDDA	Power Supply		2.4		3.6	V
VOUT	Output Range		0		VDDA	V
VIN	Input Common Range		0		VDDA	V
IOPA	OPA current			120		uA
IOA_ LOAD	Output Current Loading (Push OR Pull)	VDDA = 3.0V, 0.3V < Output Voltage < VDDA-0.3V			1	mA
		VDDA = 2.2V, 0.3V < Output Voltage < VDDA-0.3V			0.5	mA
CLOA D	Max Output Capacitor Load				1000	pF
SR	Slew Rate	Loading R=10K, C=100pF, 0.3 -> VDDA-0.3V		0.6		V/us
UGB	Unit Gain Bandwidth	Loading C=100pF, -3dB		1000		KHz
VOS	Offset Error	Vin = 1.2V	-5		+5	mV
DFD	Digital Filter Delay	VDDA=3.0V		2		us
CSA	Sample Capacitor			10		pF

7.10 CMP Management System

Typical values are at TA=25°C and VDD3V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I _{MC}	Operation Supply Current	ENCMP[0]=1, CMPHS[0]=1		10		uA
	Low Power Mode	ENCMP[0]=1, CMPHS[0]=0		1		
V _{IC}	Common-mode Input Voltage		0		VDD3V-1	V
V _{OS}	Offset Voltage		-5		5	mV
V _{hys}	Input Hysteresis		0	0.7	1.5	mV
V _{REF}	Reference Voltage	CPPS[1:0]=11		1.2		V
	Temperature Drift	CPPS[1:0]=11		80		ppm/°C
I _R	Multi-node Resistor Current	CPRLS[0]=0		10		uA
		CPRLS[0]=1		30		

8. Revision History

Major differences are stated thereinafter:

Version	Page	Summary of Changes	Date
V01	ALL	First edition	2013/05/20
V05	ALL	(1)Added HY16F184/187 Pin out (2)In Ordering Information added HY16F184/187 description. (3)In Package Information added LQFP48 and QFN33 description.	2013/09/16
V06	ALL	(1)name change: VDD3 to VDD3V. VDD to VDD18.	2013/12/20
V07	ALL	(1)Remove PT4.0 sign (2)Original Description of OPO be revised to analog OPO (3)Digital OPO1 and OPO2 are revised to be OPOD1 and OPOD2 Digital Output (3)Revise Electronic Characteristic	2014/05/05
V08	ALL	“DAC “ be revised to be as “8-bit Resistance Ladders”	2015/06/09
	ALL	HSXT External High Speed Oscillator revised as 16MHz	
	CH4.5	REFOI is revised as REFO_I	
	CH4.6	ADC Network input OPO is Revised to be OPOI, REFO is revised to be REFO_I	
	CH4.7	OPAMP Network OPNS[3]is revised as OPOI, OPNS[4]is revised as OPO, R2ROPoutput description revise, REFO is revised as REFO_I	
	CH4.8	8-bit Resistance Ladders Network input pin’s REFO is revised as REFO_I	
	CH7.3	Capacitor Loading of REFO Buffer the unit is revised from pF to nF, and add Min value 22nF	