HYCON 紘康科技

HY16F184
HY16F187
HY16F188
User's Guide

High Precision Mixed-Signal Controller
Embedded 65nV Resolution ADC
32-bit Low Power MCU
64KB Flash
8KB SRAM

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1. General Description

1.1. Introduction

HY16F18 series is a high performance mixed-signal controller. It can be used for very precise measurement and control. An analog front-end circuit, a 24-bit ADC, a power management, a non-volatile memory, and 32-bit MCU are integrated in HY16F188. It allows designer to realize a low power low cost mixed-signal system.

The analog front-end circuit includes an 8-BIT RESISTANCE LADDERS, a rail-to-rail OPAMP, and a rail-to-rail input comparator. The 8-BIT RESISTANCE LADDERS are guarantee monotonic. It is a resistor ladder with 600ohm for each LSB. The resistor has low temperature coefficient. The rail-to-rail OPAMP has an input network that can be used for variance analog circuit configurations such as, integrator, current-to-voltage converter, programmable gain amplifier, and SAR ADC. The rail-to-rail input comparator consumes very low power for continuous monitor the analog signal. It can be used as supply voltage monitor, external wake-up trigger source, or capacitive touch-key driver.

The ultra-low noise 24-bit ADC is embedded. The maximum output rate is 10.24KSPS with 21-bit ENOB. The minimum noise level is 65nV RMS. The low noise amplifier with programmable gain is used with ADC. The maximum gain is 128. There is 4-bit ADC input that is used to extend the measurement range. There is a build-in analog input buffer for reference allow high output resistance reference source.

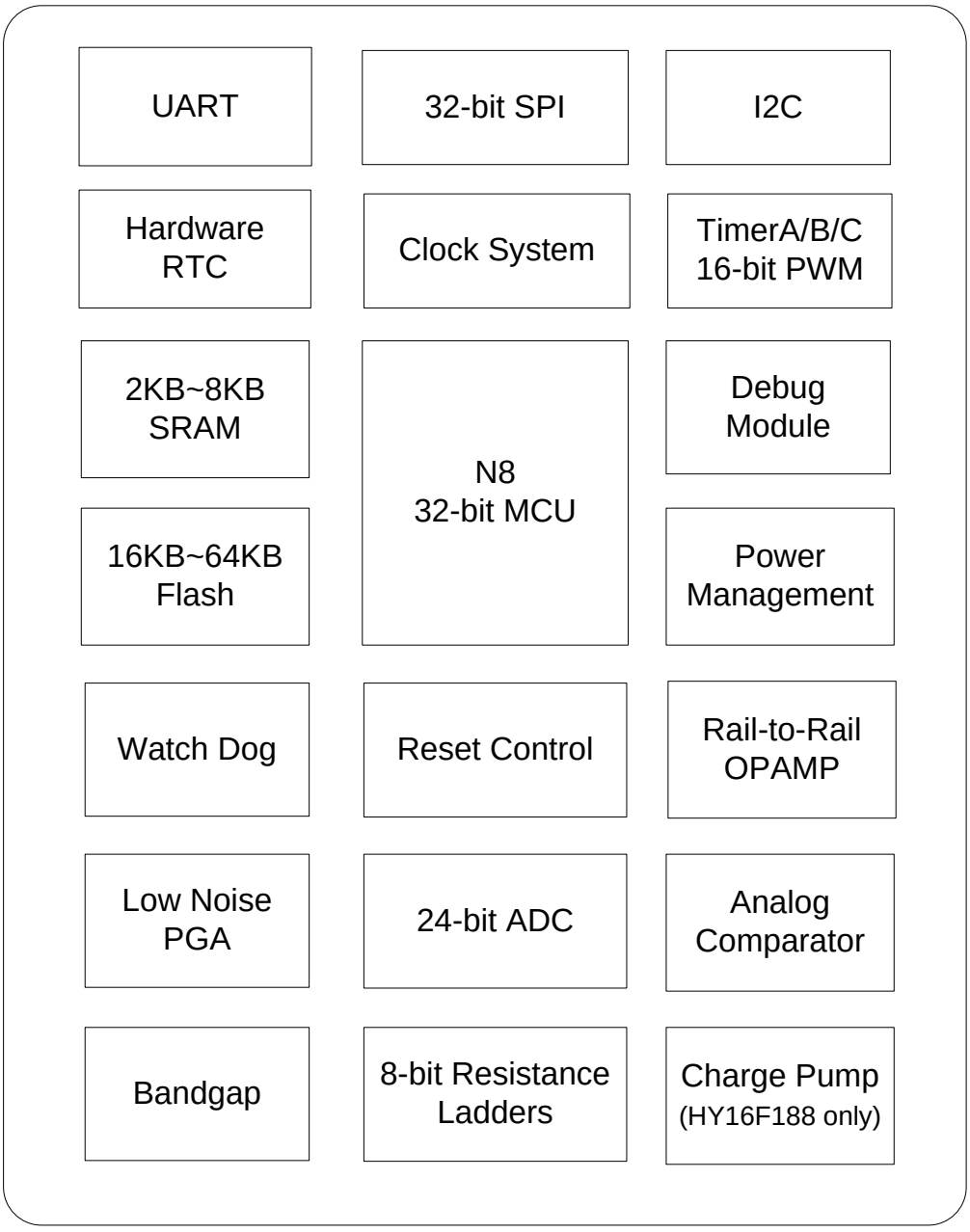
The power management provides selectable regulated voltage for analog circuit. The digital power is also provided by internal LDO. A charge pump is implemented to obstruct power disturb from system. It also enables low operation voltage down to 2.0V.

It has a 64Kbytes embedded flash memory. It can be used for program and data store. The data can be saved into flash during the operation. It also has 8K-bytes SRAM for the system.

A high performance 32-bit MCU core is used. The MCU can operate one instruction per clock cycle and up to 10MIPS. A friendly program tools are provided. The user can write C or assemble language code for the MCU. The IC has in-circuit-emulation function allows easy debug environment. It can operate from 2.2V to 3.6V in -40 to 85℃ temperature range. Function Outline

2. Block Diagram

2.1. Block Diagram

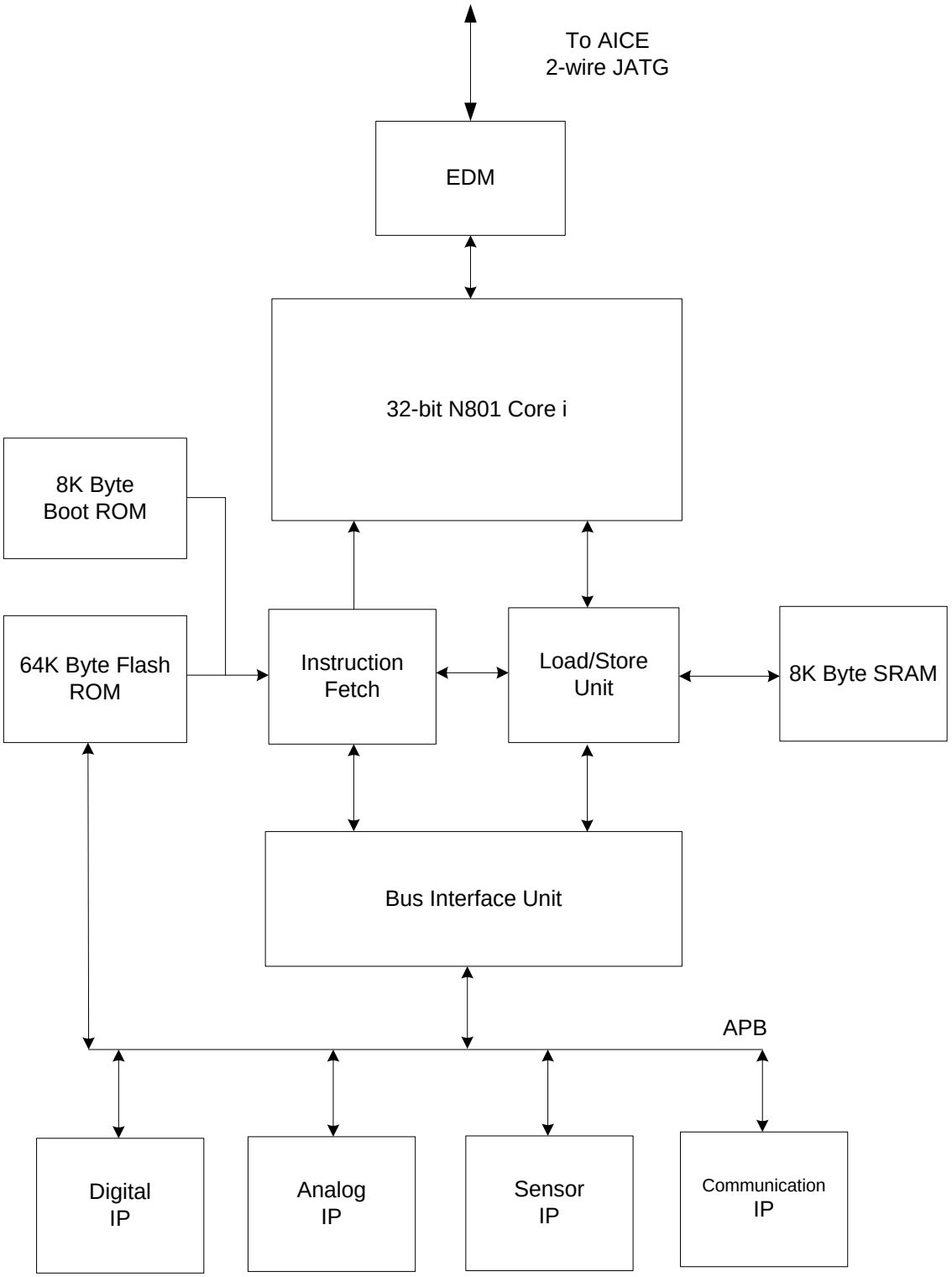


Picture 2-1: IC Function Structure Diagram

GPIO Port	OSC	Interrupt	Timer C Capture	SPI	IIC	UART	CMP	Analog	Timer B PWM
Priority	0	0	0	1	2	3	4	5	6
PT1.0		INT1.0	TCI1_1	CS_1	SCL_1	TX_1	CH1		PWM0_1
PT1.1		INT1.1	TCI2_1	CK_1	SDA_1	RX_1	CH2		PWM1_1
PT1.2		INT1.2	TCI1_2	MISO_1	SCL_2	TX_2	CH3		PWM0_2
PT1.3		INT1.3	TCI2_2	MOSI_1	SDA_2	RX_2	CL1		PWM1_2
PT1.4		INT1.4	TCI1_3	CS_2	SCL_3	TX_3	CL2		PWM0_3
PT1.5		INT1.5	TCI2_3	CK_2	SDA_3	RX_3	CL3		PWM1_3
PT1.6		INT1.6	TCI1_4	MISO_2	SCL_4	TX_4	CL4		PWM0_4
PT1.7		INT1.7	TCI2_4	MOSI_2	SDA_4	RX_4	CMPO1		PWM1_4
PT2.0		INT2.0	TCI1_5	CS_3	SCL_5	TX_5			PWM0_5
PT2.1		INT2.1	TCI2_5	CK_3	SDA_5	RX_5			PWM1_5
PT2.2		INT2.2	TCI1_6	MISO_3	SCL_6	TX_6			PWM0_6
PT2.3		INT2.3	TCI2_6	MOSI_3	SDA_6	RX_6			PWM1_6
PT2.4	LSXT1	INT2.4	TCI1_7	CS_4	SCL_7	TX_7			PWM0_7
PT2.5	LSXT2	INT2.5	TCI2_7	CK_4	SDA_7	RX_7			PWM1_7
PT2.6	HSXT1	INT2.6	TCI1_8	MISO_4	SCL_8	TX_8			PWM0_8
PT2.7	HSXT2	INT2.7	TCI2_8	MOSI_4	SDA_8	RX_8			PWM1_8
PT3.0							OPO1		
PT3.1							OPO2	DAO	
AIO4								AIO4	
AIO5								AIO5	
PT3.4								AIO6	
PT3.5								AIO7	
PT3.6								REFO	
PT3.7								OPO	
AIO0								AIO0	
AIO1								AIO1	
AIO2								AIO2	
AIO3								AIO3	

Table2-1 IC IO pin function table

2.2. Introduction



Picture2.2: IC Test Structure Diagram

3. Memory Structure

3.1. Introduction

The MCU used in HY16F188 is license Andes N801. It is a 32-bit CPU core.

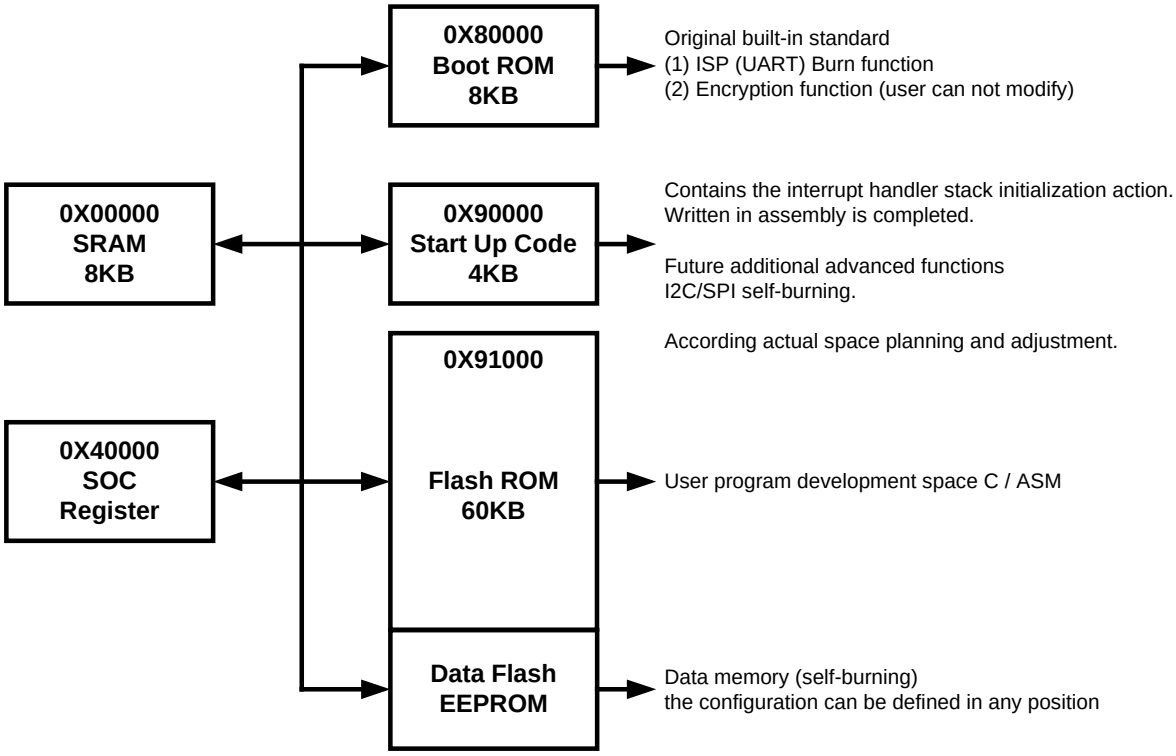
(1)0X0_0000–0X1_FFFF SRAM (8K Byte)

(2)0X4_0000–0X4_FFFF SOC Register (64K Byte)

(3)0X8_0000–0X8_1FFF Boot ROM (8K Byte)

(4)0X9_0000–0X9_FFFF Main Program Flash (64K Byte)

(5)0XD_0000–0XD_03FF Information Area Flash (1K Byte)



Picture 3-1: Flash Distributed Picture

3.2. Memory Location

Please refer to following table for IC control memory distribution. Table 3-1

Module	Description	Base Address
INT	Interrupt Flag	0X4_0000
SYS	System Register	0X4_0100
CLK	Clock System Register	0X4_0300
PMU	Power Management Unit	0X4_0400
MC	Memory Controller	0X4_0600
PIO	Port I/O Control	0X4_0800
TMR	Timer Register	0X4_0C00
UART	UART Mode, Communication Interface	0X4_0E00
SPI	SPI Mode, Communication Interface	0X4_0F00
I2C	I2C Mode, Communication Interface	0X4_1000
ADC	Analog-to-Digital Module	0X4_1100
DAC	Digital-to-Analog Module	0X4_1700
CMP	Comparator Network Module	0X4_1800
OPN	Operational Amplifier	0X4_1900
RTC	Real Time Clock	0X4_1A00

Each register can contain mask bits, mask bits are used to enable the respective control bits are written only in the control bits corresponding mask bit is 1, the corresponding control bits can be written value, otherwise the write the failure, you cannot change the value of the scratchpad. As shown in Figure 3-2;
register a total of 32, including 16-bit mask. Mask bits are divided into eight groups, each controlled by a corresponding 8 8 control bits. According to the distribution of the contents of the register: BIT [31:24] control the BIT [23:16], and BIT [15: 8] control the BIT [7: 0]; only when the mask is set to <1>, the corresponding bit value can be written.
If you want to bit [5: 0] is written 101010b, that is, as long as the low 16 operation, the register operation mode is: 0x3F2A; wherein 0X3F is BIT [15: 8] of the written value, enabling BIT [5: 0] corresponding mask bit, 0X2A is on the BIT [5: 0] value written.

INT Base Address + 0X10 (0X40010)									
Symbol	INTPT1 (Interrupt Control Register 4)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	PT17IE	PT16IE	PT15IE	PT14IE	PT13IE	PT12IE	PT11IE	PT10IE
RW	R0W-0	RW-0							
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	PT17IF	PT16IF	PT15IF	PT14IF	PT13IF	PT12IF	PT11IF	PT10IF
RW	R0W-0	RW0-0							

FIG. 3-2 Basic structure of register

3.3. SRAM

There are 8K Bytes SRAM in the HY16F188. The start address is 0X0000 to 0X1FFF. The MCU can choice it is one byte, two bytes (half word), or four bytes (word) access. The SRAM can access a data within 1 clock cycle.

3.4. Flash ROM

There is a total 64K bytes Flash memory in the HY16F188. The start address is 0X90000 to 0X9FFFF. The user program code is stored in the Flash. To program the Flash memory, the user needs to use the EDM command to read or write flash control unit. There is portion of flash is reserved for user to store the data. It will be defined later. System Flash has 1K byte.

3.5. Bus Interface Unit

In the HY16F188, the register read or write is controlled by a 32-bit Advanced Peripheral Bus APB. It can write a 32-bit data within one clock. However, it is important for value to prevent over-write the data value while other data is writing, the HY16F188 introduces the mask function.

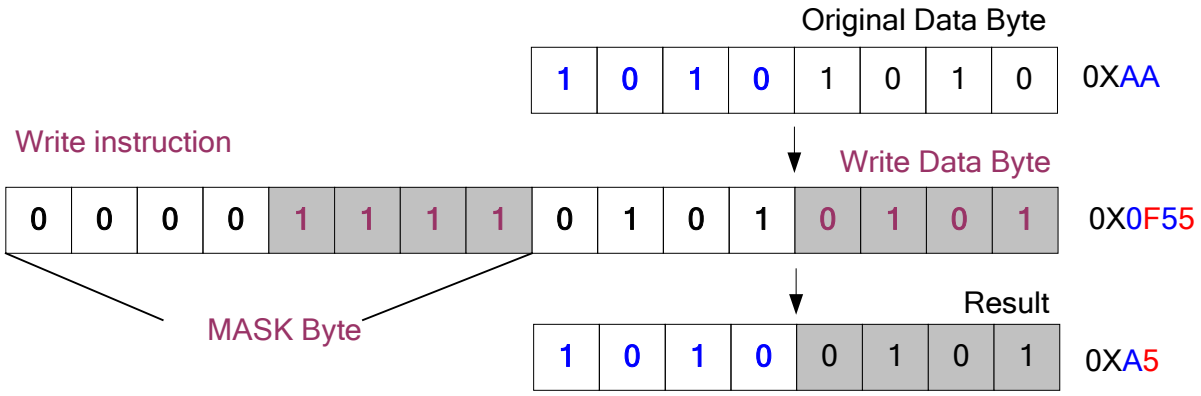


FIG. 3-3 Data flow structure

3.6. Boot ROM

There is an 8K bytes mask ROM in HY16F188. The start address is 0x80000 to 0x81FFF. It is used for boot code, flash control code and security code. If the reset happened, the program counter will start from 0x80000.The software in the boot ROM includes the hardware information, in-system-program protocol, and security protocol.

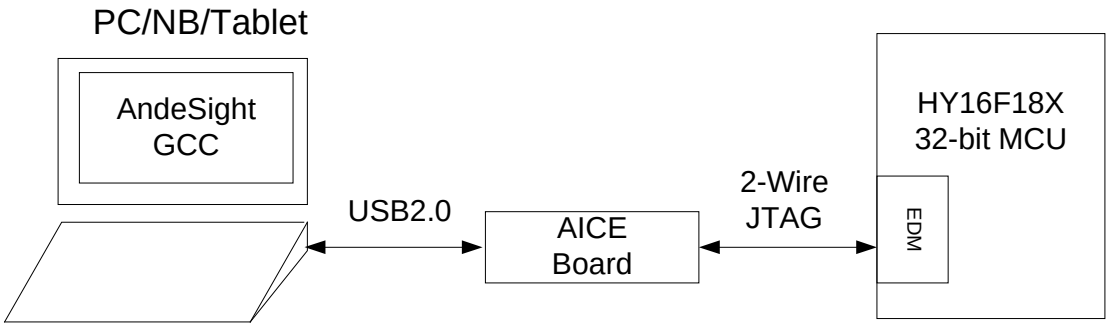


FIG. 3-4 Chip development connection diagram

3.7. EDM

Embedded Debug Module (EDM) is provided by Andes. It can input an instruction to MCU and control the HY16F188 in the debug mode. It is the bridge between the MCU and AICE. It uses a two wire protocol and JTAG style interface. It can access the IP registers on the APB, general propose GPR register, SRAM on the DLM and ROM Flash on the ILM. It has highest priority for APB bus control. To enter the debug or testing mode, use EDM to send the command. For debug mode, the EDM has 2 regular breakpoint and watch point registers, and 6 simple breakpoint register.

3.8. Information Memory

There is 1K-Bytes additional memory space in the flash for information data. During the normal mode, the MCU cannot access the data form this block. The information only can be accessed in the development mode. In the development mode, there are 2 ways to access or write the data in the block: MCU in Boot ROM code, HYCON I2C. The EDM bus is defended when the EDM controls the APB/MCU. It is usually used when users is debugging. The MCU in Boot ROM code is defended when the MCU is running the instructions in the Boot ROM. It is usually used when the MCU is after reset and the development programming mode. The HYCON I2C is defended when the HYCON I2C controls the APB/MCU. It is usually used in the testing mode and mass programming mode.

4. System Register

4.1. Overall description

Manage the operating mode of the system and the reset status of the chip, such as WDT, external reset, under voltage reset, etc.

4.2. Register Address

SYS Register Address	31	24	23	16	15	8	7	0
SYS base address + 0X04 (0X40104)	-		-		MASK0		REG0	

-Reserved

4.3. Register Functions

Operate the register SYS0 [4] can set the operating mode of the system as SLEEP mode/IDEL mode. The user can check the register SYS0 [3] to understand what the current operating mode of the system is. The setting of the operating mode of the chip will be specified at the chapter 25.

4.3.1. System Flag Register 0

SYS Base Address + 0X04 (0X40104)								
Symbol	SYS0 (SYS Control Register 0)							
Bit	[31:16]							
Name	RSV							
RW	R-0							
Bit	[15:8]	[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	F_{CRST}	IDLE	$F_{SLP/IDLE}$	F_{WDT}	-	F_{BOR}
RW	R0W-0	-	RW0-0					RW0-1

Bit	Name	Description	
Bit[05]	F_{CRST}	CPU Core Reset flag	
		0	Normal
		1	ICP Core has already been triggered before.
Bit[04]	IDLE	IDEL Mode Control Bit	
		0	Sleep Mode
		1	IDLE Mode
Bit[03]	$F_{SLP/IDLE}$	Sleep/Idle Flag (Low voltage reset or reset circuit reset can reset the bit.)	
		0	Normal
		1	Sleep Mode or Idle Mode
Bit[02]	F_{WDT}	WDT Flag (Low voltage reset or external reset can clear the bit.)	
		0	Normal
		1	WDT is reset or interrupted.
Bit[00]	F_{BOR}	Low Voltage Reset (BOR) Flag (The bit will be automatically cleared after the voltage of the chip is higher than 1.8V.)	
		0	Normal
		1	Low voltage reset has occurred.

5. Power Management

5.1. Overall description

The power management of HY16F18 series consist a charge pump regulator, a wide Band gap reference, a narrow Band gap reference, a VDDA LDO, a VDD (VDD1.8V) LDO, and reference output buffer. The HY16F18 series only requires one voltage source to operate. The operation voltage range is 2.2 to 3.6V. However, for the operation voltage range between 2 to 2.4V, the HY16F18 series needs to enable the charge pump regulator to provide power for some analog IPs and Flash. In the HY16F18 series, the power systems can be broken into three sections: I/O circuit, analog circuit, and digital circuit. The I/O circuit power is driven by VDD3V. The analog circuit power is driven by internal VDDA LDO. Finally, the digital circuit power is driven by the internal VDD18 LDO.

When the MCU is in standby mode, the minimum power is consumed to maintain the data store in register and SRAM. At the standby mode, coarse Band gap reference, BOR and VDD LDO are turn-on. These blocks total consumes only 1.5uA in room temperature. For auto wake up mode, the low speed oscillator needs to be turn-on. The internal low speed oscillator consumes additional 0.5uA in room temperature.

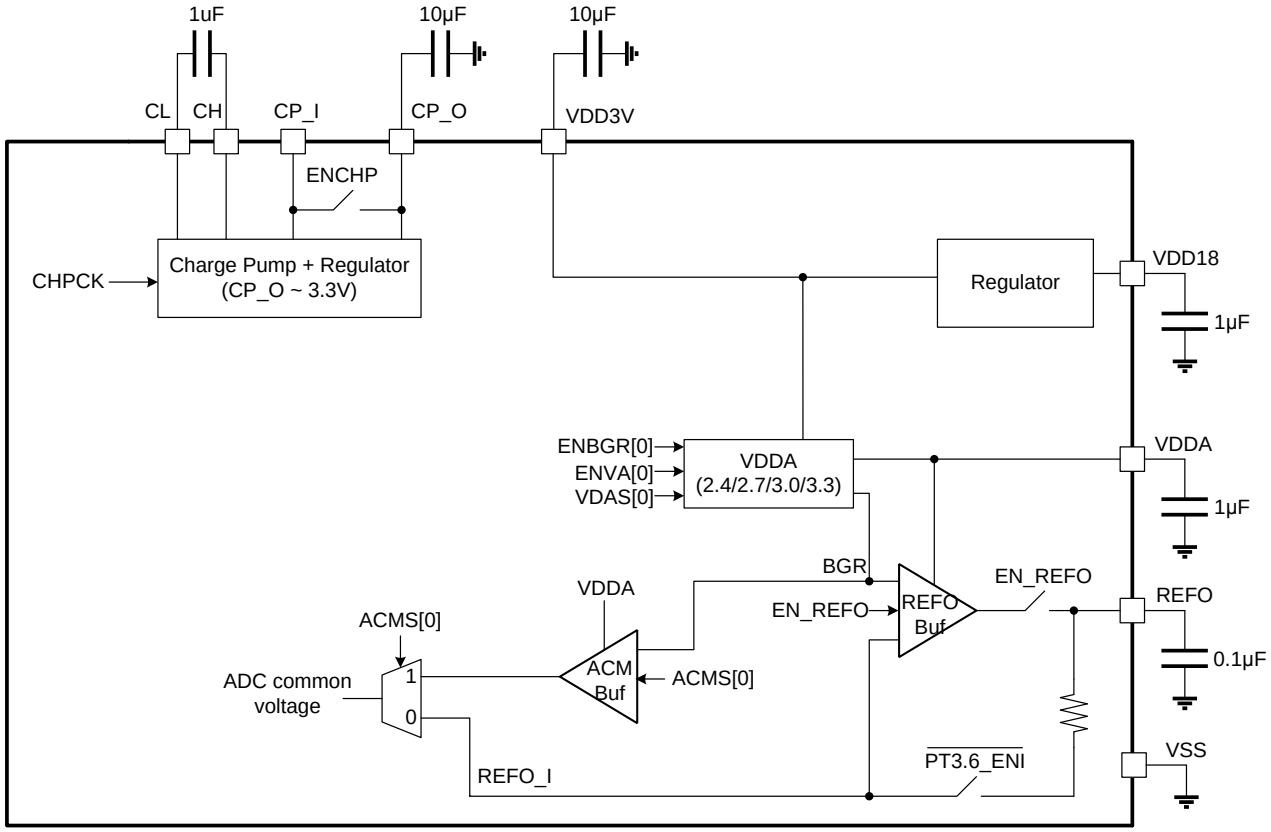


FIG. 5-1 Function block diagram

Chip operating voltage and VDD 18

The operating voltage of the chip is inputted via the pin VDD3V, and the voltage range is 2.2V~3.6V; besides, the pin should be connected to a 10uF ground capacitor, which can make VDD3V become more stable. If the operating voltage of the chip is used to drive a high current load, the operating voltage of the chip may be decreased and the chip may be reset; in this situation, it is necessary to enable the charge pump boost circuit to output a stable voltage to VDD3V so as to make sure the chip can work normally.
The VDD LDO output is 1.8V and it requires a bypass capacitor with 1uF. It has a low power mode. To reach the minimum power consumption, PMU [0] (VDDLP) is needed to set 1. This register is usually be set to 1 before enter standby mode and clear to 0 after wake up the MCU.

VDDA voltage

The chip has a voltage regulator circuit LDO: VDDA and the VDDA voltage should be enabled when using ADC. It can have different operating modes and different output voltages. It has four different operating modes; the first mode is to be short-circuited to the VDD3V; and the VDDA is close to the VDD3V during the mode. The second mode is Weak pull down; during the mode, the VDDA is close to the VSS. The third mode is High Z; and it is possible to input the voltage into the VDDA from outside but the inputted voltage should not exceed VDD3V. The four modes is adjustable voltage regulating mode LDO; during the mode, the VDDA can output four different voltages: 2.4V, 2.7V, 3.0V and 3.3V. For better performance, the voltage difference between VDD3V and VDDA. Should be higher than 0.2V and can drive at most 10mA. Additionally, it also needs to be connected to a 1uF bypass capacitor

Low-voltage detection circuit (BOR)

The BOR circuit is used to monitor the stability of the power system and the MCU. When the BOR detects the VDD3V and VDD18 are lower the detecting voltage of the BOR, the BOR will be triggered to reset the system and the chip; the chip will work normally until the BOR detects the operating voltage of the chip exceeds the voltage of the BOR.

Charge Pump

The charge pump regulator can be used to separate system power and IC power. For some applications need to drive a DC motor, the charge pump can reduce the disturb form rush current by motor's inductance. To enable the charge pump, the register PMU [2]

ENCHP need to set 1. It also requires two external capacitors (Ccp1 and Ccp2) for charge pump function. When the charge pump is operating, the power source is from CP_I. If the application does not have a noise power source, the charge pump can disable and the power is connected to VDD3V. The external capacitors Ccp2 and Ccp1 are not necessary. The IC power can be provided by VDD3V. In order to prevent the power glitch issue, the ratio of Ccp2 and Ccp1 should be 10 ~1000nF. The minimum side of Ccp2 should be larger than 10nF. If the Ccp2 is 10nF, the capacitance of Ccp1 should be larger than 100nF. A larger capacitance for Ccp1 would make the system more stable. CP_O output and VDD3V connection need to short-circuit through the external PCB.

Bandgap and common mode voltage (REFO)

When the VDDA is higher than 2.4V, the analog circuit can work. However, the analog circuit needs the current offset and the reference voltage. Therefore, the Bandgap reference voltage should be enabled before the analog circuit is enabled; the Bandgap reference voltage can be enabled by setting the register PMU [4] (ENBGR) as 1. Only after the Bandgap reference voltage is enabled, the common mode voltage (REFO) can effectively output 1.2V.

It is necessary to provide a common mode voltage (REFO) for the ADC to enable it. If the user wants to use the internal power supply, the ACMS should be set as 1; if the user wants to the external power supply, the ACMS should be set as 0 to output a common mode voltage (REFO). The user will need to use a reference voltage to drive the external circuit; therefore, the ENRFO should be set as 1 to output the common mode voltage to the pin; besides, the REFO is the Bandgap reference voltage with buffer. The output voltage of the REFO pin is about 1.2V and has +/-1mA push-pull driving ability. It can driver a 22~1000nF big capacitor load. If the external REFO voltage output is used, the common mode voltage for the ADC can be provided by an external power supply; in this case, the ACMS can be set as 0 to save more power.

The following table shows the voltage sources for all modules.

Table 5-1 Chip Power supply distribution

Block Name	Voltage source	Note	Block Name	Voltage source	Note
32-bit CPU Core N801	VDD18	-	Timer A/B/C PWM	VDD18	-
08KB SRAM	VDD18	-	GPIO Port	VDD3V	-
64KB Flash ROM	VDD3V/ VDD18	-	24-bit SD ADC	VDDA	-
Clock System	VDD18	-	08-bit DAC	VDDA	-
Watch Dog Timer	VDD18	-	Rail-to-Rail OPAMP	VDDA	-
Hardware RTC	VDD18	-	Analog Comparator	VDD3V	-
Charge Pump	VIN	-			
BOR	VDD3V/ VDD18	-			
Band Gap/Reference	VDDA	1.2V			
Hardware EUART	VDD18/VDD3V	-			
32-bit Hardware SPI	VDD18/VDD3V	-			
Hardware I2C	VDD18/VDD3V	-			

5.2. Register Address

Power Register Address	31	24	23	16	15	8	7	0
PMU base address + 0X00 (0X40400)	MASK1		REG1		MASK0		REG0	

5.3. Register Functions

5.3.1. Power Register PMU

Power Base Address + 0X00 (0X40400)								
Symbol	PMU (PMU Control Register)							
Bit	[31:24]	[23:20]	[19:18]			[17:16]		
Name	MASK	-	VDAS			ENVA		
RW	R0W-0	-	RW-0					
Bit	[15:08]	[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	-	ENBGR	ACMS	ENCHP	ENRFO	VDDLP
RW	R0W-0	-	RW-0					

Bit	Name	Description	
Bit[19~18]	VDAS	VDDA output voltage selection	
		00	VDDA output voltage=2.4V
		01	VDDA output voltage=2.7V
		10	VDDA output voltage=3.0V
		11	VDDA output voltage=3.3V
Bit[17~16]	ENVA	VDDA LDO Enable Control	
		00	High Z
		01	Short to VDD3V
		10	Weak pull down
		11	VDDA LDO 2.4/2.7/3.0/3.3V Set by VDAS

Bit	Name	Description	
Bit[04]	ENBGR	Band gap Enable Control	
		0	Disable
		1	Enable(would turn on by LDO)
Bit[03]	ACMS	ADC analog ground source selection	
		0	External analog ground
		1	Enable buffer and use internal source: (need to work with ADC)
Bit[02]	ENCHP	Charge Pump Enable Control	
		0	Disable
		1	Enable
Bit[01]	ENRFO	Reference Buffer Enable Control	
		0	Disable
		1	Enable
Bit[00]	VDDLP	VDD LDO with low power control	
		0	Normal (from sleep mode wake up needs to set 0)
		1	Low power

6. Clock System

6.1. Overall description

The clock control system provides the clocks for the whole chip, including the system clocks (CPU clock, APB clock) and all peripheral operating clocks (timer, communication interface, RTC, analog circuit, etc.) Each function module has a clock switch controller, clock source selection and frequency divider. Under the SLEEP mode, the controller always closes the external crystal oscillators, internal crystal oscillators and system clocks to minimize the system power consumption.

The operating clock sources include the external crystal oscillators, internal HAO and LPO oscillators; with the frequency divider, the frequency sources of the CPU and the peripheral devices can be flexibly allocated and managed to adjust the power consumption of the chip in order to save the energy.

6.1.1. External oscillators

There are two external oscillators, including the high-speed crystal oscillator (HSXT) and the low-speed crystal oscillator (LSXT). The chip has two independent input pins for the external high-speed crystal oscillator and low-speed crystal oscillator; thus, the user can connect the two external oscillators to the chip at the same time. The external oscillator should be connected to a resistor in parallel, or the crystal oscillator will not work even if it is soldered at the pin; besides, the crystal oscillator can be connected to two 10~20pF ground capacitors and the capacitance of each capacitor is subject to the parasitic capacitor caused by the layout of the PCB.

The parallel resistor between the pins of the oscillator and the capacitor C2/C1 parameters of each pin of the oscillator will vary with the frequency, brand of the external crystal oscillator and the layout of the PCB. The following table lists suggested allocation of the R1/C1/C2 parameters and the frequency sources for your reference. In the absence of special circumstances, it can also be capacitive default.

Type	Symbol	External crystal oscillator parameters				Instruction execution status	
		Frequency	R1/Ω	C1	C2	Sleep mode	Idle mode
Low-speed oscillator	LSXT	32768Hz	10M	10pF	10pF	Stop	Available
High-speed oscillator	HSXT	4~16MHz	1M	10pF	10pF	Stop	Available

6-1 Suggest external crystal oscillator configuration

Using an external crystal oscillator parameter Note:

- The external crystal shock 4MHz / 8MHz stabilization time is about 30ms, External 32768Hz crystal shock stabilization time is about 1.3s.
- After Sleep instruction execution, external crystal earthquake shock all stops.
- When External crystal oscillator parameter, note that the pin input / output configuration, the use shall not be required to set the configuration pin internal pullup resistor, in order to avoid abnormal operation. And the external resistor R1 must not default.
- To use an external oscillator (HSXT), recommended choosing the MCU clock / 2, can reducing the oscillator frequency source interference, and strengthening anti-jamming capability.

6.1.2. Internal crystal oscillators HAO and LPO

- The HAO is an internal high-speed RC oscillator of the chip and its typical output frequency is 2MHz/4MHz/10MHz; besides, it has several features, such as quick start, high anti-interference and low power consumption, etc. The output frequency of the HAO is adjustable; therefore, the user can adjust the output frequency of the HAO by software.

Matter needing attentions of using internal crystal oscillators:

- The output frequency of the HAO can be adjusted by modifying the register HAOTR 0x40304[7:0] Example: When set HAO work at 2MHz, if the actual output is only 1.99MHz, it can be controlled by adjusting the position HAOTR [7: 0] to adjust the frequency of the output, HAOTR default is 0x80, adjustments can be increased up HAO actual operating frequency.
- The default oscillator of the chip is the internal 2MHz HAO; the user can modify the default settings register 0x40300[4:3] to change the output frequencies of other HAOs.
- The stabilization time of the 4MHz HAO is about 0.5ms;
- After the SLEEP instruction is executed, all HAO oscillators will stop and enter the SLEEP mode.
- After the IDEL instruction is executed, all HAO oscillators will not stop, but the CPU will enter the IDEL mode.

The LPO is the internal low-speed RC oscillator of the chip; its output frequency is 35 kHz and has low power consumption; it will immediately start after the chip is power-on or wakened; besides, it cannot be enabled; in other words, the LPO will keep working during the whole operation process of the chip.

- The stabilization time of the LPO is about 510us and it is the only operating clock source of the WDT.

- After the SLEEP instruction is executed, all LPO oscillators will stop.
- After the IDEL instruction is executed, all LPO oscillators will not stop, but the CPU will enter the IDEL mode.

Typical output frequencies of the HAO and LPO are as shown in following Table 6-2.

Symbol	Frequency	Frequency source configuration			Instruction execution status	
		ENHAO[1]	HAOM[1:0]	CKHS[1]	Sleep	Idle
HAO	2MHz	1	00B	0	Stop	Oscillate
	4MHz	1	01B	0	Stop	Oscillate
	10MHz	1	10B	0	Stop	Oscillate
LPO	35kHz	Start after the chip is power-on		CKLS=0	Stop	Oscillate

Table 6-2 internal crystal oscillator configuration

HAO calibration method:

Chip HAO will have about +/- 10% error range, If the user wants a more accurate HAO operating frequency, the HYCON C library can be calibrated (DrvCLOCK_CalibrateHAO this function), This function can be set to control the HAO oscillation frequency error within the range of +/- 2%, Detailed HAO frequency specifications, refer to the document DS-HY16F188_EN Note, the function can refer to the following or document APD-HY16IDE004_EN:

-Function
void DrvCLOCK_CalibrateHAO (short int uMHz)
- Function
According to the factory calibration parameters of HAO to calibrate HAO, and need to corresponding to the selected HAO frequency.
Configure the register 0x40304[7:0]
-Input parameters
uMHz [in] pending correction of HAO frequency mode selection
0: Correction 2MHz; 1: Correction 4MHz; 2: Correction 10MHz;

6.1.3. CPU and external peripheral operating frequency sources configuration

Both of the external and internal crystal oscillators can provide the frequency sources for the CPU and the frequency sources will be provided for the CPU after passing the frequency dividers. The chip can determine the frequency source of the CPU is the HS_CK or LS_CK via the frequency selector MCUCKS [1] and perform the frequency

division via the frequency divider ENMCD [1]. Thus, there are multiple operating frequency modes for the CPU to select from to determine the instruction cycle of the chip.

Similarly, the external peripheral operating frequency sources are also provided by the external, internal crystal oscillators and the HS_CK or LS_CK passing the frequency dividers; or the frequency sources can be directly provided by the crystal oscillators, such as the WDT. As the external peripheral operating frequency configuration may vary with the different operations, please refer to the following figure for more information.

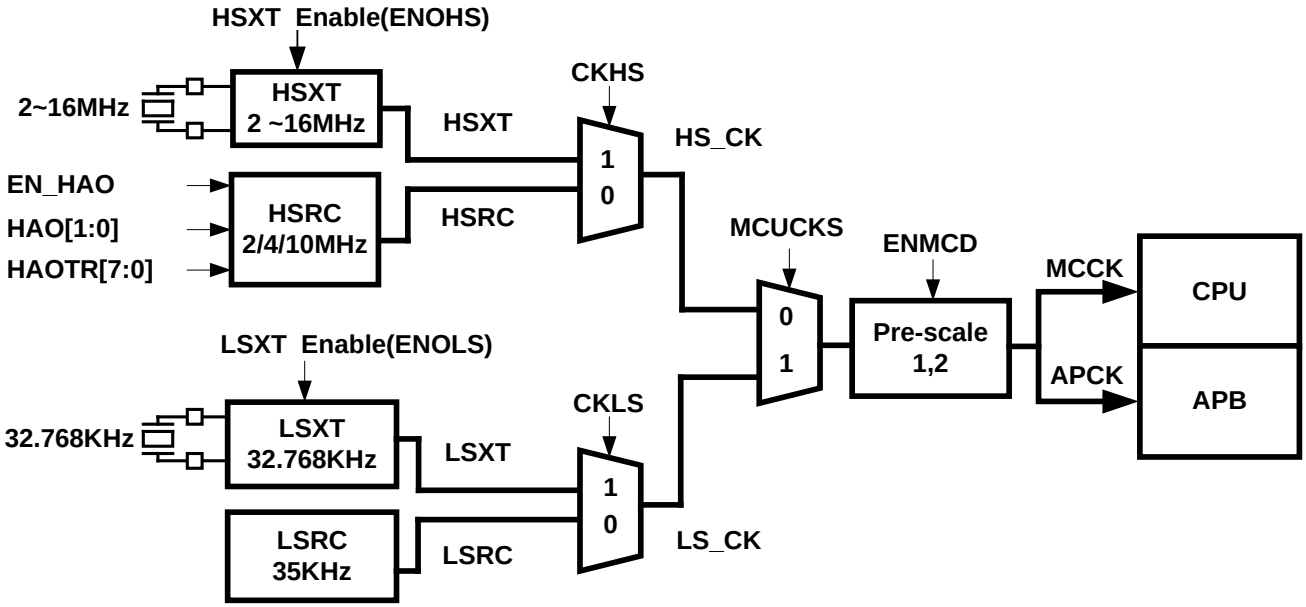


Table 6-1 CPU operating frequency source configuration diagram

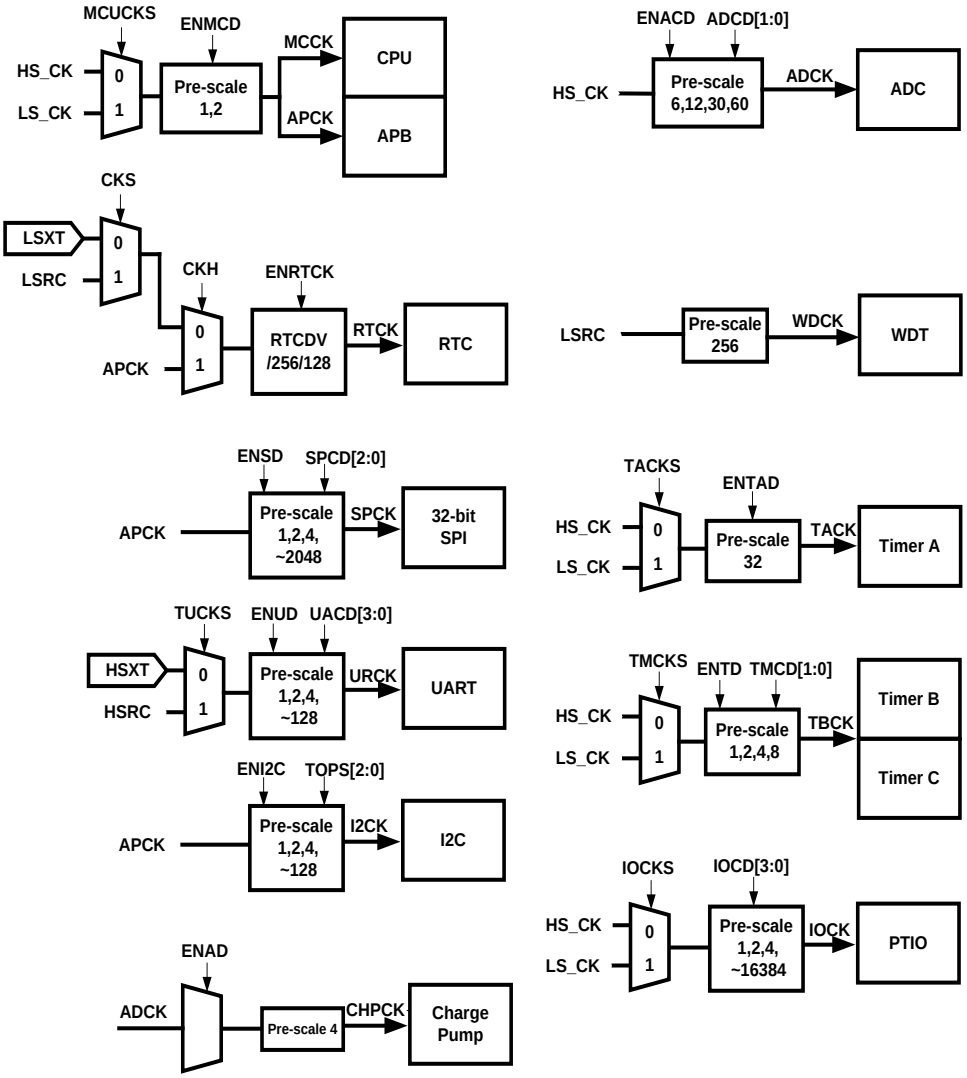


Table 6-2 External peripheral operating frequency configuration diagram

6.2. Register Address

Clock Register Address	31 24	23 16	15 8	7 0
CLK base address + 0X00 (0X40300)	-	-	MASK0	REG0
CLK base address + 0X04 (0X40304)	-	-	-	HAOTR
CLK base address + 0X08 (0X40308)	MASK1	REG1	MASK2	REG2
CLK base address + 0X0C (0X4030C)	MASK3	REG3	MASK4	REG4

-Reserved

6.3. Register Functions

6.3.1. Clock system register CLKCR0

Clock Base Address + 0X00 (0X40300)								
Symbol	CLK0 (Clock Control Register 0)							
Bit	[31:16]							
Name	RSV(Reserved)							
RW	R-0							
Bit	[15:8]	[7]	[6]	[5]	[4:3]	[2]	[1]	[0]
Name	MASK	OHS_HS	CKLS	CKHS	HAO	ENOLS	ENOHS	ENHAO
RW	R0W-0	RW-0						RW-1

Bit	Name	Description	
Bit[7]	OHS_HS	External oscillator mode selection	
		0	HSXT<4MHz
		1	HSXT>4MHz
Bit[6]	CKLS	Chip low-speed frequency source selection	
		0	Internal low-speed oscillator (LPO)
		1	External low-speed oscillator (LSXT)
Bit[5]	CKHS	Chip high-speed frequency source selection	
		0	internal High-speed oscillator (HAO)
		1	External high-speed oscillator (HSXT)
Bit[4~3]	HAO	Internal high-speed oscillator mode configuration	
		[00]	2MHz
		[01]	4MHz
		[10]	10MHz
		[11]	Reserved
Bit[02]	ENOLS	External low-speed oscillator enablement control	
		0	Disable
		1	Enable
Bit[01]	ENOHS	External high-speed oscillator enablement control	
		0	Disable
		1	Enable
Bit[00]	ENHAO	Internal high-speed oscillator enablement control	
		0	Disable
		1	Enable

6.3.2. Clock system register CLKCR1

Clock Base Address + 0X04 (0X40304)		
Symbol	CLK1 (Clock Control Register 1)	
Bit	[31:16]	
Name	Reserved	
RW	R-0	
Bit	[15:8]	[7:0]
Name	Reserved	HAOTR
RW	R-0	RW-80H

Bit	Name	Description	
Bit[7:0]	HAOTR	Internal High Speed Oscillator Trim Register (Register Only)	
		0	Set 0
		1	Set 1

1LSB.Step = 0.125%

0000_0000 is the Slowest

1000_0000 is the Default

1111_1111 is the Fastest

6.3.3. Clock system register CLKCR2

Clock Base Address + 0X08 (0X40308)								
Symbol	CLK2 (Clock Control Register 2)							
Bit	[31:24]	[23]	[22]	[21]	[20]		[19:16]	
Name	MASK	ENRTCK	-	TUCKS	ENUD		UACD	
RW	R0W-0	RW-0	-	RW-0				
Bit	[15:08]	[7]	[6]	[5:4]	[3]	[2]	[1]	[0]
Name	MASK	TMCKS	ENTD	TMCD	TACKS	ENTAO	ENMCD	MCUCKS
RW	R0W-0	RW-0						

Bit	Name	Description	
Bit[23]	ENRTCK	RTC Clock Source control	
		0	Disable (The RTC register cannot be written in and unlocked.)
		1	Enable (The RTC register can be unlocked.)
Bit[21]	TUCKS	EUART clock source selection	
		0	HSXT : External high speed oscillator
		1	HAO: Internal high speed oscillator
Bit[20]	ENUD	EUART clock source enablement control	
		0	Disable
		1	Enable
Bit[19~16]	UACD	EUART clock source frequency divider configuration	
		0000	EUART clock source/1
		0001	EUART clock source/2
		0010	EUART clock source/4
		0011	EUART clock source/8
		0100	EUART clock source/16
		0101	EUART clock source/32
		0110	EUART clock source/64
		0111	EUART clock source/128
		1000	Reserved
		1001	Reserved
		1010	Reserved
		1011	Reserved
		1100	Reserved
		1101	Reserved
		1110	Reserved
		1111	Reserved

Bit	Name	Description	
Bit[07]	TMCKS	Timer B,C clock source selection	
		0	HS_CK
		1	LS_CK
Bit[06]	ENTD	Timer B,C clock source enablement control	
		0	OFF
		1	ON
Bit[5~4]	TMCD	Timer B,C clock source frequency divider configuration	

		00	clock/1
		01	clock/2
		10	clock/4
		11	clock/8
Bit[03]	TACKS	Timer A clock source selection	
		0	HS_CK
		1	LS_CK
Bit[02]	ENTAO	Timer A clock source frequency divider configuration	
		0	Disable the frequency divider
		1	Timer A clock/32
Bit[01]	ENMCD	MCU input clock source frequency divider configuration	
		0	MCU clock/1
		1	MCU clock/2
Bit[00]	MCUCKS	MCU input clock source selection	
		0	HS_CK
		1	LS_CK

6.3.4. Clock system register CLKCR3

Clock Base Address + 0X08 (0X4030C)						
Symbol	CLK3 (Clock Control Register 3)					
Bit	[31:24]	[23:21]	[20]	[19:16]		
Name	MASK	-	IOCKS	IOCD		
RW	R0W-0	-	RW-0			
Bit	[15:08]	[7]	[6]	[5:4]	[3]	[2:0]
Name	MASK	ADCKP	ENACD	ADCD	ENSD	SPCD
RW	R0W-0	RW-0				

Bit	Name	Description	
Bit[20]	IOCSK	GPIO input clock source selection	
		0	HS_CK
		1	LS_CK
Bit[19~16]	IOCD	GPIO clock frequency divider configuration	
		0000	Disable
		0001	GPIO clock source/ 1
		0010	GPIO clock source/ 2
		0011	GPIO clock source/ 4
		0100	GPIO clock source/ 8
		0101	GPIO clock source/ 16
		0110	GPIO clock source/ 32
		0111	GPIO clock source/ 64
		1000	GPIO clock source/ 128
		1001	GPIO clock source/ 256
		1010	GPIO clock source/ 512
		1011	GPIO clock source/ 1024
		1100	GPIO clock source/ 2048
		1101	GPIO clock source/ 4096
		1110	GPIO clock source/ 8192
		1111	GPIO clock source/ 16384
Bit[07]	ADCKP	ADC input clock phase shift	
		0	ADC clock rising edge is CPU clock low
		1	ADC clock rising edge is CPU clock high
Bit[06]	ENACD	Enable ADC clock source divider	
		0	Disable
		1	Enable

Bit[5~4]	ADCD	Enable ADC clock divider	
		00	ADC clock/6
		01	ADC clock/12
		10	ADC clock/30
		11	ADC clock/60
Bit[03]	ENSD	SPI clock switch	
		0	Disable
		1	Enable
Bit[2~0]	SPCD	SPI clock frequency divider configuration	
		000	SPI clock source/1
		001	SPI clock source/2
		010	SPI clock source/4
		011	SPI clock source/8
		100	SPI clock source/32
		101	SPI clock source/128
		110	SPI clock source/512
		111	SPI clock source/2048

7. Interrupt Mode

7.1. Overall description

Interrupt vectors and interrupt priority Description:

The interrupt module includes the interrupt startup controller, interrupt enable controller and interrupt event flag register to manage the overall interrupt service, such as communication interrupt, timer interrupt, ADC interrupt, comparator interrupt and IO external interrupt. The chip provides 6-stage interrupt source and also provides 4-stage interrupt vector priorities, including HW0, HW1…HW5 (from high priority to low priority). The interrupt service is composed of the interrupt event flag (INTF), interrupt event service intelligent startup (INTE), interrupt general control GIE and vector addresses HW0~HW5. When the interrupt event occurs and the interrupt event service is enabled, the program counter PC will turn to the interrupt service vector addresses HW0~HW5 of the program memory at the next instruction cycle to execute the interrupt service program.

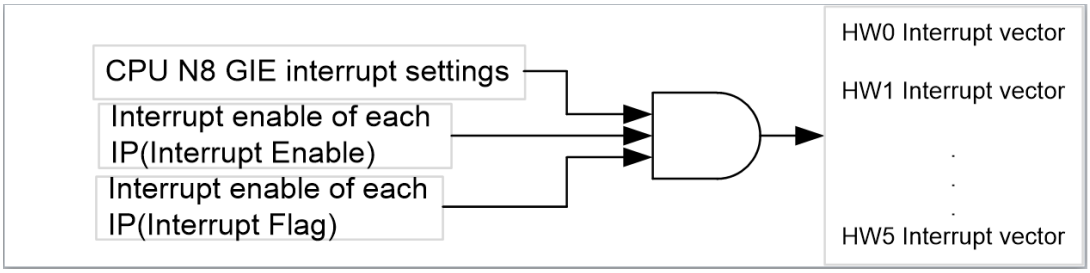


Figure 7-1 Interrupt Service Chart

Detail operation description:

- The user can set the corresponding interrupt enable bit to be 1 or clear the bit 0 to enable or disable the corresponding interrupt function. The interrupt function can be enabled by setting the corresponding interrupt enable bit to be 1.
- After the interrupt event takes place, the interrupt flag will be generated; the user can clear the flag to cancel the interrupt request.
- It is necessary to set the global interrupt enable bit GIE=1, or any interrupt cannot be enabled.
- The interrupt vector priority will be determined when multiple interrupt requests take place at the same time; the interrupt vector with high priority should be replied first.
- During the execution of the interrupt vector service program, the high-level interrupt vectors can terminate the current interrupt service to execute the high-level interrupt service.

- when the advanced interrupt service executed, the program will Back to the original interrupt service program, continue down the implementation program

The corresponding interrupt vector program entry addresses of the interrupts of the chip are as shown in the following table.

Interrupt Vector Address	N801	Interrupt Function
INT Base Address + 0x00 (COM)	HW0	void HW0_ISR(void)
INT Base Address + 0x04 (Timer ABC WDT HW RTC)	HW1	void HW1_ISR(void)
INT Base Address + 0x08 (ADC)	HW2	void HW2_ISR(void)
INT Base Address + 0x0C (CMP/OPA)	HW3	void HW3_ISR(void)
INT Base Address + 0x10 (PT1)	HW4	void HW4_ISR(void)
INT Base Address + 0x14 (PT2)	HW5	void HW5_ISR(void)

7.2. Register Address

Interrupt Register Address	31 24	23 16	15 8	7 0
INT base address + 0x00 (COM) (0X40000)	MASK0	REG0	MASK1	REG1
INT base address + 0x04 (TMR) (0X40004)	MASK2	REG2	MASK3	REG3
INT base address + 0x08 (ADC) (0X40008)	MASK4	REG4	MASK5	REG5
INT base address + 0x0C (CMP) (0X4000C)	MASK6	REG6	MASK7	REG7
INT base address + 0x10 (PT1) (0X40010)	MASK8	REG8	MASK9	REG9
INT base address + 0x14 (PT2) (0X40014)	MASK10	REG10	MASK11	REG11

-Reserved

7.3. Register Functions

7.3.1. Interrupt control register INTCOM

INT Base Address + 0X00 (0X40000)								
Symbol	INTCOM (Interrupt Control Register 0)							
Bit	[31:24]	[23:22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	I2CEIE	I2CIE	UTXIE	URXIE	STXIE	SRXIE
RW	R0W-0	-	RW-0					
Bit	[15:08]	[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	I2CEIF	I2CIF	UTXIF	URXIF	STXIF	SRXIF
RW	R0W-0	-	RW0-0					

Bit	Name	Description	
Bit[21]	I2CEIE	I2C error interrupt enable control	
		0	Disable
		1	Enable
Bit[20]	I2CIE	I2C Interrupt enable control	
		0	Disable
		1	Enable
Bit[19]	UTXIE	UART transmits (TX) interrupt enable control	
		0	Disable
		1	Enable
Bit[18]	URXIE	UART receives (RX) interrupt enable control	
		0	Disable
		1	Enable
Bit[17]	STXIE	SPI transmits (TX) interrupt enable control	
		0	Disable
		1	Enable
Bit[16]	SRXIE	SPI receives (RX) interrupt enable control	
		0	Disable
		1	Enable
Bit[05]	I2CEIF	I2C error interrupt flag (level-trigger)	
		0	Normal
		1	I2C error takes place and interrupt occurs
Bit[04]	I2CIF	I2C interrupt flag (level-trigger)	
		0	Normal
		1	I2C interrupt occurs
Bit[03]	UTXIF	UART transmits (TX) interrupt flag (level-trigger)	

		0	Normal
		1	UART transmission (TX) interrupt occurs.
Bit[02]	URXIF	UART receives (RX) interrupt flag (level-trigger)	
		0	Normal
		1	UART receives (RX) interrupt occurs.
Bit[01]	STXIF	SPI transmission (TX) interrupt flag (level-trigger)	
		0	Normal
		1	SPI transmission (TX) interrupt occurs.
Bit[00]	SRXIF	SPI reception (RX) interrupt flag (level-trigger)	
		0	Normal
		1	SPI reception (RX) interrupt occurs.

7.3.2. Interrupt control register INTTMR

INT Base Address + 0X04 (0X40004)								
Symbol	INTTMR (Interrupt Control Register 1)							
Bit	[31:24]	[23:22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	RTCIE	WDTIE	TMC1IE	TMC0IE	TMBIE	TMAIE
RW	R0W-0	-	RW-0					
Bit	[15:08]	[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	RTCIF	WDTIF	TMC1IF	TMC0IF	TMBIF	TMAIF
RW	R0W-0	-	RW0-0					

Bit	Name	Description	
Bit[21]	RTCIE	RTC interrupt enable control	
		0	Disable
		1	Enable
Bit[20]	WDTIE	WDT interrupt enable control	
		0	Disable
		1	Enable
Bit[19]	TMC1IE	TMC1 interrupt enable control	
		0	Disable
		1	Enable
Bit[18]	TMC0IE	TMC0 interrupt enable control	
		0	Disable
		1	Enable
Bit[17]	TMBIE	Timer TMB interrupt enable control	
		0	Disable
		1	Enable
Bit[16]	TMAIE	Timer TMA interrupt enable control	
		0	Disable
		1	Enable
Bit[05]	RTCIF	RTC interrupt flag	
		0	Normal
		1	RTC interrupt occurs
Bit[04]	WDTIF	WDT interrupt flag	
		0	Normal
		1	WDT interrupt occurs
Bit[03]	TMC1IF	TMC1 interrupt flag	
		0	Normal
		1	TMC1 interrupt occurs
Bit[02]	TMC0IF	TMC0 interrupt flag	
		0	Normal

		1	TMC0 interrupt occurs
Bit[01]	TMBIF	Timer TMB interrupt flag	
		0	Normal
		1	Timer TMB interrupt occurs
Bit[00]	TMAIF	Timer TMA interrupt flag	
		0	Normal
		1	Timer TMA interrupt occurs

Note: If any of IE (RTC / WDT / TMA / TMB / TMC0 / TMC1) is not turned on, When IE (Interrupt Enable) is disable, even if the count has overflowed, it will not generate an interrupt request flag. To generate an interrupt request flag, the corresponding IE (Interrupt Enable) to open, so that count overflow will generate an interrupt request flag.

7.3.3. Interrupt control register INTADC

INT Base Address + 0X08 (0X40008)			
Symbol	INTADC (Interrupt Control Register 2)		
Bit	[31:24]	[23:17]	[16]
Name	MASK	-	ADCIE
RW	R0W-0	-	RW-0
Bit	[15:08]	[07:01]	[00]
Name	MASK	-	ADCIF
RW	R0W-0	-	RW0-0

Bit	Name	Description	
Bit[16]	ADCIE	ADC converter interrupt enable control	
		0	Disable
		1	Enable
Bit[00]	ADCIF	ADC converter interrupt flag	
		0	Normal
		1	ADC converter interrupt occurs.

7.3.4. Interrupt control register INTCMP

INT Base Address + 0X0C (0X4000C)				
Symbol	INTCMP (Interrupt Control Register 3)			
Bit	[31:24]	[23:18]	[17]	[16]
Name	MASK	-	CPOIE	OPOIE
RW	R0W-0	-	RW-0	
Bit	[15:08]	[07:02]	[01]	[00]
Name	MASK	-	CPOIF	OPOIF
RW	R0W-0	-	RW0-0	

Bit	Name	Description	
Bit[17]	CPOIE	Multi-function comparator output (CPO) interrupt enable control	
		0	Disable
		1	Enable
Bit[16]	OPOIE	Low-noise OP amplifier output (OPO) interrupt enable control	
		0	Disable
		1	Enable
Bit[01]	CPOIF	Multi-function comparator output (CPO) interrupt flag	

		0	Normal
		1	Multi-function comparator output (CPO) interrupt occurs.
Bit[00]	OPOIF	Low-noise OP amplifier output (OPO) interrupt flag	
		0	Normal
		1	Low-noise OP amplifier output (OPO) interrupt occurs

7.3.5. Interrupt control register INTPT1

INT Base Address + 0X10 (0X40010)									
Symbol	INTPT1 (Interrupt Control Register 4)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	PT17IE	PT16IE	PT15IE	PT14IE	PT13IE	PT12IE	PT11IE	PT10IE
RW	R0W-0	RW-0							
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	PT17IF	PT16IF	PT15IF	PT14IF	PT13IF	PT12IF	PT11IF	PT10IF
RW	R0W-0	RW0-0							

Bit	Name	Description	
Bit[23]	PT17IE	PT17 external interrupt enable control	
		0	Disable
		1	Enable
Bit[22]	PT16IE	PT16 external interrupt enable control	
		0	Disable
		1	Enable
Bit[21]	PT15IE	PT15 external interrupt enable control	
		0	Disable
		1	Enable
Bit[20]	PT14IE	PT14 external interrupt enable control	
		0	Disable
		1	Enable
Bit[19]	PT13IE	PT13 external interrupt enable control	
		0	Disable
		1	Enable
Bit[18]	PT12IE	PT12 external interrupt enable control	
		0	Disable
		1	Enable
Bit[17]	PT11IE	PT11 external interrupt enable control	
		0	Disable
		1	Enable
Bit[16]	PT10IE	PT10 external interrupt enable control	
		0	Disable
		1	Enable

Bit	Name	Description	
Bit[07]	PT17IF	PT17 Interrupt Flag	
		0	Normal
		1	Interrupted
Bit[06]	PT16IF	PT16 Interrupt Flag	
		0	Normal
		1	Interrupted
Bit[05]	PT15IF	PT15 Interrupt Flag	
		0	Normal

		1	Interrupted
Bit[04]	PT14IF	PT14 Interrupt Flag	
		0	Normal
		1	Interrupted
Bit[03]	PT13IF	PT13 Interrupt Flag	
		0	Normal
		1	Interrupted
Bit[02]	PT12IF	PT12 Interrupt Flag	
		0	Normal
		1	Interrupted
Bit[01]	PT11IF	PT11 Interrupt Flag	
		0	Normal
		1	Interrupted
Bit[00]	PT10IF	PT10 Interrupt Flag	
		0	Normal
		1	Interrupted

7.3.6. Interrupt control register INTPT2

INT Base Address + 0X14 (0X40014)									
Symbol	INTPT2 (Interrupt Control Register 5)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	PT27IE	PT26IE	PT25IE	PT24IE	PT23IE	PT22IE	PT21IE	PT20IE
RW	R0W-0	RW-0							
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	PT27IF	PT26IF	PT25IF	PT24IF	PT23IF	PT22IF	PT21IF	PT20IF
RW	R0W-0	RW0-0							

Bit	Name	Description	
Bit[23]	PT27IE	PT27 Interrupt Enable	
		0	Disable
		1	Enable
Bit[22]	PT26IE	PT26 Interrupt Enable	
		0	Disable
		1	Enable
Bit[21]	PT25IE	PT25 Interrupt Enable	
		0	Disable
		1	Enable
Bit[20]	PT24IE	PT24 Interrupt Enable	
		0	Disable
		1	Enable
Bit[19]	PT23IE	PT23 Interrupt Enable	
		0	Disable
		1	Enable
Bit[18]	PT22IE	PT22 Interrupt Enable	
		0	Disable
		1	Enable
Bit[17]	PT21IE	PT21 Interrupt Enable	
		0	Disable
		1	Enable
Bit[16]	PT20IE	PT20 Interrupt Enable	
		0	Disable
		1	Enable

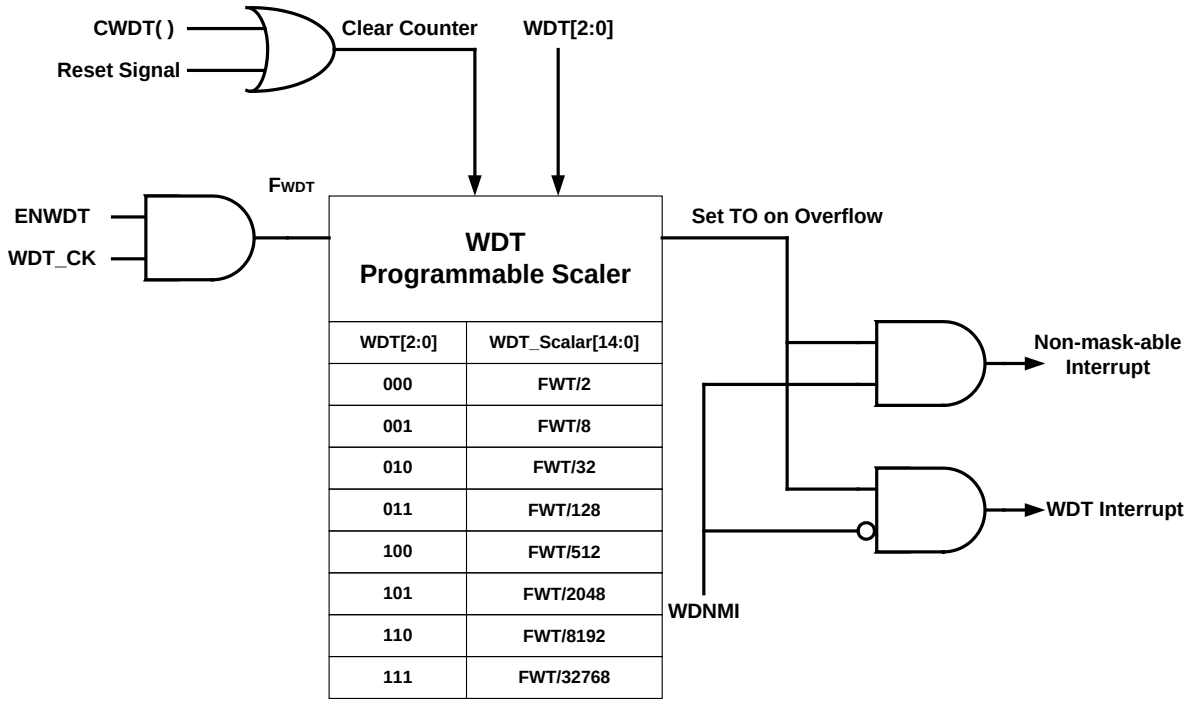
Bit	Name	Description	
Bit[07]	PT27IF	PT27 Interrupt Flag	
		0	Normal
		1	Interrupted
Bit[06]	PT26IF	PT26 Interrupt Flag	
		0	Normal
		1	Interrupted
Bit[05]	PT25IF	PT25 Interrupt Flag	
		0	Normal
		1	Interrupted
Bit[04]	PT24IF	PT24 Interrupt Flag	
		0	Normal
		1	Interrupted
Bit[03]	PT23IF	PT23 Interrupt Flag	
		0	Normal
		1	Interrupted
Bit[02]	PT22IF	PT22 Interrupt Flag	
		0	Normal
		1	Interrupted
Bit[01]	PT21IF	PT21 Interrupt Flag	
		0	Normal
		1	Interrupted
Bit[00]	PT20IF	PT20 Interrupt Flag	
		0	Normal
		1	Interrupted

8. Watch Dog Timer

8.1. Introduction

The watch dog timer (WDT) is, as the name implies, the watcher of the chip, and its main function is to generate the wake-up event or execute basic reset function after the chip crashes accidentally.

- Active Mode
  The WDT overflows and then generate the reset signal to reset the chip.
  The WDT can be cleared by using software.
- Sleep Mode
  The WDT is disabled, and cannot work.
- Idle Mode
  The watchdog timer overflows without generating a reset signal and the WDT cannot restart the MCU.



WDT[2:0]	WDT_Scalar[14:0]
000	FWT/2
001	FWT/8
010	FWT/32
011	FWT/128
100	FWT/512
101	FWT/2048
110	FWT/8192
111	FWT/32768

FIG. 8-1 WDT block diagram

8.1.1. WDT operating instruction

Setting the frequency divider WDTP [2:0] can determine the operating frequency and the overflow value of the WDT. After the WDT overflows, the WDT reset signal or interrupt event can be generated. The control bit WDNMI 0x40108[6] determines the reset signal or the interrupt request signal will be generated after the WDT overflows; if 0 is written in the bit, the WDT will generate the interrupt request signal. Please refer to the chapter

about the interrupt control chapter for more information about the interrupt mode. The WDT can start up only when the chip is in operation; the WDT can start up by setting the control bit ENWDT [1] as <1>. It is necessary to enable the global interrupt control bit GIE before enabling the interrupt function.

The operating frequency source of the WDT is LPO; therefore, the calculation of the theoretical values of the operating frequency and the overflow value of the WDT is as follows:

WDT= LPO /256 /WDTP[2:0] （Equation 8-1）

LPO is the frequency of the internal low-speed RC oscillator; and WDTP is the frequency divider；

Assuming that LPO=33.9 KHz and WDTP=32768, the operating frequency of the WDT is: 33900Hz/256/WDT_PS(32768)=0.00404Hz

8.2. Register Address

SYS Register Address	31	24	23	16	15	8	7	0
SYS base address + 0X08 (SYS) (0X40108)	WDTO1		WDTO0		MASK0		REG0	

8.3. Register Functions

8.3.1. WDT Register0

SYS Base Address + 0X08 (0X40108)							
Symbol	WDTCR (WDT Control Register)						
Bit	[31]	[30:16]					
Name	-	WDTO					
RW	-	R-0					
Bit	[15:8]	[7]	[6]	[5]	[4]	[3]	[2:0]
Name	MASK	-	WDNMI	CLWDT	ENWDT	-	WDTP
RW	R0W-0	-	RW1-0	RW-0	RW1-0	-	RW-7

Bit	Name	Description	
Bit[30~16]	WDTO	counter register of WDT	
		0	Set 0
		1	Set 1
Bit[06]	WDNMI	WDT interrupt operating mode selection	
		0	Timer mode
		1	Reset mode **(As long as the Reset Mode is set, the Timer Mode cannot be switched)**
Bit[05]	CLWDT	WDT reset control	
		0	Disable
		1	Enable
Bit[04]	ENWDT	WDT enable control	
		0	Disable
		1	Enable **(As long as the setting is on , it will not turn off)**
Bit[2~0]	WDTP	WDT overflow value configuration	
		[000]	0 : WCLK / 2
		[001]	1 : WCLK / 8
		[010]	2 : WCLK / 32
		[011]	3 : WCLK / 128
		[100]	4 : WCLK / 512
		[101]	5 : WCLK / 2048
		[110]	6 : WCLK / 8192
		[111]	7 : WCLK / 32768

9. Timer A Management

9.1. Introduction

Timer A is a 16-bit up counter and can be operated in Active mode and the Wait mode. It can be used to generate different output frequencies.

Main features:

(1) Up counter
(2) 16-stage overflow values are available to be selected.
(3) Overflow generates an interrupt event.
(4) The values of the counter can be read

Initial configuration of Timer A (TMA):

TMA is a 16-bit up counter. Its input clock source is the TACK and it will perform the counting according to each rising edge of the TACK and the frequency of the input clock source is controlled by the clock system management module. The function of the TMA can be enabled or disabled by setting the control bit ENTA [1] as 1 or 0.

The overflow value of the TMA can be adjusted by the frequency divider TAS [3:0]; the user can change the overflow value by modifying the value of the frequency divider TAS to generate the counting values with different frequencies. The control bit TACLR [1] is set as 1 but the TMA is reset and the counter register becomes 0; after the counter register is cleared, the control bit TACLR will automatically become 0.

After the TMA overflows, the interrupt request will be generated and the TMA interrupt flag TMAIF will be set as <1>; if the TMA interrupt function is enabled and the global interrupt control bit is set as 1, the chip will enter the TMA interrupt service event in response to the TMA interrupt request. The TMA interrupt request can be cancelled by clearing the TMA interrupt flag; in this way, the chip will not reply the TMA interrupt.

The TMA has a 16-stage frequency dividing configuration, which allows the TMA to have a wide counting range; the calculation of the overflow value of the TMA is as follows:

TAR[15:0]=1/（TACK/32/TAS[3:0]） （Equation 9-1）

The TACK is the input clock source of the TMA and the TAS[3:0] is the frequency dividing value;

Assuming the TMA selects the LS_CK, and the LS_CK is from the LPO; then TACK=35 KHz, TAS[3:0]=1001B=/1024 and the theoretical value of the overflow value of the Timer A: 35000Hz/32/TAS(1024)=35000Hz/32/1024=1.068Hz

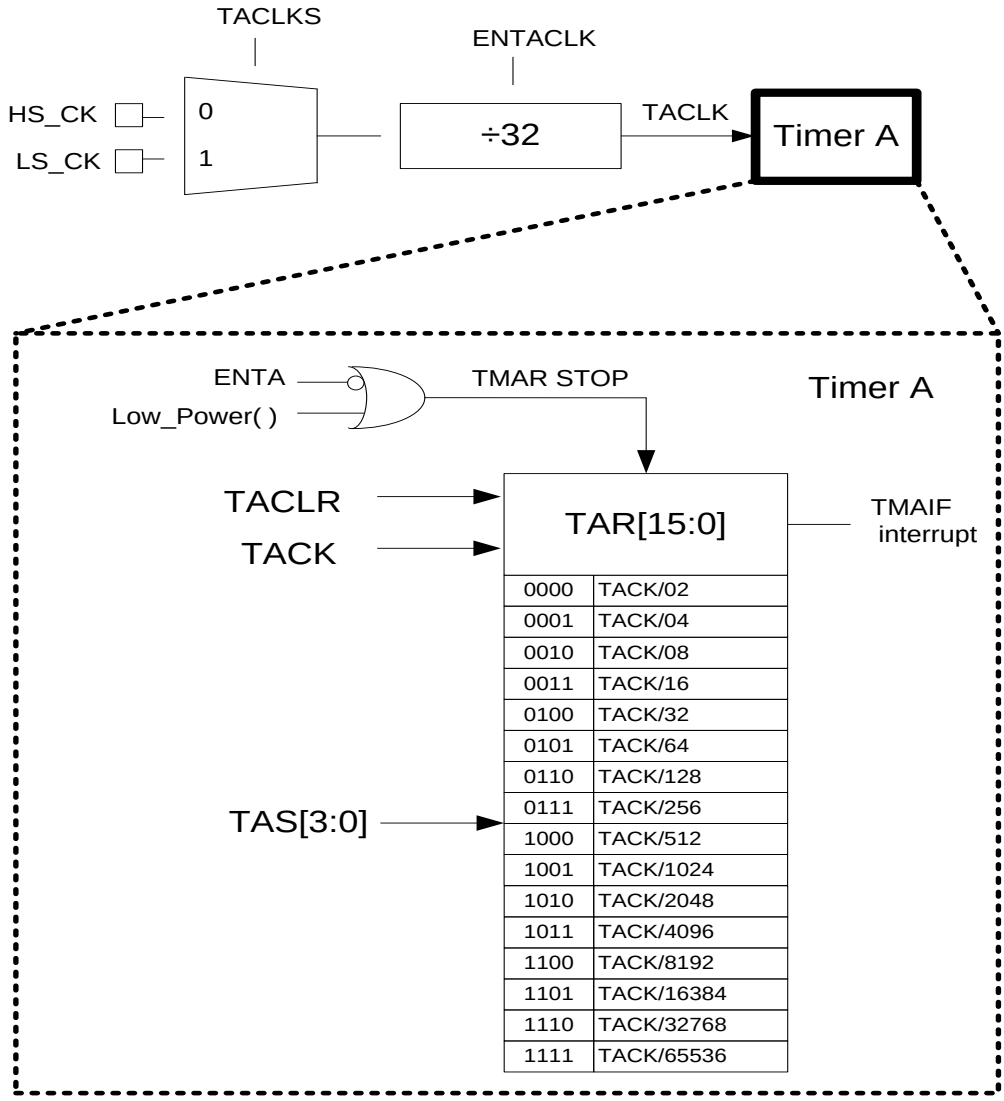


FIG. 9-1 Timer A block diagram

9.2. Register Address

TMR Register Address	31	24	23	16	15	8	7	0
TMA base address + 0x00(0X40C00)	TAR1		TAR0		MASK0		REG0	

9.3. Register Functions

9.3.1. TMA Register TMACR

TMA Base Address + 0X00 (0X40C00)					
Symbol	TMACR(TMA Control Register)				
Bit	[31:16]				
Name	TAR				
RW	R-0				
Bit	[15:8]	[7:6]	[5]	[4]	[3:0]
Name	MASK	-	ENTA	TACLR	TAS
RW	R0W-0	-	RW-0		RW-0XF

Bit	Name	Description	
Bit[31-16]	TAR	Timer A counter	
		TAR[31:16] is the 16-bit timer A counter value output register from MSB to LSB	
Bit[5]	ENTA	Enable timer A	
		0	Disable
		1	Enable
Bit[4]	TACLR	Clear timer A Count value	
		0	Normal
		1	Clear (edge clear. Auto return to 0)
Bit[3~0]	TAS	Timer A divider input	
		0000	Timer A clock/2
		0001	Timer A clock/4
		0010	Timer A clock/8
		0011	Timer A clock/16
		0100	Timer A clock/32
		0101	Timer A clock/64
		0110	Timer A clock/128
		0111	Timer A clock/256
		1000	Timer A clock/512
		1001	Timer A clock/1024
		1010	Timer A clock/2048
		1011	Timer A clock/4096
		1100	Timer A clock/8192
		1101	Timer A clock/16384
		1110	Timer A clock/32768
		1111	Timer A clock/65536

10. Timer B Management

10.1. Introduction

The Timer B is a 16-bit counter, which can be used to perform time counting, time controlling, clock generating and time delaying, etc. It will generate the interrupt signal when the counting flow takes place, and the program can read the current counting value of the TMB; besides, the TMB can be also used to generate the waveform of the PWM. It can be operated under the active mode and the wait mode.

The 16-bit counter register of the Timer B can be separated into two independent 8-bit counter registers; thus, the TMB has four counting methods:

- 16-bit up counting method, which can generate the interrupt signal;
- 16-bit counting method; it will increase to the overflow value and then decrease to 0, which can generate the interrupt signal;
- Two independent 8-bit up counting methods; the low 8-bit counter overflows and then the high 8-bit counter is automatically added by 1, which can generate the interrupt signal;
- 8 + 8-bit count up mode, low 8-bit counter overflow, high 8-bit counter is automatically increased by 1, can generate an interrupt signal.

Moreover, the TMB has three counter overflow controller: TBC0, TBC1 and TBC2. TMB can also serve as the PWM waveform generator, which can provide two PWM waveforms PWM0/PWM1; and each has multiple operation modes and can satisfy different PWM output requirements; the operation modes are as follows:

- PWMA /PWMB /PWMC /PWMD /PWME /PWMF /PWMG

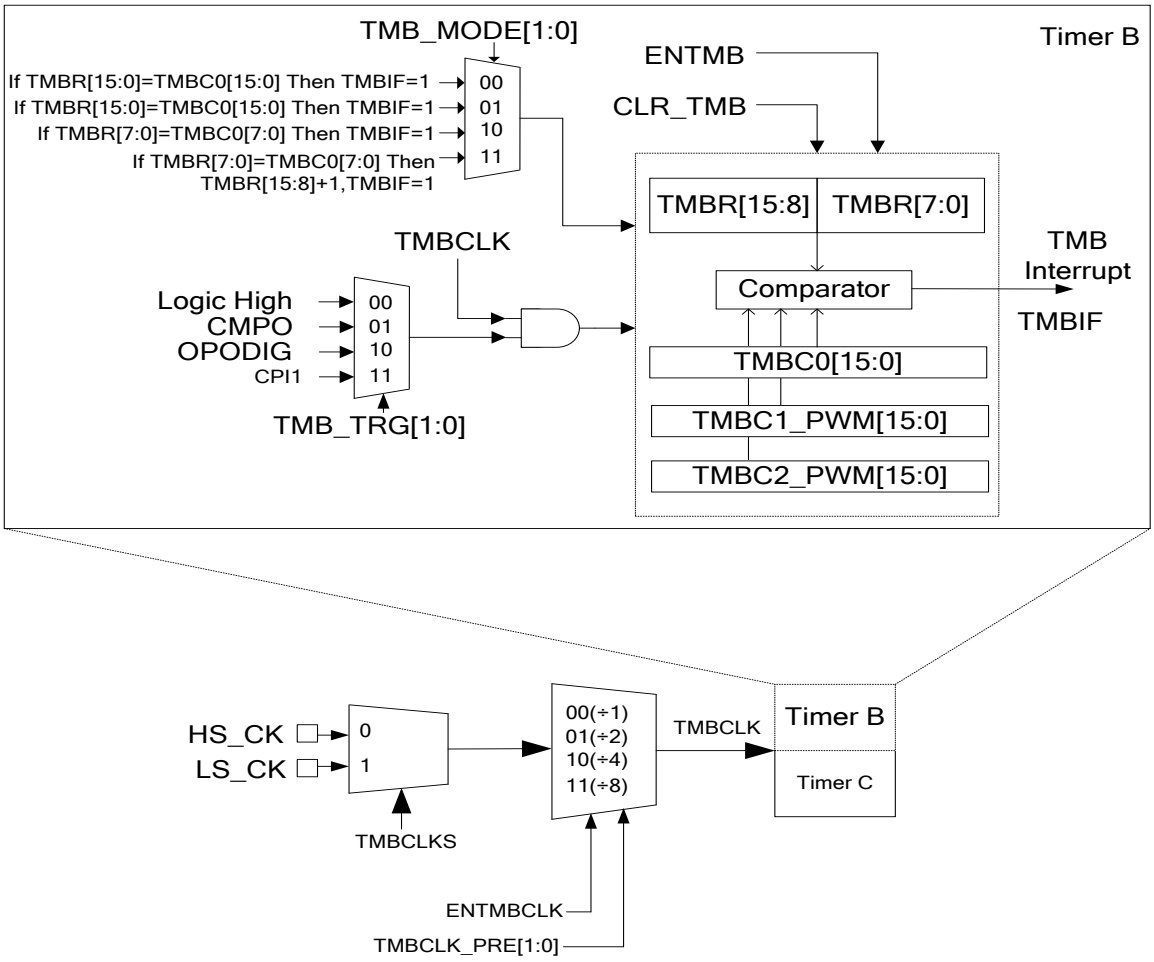


FIG. 10-1 Timer B block diagram

Note: The TBR in the Timer B block diagram represents the TBR described in this article. TMBR [15:8] =TBR [15:8], TMBR [7:0] =TBR [7:0]

10.1.1. Timer mode

The Timer B is a 16-bit up counter, which can be used to generate the PWM waveforms. It can be used to perform the time counting, time controlling, clock generating, etc., and can generate the interrupt signal when the counter overflow takes place. The TMB can be operated under the operation mode and the IDEL mode.

It has four different counting methods, and can generate the counting values with different frequencies:

(1)16-bit up counting method, which can generate the interrupt signal;

(2)16-bit counting method; it will increase to the overflow value and then decrease to 0, which can generate the interrupt signal;

(3)Two independent 8-bit up counting methods; the maximum count value 0xFF, can generate an interrupt signal

(4) The low 8-bit counter overflows and then the high 8-bit counter are automatically added by 1, which can generate the interrupt signal;

It has four different counting-trigger signal sources, which can be applied to count different events:

(1)Continuous counting method is always enabled;

(2)The comparator outputs (CMPO) high-potential trigger.

(3)The OP amplifier outputs (OPOD) high-potential trigger.

(4)The Timer C outputs (CPI1) high-potential trigger.

The operating clock source of the TMB is HS_CK or LS_CK, which will pass through the frequency divider to generate the frequency source TBCLK to provide the operating frequency for the TMB. To set the divide-by-count TMCD [1: 0], the TMB can be set for different counting cycles. The clock source of the TMB can be set at the clock system control module.

TMBR：16-bit timer/counter registers

The TMBR is a 16-bit timer/counter register, which can be separated into two independent 8-bit timer/counter registers in order to satisfy the four different counting methods of the TMB. The TMBR will crease or decrease at each rising edge of the TBCLK; under different counting methods, the TMBR will increase or decrease according to different conditions. TMBR can be automatically cleared by setting the control bit TBRST [1] as <1> and the control bit TBRST will automatically become 0 after the TMBR is cleared. The program can also read the current counting value of the TMBR for other purposes.

The TBEN is the enable control signal of the TMB. If the bit is set as 1, the counting function of the TMB will be enabled; if the bit is set as 0, the counting function of the TMB will be disabled.

The TBEBS [1:0] is the counting-trigger signal source controller; the controller can provide four different counting-trigger signal sources.

TBM [3:2] is the counting method controller of the TMB; the controller can provide four different counting methods. The TBRST is the control bit of the TMB counter register. If the bit is set as <1>, the counter register will be automatically cleared and then the bit will automatically become 0.

Operating configuration when TMB serves as a timer/counter:

- Set the operating clock source of the TMB and set the control bits 0x40308[6](ENTD) and 0x40308[5:4](TMCD);
- Select the counting mode and set the control bit TBM[3:2];

- Select the counting-trigger signal source and set the TBEBS[1:0]; as a timer, it can be set as 00b, which means it is always enabled and continuously perform counting;
- Set the timer/counter overflow value is TBC0[15:0];
- Set the control bit TBRST as <1> to clear the counting register;
- Enable the TMB and the control bit TBEN is set as <1>.

The calculation of the theoretical overflow value of the Timer B:

T = TBC0*1 / TBCLK; TBCLK=HS_CK (or LS_CK) / TMCD; (Equation 10-1)

Then

T=TBC0*TMCD / HS_CK (or LS_CK); (Equation 10-2)

The TMB has four different counting methods, and different counting method have different overflow conditions, which will be specified later.

TMB counting method 0

When register TBM [3:2] =00b, the register control bit TMBR serves as a 16-bit up counter. Under the mode, the TMBR will be automatically added by 1 at each rising edge of the TBCLK; if the counting value of the TMBR is higher than Register control bits TBC0 [15: 0], the TMBR will become 0 at the next rising edge and the timer interrupt flag TBCLK is set as <1>; if the interrupt function of the TMB and the global interrupt function are enabled, the chip will reply the TMB interrupt. Then, the TMBR will restart the up counting. The schematic view of the counting waveform of the mode is as shown in the follow figure. The counting cycle calculation method of the TMB under the mode:
T=TBC0*TMCD / HS_CK (or LS_CK)

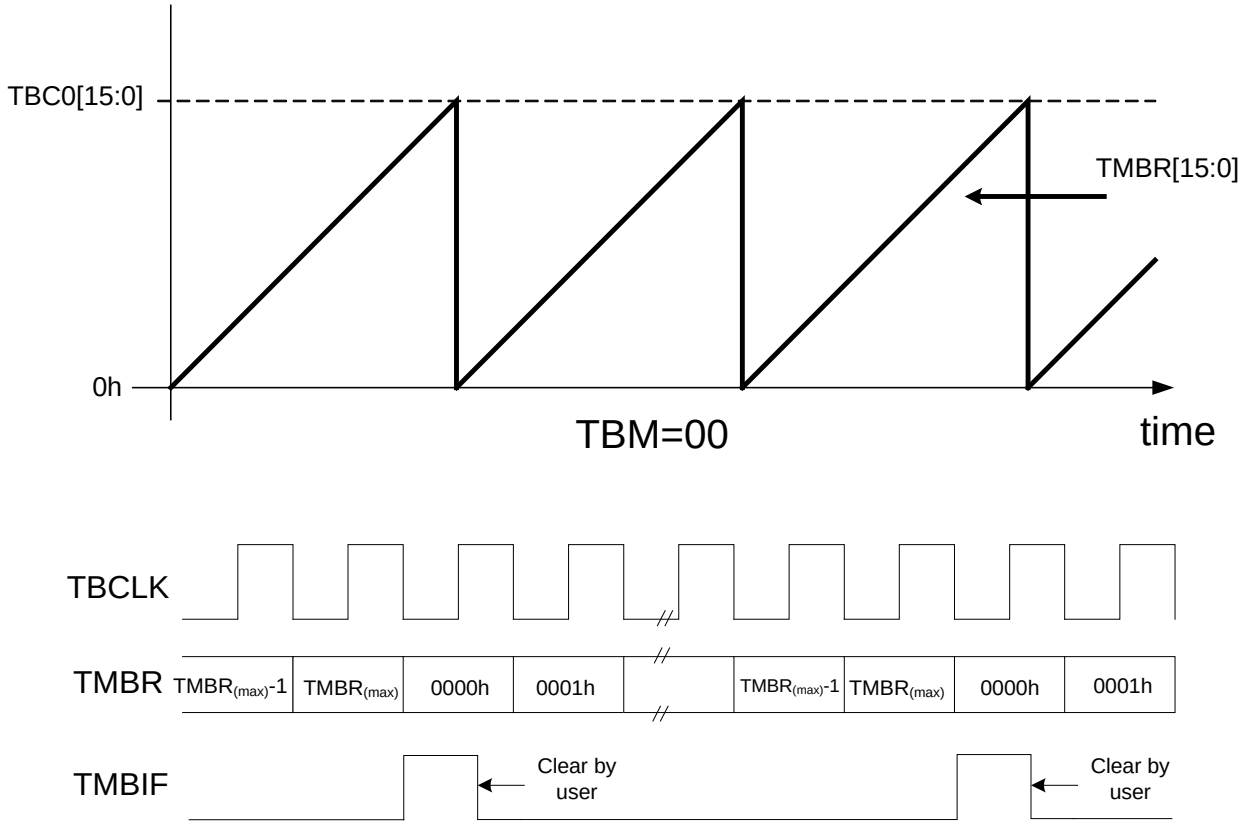


FIG. 10-2 Schematic view of counting waveform of counting method 0

TMB counting method 1

When TBM [3:2] =01b, the TMB will perform incremental counting and then perform decreasing counting; the TMBR is a 16-bit counter. After enabled, the TMB will perform incremental counting, and the TMBR will automatically be added 1 at each rising edge of the TBCLK. When the TMBR is equal to TBC0, the TMBR will be changed to downward mode, but the interrupt flag TMBIF is still 0; at the next rising edge of the TBCLK, the TMBR will be changed to perform decreasing counting; the interrupt request will take place until the TMBR is decreased to 0 and the interrupt flag TMBIF is set as <1>, and then the TMBR will start to perform incremental counting at the next rising edge of the TBCLK. The above process will be kept repeating. The schematic view of the counting waveform of the mode is as shown in the following figure.

In the mode, the calculation method of the counting cycle of the TMB is:

T=2*TBC0*TMCD / HS_CK (or LS_CK)

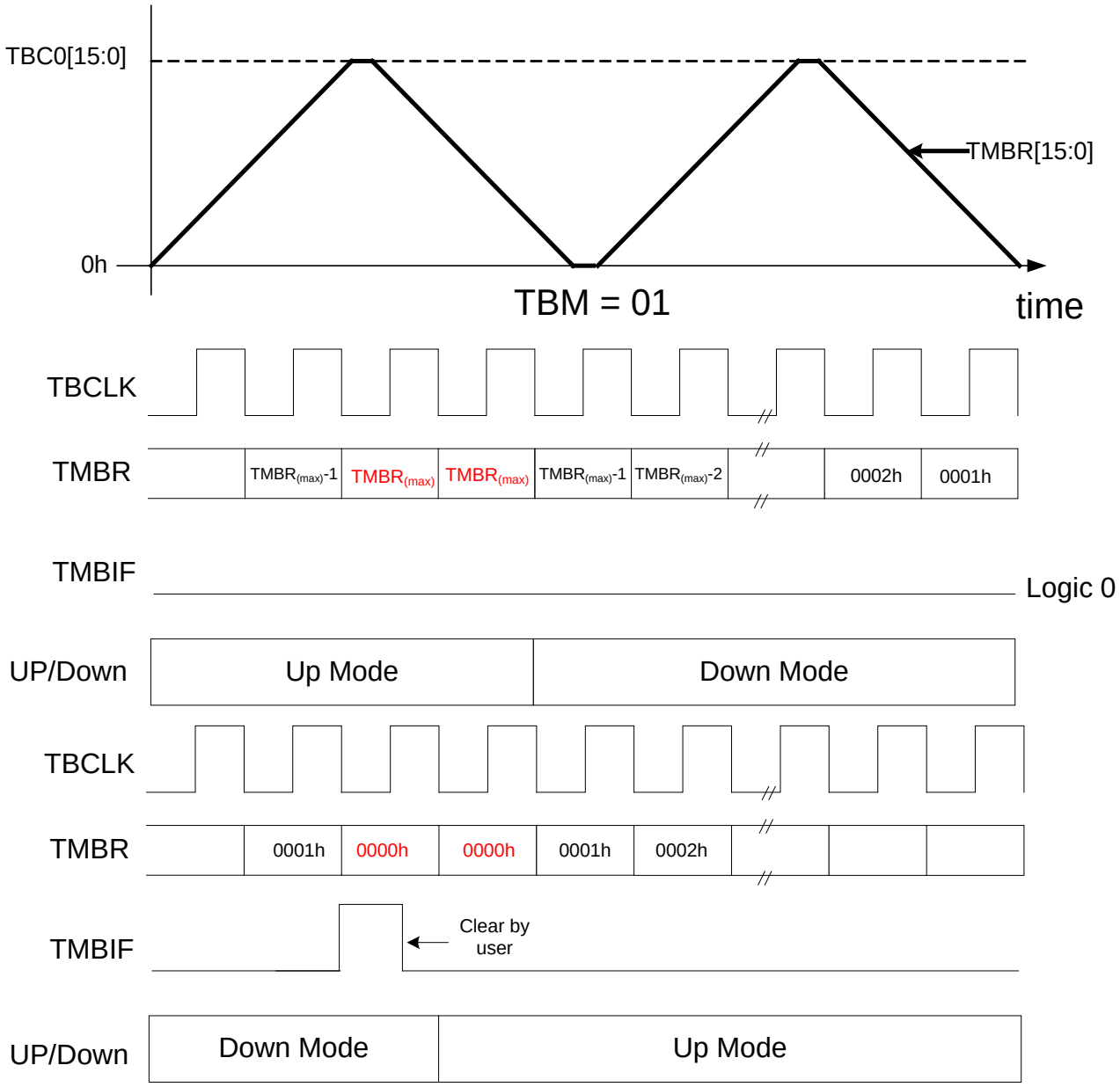


FIG. 10-3 Schematic view of counting waveform of counting method 1

TMB counting method 2

When TBM [3:2] =10b, the TMB will perform incremental counting, but the TMBR is separated into two independent 8-bit counters: TMBR [15:8] and TMBR [7:0]. Besides, the two independent 8-bit counters perform incremental counting at the same time. The overflow value of the TMBR [15:8] is controlled by the TBC0 [15:8] and the overflow value of the TMBR [7:0] is controlled by TBC0 [7:0]. The two counters will be automatically added by 1 at each rising edge of the TBCLK. If the TMBR [15:8] is equal to the TBC0 [15:8], the TMBR [15:8] will become 0 at the next rising edge of the TBCLK but the interrupt flag TMBIF is still 0; if the TMBR [7:0] is equal to TBC0 [7:0], TMBR [7:0] will become 0 at the next rising edge of the TBCLK and the interrupt flag TMBIF will be set as <1>. At this time, if the TMB interrupt function and the global interrupt enable function are enabled, the chip will reply to the TMB interrupt. Under the mode, the interrupt request is controlled by the counter TMBR [7:0]; therefore, during the mode, please pay attention to set the value of the TBC0 [7:0] in order to control the TMB interrupt vector. The schematic view of the counting waveform of the mode is as shown in the following figure.

In the mode, the calculation method of the counting cycle of the interrupt method of the mode is: T=TBC0 [7:0]*TMCD / HS_CK (or LS_CK);

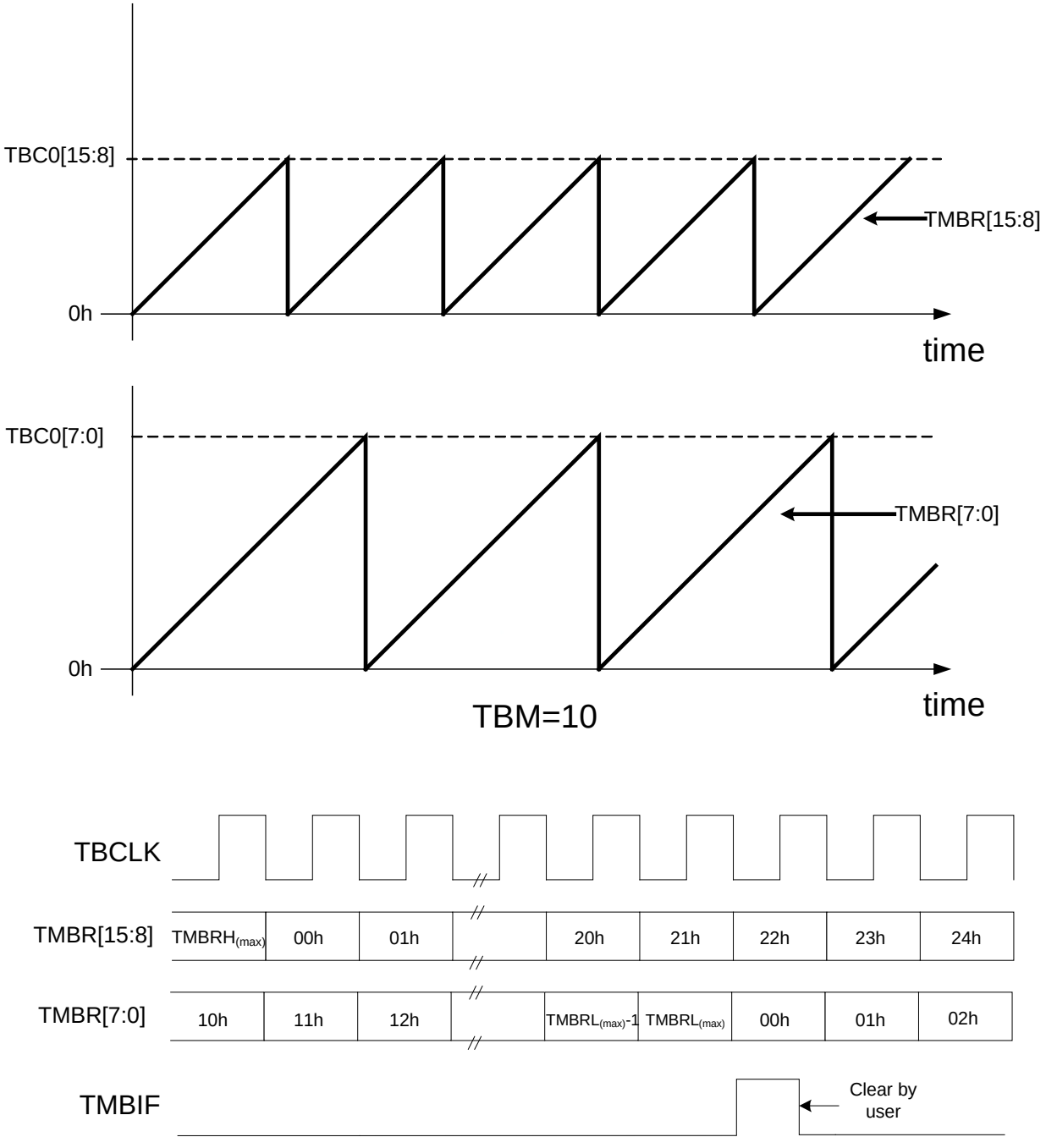


FIG. 10-4 Schematic view of counting waveform of counting method 2

TMB counting method 3

When TBM [3:2] =11b, the TMB will perform incremental counting, and the TMBR is separated into two counters: TMBR [15:8] and TMBR [7:0]; and both of them are under incremental counting mode. The overflow value of the TMBR [7:0] is controlled by the TBC0 [7:0] and the overflow value of the TMBR [7:0] is controlled by TBC0 [7:0]. TMBR [7:0] will be automatically added by 1 at each rising edge of the TBCLK; if the TMBR [7:0] is equal to the TBC0 [7:0], the TMBR will become 0 at the next rising edge of the TBCLK; besides the TMBIF will become 1 and the TMBR [15:8] will be automatically added by 1. At this time, if the TMB interrupt function and the global interrupt enable function are enabled, the chip will reply to the TMB interrupt. The schematic view of the counting waveform of the mode is as shown in the following figure.

In the mode, the calculation method of the counting cycle of the interrupt method of the mode is: T=TBC0 [7:0]*TMCD / HS_CK (or LS_CK);

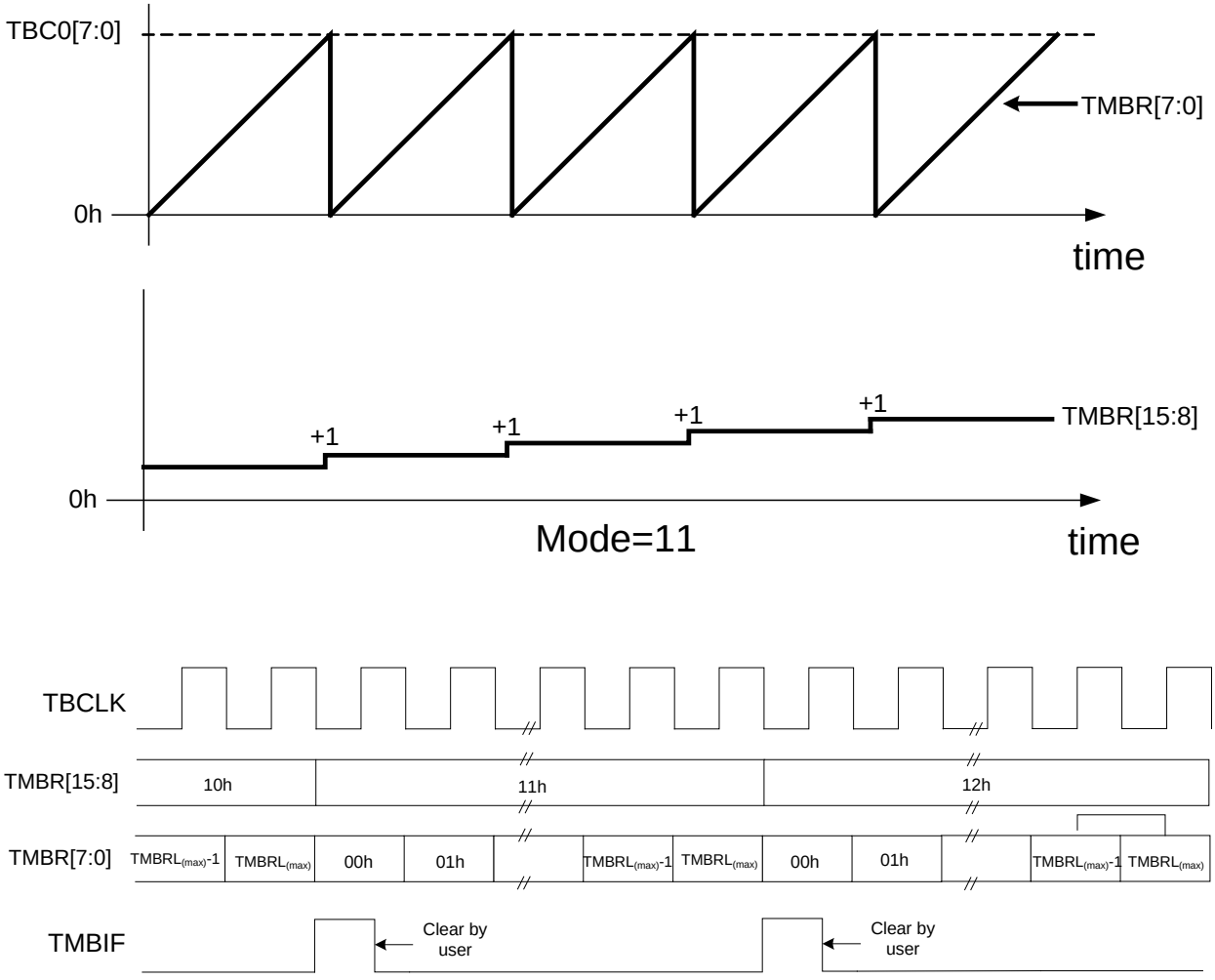


FIG. 10-5 Schematic view of counting waveform of counting method 3

10.1.2. PWM function mode

When the timer B works under the PWM mode, the combinations of the different counting methods and different PWM mode selectors can generate different PWM waveforms. The chip has only two PWMs: PWM0/PWM1, which can be simply considered two PWM waveform generators; the combinations of the different counting methods and different PWM operating modes can generate many kinds of PWM waveforms. The chip provides many output pins for the output of the PWM, and each PWM waveform generator is corresponding to 8 output IO ports; therefore, the usage and output of the PWM is very flexible. However, the TMB is necessary for the function; that is to say, the TMB should be enabled to set the counting cycle of the TMB.

Each of the PWM waveform generators (PWM0/PWM1) has many operating modes: PWMA, PWMB, PWMC, PWMD, PWME, PWMF and PWMG. The operating modes of the PWM0 and PWM1 can be changed by setting the control bits O0MD 0x40C04 [18:16] and 0x40C04 [22:20]. The phase of the output waveform of the PWM can be changed by setting the control bits O1PMR 0x40C04 [23] and O0PMR 0x40C04 [19]. The user can check the current operating mode of the PWM 0x40C08 [21:16] via the PWM operating mode flag register; if the flag is 1, it means the operating mode is enabled. The TBC1 0x40C10 [15:0]/TBC2 0x40C10 [31:16] are the duty cycle controller of the PWM0/PWM1 respectively; the duty cycles of the PWMs can be changed by setting the values of the TBC1/TBC2.

The chip provides 8 output IOs for each PWM, and the corresponding pins are distributed over the PT1/PT2; the selection and enablement of the output pins of the PWM1 and PWM0 are controlled by the controllers PTPW 0x40840[4:2], PTPW1E 0x40840[1] and PTTPW0E 0x40840[0]. The output and disablement of the PWMs can be controlled by the enablement and disablement of the output pins of the PWMs. If the user wants to completely disable the PWMs, it is necessary to disable the output pins of the TMB and the PWMs. The output pins of the PWMs are as shown in Table 10.1.

Serial number PTPW[2:0]	PWM0 Output pins	PWM1 Output pins	Serial number TPW[2:0]	PWM0 Output pins	PWM1 Output pins
000	PT1.0	PT1.1	100	PT2.0	PT2.1
001	PT1.2	PT1.3	101	PT2.2	PT2.3
010	PT1.4	PT1.5	110	PT2.4	PT2.5
011	PT1.6	PT1.7	111	PT2.6	PT2.7

Table 10-1 PWM output pin distribution

PWM initialize operation description:

(1) Select the PWM operating mode and duty cycle, the output waveform phase, that is, set O0MD / O0PMR, O1MD / O1PMR, write the value to TBC1 / TBC2;

(2) Select the PWM output IO port, and the corresponding IO port needs to be set to output mode; control output IO enable and disable, can control the PWM output and shutdown, if you want to completely turn off the PWM, you must turn off the TMB.

(3) Set the working clock frequency of the TMB, set ENTD = 1, TMCD [1: 0];

(4) Select the TMB count mode and trigger the count signal source, set the control bit TBM, TBEBS;

(5) Set the TMB count cycle value, and open the TMB, that is, TBEN = 1, write the value to TBC0;

The waveform of the PWM is generated by the combination of the TMBR, TBC0, TBC1 and TBC0; and there are 6 kinds of operating modes; thus, the operating conditions of the operating modes are different from each other. The 6 operating modes will be respectively specified later. The usage conditions and the controls of the two independent PWMs: PWMO0 and PWMO1; therefore, they will not be specified separately.

PWMA mode

The PWMA mode is a 16-bit PWM; the counting value of the TMBR is compared with the TBC1 and the waveform period of the PWM is controlled by the TBC0.

PWM output state controlled conditions:

PWM = 1, when TMBR [15:0] >= TBC1 [15:0];

PWM = 0, when TMBR [15:0] < TBC1 [15:0];

PWM period:

PWM Period = TMBR[15:0]*TMCD / HS_CK(or LS_CK)；

PWM duty cycle:

PWM Duty= TBC1/(TMBR[15:0]+1)

PWM Duty Cycle=（PWM Duty） *TMCD / HS_CK(or LS_CK)；

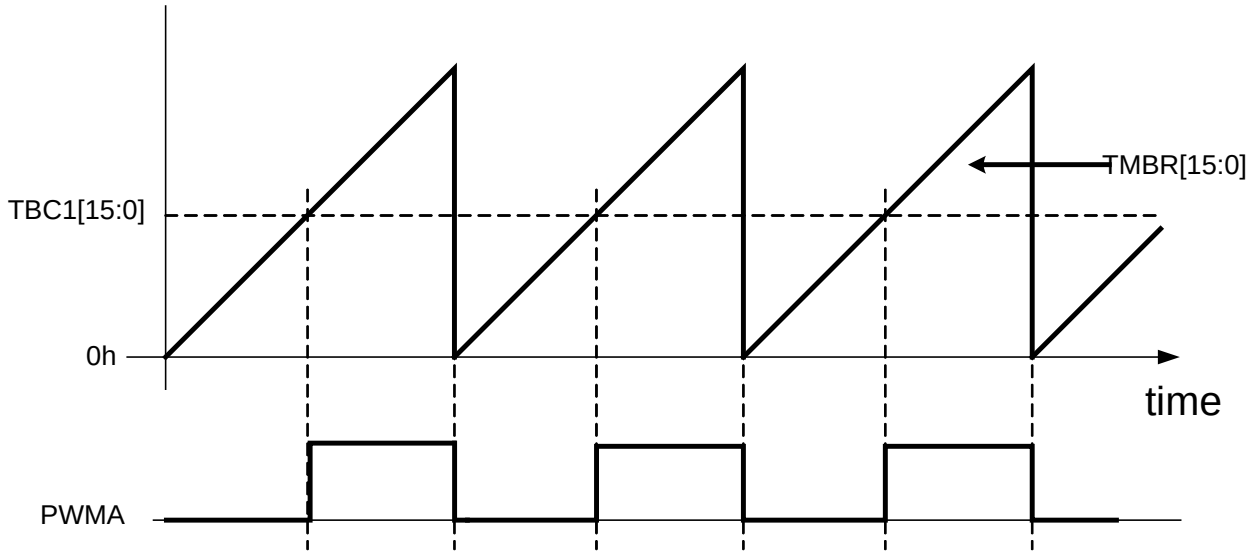


FIG. 10-6 Waveform schematic view and counting waveform schematic view of PWM mode A

PWMB Mode

The PWMB mode is a 16-bit PWM; the counting value of the TMBR is compared with the TBC2 and the waveform period of the PWM is controlled by the TBC0.

PWM output state controlled conditions:

PWM = 1, when TMBR [15:0] >= TBC2 [15:0];

PWM = 0, when TMBR [15:0] < TBC2 [15:0];

PWM period:

PWM Period = TMBR [15:0]*TMCD / HS_CK (or LS_CK);

PWM duty cycle:

PWM Duty= TBC2/ (TMBR [15:0] +1)

PWM Duty Cycle= (PWM Duty) *TMCD / HS_CK (or LS_CK);

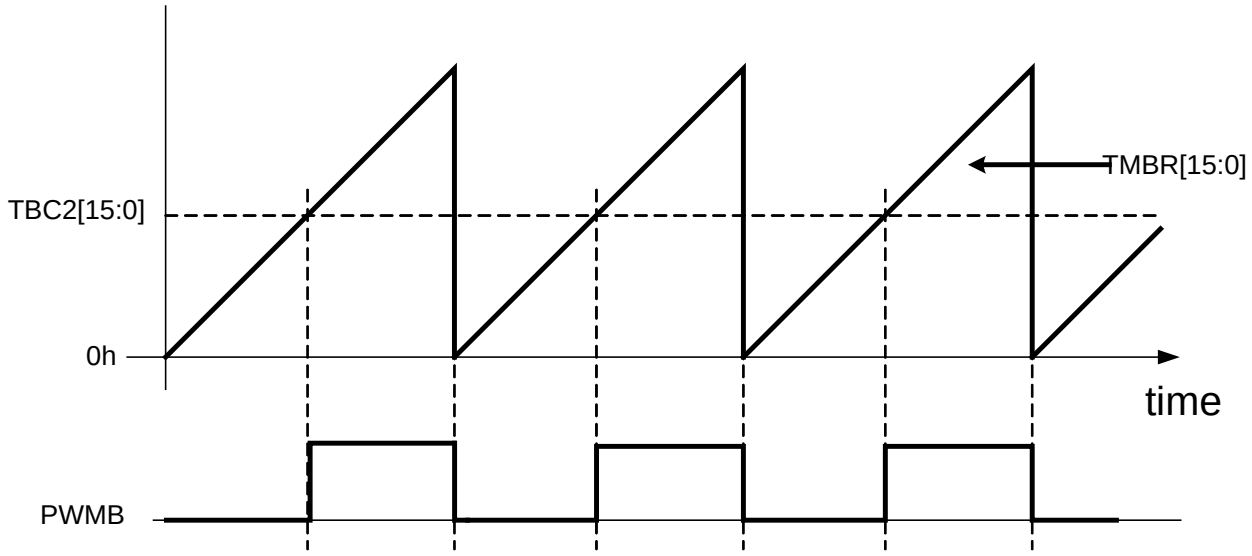


FIG. 10-7 Waveform schematic view and counting waveform schematic view of PWM mode B

PWMC Mode

The PWMC mode is an 8-bit PWM; the counting value of the TMBR is compared with the TBC1 [7:0] and many PWM waveforms appear within the period of the TBC0.
PWM output status control conditions:
PWM = 1, when TMBR [7:0] >= TBC1 [7:0].
PWM = 0, when TMBR [7:0] < TBC1 [7:0].

PWM period:
PWM Period = TMBR [7:0]*TMCD / HS_CK (or LS_CK);

PWM duty cycle:
PWM Duty= TBC1 [7:0]/ (TMBR [7:0] +1)
PWM Duty Cycle= (PWM Duty) *TMCD / HS_CK (or LS_CK);

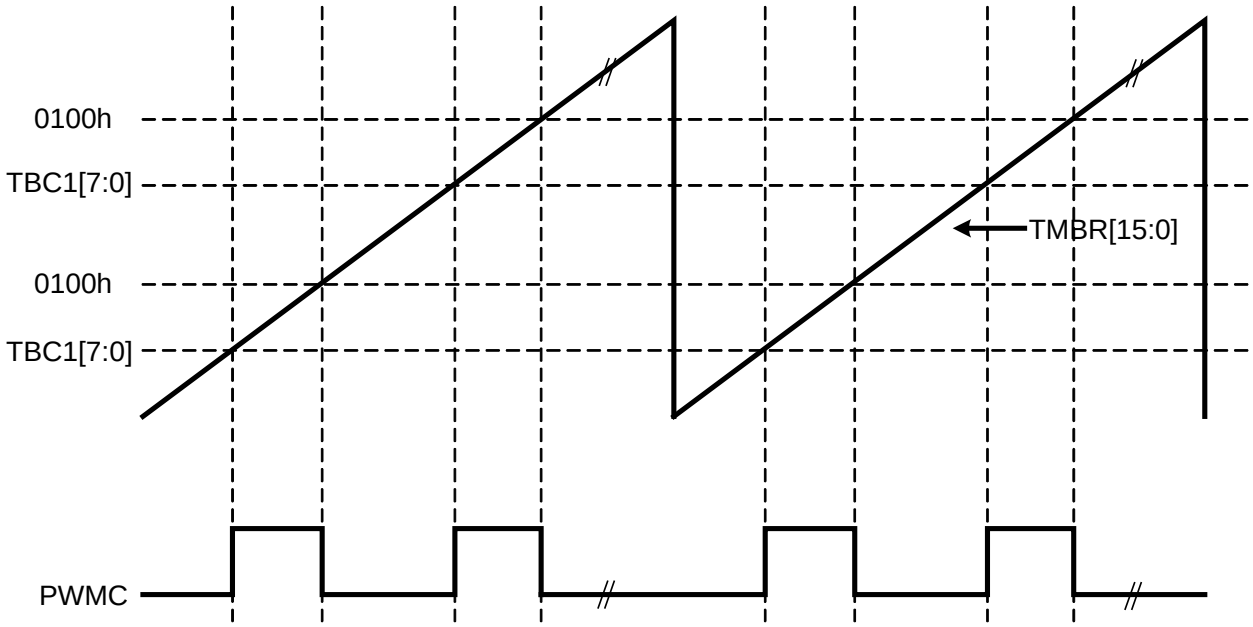


FIG.10-8 Waveform schematic view and counting waveform schematic view of PWM mode C

PWMD Mode

The PWMD mode is an 8-bit PWM; the counting value of the TMBR is compared with the TBC2 [7:0] and many PWM waveforms appear within the period of the TBC0.
PWM output status control conditions:
PWM = 1, when TMBR [15:8] >= TBC2 [7:0];
PWM = 0, when TMBR [15:8] < TBC2 [7:0];

PWM period:
PWM Period = TMBR [15:8]*TMCD / HS_CK (or LS_CK);

PWM duty cycle:
PWM Duty= TBC2 [7:0]/ (TMBR [15:8] +1)
PWM Duty Cycle= (PWM Duty) *TMCD / HS_CK (or LS_CK);

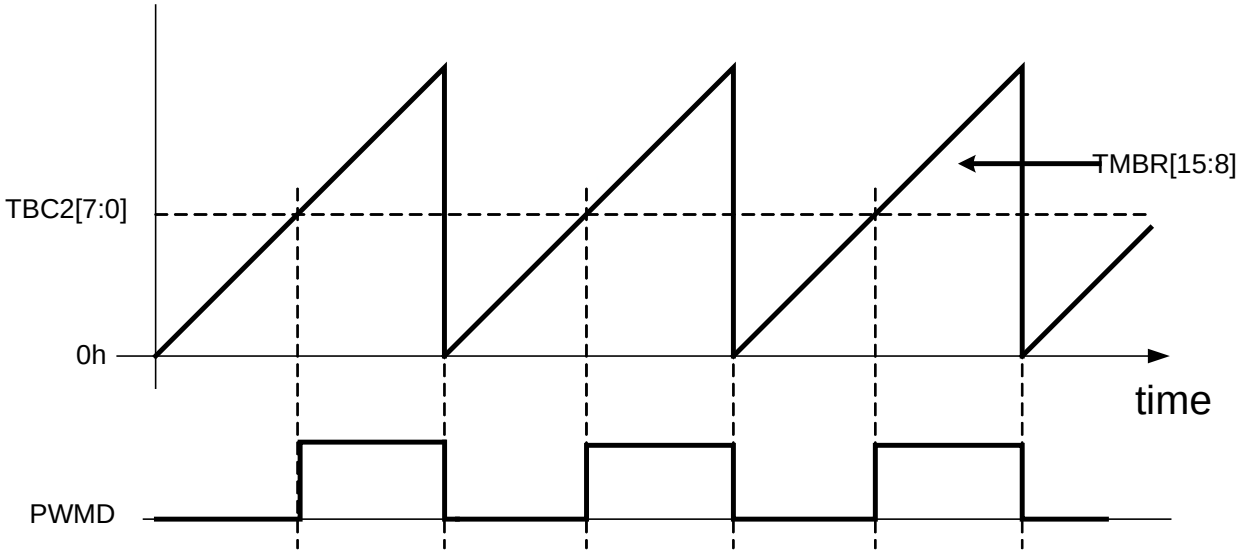


FIG.10-9 Waveform schematic view and counting waveform schematic view of PWM mode D

PWMF Mode

The PWMF is a 16-bit PWM. The counting value of the TMBR is compared with the TBC1 and TBC2, and the TBC2 should be larger than TBC1; the TMBR will keep increasing until overflowing.

PWM output status control conditions:

PWM = 1, when TBC1 [15:0] =< TMBR [15:0] <= TBC2 [15:0];

PWM = 0, when TMBR [15:0] > TBC2 [15:0] or TMBR [15:0] <= TBC1 [15:0];

PWM=1; the time is: t = clock × (TBC2 – TBC1);

PWM period:

PWM Period = TMBR [15:0]*TMCD / HS_CK (or LS_CK);

PWM duty cycle:

PWM Duty= (TBC2-TBC1)/ (TMBR [15:0] +1)

PWM Duty Cycle= (PWM Duty) *TMCD / HS_CK (or LS_CK);

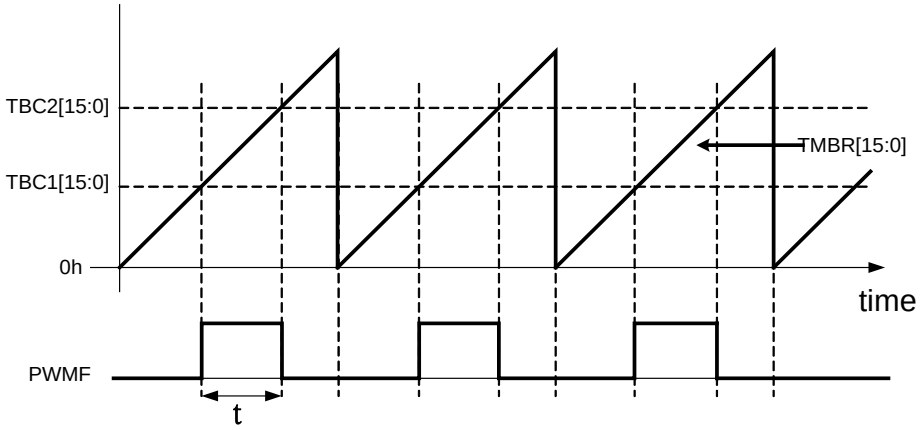


FIG.10-10 Waveform schematic view and counting waveform schematic view of PWM mode F

PWMG Mode

The PWMG is a 16-bit PWM mode and the duty cycle of the output waveform is 50%, which is the PFD waveform. The counting value of the TMBR is not compared with the TBC1/TBC2, and the period of the output waveform is related to the TBC0.

PWM period:

PWM Period = TBC0 [15:0]*TMCD / HS_CK (or LS_CK);

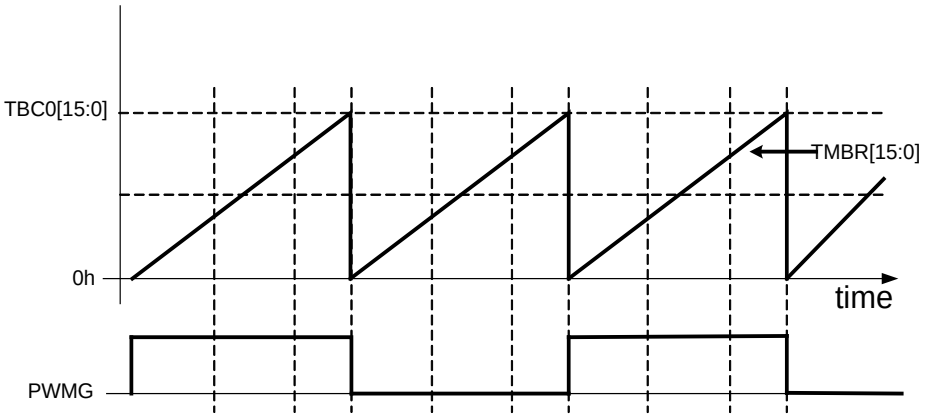


FIG.10-11 Waveform schematic view and counting waveform schematic view of PWM mode G

10.2. Register Address

TMR Register Address	31 24	23 16	15 8	7 0
TMR base address + 0x00(0X40C04)	MASK1	REG1	MASK0	REG0
TMR base address + 0x08 (0X40C08)	-	REG2	TBCR	TBCR
TMR base address + 0x0C (0X40C0C)	-	-	TBC0	TBC0
TMR base address + 0x10 (0X40C10)	TBC2	TBC2	TBC1	TBC1

-Reserved

10.3. Register Functions

10.3.1. TMB Register0

TMA Base Address + 0X04 (0X40C04)						
Symbol	TMBCR0(TMB Control Register 0)					
Bit	[31:24]	[23]	[22:20]		[19]	[18:16]
Name	MASK	O1PMR	O1MD		O0PMR	O0MD
RW	R0W-0	RW-0				
Bit	[15:8]	[7:6]	[5]	[4]	[3:2]	[1:0]
Name	MASK	-	TBEN	TBRST	TBM	TBEBS
RW	R0W-0	-	RW-0			

Bit	Name	Description	
Bit[23]	O1PMR	PWM1:The output of the inverting control	
		0	Inverting output
		1	No inverting output
Bit[21-20]	O1MD	PWM1 Output mode	
		0	PWMA
		1	PWMB
		2	PWMC
		3	PWMD
		4	RSV
		5	PWMF
		6	PWMG
		7	PWMG
Bit[19]	O0PMR	PWM0: The output of the inverting control	
		0	Inverting output
		1	No inverting output
Bit[18-16]	O0MD	PWM0 Output mode	
		0	PWMA
		1	PWMB
		2	PWMC
		3	PWMD
		4	RSV
		5	PWMF
		6	PWMG
		7	PWMG

Bit	Name	Description	
Bit[5]	TBEN	Timer B Enable control	
		0	Disable
		1	Enable
Bit[4]	TBRST	Timer B Reset	
		0	Normal
		1	Clear TBR Auto back to 0
Bit[3~2]	TBM	Timer B counting mode selection	
		00	16-bit saw tooth _ count _ up to a maximum of TBC0
		01	16-bit_triangular wave_up_count _down _count range from 0 to TBC0
		10	2 Groups_ Independent 8Bit _ saw tooth _ counting up, respectively TBC0 Bit 15-8 Bit 7-0 with a maximum
		11	A group of 8-Bit_ saw tooth _ count _ up to a maximum of TBC0 Bit 7-0, A group count before an 8-Bit saw tooth Overflow
Bit[1~0]	TBEBS	Timer B Enable signal	
		00	1 (logic high)(Always enable)

		01	CMPO(High from Comparator)
		10	OPOD(High from Rail-to-Rail OPAMP)
		11	CPI1(CPI1 High from Timer C)

10.3.2. TMB Register1

TMR Base Address + 0X08 (0X40C08)							
Symbol	TMBCR1(TMB Control Register 1)						
Bit	[31:22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	-	PWMFF	-	PWMDF	PWMCF	PWMBF	PWMAF
RW	-	R-X	-	R-X			
Bit	[15:0]						
Name	TMBC						
RW	R-X						

Bit	Name	Description	
Bit[23-16]	PWM Flag	PWM A/B/C/D/F Flag	
		0	Normal
		1	Flag
Bit[15-0]	TMBC	Timer B 16-bit Counter	

10.3.3. TMB Register2

TMR Base Address + 0X08 (0X40C0C)	
Symbol	TMBCOD(TMB Counter overflow condition Register)
Bit	[31:16]
Name	-
RW	-
Bit	[15:0]
Name	TBC0:Timer B Overflow Condition
RW	RW-0XFFFF

Bit	Name	Description
Bit[15-0]	TBC0	Timer B Overflow Condition

10.3.4. TMB Register3

TMR Base Address + 0X08 (0X40C10)																
Symbol	TMB3(TMB Control Register 3)															
Bit	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	TBC2: PWM Condition 2															
RW	RW-0XFFFF															
Bit	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	TBC1: PWM Condition 1															
RW	RW-0XFFFF															

Bit	Name	Description
Bit[31-16]	TBC2	PWM Condition 2
Bit[15-0]	TBC1	PWM Condition1

11. Timer C Management

11.1. Introduction

The timer C is designed to execute the capture function, which can be used to perform frequency measurement, event counting, interval time measurement, etc. It can generate the interrupt signal when the counter overflow takes place; and it should be used together with the TMB counter register.

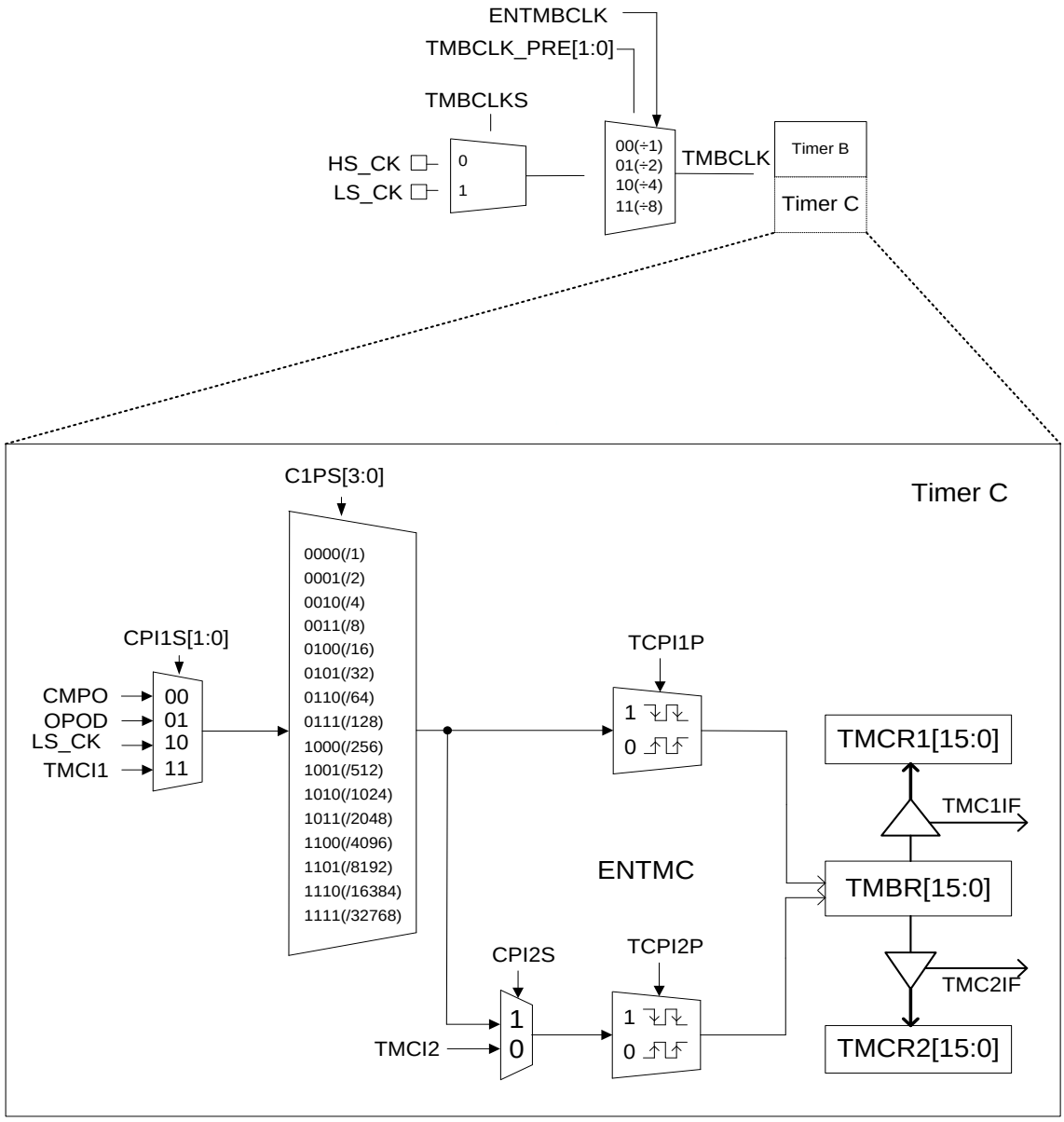


Fig. 11-1 TMC function block diagram

TMC clock source selection

The clock source of the TMC is equal to that of the TMB; all of them are generate by make the HS_CK or LS_CK pass the frequency divider to generate the clock source TMBCLK. The capture function of the TMC can be enabled or disabled by setting the control bit TCEN [0].

TMC capture counting value

The capture counting value of the TMC is finished by the counter register's control bit TMBR 0x40C08 [15:0] of the TMB. When Timer B start TMBR began counting, after CPI1P trigger occurs, the value of TMBR placed TCR0 and interruption (TMC0IF), after CPI2P trigger occurs, the value of TMBR placed TCR1 and interruption (TMC1IF).

Capture comparator 1

The capture comparator 1 has four capture signal input sources, and the input signal source can be set by setting the selector CPI1S 0x40C14[21:20]; and the input signal should further pass the frequency divider CP1PS 0x40C14[19:16]; the frequency divider can perform the frequency dividing on the input signal to slow the input signal; in this way, the input signals with high frequency can be measured. The setting of the controller CPI1P 0x40C14[1] can determine the trigger edge of the capture signal is the rising edge or the falling edge. After the capture event is finished, the interrupt signal can be generated and the interrupt flag TMC0IF 0x40004[2] is set as <1>.

The capture signal input source of the capture comparator 1:

Input signal source symbol	Function description
CMPO	The output status of the comparator
OPOD	The output status of the OP amplifier
LS_CK	Chip low-speed frequency source
TCI1	Input from the IO

The input of the capture comparator 1(When the control bit CPI1S 0x40C14 [21:20] = 11b time):

Serial number	TCI1	TCI2	Serial number	TCI1	TCI2
000	PT1.0	PT1.1	100	PT2.0	PT2.1
001	PT1.2	PT1.3	101	PT2.2	PT2.3
010	PT1.4	PT1.5	110	PT2.4	PT2.5
011	PT1.6	PT1.7	111	PT2.6	PT2.7

Initial Operation of capture comparator 1:

(1)Select the operating clock source TMBCLK of the TMC;

(2)Set the capture signal input source and the input signal source frequency dividing value, which is to set the values of the CPI1S[1:0] and CP1PS [3:0];

(3)Set the capture signal trigger edge, which is to set the value of the CPI1P;

(4)If the TCI1 is selected to be the capture signal input source, it is necessary to set the input IO to select the corresponding IO as the input mode;

(5)If the interrupt function is used, it is necessary to enable TMC0IE 0x40004[18]=<1> and enable the global interrupt function GIE=<1>;

(6)Enable the TMC and enable the TCEN 0x40C14 [0]=<1>.

Capture comparator 2

The capture comparator 2 has 2 capture signal input sources, and the input signal source can be set by setting the selector CPSS 0x40C14 [22]; and the input signal does not have to pass the frequency divider. The setting of the controller CPI2P 0x40C14 [2] can determine the trigger edge of the capture signal is the rising edge or the falling edge. After the capture event is finished, the interrupt signal can be generated and the interrupt flag TMC1IF 0x40004[3].

The capture signal input of the capture comparator 2 is:

Input from IO port;

It is consistent with the input source of the capture comparator 1;

Initial Operation of the capture comparator 2:

(1)Select the operating clock source TMBCLK of the TMC;

(2)Set the capture signal input source, which is to set the values of the CPSS 0x40C14[22];

(3)Set the capture signal trigger edge, which is to set the value of the CPI2P 0x40C14[2];

(4)If the TCI2 is selected to be the capture signal input source, it is necessary to set the input IO to select the corresponding IO as the input mode;

(5)If the interrupt function is used, it is necessary to enable TMC1IE 0x40004 [19] =<1> and enable the global interrupt function GIE=<1>;

(6)Enable the TMC and enable the TCEN 0x40C14 [0] =<1>.

11.2. Register Address

TMR Register Address	31	24	23	16	15	8	7	0
TMR base address + 0x14(0X40C14)	MASK1		REG1		MASK0		REG0	
TMR base address + 0x18 (0X40C18)	TCR2		TCR2		TCR1		TCR1	

11.3. Register Functions

11.3.1. TMC Register0

TMR Base Address + 0X14 (0X40C14)							
Symbol	TMCCR0(TMC Control Register 0)						
Bit	[31:24]	[23]	[22]	[21:20]	[19:16]		
Name	MASK	-	CPSS	CPI1S	CP1PS		
RW	R0W-0	-	RW-0	RW-0	RW-0		
Bit	[15:08]	[7:3]			[2]	[1]	[0]
Name	MASK	-			TCPI2P	TCPI1P	TCEN
RW	R0W-0	-			RW-0		

Bit	Name	Description	
Bit[22]	CPI2S	Capture 1 input source selection	
		0	TC2 from I/O port
		1	The same as capture 1 input
Bit[21~20]	CPI1S	Capture 0 input source selection	
		00	CMPO (comparator output)
		01	OPOD (rail-to-rail OPAMP digital output)
		10	Low speed clock source
		11	TC1 from I/O port
Bit[19~16]	C1PS	C1PSM bit control C1PS bit write enable	
		0000	CPI1 frequency/1
		0001	CPI1 frequency/2
		0010	CPI1 frequency/4
		0011	CPI1 frequency/8
		0100	CPI1 frequency/16
		0101	CPI1 frequency/32
		0110	CPI1 frequency/64
		0111	CPI1 frequency/128
		1000	CPI1 frequency/256
		1001	CPI1 frequency/512
		1010	CPI1 frequency/1024
		1011	CPI1 frequency/2048
		1100	CPI1 frequency/4096
		1101	CPI1 frequency/8192
		1110	CPI1 frequency/16384
		1111	CPI1 frequency/32768
Bit[02]	TCPI2P	Capture2 Trigger Edge Selection	
		0	Positive Trigger Edge Selection
		1	Negative Trigger Edge Selection
Bit[01]	TCP1P	Capture1 Trigger Edge Selection	
		0	Positive
		1	Negative
Bit[00]	TCEN	Timer C enable control	
		0	Disable (do not clear TCR0 and TCR1)
		1	Enable

11.3.2. TMC Register1

TMR Base Address + 0X18 (0X40C18)	
Symbol	TMCCR1(TMC Control Register 1)
Bit	[31:16]
名稱	TCR2
RW	R-X
Bit	[15:00]
名稱	TCR1
RW	R-X

Bit	Name	Description
Bit[31-16]	TCR2	Timer C Channel 2 Interception Results
Bit[15-00]	TCR1	Timer C Channel 1 Interception Results

12. GPIO PT1 Management

12.1. Introduction

The PT1 has 8 IO pins, which can be used as the common universal IO ports, and can also be reused as the input or output IO ports of the capture comparator, SPI, IIC, UART comparator, PWM and external interrupt modules, etc. Different reuses need different configurations.

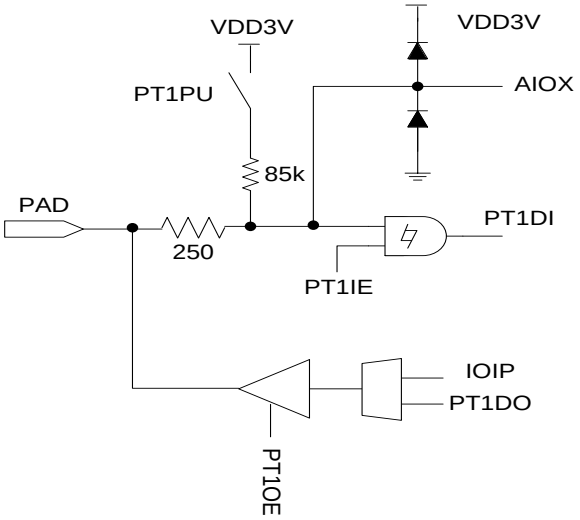


FIG. 12-1 PT1 function block diagram

PT1 has the functions of the input, output, internal pull-up resistors and the external interrupt input port; and different functions should be set by different controllers.

Internal pull-up resistor

The controller PT1PU 0x40800[23:16] can enable or disable the internal pull-up resistor of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit of the IO port is set as <1>, the internal pull-up resistor will be enabled; if it is set as <0>, the internal pull-up resistor will be disabled. If the IO port is under the input mode and there is no external pull-up resistor, the internal pull-up resistor should be enabled, especially in low power consumption mode, which can prevent from electric leakage and increase the power consumption. If it serves as the analog signal input port, it is not necessary to enable the internal pull-up resistor.

Output mode

The controller PT1OE 0x40800 [7:0] can enable or disable the output mode of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit of the IO port is set as <1>, the output mode of the corresponding IO port will be enabled; if it is set

as <0>, the output mode of the corresponding IO port will be disabled. The control bit PT1DO 0x40804 [7:0] can determine whether the output status of the pin of the corresponding IO port is 1 or 0. Under the low-power mode, if the IO should enable the output mode, the output status can be set according to the peripheral circuit to decrease the power consumption of the chip. During the mode, the internal pull-up resistor of the IO cannot be enabled, and the input mode and the output mode cannot be enabled at the same time; therefore, when the output mode is enabled, the input mode of the IO port should be disabled.

Input mode

The controller PT1IE 0x40804[23:16] can enable or disable the input mode of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit of the IO port is set as <1>, the input mode of the corresponding IO port will be enabled; if it is set as <0>, the input mode of the corresponding IO port will be disabled. The control bit PT1DI 0x40808 can determine whether the input status of the pin of the corresponding IO port is 1 or 0. If the IO is set as the input mode and the chip is not connected to the external pull-up resistor, the internal pull-up resistor should be enabled; the IO pin is not allowed to be floating in order to prevent from the electric leakage of the chip. Especially in the low-power mode, it is suggested the IO pin should be set as the input mode. If it serves as the analog signal input port, it is not necessary to set the corresponding IO pin as the input mode. The output mode of the IO pin should be disabled before its input mode is enabled.

External interrupt input

The PT1 has 8 IO pins, and all of them can be reused as external interrupt input pins. The mode should set the IO port to be the input mode and enable the internal pull-up resistor. It is necessary to set the external interrupt trigger edge by the controller PT1#ITT 0x4080C[23:00] and enable the control bit PT1ITD[0] to enable the interrupt trigger edge. The controller PT1IDF 0x4080C[31:24] can enable the interrupt response function of the corresponding IO pin INTPT1 0x40010; when the external interrupt signal generates, the interrupt flag of the corresponding IO pin is set as 1. When the global interrupt GIE and the IO external interrupt function are enabled, the chip will stop the current program right away and execute the IO external interrupt program.

12.2. Register Address

GPIO Register Address	31 24	23 16	15 8	7 0
GPIO base address + 0x00(0X40800)	MASK1	PT1PU	MASK0	PT1OE
GPIO base address + 0x04 (0X40804)	MASK3	PT1IE	MASK2	PT1DO
GPIO base address + 0x08(0X40808)	-	-	-	PT1DI
GPIO base address + 0x0C (0X4080C)	PT1ITD	PT1ITT	PT1ITT	PT1ITT

-Reserved

12.3. Register Functions

12.3.1. PT1 Register0

GPIO Base Address + 0X00 (0X40800)									
Symbol	PT1CR0 (PT1 Control Register 0)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	PT1PU7	PT1PU6	PT1PU5	PT1PU4	PT1PU3	PT1PU2	PT1PU1	PT1PU0
RW	R0W-0	RW-0							
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	PT1OE7	PT1OE6	PT1OE5	PT1OE4	PT1OE3	PT1OE2	PT1OE1	PT1OE0
RW	R0W-0	RW-0							

Bit	Name	Description	
Bit[23~16]	PT1PU	Port 1 pull up control	
		0	Disable internal pull up
		1	Enable internal pull up
Bit[7~0]	PT1OE	Port 1 PAD output enable	
		0	Disable
		1	Enable

12.3.2. PT1 Register1

GPIO Base Address + 0X04 (0X40804)									
Symbol	PT1CR1 (PT1 Control Register 1)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	PT1IE7	PT1IE6	PT1IE5	PT1IE4	PT1IE3	PT1IE2	PT1IE1	PT1IE0
RW	R0W-0	RW-0							
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	PT1DO7	PT1DO6	PT1DO5	PT1DO4	PT1DO3	PT1DO2	PT1DO1	PT1DO0
RW	R0W-0	RW-0							

Bit	Name	Description	
Bit[23~16]	PT1IE	Port 1 PAD input enable	
		0	Disable
		1	Enable
Bit[7~0]	PT1DO	Port 1 PAD output Data	
		0	Set 0
		1	Set 1

12.3.3. PT1 Register2

GPIO Base Address + 0X08 (0X40808)									
Symbol	PT1CR2(PT1 Control Register 2)								
Bit	[31:16]								
Name	-								
RW	-								
Bit	[15:8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	-	PT1DI7	PT1DI6	PT1DI5	PT1DI4	PT1DI3	PT1DI2	PT1DI1	PT1DI0
RW	-	R-0							

Bit	Name	Description	
Bit[7~0]	PT1DI	It is an input signal form PAD	
		0	Pad input is Low
		1	Pad input is High

12.3.4. PT1 Register3

GPIO Base Address + 0X0C (0X4080C)						
Symbol	PT1CR3 (PT1 Control Register 3)					
Bit	[31:24]	[23:21]	[21:18]	[17:16]		
Name	PT17IDF~ PT10IDF	PT17ITT	PT16ITT	PT15ITT		
RW	R-0	RW-0				
Bit	[15]	[14:12]	[11:9]	[8:6]	[5:3]	[2:0]
Name	PT15ITT	PT14ITT	PT13ITT	PT12ITT	PT11ITT	PT10ITT
RW	RW-0					

Bit	Name	Description	
Bit[31]	PT17IDF	PT1.7 Interrupt condition flag For example: check this flag before entering the Sleep Mode: When Bit = 1b, can be PT1.7 pin wake up MCU. When Bit = 0b, PT1.7 pin cannot be awakened MCU.	
		When PT17ITT=0	Always 0. Explanation : When PT17ITT set to 000, the Bit [31] = 0b
		When PT17ITT=1	Inverse DI. Explanation : Before entering Sleep Mode, if PT1.7 status is Low, the Bit [31] = 1b
		When PT17ITT=2	Same as DI. Explanation: Before entering Sleep Mode, if PT1.7 status is High, the Bit [31] = 1b
		When PT17ITT=3	Same as S1. Explanation: When PT1.7 Potential change, which produce an interrupt is triggered
		When PT17ITT=4	Same as DI. Explanation: Before entering Sleep Mode, if PT1.7 status is High, the Bit [31] = 1b
		When PT17ITT=5	Inverse DI. Explanation: Before entering Sleep Mode, if PT1.7 status is Low, the Bit [31] = 1b

		When PT17ITT=6	Same as DI. Explanation: Before entering Sleep Mode, if PT1.7 status is High, the Bit [31] = 1b
		When PT17ITT=7	Inverse DI. Explanation: Before entering Sleep Mode, if PT1.7 status is Low, the Bit [31] = 1b

Bit[30~24]	PT1NIDF	PT1.N Interrupt condition flag (N represent 6~0)	
		When PT1NITT=0	Always 0
		When PT1NITT=1	Inverse DI
		When PT1NITT=2	Same as DI
		When PT1NITT=3	Same as S1
		When PT1NITT=4	Same as DI
		When PT1NITT=5	Inverse DI
		When PT1NITT=6	Same as DI
		When PT1NITT=7	Inverse DI

Bit	Name	Description			
Bit[23~0]	PT1#ITT	Port 1.# select the interrupt trigger method (# represent 7~0)			
		000	Disable the GPIO interrupt trigger to not reply to the interrupt.		
		001	Rising edge trigger	101	High potential trigger
		010	Falling edge trigger	110	Low potential trigger
		011	Potential change trigger	111	High potential trigger
		100	Low potential trigger		

13. GPIO PT2 Management

13.1. Introduction

The PT2 has 8 IO pins, and can be used as common universal IO ports or reused as the input or output IO ports of many function modules, such as capture comparator, SPI, IIC, PWM, external crystal oscillator and external interrupt input, etc. Different reuses need different configurations.

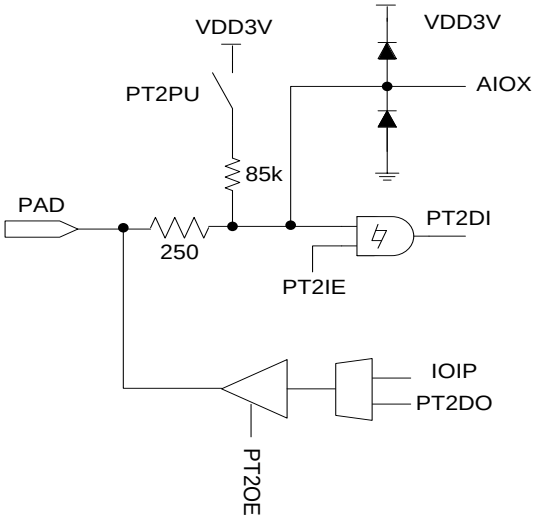


FIG. 13-1 PT2 function block diagram

The PT2 has the functions of the input, output, internal pull-up resistor and external interrupt input port; and different functions need to be set by different controllers.

Internal pull-up resistor

The controller PT2PU 0x40810[23:16] can enable or disable the internal pull-up resistor of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit of the IO port is set as <1>, the internal pull-up resistor will be enabled; if the corresponding bit of the IO port is set as <0>, the internal pull-up resistor will be disabled. If the IO port is under the input mode and there is no external pull-up resistor, the internal pull-up resistor should be enabled, especially in low power consumption mode, which can prevent from electric leakage and increase the power consumption. If it serves as the analog signal input port, it is not necessary to enable the internal pull-up resistor.
PS: When PT2.4~PT2.7 serves as the external crystal oscillator input pins, the internal pull-up resistor cannot be enabled, or the crystal oscillator cannot work normally.

Output mode

The controller PT2OE 0x40810 can enable or disable the output mode of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit of the IO port is set as <1>, the output mode of the corresponding IO port will be enabled; if it is set as <0>, the output mode of the corresponding IO port will be disabled. The control bit PT2DO0x40814 can determine whether the output status of the pin of the corresponding IO port is 1 or 0. Under the low-power mode, if the IO should enable the output mode, the output status can be set according to the peripheral circuit to decrease the power consumption of the chip. During the mode, the internal pull-up resistor of the IO cannot be enabled, and the input mode and the output mode cannot be enabled at the same time; therefore, when the output mode is enabled, the input mode of the IO port should be disabled.

PS: When the PT2.4~PT2.7 serves as the external crystal oscillator input pins, the output mode should be disabled.

Input mode

The controller PT2IE 0x40814[23:16] can enable or disable the input mode of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit controller is set as <1>, the input mode of the corresponding IO port will be enabled; if it is set as <0>, the input mode of the corresponding IO port will be disabled. Whether the current input mode of the corresponding IO pin is 0 or 1 can be read via the controller PT2DI0x40818. If the IO is set as the input mode and the chip is not connected to the external pull-up resistor, the internal pull-up resistor should be enabled; the IO pin is not allowed to be floating in order to prevent from the electric leakage of the chip. Especially in the low-power mode, it is suggested the IO pin should be set as the input mode. If it serves as the analog signal input port, it is not necessary to set the corresponding IO pin as the input mode. The output mode of the IO pin should be disabled before its input mode is enabled.

External interrupt input

The PT2 has 8 IO pins, and all of them can be reused as external interrupt input pins. The mode should set the IO port to be the input mode and enable the internal pull-up resistor. It is necessary to set the external interrupt trigger edge by the controller PT2#ITT 0x4081C [23:00] and enable the control bit PT2IDF 0x4081C [31:24] to enable the interrupt trigger edge. The controller INTPT2 0x40014can enable the interrupt response function of the corresponding IO pin; when the external interrupt signal generates, the interrupt flag of the corresponding IO pin is set as 1. When the global interrupt GIE and the IO external interrupt function are enabled, the chip will stop the current program right away and execute the IO external interrupt program.

13.2. Register Address

GPIO Register Address	31	24	23	16	15	8	7	0
GPIO base address + 0x00(0X40810)	MASK1		PT2PU		MASK0		PT2OE	
GPIO base address + 0x04 (0X40814)	MASK3		PT2IE		MASK2		PT2DO	
GPIO base address + 0x08(0X40818)	-		-		-		PT2DI	
GPIO base address + 0x0C (0X4081C)	PT2ITD		PT2ITT		PT2ITT		PT2ITT	

-Reserved

13.3. Register Functions

13.3.1. PT2 Register0

GPIO Base Address + 0X10 (0X40810)									
Symbol	PT2CR0 (PT2 Control Register 0)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	PT2PU7	PT2PU6	PT2PU5	PT2PU4	PT2PU3	PT2PU2	PT2PU1	PT2PU0
RW	R0W-0	RW-0							
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	PT2OE7	PT2OE6	PT2OE5	PT2OE4	PT2OE3	PT2OE2	PT2OE1	PT2OE0
RW	R0W-0	RW-0							

Bit	Name	Description	
Bit[23~16]	PT2PU	Port 2 pull up control	
		0	Disable pull up
		1	Enable pull up internally
Bit[7~0]	PT2OE	Port 2 PAD output enable	
		0	Disable
		1	Enable

13.3.2. PT2 Register1

GPIO Base Address + 0X14 (0X40814)									
Symbol	PT2CR1 (PT2 Control Register 1)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	PT2IE7	PT2IE6	PT2IE5	PT2IE4	PT2IE3	PT2IE2	PT2IE1	PT2IE0
RW	R0W-0	RW-0							
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	PT2DO7	PT2DO6	PT2DO5	PT2DO4	PT2DO3	PT2DO2	PT2DO1	PT2DO0
RW	R0W-0	RW-0							

Bit	Name	Description	
Bit[23~16]	PT2IE	Port 2 PAD input enable	
		0	Disable
		1	Enable
Bit[7~0]	PT2DO	Port 2 PAD output Data	
		0	Set 0
		1	Set 1

13.3.3. PT2 Register2

GPIO Base Address + 0X18 (0X40818)									
Symbol	PT2CR2 (PT2 Control Register 2)								
Bit	[31:16]								
Name	-								
RW	-								
Bit	[15:8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	-	PT2DI[7]	PT2DI[6]	PT2DI[5]	PT2DI[4]	PT2DI[3]	PT2DI[2]	PT2DI[1]	PT2DI[0]
RW	-	R-0							

Bit	Name	Description	
Bit[7~0]	PT2DI	It is an input signal form PAD	
		0	Pad input is Low
		1	Pad input is High

13.3.4. PT2 Register3

GPIO Base Address + 0x1C (0x4081C)						
Symbol	PT2CR3 (PT2 Control Register 3)					
Bit	[31:24]		[23:21]	[21:18]	[17:16]	
Name	PT2IDF		PT27ITT	PT26ITT	PT25ITT	
RW	RW-0					
Bit	[15]	[14:12]	[11:9]	[8:6]	[5:3]	[2:0]
Name	PT25ITT	PT24ITT	PT23ITT	PT22ITT	PT21ITT	PT20ITT
RW	RW-0					

Bit	Name	Description	
Bit[31]	PT27IDF	PT2.7 Interrupt condition flag For example: check this flag before entering the Sleep Mode: When Bit = 1b, can be PT2.7 pin wake up MCU. When Bit = 0b, PT2.7 pin cannot be awakened MCU.	
		When PT27ITT=0	Always 0. Explanation : When PT27ITT set to 000, the Bit [31] = 0b
		When PT27ITT=1	Inverse DI. Explanation : Before entering Sleep Mode, if PT2.7 status is Low, the Bit [31] = 1b
		When PT27ITT=2	Same as DI. Explanation: Before entering Sleep Mode, if PT2.7 status is High, the Bit [31] = 1b
		When PT27ITT=3	Same as S1. Explanation: When PT2.7 Potential change, which produce an interrupt is triggered
		When PT27ITT=4	Same as DI. Explanation: Before entering Sleep Mode, if PT2.7 status is High, the Bit [31] = 1b
		When	Inverse DI. Explanation:

		PT27ITT=5	Before entering Sleep Mode, if PT2.7 status is Low, the Bit [31] = 1b
		When PT27ITT=6	Same as DI. Explanation: Before entering Sleep Mode, if PT2.7 status is High, the Bit [31] = 1b
		When PT27ITT=7	Inverse DI. Explanation: Before entering Sleep Mode, if PT2.7 status is Low, the Bit [31] = 1b

Bit[30~24]	PT2NIDF	PT2.N Interrupt condition flag (N represent 6~0)	
		When PT2NITT=0	Always 0
		When PT2NITT=1	Inverse DI
		When PT2NITT=2	Same as DI
		When PT2NITT=3	Same as S1
		When PT2NITT=4	Same as DI
		When PT2NITT=5	Inverse DI
		When PT2NITT=6	Same as DI
		When PT2NITT=7	Inverse DI

Bit	Name	Description			
Bit[23~0]	PT2#ITT	Port 2.# select the interrupt trigger method (# represent 7~0)			
		000	Disable the GPIO interrupt trigger to not reply to the interrupt.		
		001	Rising edge trigger	101	High potential trigger
		010	Falling edge trigger	110	Low potential trigger
		011	Potential change trigger	111	High potential trigger
		100	Low potential trigger		

14. GPIO PT3 Management

14.1. Introduction

The PT3 has 6 IO pins, and can be used as common universal IO ports or reused as the input or output IO ports of many function modules, such as OP amplifier, 8-bit resistance ladder and ADC converters, etc. Different reuses need different configurations.

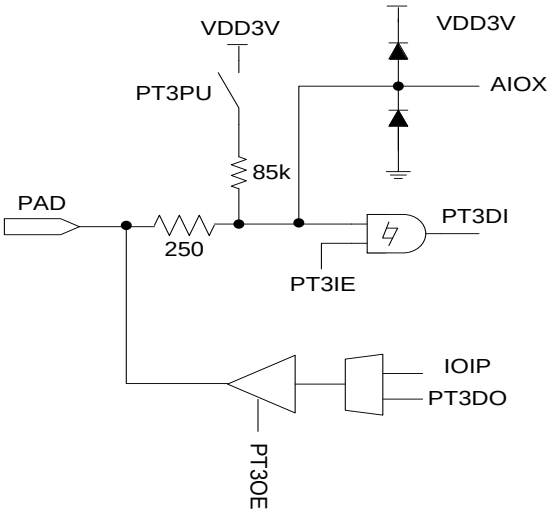


FIG. 14-1 PT3 function block diagram

The PT3 has the functions of the input, output and internal pull-up resistors; and different functions need to be set by different controllers.

Internal pull-up resistor

The controller PT3PU 0x40820[23:16] can enable or disable the internal pull-up resistor of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit of the IO port is set as <1>, the internal pull-up resistor will be enabled; if it is set as <0>, the internal pull-up resistor will be disabled. If the IO port is under the input mode and there is no external pull-up resistor, the internal pull-up resistor should be enabled, especially in low power consumption mode, which can prevent from electric leakage and increase the power consumption. If it serves as the analog signal input port, it is not necessary to enable the internal pull-up resistor.

Output mode

The controller PT3OE0x40820 [7:0] can enable or disable the output mode of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit of the IO port is set as <1>, the output mode of the corresponding IO port will be enabled; if it is set as <0>, the output mode of the corresponding IO port will be disabled. The control bit PT3DO0x40824 [7:0] can determine whether the output status of the pin of the corresponding IO port is 1 or 0. Under the low-power mode, if the IO should enable the output mode, the output status can be set according to the peripheral circuit to decrease the power consumption of the chip. During the mode, the internal pull-up resistor of the IO cannot be enabled, and the input mode and the output mode cannot be enabled at the same time; therefore, when the output mode is enabled, the input mode of the IO port should be disabled.

Input mode

The controller PT3IE0x40824 [23:16] can enable or disable the input mode of each IO port, and each bit is corresponding to each IO port pin. If the corresponding bit of the IO port is set as <1>, the input mode of the corresponding IO port will be enabled; if it is set as <0>, the input mode of the corresponding IO port will be disabled. Whether the current input status of the corresponding IO pin is 1 or 0 can be read via the controller PT3DI0x40828 [7:0]. If the IO is set as the input mode and the chip is not connected to the external pull-up resistor, the internal pull-up resistor should be enabled; the IO pin is not allowed to be floating in order to prevent from the electric leakage of the chip. Especially in the low-power mode, it is suggested the IO pin should be set as the input mode. If it serves as the analog signal input port, it is not necessary to set the corresponding IO pin as the input mode. The output mode of the IO pin should be disabled before its input mode is enabled.

14.2. Register Address

GPIO Register Address	31 24	23 16	15 8	7 0
GPIO base address + 0x00(0X40820)	MASK1	PT3PU	MASK0	PT3OE
GPIO base address + 0x04 (0X40824)	MASK3	PT3IE	MASK2	PT3DO
GPIO base address + 0x08(0X40828)	-	-	REG4	PT3DI
GPIO base address + 0x0C (0X4082C)	PT3ITD	PT3ITT	PT3ITT	PT3ITT

-Reserved

14.3. Register Functions

14.3.1. PT3 Register0

GPIO Base Address + 0X20 (0X40820)									
Symbol	PT3CR0 (PT3 Control Register 0)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	PT3PU7	PT3PU6	PT3PU5	PT3PU4	-	-	PT3PU1	PT3PU0
RW	R0W-0	RW-0							
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	PT3OE7	PT3OE6	PT3OE5	PT3OE4	-	-	PT3OE1	PT3OE0
RW	R0W-0	RW-0							

Bit	Name	Description	
Bit[23~16]	PT3PU	Port 3 pull up control	
		0	Disable pull up
		1	Enable pull up internally
Bit[7~0]	PT3OE	Port 3 PAD output enable	
		0	Disable
		1	Enable

14.3.2. PT3 Register1

GPIO Base Address + 0X24 (0X40824)									
Symbol	PT3CR1 (PT3 Control Register 1)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	PT3IE7	PT3IE6	PT3IE5	PT3IE4	-	-	PT3IE1	PT3IE0
RW	R0W-0	RW-0							
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	PT3DO7	PT3DO6	PT3DO5	PT3DO4	-	-	PT3DO1	PT3DO0
RW	R0W-0	RW-0							

Bit	Name	Description	
Bit[23~16]	PT3IE	Port 3 PAD input enable	
		0	Disable
		1	Enable
Bit[7~0]	PT3DO	Port 3 PAD output Data	
		0	Set 0
		1	Set 1

14.3.3. PT3 Register2

GPIO Base Address + 0X28 (0X40828)									
Symbol	PT3CR2 (PT3 Control Register 2)								
Bit	[31:24]	[23:18]						[17]	[16]
Name	MASK	-						PT3AO	-
RW	R0W-0	-						R-X	-
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	-	PT3DI[7]	PT3DI[6]	PT3DI[5]	PT3DI[4]	-	-	PT3DI[1]	PT3DI[0]
RW	-	R-0							

Bit	Name	Description	
Bit[17]	PT3A0	DAO Output to PT3.1 enable	
		0	Disable
		1	Enable
Bit[7~0]	PT3DI	It is an input signal form PAD	
		0	Pad input is Low
		1	Pad input is High

14.4. Analog to digital multiplexing function Switchover Considerations

PT3.0~PT3.7 not only could be used as normal digital function, but can beset and analog function too. While doing the switch of analog function, should notice the setting of register to avoid the normal function using.

PT3.7/OPO Multiplexed pins:
-Design as OPO output; control resister OPOE 0x41900[1]=1b, PT3PU7=PT3OE7=PT3IE7=0b
-Design as PT3.7 GPIO input; control resister OPOE 0x41900[1]=0b, PT3IE7=1b(Even not set as input, still must be forcibly set)
-Design as PT3.7 GPIO output; control resister OPOE 0x41900[1]=0b, PT3IE7=1b(Even not set as input, still must be forcibly set), PT3OE7=1b

PT3.6/REFO Multiplexed pins:
Design as REFO output; control resister ENRFO 0x40400[1]=1b, PT3PU6=PT3OE6=PT3IE6=0b
Design as REFO input; control resister ENRFO 0x40400[1]=0b, PT3PU6=PT3OE6=PT3IE6=0b
Design as PT3.6 GPIO input; control resister ENRFO 0x40400[1]=0b, PT3IE6=1b(Even not set as input, still must be forcibly set)
Design as PT3.6 GPIO output; control resister ENRFO 0x40400[1]=0b, PT3IE6=1b(Even not set as input, still must be forcibly set), PT3OE6=1b

Other GPIO use method: (PT3.5~PT3.0 all as follows description)
EX: PT3.5/AIO7 Multiplexed pins:
Design as AIO7 input; PT3PU5=PT3OE5=PT3IE5=0b
Design as PT3.5 GPIO Output; PT3IE5=0b, PT3PU5=0b, PT3OE5=1b.
Design as PT3.5 GPIO input; PT3IE5=1b, PT3PU5=1b, PT3OE5=0b. (PT3PU5=1b set as input not floating)

15. GPIO Management

15.1. Introduction

The chip has multiple universal IO ports, and most of them have reuse functions; their reuse functions should be controlled by the registers. The chapter will introduce the control of the reuse functions of the IO ports.

The following table lists the reuse functions of all IO pins and their priority level; 0 stands for the highest level and 6 stands for the lowest level.

GPIO Port	OSC	Interrupt	Timer C Capture	SPI	IIC	UART	CMP	Analog	Timer B PWM
Priority	0	0	0	1	2	3	4	5	6
PT1.0		INT1.0	TCI1_1	CS_1	SCL_1	TX_1	CH1		PWM0_1
PT1.1		INT1.1	TCI2_1	CK_1	SDA_1	RX_1	CH2		PWM1_1
PT1.2		INT1.2	TCI1_2	MISO_1	SCL_2	TX_2	CH3		PWM0_2
PT1.3		INT1.3	TCI2_2	MOSI_1	SDA_2	RX_2	CL1		PWM1_2
PT1.4		INT1.4	TCI1_3	CS_2	SCL_3	TX_3	CL2		PWM0_3
PT1.5		INT1.5	TCI2_3	CK_2	SDA_3	RX_3	CL3		PWM1_3
PT1.6		INT1.6	TCI1_4	MISO_2	SCL_4	TX_4	CL4		PWM0_4
PT1.7		INT1.7	TCI2_4	MOSI_2	SDA_4	RX_4	CMPO1		PWM1_4
PT2.0		INT2.0	TCI1_5	CS_3	SCL_5	TX_5			PWM0_5
PT2.1		INT2.1	TCI2_5	CK_3	SDA_5	RX_5			PWM1_5
PT2.2		INT2.2	TCI1_6	MISO_3	SCL_6	TX_6			PWM0_6
PT2.3		INT2.3	TCI2_6	MOSI_3	SDA_6	RX_6			PWM1_6
PT2.4	LSXT1	INT2.4	TCI1_7	CS_4	SCL_7	TX_7			PWM0_7
PT2.5	LSXT2	INT2.5	TCI2_7	CK_4	SDA_7	RX_7			PWM1_7
PT2.6	HSXT1	INT2.6	TCI1_8	MISO_4	SCL_8	TX_8			PWM0_8
PT2.7	HSXT2	INT2.7	TCI2_8	MOSI_4	SDA_8	RX_8			PWM1_8
PT3.0							OPO1		
PT3.1							OPO2	DAO	
AIO4								AIO4	
AIO5								AIO5	
PT3.4								AIO6	
PT3.5								AIO7	
PT3.6								REFO	
PT3.7								OPO	
AIO0								AIO0	
AIO1								AIO1	
AIO2								AIO2	
AIO3								AIO3	

Table 15-1 IO pin reuse functions and priority levels

15.2. Register Address

GPIO Register Address	31 24	23 16	15 8	7 0
GPIO base address + 0x40(0X40840)	MASK1	PTCN1	MASK0	PTCN0
GPIO base address + 0x44 (0X40844)	MASK3	PTCN3	MASK2	PTCN2

15.3. Register Functions

15.3.1. GPIO reuse function control register GPIOMCR0

GPIO Base Address + 0X40 (0X40840)								
Symbol	GPIOMCR0 (GPIO multiplex Control Register 0)							
Bit	[31:24]	[23:22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	-	-	PTCOPS	PTCOPE	-	PTCCPE
RW	R0W-0	-	RW-0	RW-1	RW-0	RW-0	-	RW-0
Bit	[15:08]	[7:5]		[4:2]			[1]	[0]
Name	MASK	PTCTC[2:0]		PTPW[2:0]			PTPW1E	PTPW0E
RW	R0W-0	RW-0						

Bit	Name	Description	
Bit[19]	PTCOPS	Rail-to-rail OPAMP digital output to port selection	
		0	Port 3.0
		1	Port 3.1
Bit[18]	PTCOPE	Rail-to-rail OPAMP digital output to port enable control	
		0	Disable (no output to any port)
		1	Enable (to port that is determined by OPPTS)
Bit[16]	PTCCPE	Comparator output/input to port enable control	
		0	Disable (no input/output to any port)
		1	Enable (output to port that is determined by CPPTS)

Bit	Name	Description		
Bit[7~5]	PTCTC	Timer C output to port selection		
		000	Port 1.0 =TCI1	Port 1.1 =TCI2
		001	Port 1.2 =TCI1	Port 1.3 =TCI2
		010	Port 1.4 =TCI1	Port 1.5 =TCI2
		011	Port 1.6 =TCI1	Port 1.7 =TCI2
		100	Port 2.0 =TCI1	Port 2.1 =TCI2
		101	Port 2.2 =TCI1	Port 2.3 =TCI2
		110	Port 2.4 =TCI1	Port 2.5 =TCI2
		111	Port 2.6 =TCI1	Port 2.7 =TCI2
Bit[4~2]	PTPW	PWM output to port selection		
		000	Port 1.0 =PWMO0	Port 1.1 =PWMO1
		001	Port 1.2 =PWMO0	Port 1.3 =PWMO1
		010	Port 1.4 =PWMO0	Port 1.5 =PWMO1
		011	Port 1.6 =PWMO0	Port 1.7 =PWMO1
		100	Port 2.0 =PWMO0	Port 2.1 =PWMO1
		101	Port 2.2 =PWMO0	Port 2.3 =PWMO1
		110	Port 2.4 =PWMO0	Port 2.5 =PWMO1
		111	Port 2.6 =PWMO0	Port 2.7 =PWMO1
Bit[1]	PTPW1E	PWM 1 output to port enable control		
		0	Disable (no output to any port)	
		1	Enable (to port that is determined by PWPS)	
Bit[0]	PTPW0E	PWM 0 output to port enable control		
		0	Disable (no output to any port)	
		1	Enable (to port that is determined by PWPS)	

15.3.2. GPIO reuse function control register GPIOMCR1

GPIO Base Address + 0X44 (0X40844)						
Symbol	GPIOMCR1 (GPIO Multiplex Control Register 1)					
Bit	[31:24]	[23:20]			[19:17]	[16]
Name	MASK	-			I2CPTS[2:0]	I2CPTEn
RW	R0W-0	-			RW-0	
Bit	[15:08]	[7]	[6:5]	[4]	[3:1]	[0]
Name	MASK	-	PTCSP[1:0]	PTSPE	PTUR[2:0]	PTURE
RW	R0W-0	-	RW-0			

Bit	Name	Description		
Bit[19~17]	I2CPTS	I2C output to port selection		
		000	Port 1.0 =SCL	Port 1.1 =SDA
		001	Port 1.2 =SCL	Port 1.3 =SDA
		010	Port 1.4 =SCL	Port 1.5 =SDA
		011	Port 1.6 =SCL	Port 1.7 =SDA
		100	Port 2.0 =SCL	Port 2.1 =SDA
		101	Port 2.2 =SCL	Port 2.3 =SDA
		110	Port 2.4 =SCL	Port 2.5 =SDA
		111	Port 2.6 =SCL	Port 2.7 =SDA
Bit[16]	I2CPTEn	I2C Input/ Output to port enable control		
		0	Disable (no output to any port)	
		1	Enable (to port that is determined by I2CPTS)	

Bit	Name	Description		
Bit[6~5]	PTCSP	SPI Input/ Output to port selection		
		00	Port1.0 =CS, Port1.1 =CK, Port1.2 = MISO, Port1.3 =MOSI	
		01	Port1.4 =CS, Port1.5 =CK, Port1.6 = MISO, Port1.7 =MOSI	
		10	Port2.0 =CS, Port2.1 =CK, Port2.2 = MISO, Port2.3 =MOSI	
		11	Port2.4 =CS, Port2.5 =CK, Port2.6 = MISO, Port2.7 =MOSI	
Bit[4]	PTSPE	SPI Input/ Output to port enable control		
		0	Disable (no output to any port)	
		1	Enable (to port that is determined by SPPTS)	
Bit[3~1]	PTUR	UART output to port selection		
		000	Port 1.0 =TX	Port 1.1 =RX
		001	Port 1.2 =TX	Port 1.3 =RX
		010	Port 1.4 =TX	Port 1.5 =RX
		011	Port 1.6 =TX	Port 1.7 =RX
		100	Port 2.0 =TX	Port 2.1 =RX
		101	Port 2.2 =TX	Port 2.3 =RX
		110	Port 2.4 =TX	Port 2.5 =RX
		111	Port 2.6 =TX	Port 2.7 =RX
Bit[0]	PTSPE	EUART Input/ Output to port enable control		
		0	Disable (no output to any port)	
		1	Enable (to port that is determined by PTUR)	

16. ΣΔ 24-bit ADC

16.1. Introduction

The chip has an embedded high-performance 24-bit A/D converter (24-bitΣΔADC). The ADC has a pre low-noise programmable gain amplifier (Low Noise PGA), which can be used to amplify input signals. The gain programmable setting range is 1~128. The sampling rate of the ADC can be programmed by the register. The highest designed sampling rate is 350 KHz per second. It has a 3-stage regulator for filtering the quantized noise of the regulator. The programmable range of the over-sampling rate of the ADC is 32~32768. It is designed to measure the sensors with extremely small signals, such as strain meter, pressure gauge and industry process control.

Features:

1. The settable sampling rate is 40 KHz~350 KHz;
2. The resolution of the effective number (ENOB) of bits is up to 21 bits;
3. The lowest input noise is 65nV RMS;
4. The settable over-sampling rate is 32~32768;
5. The highest output rate is 10 KHz;
6. The multiplier gain of the built-in low-noise programmable gain amplifier is 1~128;
7. Built-in temperature sensor is provided;
8. Built-in 4-bit DAC is provided to adjust the offset;
9. 3-stage comb filter is provided.

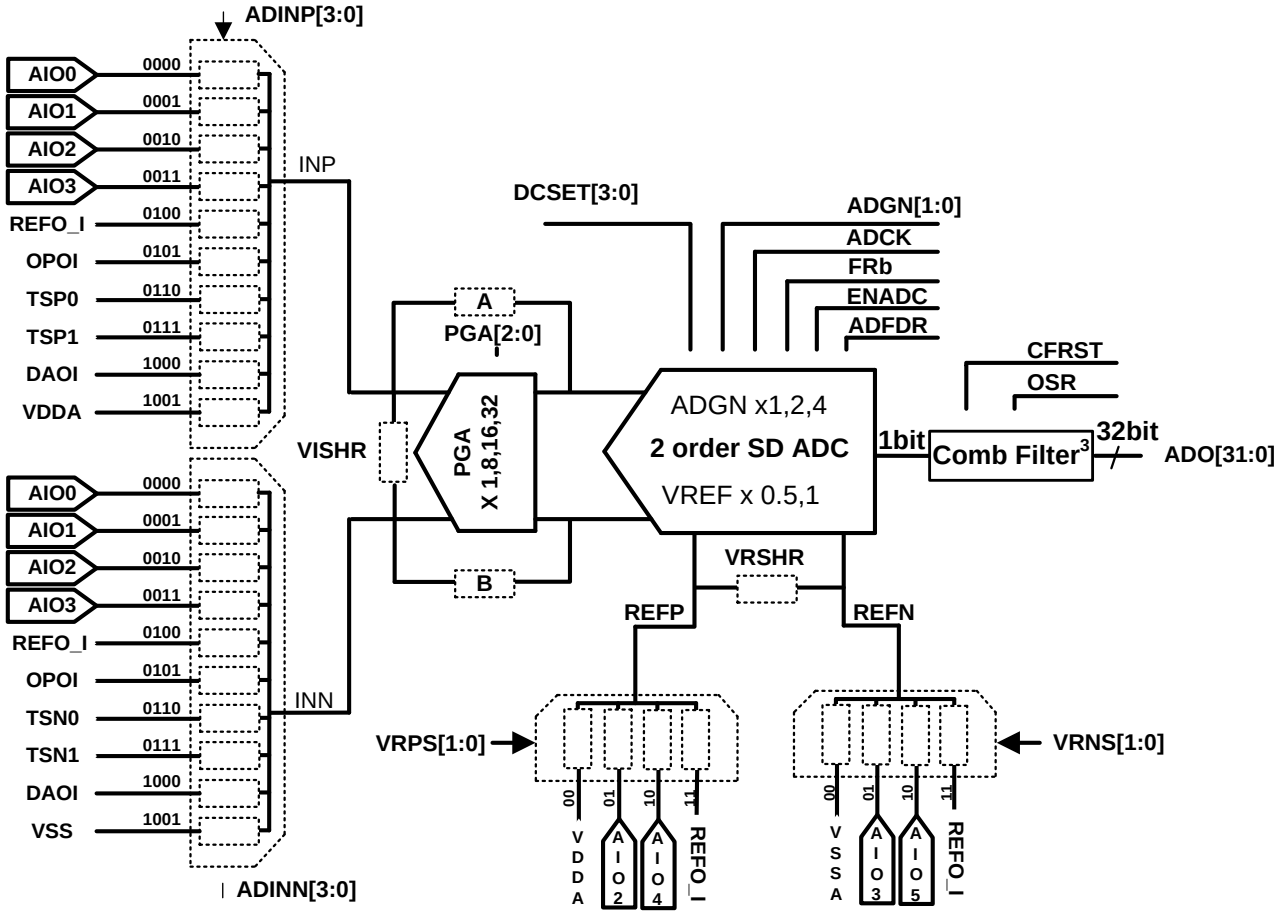
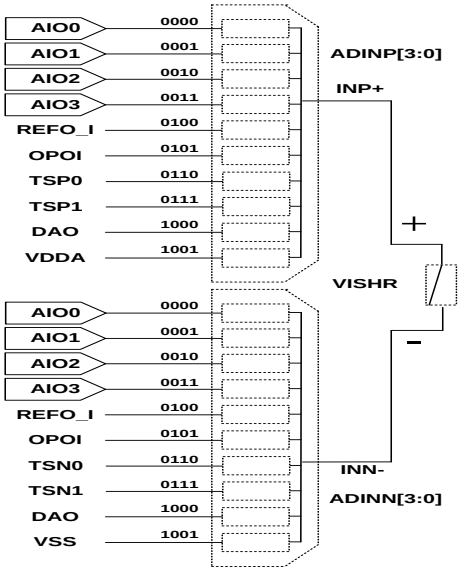


Figure 16-1 ADC function block diagram

16.1.1. fully differential signal input terminal

ADC input signal is fully differential input mode, the input end is the positive input and negative input terminal composition. Positive and negative signal input channel consists of four external signal input channels and six internal signal input channel and the input impedance of ADC signal input is 200K. Through the controller ADINP [3: 0], ADINN [3: 0] select positive and negative signal input channel, but the positive input can only select one signal input channel at the same time, the negative input terminal at the same time only select one signal input channel. Positive and negative selectable same input channels, so that the differential signal is zero. ADC internal configuration of a signal input channel short-circuit switch, can be set via control bit VISHR the positive and negative input terminal short circuit from the inside. The map shows the positive side and the negative side of the signal input channel



ADINP[3:0]	positive input	ADINN[3:0]	negtive input
0000	AIO0	0000	AIO0
0001	AIO1	0001	AIO1
0010	AIO2	0010	AIO2
0011	AIO3	0011	AIO3
0100	REFO_I	0100	REFO_I
0101	OPOI	0101	OPOI
0110	TSP0	0110	TSN0
0111	TSP1	0111	TSN1
1000	DAO	1000	DAO
1001	VDDA	1001	VSSA

Figure 16-2 ADC signal input channel

Increasing the amplification of the input signal via an internal re-conversion, so the input signal voltage range also limits, in order to be able to get a higher ADC output resolution and linearity, recommendations differential voltage value ΔSI guess signal = ± 0.9 * ΔVREF (ΔSI = INP-INN). The input signal voltage as shown in Table 16-1.

External input	Voltage input range
ADINP+	VSSA-0.2V ≦ INP+ ≦ VDDA+0.1V
ADINN-	VSSA-0.2V ≦ INN- ≦ VDDA+0.1V

Table 16-1 Input signal voltage range table

16.1.2. Built-gain amplifier

ADC contains two gain amplifiers: a low noise, low temperature coefficient of programmable gain amplifier PGA, magnification 8/16/32; a programmable gain amplifier ΣAD, magnification 1/2/4. Thus, the maximal magnifying power of the combination of the two gain amplifiers is 128. But the amplification and ADC output value of significant digits (ENOB) is inversely proportional to the column, the greater the magnification, the smaller the value of the ENOB of. So set magnification according to the actual need to configure. Through the controller PGA [2: 0] can select the PGA gain the magnification, magnification PGA selection as shown in Table; through the controller ADGN [1: 0] can choose ΣAD gain magnification, ΣAD magnification selection as table

	PGA					ΣAD			
PGA[2:0]	000	001	011	111	ADGN[1:0]	00	01	10	11
Magnification	x1	x 8	x16	x32	Magnification	x1	x2	RSV	x4

16.1.3. Reference voltage input channels

ADC reference voltage input belongs fully differential input mode, which is the reference voltage input end is the positive input and the negative input of the composition. Positive and negative inputs include two external input channels and two internal input channels. Through the controller VRPS [1: 0], VRNS [1: 0] can be set separately positive reference voltage input channel, the negative input channels. Positive input at the same time can only select one input channel; the negative input terminal can only select one input channel at the same time. A reference voltage terminal is further configured to short-circuit switch, it may be provided through the short-circuit switch closure control bit VRSHR, the reference voltage of the positive input terminal and negative input shorted.

ΔVREF voltage generated by the reference voltage after VREFP and VREFN input difference, after a programmable reference voltage attenuator as the reference voltage value of the ADC. Controller FRb [0] can be set to a reference voltage attenuation ratio, the reference voltage attenuation ratio as shown in Table 16-3.

The reference voltage is calculated as follows:

ΔVREF = VREFP-VREFN (Formula 16-1)

VREF = Gain x ΔVREF (Formula 16-2)

ΔVREF: Input voltage difference between the input voltage pin; VREF: ADC internal reference voltage value

VREFP / VREFN: input reference voltage value

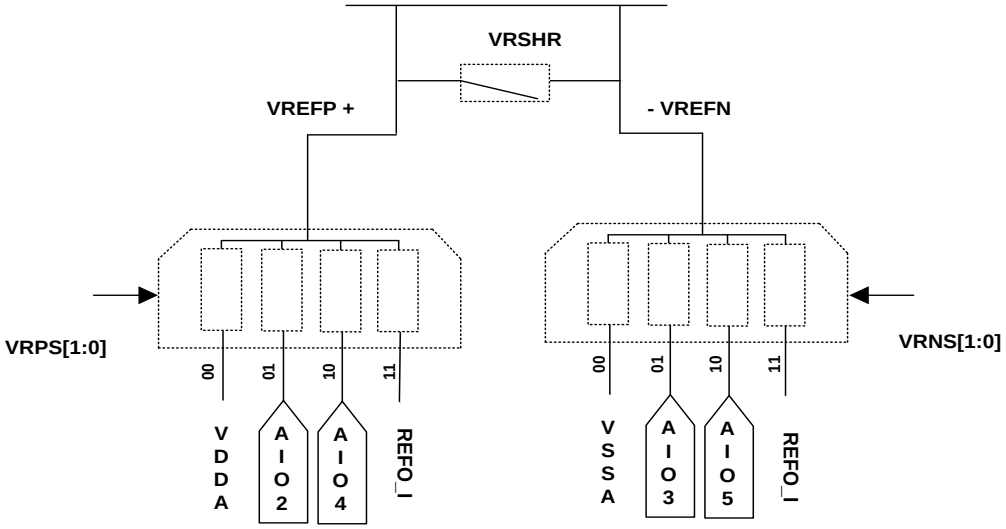


Figure 16-3 reference voltage input channels

Reference voltage attenuation ratio		
FRb[0]	0	1
Gain	1	1/2

Table 16-3 reference voltage attenuation ratio

Positive and negative reference voltage input channels input impedance 500kΩ, and VREFP or VREFN not be less than the input voltage VSSA, must not exceed VDDA; through the controller to the external input channel, increase input impedance, but maybe noted that the external input channel voltage value range.

External input	Voltage input range
AIO2 / AIO4	VSSA ≦ VREFP ≦ VDDA
AIO3 /AIO5	VSSA ≦ VREFN ≦ VDDA

Table 16-4 reference voltage external input channel voltage input range

16.1.4. Input bias of input signal

The ADC has a zero point bias translation controller, and the zero point bias translation controller DCSET[3:0] can change the position of the zero point of the signal to prevent the voltage of the input signal from being too high to exceed the maximal measurement range. After the signal to be measured adjusted via the pre PGA, the ADC modulator and the zero point bias translation, the calculation formula of the equivalent signal to be measured ΔSI_I is as follows:

ΔSI_I = PGA x ADGN x ΔSI± + (DCSET x ΔVREF) (Equation 16-3)

	DCSET[3:0]							
setting	0000	0001	0010	0011	0100	0101	0110	0111
Shift amount	0 VREF	+1/8VREF	+1/4VREF	+3/8VREF	+1/2VREF	+5/8VREF	+3/4VREF	+7/8VREF
setting	1000	1001	1010	1011	1100	1101	1110	1111
Shift amount	0 VREF	-1/8VREF	-1/4VREF	-3/8VREF	-1/2VREF	-5/8VREF	-3/4VREF	-7/8VREF

Table 16-5 measured input signal zero bias Setup Checklist

16.1.5. Comb filter

ΣΔADC adopts the 3-stage comb filter, and different over-sampling rates can be obtained by setting the controller OSR [3:0] and the different combinations of the sampling rates of the ADC so as to realize different ADC conversion output frequencies. The configuration parameters of the OSR [3:0] are as follows:

	OSR[3:0]										
setting	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010
Frequency dividing value	32768	16384	8192	4096	2048	1024	512	256	128	64	32

Table 16-6 oversampling frequency divider table

Analog to digital conversion result stored in the register ADCO [23: 0], the highest bit is the sign bit, so the relationship between the results of the conversion of the input signal as shown in Table.

	Equivalent test signal	ADCO[23:0]	
		hexadecimal	Binary
Bipolar output Two's complement format	△VR	7F FF FF	0111-1111 1111-1111 1111-1111
	△VR*(1/2	00 00 01	0000-0000 0000-0000 0000-0001
		00 00 00	0000-0000 0000-0000 0000-0000
	-△VR	FF FF FF	1111-1111 1111-1111 1111-1111
	△VR	80 00 00	1000-0000 0000-0000 0000-0000

Table 16-7 ADCO [23: 0] input signal relational tables

Comb filter provides reset control function, when the control bit is set CFRST <0>, Σ comb filter reset, then set before CFRST = 1, start comb filter, so that it will automatically be discarded ΣΔADC 2 pen information users read first pen ADC conversion value will be valid ADC value.

16.1.6. Absolute temperature sensor TPS

Absolute temperature sensor diode (BJT), whose voltage signals as changes in temperature by 0K curve, which has the following characteristics:
Temperature sensor at an ambient temperature of 0K output voltage value $V_{TPS@0k}$ = 0V;
Through measurement may enable analog-to-digital converter ADC offset voltage ($V_{ADC-OFFSET}$) automatic offset and the asymmetry BJT;
Only a single point calibration temperature calibration error can meet the ± 2 ˚C;

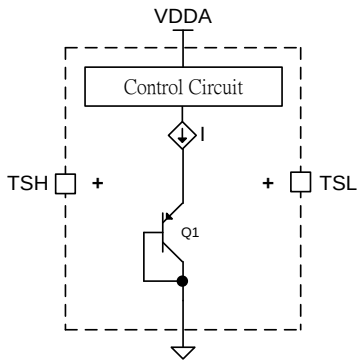


Fig 16-4 absolute temperature sensor Application block diagrams

- **TPS initial setup and calculated as follows:**
  - Enable the ADC and the function of the TPS can be automatically enabled right away.
  - Fix the related configuration of the ADC and the system operating frequencies, and the configurations for the TPS calibration and measurement should be the same with each other.
  - When it is under the same temperature Ta (°C) and the values of the V_{TSH0} / V_{TSL0} and V_{TSH1} / V_{TSL1} are measured, add the two values and calculate the average to obtain the corresponding voltage $V_{TS@Ta}$ of the TPS under the temperature Ta.

    - measuring V_{TSH0} / V_{TSL0} time, INxP [2: 0] Set <111> and INxN [2: 0] Set <110>
    - measuring V_{TSH1} / V_{TSL1} time, INxP [2: 0] Set <110> and INxN [2: 0] Set <111>
    - The value of V_{TSH0}/ V_{TSL0} and V_{TSH1}/ V_{TSL1} value addition operation and then divided by 2. to obtain the $ADC_{TPS@Ta}$

- TPS output voltage V_{TS} temperature change is a linear curve, it can be deduced its gain value G_{TPS} (or called slope).

$$G_{TPS} = \frac{ADC_{TPS@Ta}}{(273.15 + T_{offset} + T_A)K} \quad \text{..... (Equation 16-4)}$$

G_{TPS} : The gain or slope of the TPS sensor ($\frac{\text{ADC count}}{K}$)

$ADC_{TPS@Ta}$: ADC values measured at calibration temperature

$K : °C + 273.15$

T_{offset} : Temperature offset

TPS in the temperature conversion is not ideal, so in fact not at ℃ = K-273.15
Instead ℃ = K + KT = K + (- 273.15-T_{offset})
For the KT values, refer to the TPS specification in the IC Data sheet ADC section.
HY16F18x KT value of -285, ℃ = K-285 -> K=℃+285

TPS Example description

It is assumed that TPS calibration will be performed at 25 ° C. After calibration, the IC was moved to a higher temperature environment (65 ° C), Test the temperature in the environment.

(1) Set INxP [2: 0] to set <111> and INxN [2: 0] to set <110>, The ADC measures a digital code ADC_{TPS0} = 5897634.

(2) Set INxP [2: 0] to set <110> and INxN [2: 0] to set <111>, The ADC measures a digital code ADC_{TPS1} = 5827679.

(3) Calculate $ADC_{TPS\ @\ 25}$ = (ADC_{TPS0} + ADC_{TPS1}) / 2 = 5862656. This action eliminates the Offset of the Temperature Sensor.

(4) Calculate G_{TPS}

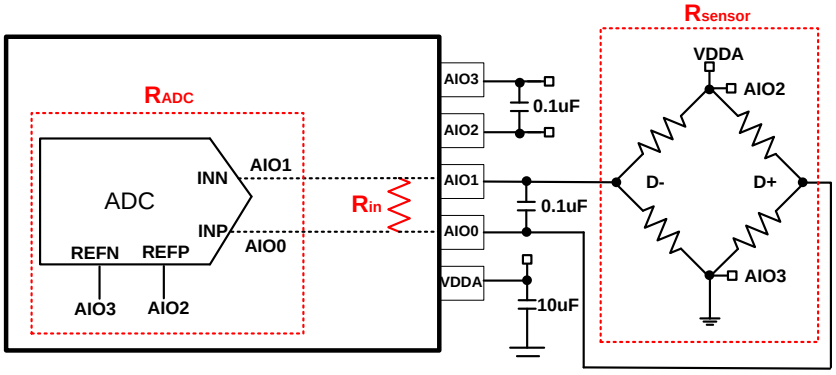
$$G_{TPS} = \frac{ADC_{TPS@Ta}}{(273.15 + T_{offset} + T_A)K} = \frac{5862656}{(285 + 25)K} = 18911.79$$

(5) After the IC was moved to a high temperature (65 ° C), Refer to steps (1) to (3) again to measure $ADC_{TPS\ @\ 65}$: 6630103

$$T_X = \frac{ADC_{TPS@65}}{G_{TPS}} - \left[273.15 + T_{offset}\right] = \frac{6630103}{18911.79} - 285 = 65.58^{o}C$$

16.1.7. ADC input impedance (R_{ADC}) description

The following figure shows: ADC input impedance (R_{ADC}) and the sensor output impedance (R_{sensor}) and the actual input to the chip input impedance (R_{in}) diagram. Users can follow the Sensor characteristics to assess whether the Sensor can be directly connected with the ADC input channel, to avoid the measurement of the impedance effect.



(R_{in}) and (R_{ADC}) and (R_{sensor}) relationship is: R_{in}= R_{sensor} // R_{ADC}

R_{in} : R_{in} is R_{sensor} parallel R_{ADC}

R_{ADC} : ADC input impedance

R_{sensor}: sensor output impedance

Note: (R_{ADC}) is not equivalent to the actual output impedance of the Sensor that can be connected to the actual HY16F ADC. When PGA and ADGN = 1 times, R_{ADC} = 2.5M, But this value is not equivalent to connect the Sensor's maximum output impedance value (R_{sensor}). Reference recommendations in the PGA and ADGN = 1 times the time, can be connected to the sensor maximum output impedance of 200k.

ADC input impedance (R_{ADC}) table

R_{ADC}(ohm) @ ADCK= 333kHz			
PGA	ADGN=1	ADGN=2	ADGN=4
1	2.5M	1.25M	626k
8	125k	125k	125k
16	62.5k	62.5k	62.5k
32	31.25k	31.25k	31.25k

Sensor output impedance (R_{sensor}) table

R_{sensor}(ohm) @ ADCK= 333kHz			
PGA	ADGN=1	ADGN=2	ADGN=4
1	200k	100k	50k
8	10k	10k	10k
16	5k	5k	5k
32	2.5k	2.5k	2.5k

16.1.8. ADC Operating Instructions

The ADC is realized by delta-sigma architecture with 24-bit resolution. To enable the ADC function, some peripheral circuits are needed set correctly. The ADC power is supplied the VDDA voltage. Thus, the VDDA is needed to higher 2.4V. To obtain a better ADC performance requires a stable VDDA supply. Since the VDDA needs some time to settle, the ADC should wait for VDDA settle and start to take the measurement. The bias and band gap is needed to turn on by set ENBGR to 1. Then a 1.2V ACM is required to enter the ADC. The ACM voltage can be chosen externally or internally. The ADC also requires a maximum 350 KHz clock input. The input clock should be set to higher than 40 KHz.

Detailed configuration as follows:

- Configure and start the ADC clock source, it is recommended the ADC sampling frequency is set at about 330kHz
- Open VDDA voltage and the bandgap reference voltage (BandGap Voltage), the common mode reference voltage (REFO) and analog sources;
- Select ADC input channel signal being measured, including the positive and negative input channels and disconnect switch input is shorted;
- configure the ADC internal gain magnification is set according to the actual situation, let ΔSI within 0.9 * VREF range;
- Set zero bias DCSET, if it is not necessary, set 0 VREF;
- select ADC reference voltage input channels, disconnect switch input is shorted, and select the reference voltage decay rate, the proposed reference voltage VREF = 0.8v ~ 1.2v;
- divider value is set oversampling OSR [3: 0], you need to be set according to actual needs ENOB;
- be turned on ADC interrupt function, and enables the global interrupt GIE;
- Open ADC function;
- Reset comb filter, CFRST = 0, then start comb filter, CFRST = 1; set this bit hardware can automatically throws the first 2 pieces of the data.

16.2. Register Address

ADC Register Address	31	24	23	16	15	8	7	0
ADC base address + 0x00 (0X41100)	MASK0		REG0		MASK1		REG1	
ADC base address + 0x04 (0X41104)	REG2		REG3		MASK4		REG4	
ADC base address + 0x08 (0X41108)	ADO3		ADO2		ADO1		-	

-Reserved

16.3. Register Functions

16.3.1. ADC Control Register0

ADC Base Address + 0X00 (0X41100)

Symbol	ADCCR0 (ADC Control Register 0)					
Bit	[31:24]	[23:22]	[21]	[20]	[19:18]	[17:16]
Name	MASK	-	VISHR	VRSHR	VRPS[1:0]	VRNS[1:0]
RW	R0W-0	-	RW-0			
Bit	[15:08]	[7]	[6]	[5:2]	[1]	[0]
Name	MASK	-	ADFDR	OSR[3:0]	CFRST	ENADC
RW	R0W-0	-	RW-0			

Bit	Name	Description	
Bit[21]	VISHR	ADC signal input (positive and negative) short control	
		0	Open
		1	Short
Bit[20]	VRSHR	ADC reference input (positive and negative) short control	
		0	Open
		1	Short
Bit[19~18]	VRPS	Positive reference voltage source multiplexer	
		00	VDDA
		01	AIO2
		10	AIO4
		11	Reference buffer output(REFO)
Bit[17~16]	VRNS	Negative reference voltage source multiplexer	
		00	VSSA
		01	AIO3
		10	AIO5
		11	Reference buffer output(REFO)

Bit	Name	Description		
Bit[06]	ADFDR	Fast chopper stable mode control		
		0	Normal mode chopper frequency = ADCK/128	
		1	Fast mode chopper frequency = ADCK/32	
Bit[5~2]	OSR	ADC over sampling rate select (when clock is 327680Hz)		
		0000	32768	Data Rate 10sps
		0001	16384	Data Rate 20sps
		0010	8192	Data Rate 40sps
		0011	4096	Data Rate 80sps
		0100	2048	Data Rate 160sps
		0101	1024	Data Rate 320sps
		0110	512	Data Rate 640sps
		0111	256	Data Rate 1280sps
		1000	128	Data Rate 2560sps
		1001	64	Data Rate 5120sps
		1010	32	Data Rate 10240sps
		1011	Reserved (32768)	
		1100	Reserved (32768)	
		1101	Reserved (32768)	
		1110	Reserved (32768)	
		1111	Reserved (32768)	
Bit[01]	CFRST	Comb filter enable control		
		0	Reset (Level Reset)	
		1	On	
Bit[00]	ENADC	ADC control		
		0	Disable	
		1	Enable	

16.3.2. ADC Control Register1

ADC Base Address + 0X04 (0X41104)							
Symbol	ADCCR1 (ADC Control Register 1)						
Bit	[31:29]	[28]	[27:24]	[23:22]	[21:20]	[19]	[18:16]
Name	-	DA	DCSET[3:0]	-	ADGN[1:0]	FRb	PGA[2:0]
RW	-	RW-0	RW-0	-	RW-0	RW-0	RW-0
Bit	[15:08]			[7:4]		[3:0]	
Name	MASK			ADINP[3:0]		ADINN[3:0]	
RW	R0W-0			RW-0		RW-0	

adc_04=0X1000FF00; //ADC 0X41104 Bit_28 set 1 AIO6 8-BIT RESISTANCE LADDERS P+ VIN Useable

Bit	Name	Description	
Bit[28]	DA	AIO6 enable control for 8-BIT RESISTANCE LADDERS P+ VIN ON AIO6	
		0	Disable
		1	Enable
Bit[27~24]	DCSET	DC offset input voltage selection (VREF = REFP-REFN)	
		0000	0 VREF
		0001	+1/8 VREF
		0010	+1/4 VREF
		0011	+3/8 VREF
		0100	+1/2 VREF
		0101	+5/8 VREF
		0110	+3/4 VREF
		0111	+7/8 VREF
		1000	0 VREF
		1001	-1/8 VREF
		1010	-1/4 VREF
		1011	-3/8 VREF
		1100	-1/2 VREF
		1101	-5/8 VREF
		1110	-3/4 VREF
		1111	-7/8 VREF

Bit	Name	Description	
Bit[21~20]	ADGN	Input signal gain for modulator	
		00	Gain = 1
		01	Gain = 2
		10	Reserved
		11	Gain = 4
Bit[19]	FRb	Full reference range select	
		0	Full reference range input
		1	1/2 reference range input
Bit[18~16]	PGA	Input signal gain for modulator	
		000	Gain = 1
		001	Gain = 8
		010	Reserved (Gain = 8)
		011	Gain = 16
		100	Reserved (Gain = 16)
		101	Reserved (Gain = 24)
		110	Reserved (Gain = 24)
		111	Gain = 32

Bit	Name	Description
Bit[7~4]	ADINP	Positive input voltage source multiplexer

		0000	AIO0
		0001	AIO1
		0010	AIO2
		0011	AIO3
		0100	ACM(REFO_I)
		0101	OPO
		0110	TPSP0
		0111	TPSP1
		1000	DAO
		1001	VDDA
		1010	Reserved
		1011	Reserved
		1100	Reserved
		1101	Reserved
		1110	Reserved
		1111	Reserved
Bit[3~0]	ADINN	Negative input voltage source multiplexer	
		0000	AIO0
		0001	AIO1
		0010	AIO2
		0011	AIO3
		0100	ACM(REFO_I)
		0101	OPO
		0110	TPSN0
		0111	TPSN1
		1000	DAO
		1001	VSS
		1010	Reserved
		1011	Reserved
		1100	Reserved
		1101	Reserved
		1110	Reserved
		1111	Reserved

16.3.3. ADC Control Register2

ADC Base Address + 0X08 (0X41108)		
Symbol	ADCCR2 (ADC Control Register 2)	
Bit	[31:16]	
Name	ADCO	
RW	R-0	
Bit	[15:8]	[7:0]
Name	ADCO	RSV
RW	R-0	R-0

ADC Output Register ADO [31:0] buffer from MSB to LSB High 24-bit is effective

17. Power Mode

17.1. Introduction

The paragraph will describe different power modes and their corresponding function modules.
Under the active mode, all peripheral circuits can be enabled, and the clock of the MCU is HS_CK or LS_CK clock; under the mode, the system can freely switch to other modes and have shortest response time.
Under the low-power mode, all analog circuits can be enabled and the clock of the MCU is LS_CK clock; under the mode, the MCU works under the lowest frequency and the system can switch to other modes by executing instructions.

There are three power-saving modes, Including Sleep Mode, Idle Mode, Wait mode, allows the MCU to stop executing instructions.
These modes can be disabled by the interrupt. Once the interrupt is triggered, The MCU will leave the power saving mode. Before entering power-saving mode, the corresponding interrupt vectors must be enabled to wake up the chip. Otherwise, the chip can't achieve power saving effect. For example, in the sleep mode, the timer interrupt is invalid, and the chip only can be wakened up by the communication interrupt or IO port external interrupt or reset. In details, refer to the table below, the table lists the wake-up interrupt vector for each power-saving mode. It should be noted in different power-saving mode, only the number of functional modules can be enabled, and only some of the interrupt functions can wake up the MCU from power-saving mode.

Note that when entering Idle Mode or Sleep Mode, should be performed before entering the power saving mode, the CPU operating frequency of the low frequency after the first change to LPO, then turn off the high frequency HAO. It has turned the analogy power output is also required to make the corresponding closing action, after such power saving mode can be achieved with specification (Datasheet) as current consumption. Wake-up time: Sleep Mode > Idle Mode > Wait Mode. Sleep Mode and Idle Mode, although many are still saving ratio Wait Mode, but through interrupt wake-up time is relatively long.

17.2. Mode Definition

IP	Active Mode	Wait Mode	-
	Full Speed	Wait	-
MCU clock	Always On	By setting	-
Internal Low OSC	Always On	Always On	-
Other OSC	By setting	By setting	-
Other IPS	By setting	By setting	-
Pin Reset	By setting	By setting	-
Pin Interrupt	By setting	By setting	-
SPI Slave	By setting	By setting	-
I2C Slave	By setting	By setting	-
BOR/POR Reset	Always On	Always On	-

IP	Standby Mode	Sleep Mode	-
	Idle	Sleep	-
MCU clock	By setting	OFF	-
Internal Low OSC	Always On	OFF	-
Other OSC	By setting	OFF	-
Other IPS	By setting	OFF	-
Pin Reset	By setting	By setting	-
Pin Interrupt	By setting	By setting	-
SPI Slave	By setting	By setting	-
I2C Slave	By setting	By setting	-
BOR/POR Reset	Always On	Always On	-
Operation Current(uA)	5uA	2.5uA	-
Wake Up to Full Speed Time	50us	64ms	-

Interrupt/Reset Mode	Sleep Mode	Idle Mode	Wait Mode	Note
	Wakeup	Wakeup	Wakeup	
Power On Reset	V	V	V	Reset
PT 4.0 Reset	V	V	V	Reset
WDT Reset Type			V	WDT Reset Type
I2C TX IRQ		V	V	I2CIE
I2C RX IRQ	V	V	V	I2CIE
I2C Error IRQ			V	I2CEIE
UART TX IRQ			V	UTXIE
UART RX IRQ	V	V	V	URXIE
SPI TX IRQ			V	STXIE
SPI RX IRQ	V	V	V	SRXIE
RTC IRQ		V	V	RTCIE
WDT IRQ			V	WDTIE
TMA IRQ			V	TMAIE
TMB IRQ			V	TMBIE
TMC IRQ			V	TMCIE
ADC IRQ			V	ADCIE
CMP IRQ	V	V	V	CPIE
OPAMP IRQ			V	OPOIE
PT1 IRQ	V	V	V	PT1IE
PT2 IRQ	V	V	V	PT2IE
Debug Exception			V	EDM

SYS Base Address + 0X04 (0X40104)								
Symbol	SYS0 (SYS Control Register 0)							
Bit	[31:08]	[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	F1	IDLE	F2	F3	F4	F5
RW	R0W-0	-	RW0-0					RW0-1

F1~F5 at CH6 System Register

Bit	Name	Description	
Bit[4]	IDLE	IDLE Mode Control Register	
		0	Sleep Mode
		1	IDLE Mode

Mode	Setting	Description
Wait Mode	sys_04=0XFF10; asm("standby 0");	//Idle Set //Wait Mode
Idle Mode	sys_04=0XFF10; asm("standby 1");	//Idle Set //Idle Mode
Sleep Mode	sys_04=0XFF00; asm("standby 1");	//Sleep Set //Sleep Mode

sys_04 Address = 0X40104

Before entering Sleep Mode, you should first set 0x40104 [4] = <0>

The state of 0x40400 [0] will affect the Sleep Mode power consumption. The details are as follows:

- 0x40400 [0] = 0b -> When the sleep mode wake-up, this bit should be set to 0, the LDO into the normal mode.
- 0x40400 [0] = 1b -> Before entering the sleep mode, set this bit to 1 to make the LDO enters a low-power mode.

At sleep mode power consumption -> 0x40400 [0] = 0b --------- 3.5uA
At sleep mode power consumption -> 0x40400 [0] = 1b --------- 2.5uA

18. Rail-to-Rail OPAMP

18.1. Introduction

The chip has an embedded Rail-to-Rail OPAMP network, which is mainly used to deal with analog signals. The input range and the output range are from VSSA to VDDA. When the input signal range is between VSSA +0.1 V and VDDA - 0.1V, the open loop gain is higher than 80dB. When the output load is 50pF, the unit gain bandwidth is 1MHz. It has the 1mA input and output push-pull driving ability. The maximal drivable capacitor load is 100pF. The positive input end has 4 independent selection switches and the negative input end has 6 independent selection switches. The OPAMP network has a built-in 10pF capacitor. It can serve as input sampling capacitor or integrator. Different input channel configurations and 8-bit DAC configurations can achieve different applications. The output end of the OPAMP can be connected to an I/O pin, or used by other internal IPs. When it serves as comparator, its output is digital format. The user can set the output of the OPAMP to pass a 2us peak pulse filter. Besides, the output of the comparator can be on-and-off or opposite in phase.

The features of the OPAMP include:

1. Rail-to-Rail input range, and Rail-to-Rail output range;
2. Under a 22pF load, it can provide a 1MHz unit gain bandwidth and 60 phase margin;
3. The DC gain can be higher than 80dB;
4. 1mA push-pull output driving ability;
5. The positive input end has 4 independent selection switches and the negative input end has 6 independent selection switches.
6. Built-in 10pF capacitor;
7. It can serve as comparator with the function of a chopper;
8. Built-in peak pulse digital low-pass filter;

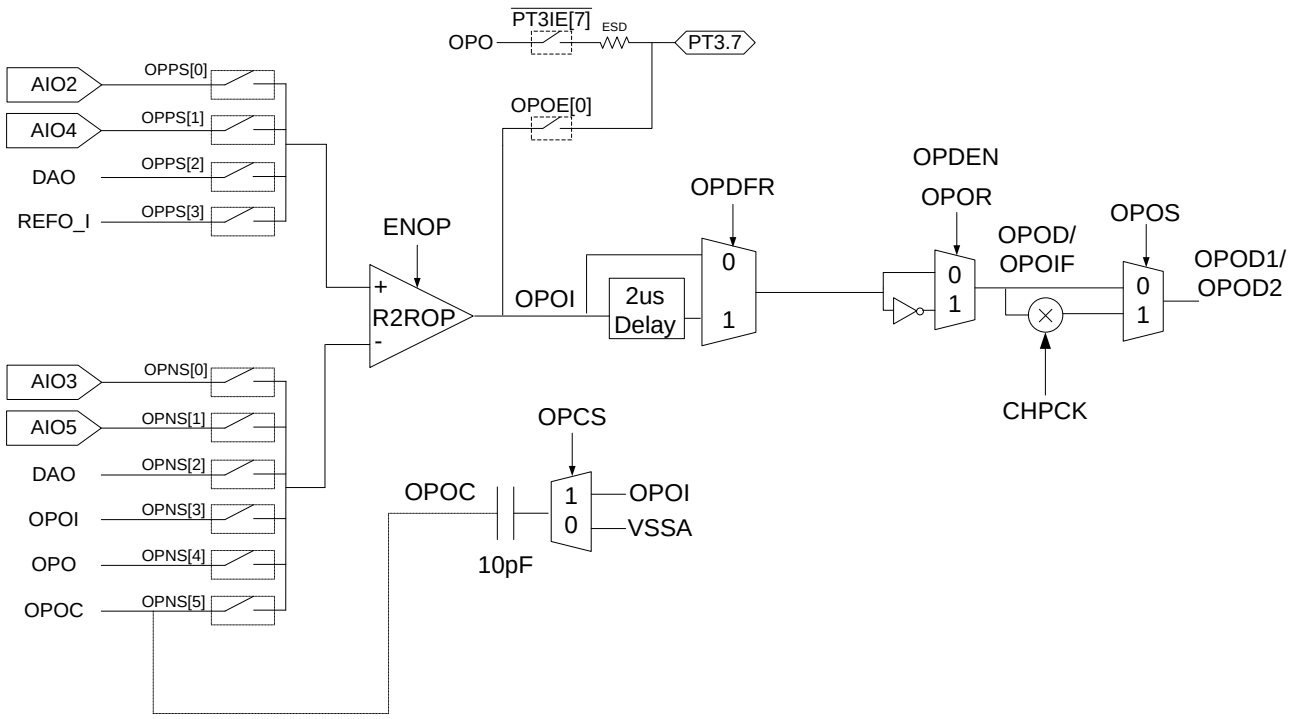


Fig 18-1 OPAMP function block diagram

18.1.1. Input channel independent selection switch

The input channel selector of the OPAMP is not a multiplexer but an independent selection switch. The positive input channel of the OPAMP is controlled by 4 switches: AIO 2, AIO 4, DAO, REFO_I, which can be respectively controlled by the control bits OPPS[0], OPPS[1], OPPS[2], OPPS[3], OPPS[4], OPPS[5] and OPPS[6]; besides. The negative input channel of the OPAMP is controlled by 8 switches: AIO3, AIO5, DAO OPOI, OPO, OPOC, AIO2 and AIO8, which can be respectively controlled by the control bits OPNS[0], OPNS[1], OPNS[2], OPNS[3], OPNS[4], OPNS[5], OPNS[6] and OPNS[7].

Operational amplifier OP AMP input channel selector is not a multiplexer, they are separate selector switch. Op amp's positive input channel, which is controlled by the four switches: AIO 2, AIO 4, DAO and REFO, through the control bit OPPS [0], OPPS [1], OPPS [2] and OPPS [3], respectively independent control. You can simultaneously select multiple positive input channels. Op amp's negative input channels, it is by 6 switch control: AIO3, AIO5, DAO OPOI, OPO and OPOC, through the control bit OPNS [0], OPNS [1], OPNS [2], OPNS [3], OPNS [4] and OPNS [5], each independently controlled. You can also select multiple negative input channels.

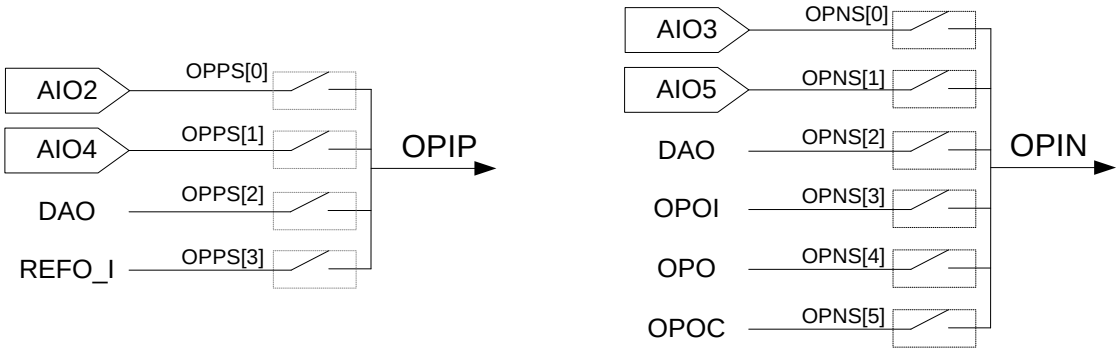


Figure 18-2 input channel configuration diagram

18.1.2. Built 10pF capacitance

The OPAMP has a built-in 10uF capacitor, which can have different functions under different configurations. The upper end of the capacitor is connected to the OPOC and can be connected to the negative input end; the switch is set by the control bit OPNS [5]; the lower end of the capacitor can be connected to the OPOI or VSSA, which can be set by the control bit OPCS[0]. There are two methods to sample the analog inputs. One is the open loop sampling technique, and the method requires the analog signals are inputted from the AIO 3 or AIO 5. The configuration of the channel switch is as follows: first, set the OPNS [5] as 1 and set the OPCS [0] as 1; then, set the OPNS [0] =1 (select the AIO3) or set the OPNS [1] =1 (select the AIO5); after the sampling is finished, set the OPNS [5] =0; the voltage data are stored in the capacitor corresponding to the VSSA. The other one is the close loop sampling technique: the method should enable the OPAMP first, which means setting the ENOP=1; then, enable the OPOI and OPO, which means setting the OPNS[4]=1 and OPNS[3]=1; afterward, the lower end of the capacitor is connected to the OPOI, which means the OPCS=1; enable the AIO2 and AIO4, which means setting the OPPS[0]=1 and OPPS[1]=1; after the sampling is finished, disable the OPOC, which means setting the OPNS[5]=0; the voltage data are also stored in the capacitor corresponding to the VSSA. The close loop method can store the offset of the OPAMP in the capacitor. Additionally, if the applications have the sensors with very high output impedance, the close loop sampling technique is a better choice. Finally, the lower end of the capacitor can be connected to the output end of the OPAMP, which means setting the OPCS=0. Meanwhile, the AIO3 and the AIO5 pins can be used to perform cumulative charge.

18.1.3. Comparator function

If the configuration of the OPAMP is set as the open loop function, the OPAMP can serve as comparator. The 1-bit binary codes can be outputted by the OPOD. If the positive input is higher than the negative input, the OPOD outputs 1; if the positive input is smaller than the negative input, the OPOD outputs 0. In order to prevent from the peak pulse interference, the outputs of the OPOD can further pass the 2us low-pass filter. If any peak pulse is smaller than 2us, the outputs of the comparator will not change. The outputs of the comparator can be changed by setting the control bit OPDR.

The output of the comparator can be also connected to the I/O pins; The PT3.0/PT3.1 is respectively the output pins of the OPO1/OPO2. The output results of the comparators can further be multiplied by the clock frequency of the charge pump (CHPCK) to output a high-frequency signal, which can serve as the LED driver.

18.1.4. Operation Description

The OPAMP is a more universal Rail-to-Rail OP amplifier. It can be used to deal with analog signals. When it is used as OP amplifier, the voltage of the VDDA is higher than 2.4V and the reference voltage of the BandGap should be enabled in advance. Within the effective input range, the OPAMP is Rail-to-Rail. However, in order to achieve better performance, it is suggested that the input common mode voltage range is between VSSA+0.1V~VDDA-0.1V. The input impedance of the OPAMP is higher than 1GΩ.

Initial Configuration:

- open VDDA, bandgap reference voltage, VDDA voltage is greater than 2.4V;
- Select OPO1 / OPO2 output IO pins, the corresponding IO pin to output mode, if not, you cannot configure;
- Select the positive input channel, the negative input channels, depending on the application configuration;
- configuration 2us low-pass filter; according to the actual need to set is turned on;
- configuration clock frequency charge pump, according to the actual need to set whether the flat rate should be multiplied;
- enable OPAMP analog output, even if we can OPOE;
- needed to enable the digital output OPAMP enable OPDEN;
- If the enable OPAMP digital output, according to actual needs, set the output results are inverted, set OPDR.
- OPAMP function is enabled, open an operational amplifier, even if we can ENOP;

18.2. Register Address

OPA Register Address	31	24	23	16	15	8	7	0
OPA base address + 0x00 (0X41900)	-		-		MASK0		REG0	
OPA base address + 0x04 (0X41904)	OPPSM		OPPS		OPNSM		OPNS	

-Reserved

18.3. Register Functions

18.3.1. OPAMP Control Register0

OPA Base Address + 0X00 (0X41900)									
Symbol	OPAMP0 (OPAMP Control Register 0)								
Bit	[31:16]								
Name	RSV								
RW	R-0								
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	OPOD	OPOS	OPDR	OPCS	OPDFR	OPDEN	OPOE	ENOP
RW	R0W-0	R-0	RW-0						

Bit	Name	Description	
Bit[7]	OPOD	OPAMP output in digital format. It is read only register	
		0	Negative input larger than positive input
		1	Positive input larger than negative input
Bit[6]	OPOS	OPO1/OPO2 with/without CPCLK multiplier selection	
		0	No CPCLK multiplier, OPO1/OPO2 is equal to OPOD
		1	With CPCLK multiplier, OPO1/OPO2 is OPOD multiply by CPCLK
Bit[5]	OPDR	OPAMP digital output with normal/inverse control	
		0	Normal
		1	Inverse
Bit[4]	OPCS	OPAMP feedback or sample capacitor connection	
		1	The capacitor is used as integrated capacitor. The bottom plate connects to OPOI
		0	The capacitor is used as sample capacitor. The bottom plate connects to VSSA
Bit[3]	OPDFR	OPAMP output with digital filter connection	
		0	Disable
		1	Enable(Pass as 2us deglitch)
Bit[2]	OPDEN	OPAMP digital output enable control	
		0	Disable
		1	Enable
Bit[1]	OPOE	OPAMP output enable	
		0	Disable
		1	Enable
Bit[0]	ENOP	OPAMP enable control.	
		0	Disable
		1	Enable

18.3.2. OPAMP Control Register1

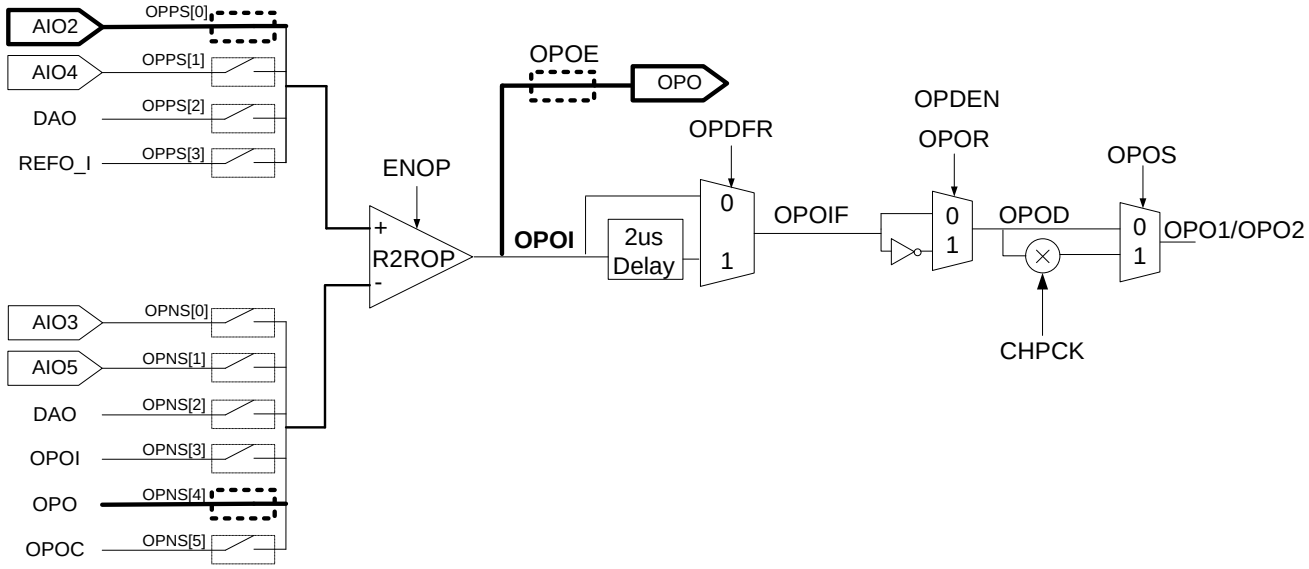
OPA Base Address + 0X04 (0X41904)			
Symbol	OPAMP1 (OPAMP Control Register 1)		
Bit	[31:24]	[23:20]	[19:16]
Name	MASK	-	OPPS[3:0]
RW	R0W-0	-	RW-0
Bit	[15:08]	[07:06]	[05:00]
Name	MASK	-	OPNS[5:0]
RW	R0W-0	-	RW-0

Bit	Name	Description	
Bit[19]	OPPS[3]	OPAMP positive input channel 3	
		0	Turn-off: High impendent
		1	Turn-on and connect to REFO_I
Bit[18]	OPPS[2]	OPAMP positive input channel 2	
		0	Turn-off: High impendent
		1	Turn-on and connect to DAO
Bit[17]	OPPS[1]	OPAMP positive input channel 1	
		0	Turn-off: High impendent
		1	Turn-on and connect to AIO4
Bit[16]	OPPS[0]	OPAMP positive input channel 0	
		0	Turn-off: High impendent
		1	Turn-on and connect to AIO2

Bit	Name	Description	
Bit[5]	OPNS[5]	OPAMP negative input channel 5	
		0	Turn-off: High impendent
		1	Turn-on and connect to OPC: Internal 10pF capacitor
Bit[4]	OPNS[4]	OPAMP negative input channel 4	
		0	Turn-off: High impendent
		1	Turn-on and connect to OPO: Internal OPAMP output
Bit[3]	OPNS[3]	OPAMP negative input channel 3	
		0	Turn-off: High impendent
		1	Turn-on and connect to OPOI: External OPAMP output
Bit[2]	OPNS[2]	OPAMP negative input channel 2	
		0	Turn-off: High impendent
		1	Turn-on and connect to DAO
Bit[1]	OPNS[1]	OPAMP negative input channel 1	
		0	Turn-off: High impendent
		1	Turn-on and connect to AIO5
Bit[0]	OPNS[0]	OPAMP negative input channel 0	
		0	Turn-off: High impendent
		1	Turn-on and connect to AIO3

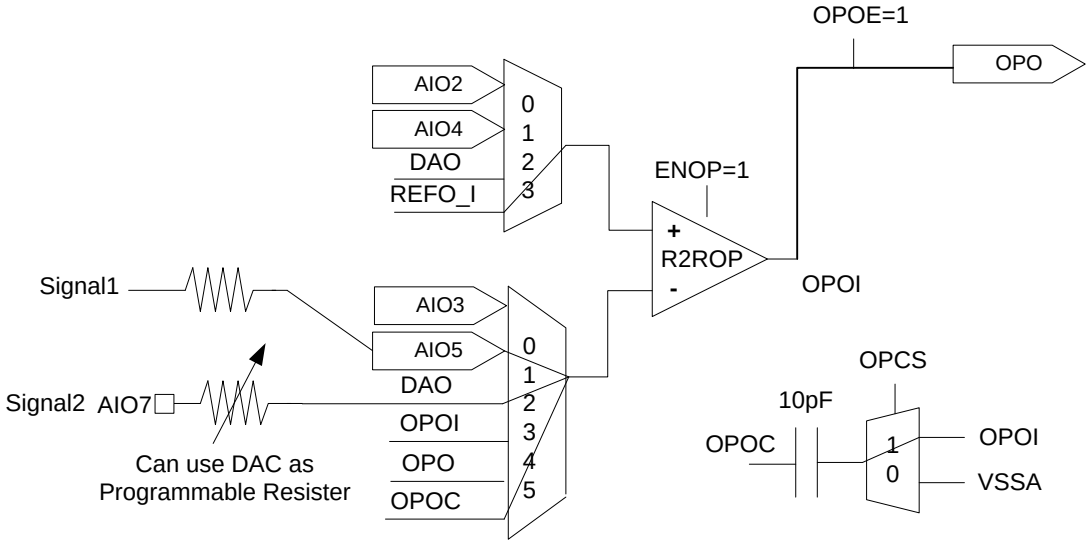
Application Circuit 01

Use as a unit gain buffer



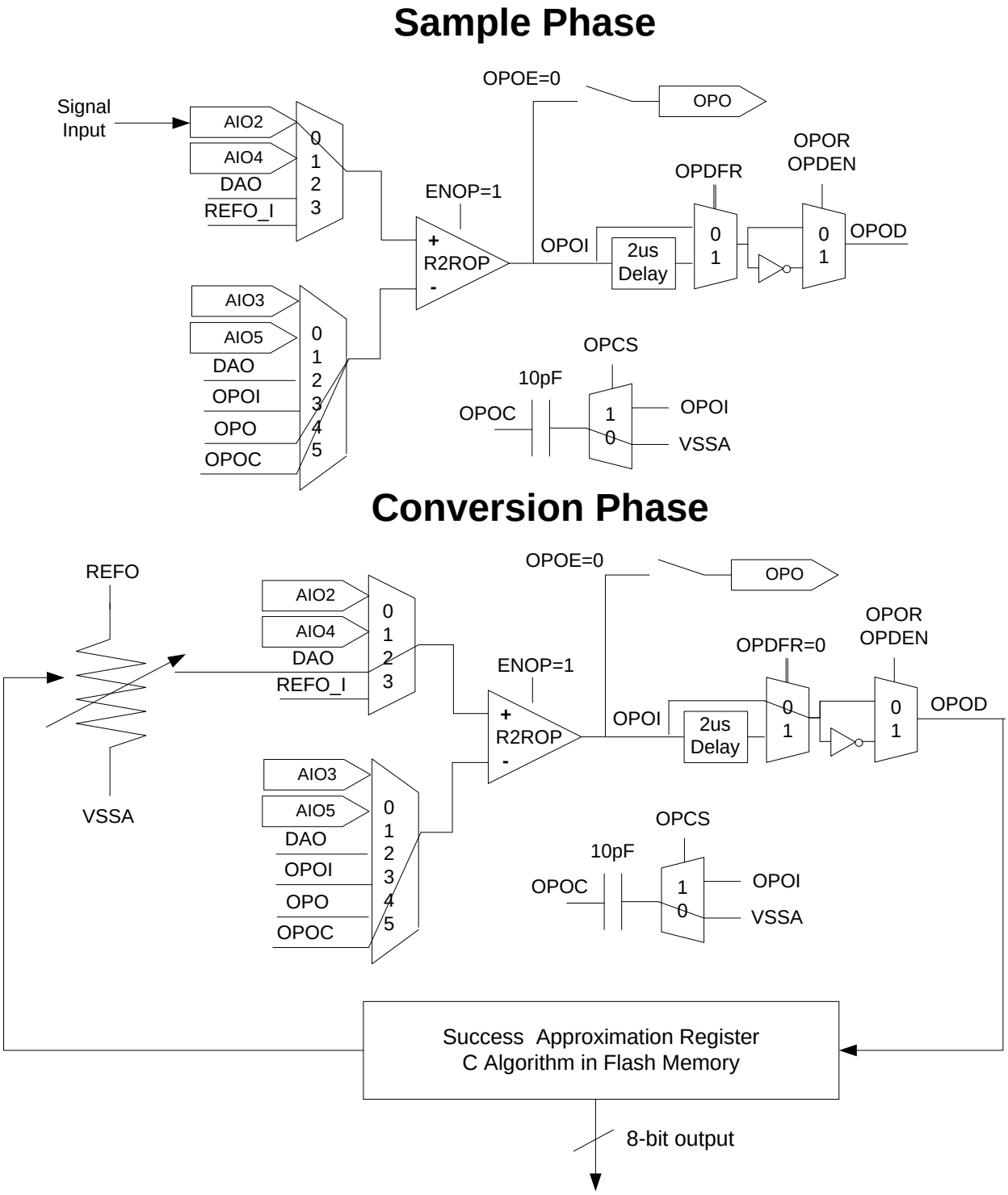
Application Circuit 02

Use as an Integrator



Application Circuit 03

Use as a 8-bit SAR ADC



19. 8-BIT RESISTANCE LADDERS Network

19.1. Introduction

The chip has an embedded 8-bit Resistance Ladder converter DAC. The DAC module is an 8-bit D/A converter, which is composed of a step resistor with absolute monotonicity.

Features of 8-bit Resistance Ladder include:

(1) 8-bit monotonic output

(2) Internal or external reference programmable selection

(3) It can serve as programmable resistor.

Operation of 8-bit Resistance Ladder:

When the ENDA is 0, the 8-bit Resistance Ladder will be disabled and no power consumption will be incurred. The Vrefp multiplexer is disabled and becomes a high impedance node. However, the Vrefn is still enabled, and connects to one of the sources. If the DAOE is set as 1, it will become a programmable resistor able to mark the ohm values.

8-bit Resistance Ladder output:

The DAO can generate the output voltages according to the data stored in the DABIT and VDA_Vrefp – VDA_Vrefn.

DABIT is based on straight binary system; the following figure is the transmission function diagram.

$$DAO = (V_{DAC\_Vrefp} - V_{DAC\_Vrefn}) \times \frac{DAbit\_in}{256} + V_{DAC\_Vrefn}$$

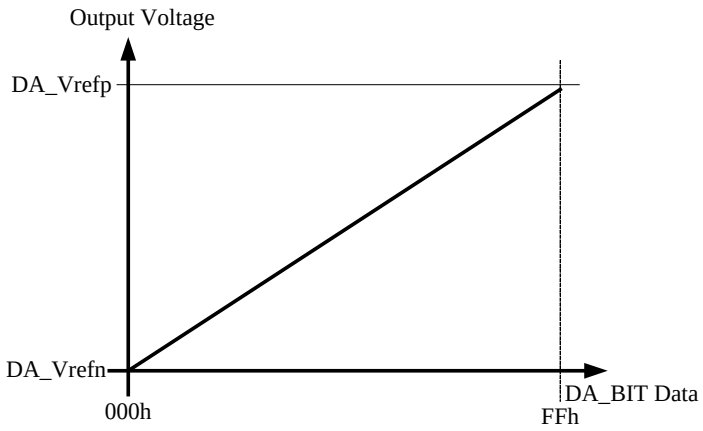


Fig 19-1 8-bit resistor ladders transfer function

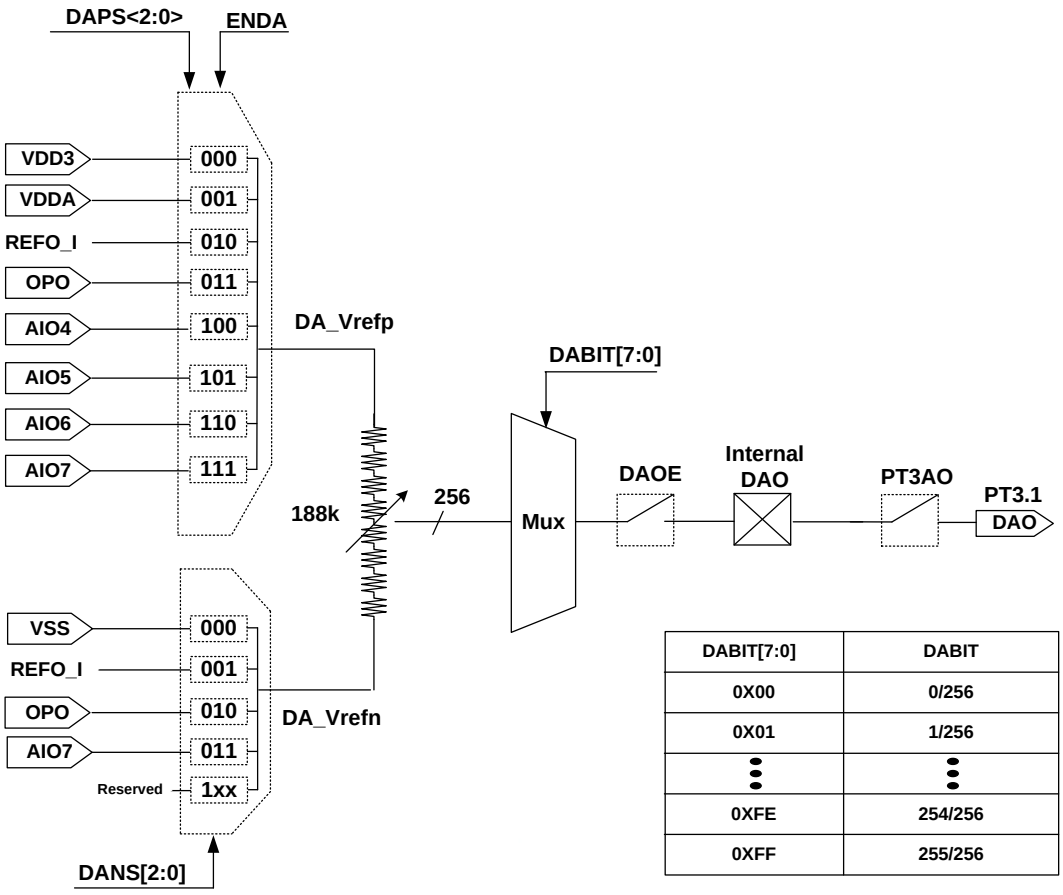


Figure 19-2 8 bit Resistance Ladder function block diagram

19.2. Register Address

8bit Resistance Ladder Register Address	31 24	23 16	15 8	7 0
8bit Resistance Ladder base address + 0x00 (0X41700)	-	-	MASK0	REG0
8bit Resistance Ladder base address + 0x04 (0X41704)	-	-	MASK1	REG1

-Reserved

19.3. Register Functions

19.3.1. 8-BIT RESISTANCE LADDERS Control Register0

8bit Resistance Ladder Base Address + 0X00 (0X41700)						
Symbol	8bit Resistance Ladder0 (8bit Resistance Ladder Control Register 0)					
Bit	[31:16]					
Name	RSV					
RW	R-0					
Bit	[15:8]	[7:6]	[5:4]	[3:2]	[1]	[0]
Name	MASK	-	DAPS[1:0]	DANS1:0]	DAOE	ENDA
RW	R0W-0	-	RW-0			

Bit	Name	Description	
Bit[5~4]	DAPS	8-BIT RESISTANCE LADDERS positive reference input selection	
		000	VDD3V
		001	VDDA
		010	REFO_I
		011	OPO
		100	AIO6 (Note1)
Bit[3~2]	DANS	8-BIT RESISTANCE LADDERS negative reference input selection	
		00	VSS
		01	REFO_I
		10	OPO
		11	AIO7
Bit[1]	DAOE	8bit Resistance Ladder output enables control.	
		0	OFF, high impendence
		1	ON, 8-BIT RESISTANCE LADDERS output
Bit[0]	ENDA	8bit Resistance Ladder enable control	
		0	Disable (turn off positive input multiplexer)
		1	Enable

(Note 1)

adc_04=0X1000FF00; //ADC 0X41104 Bit_28 Set 1 for AIO6 8-BIT RESISTANCE LADDERS P+ Useable

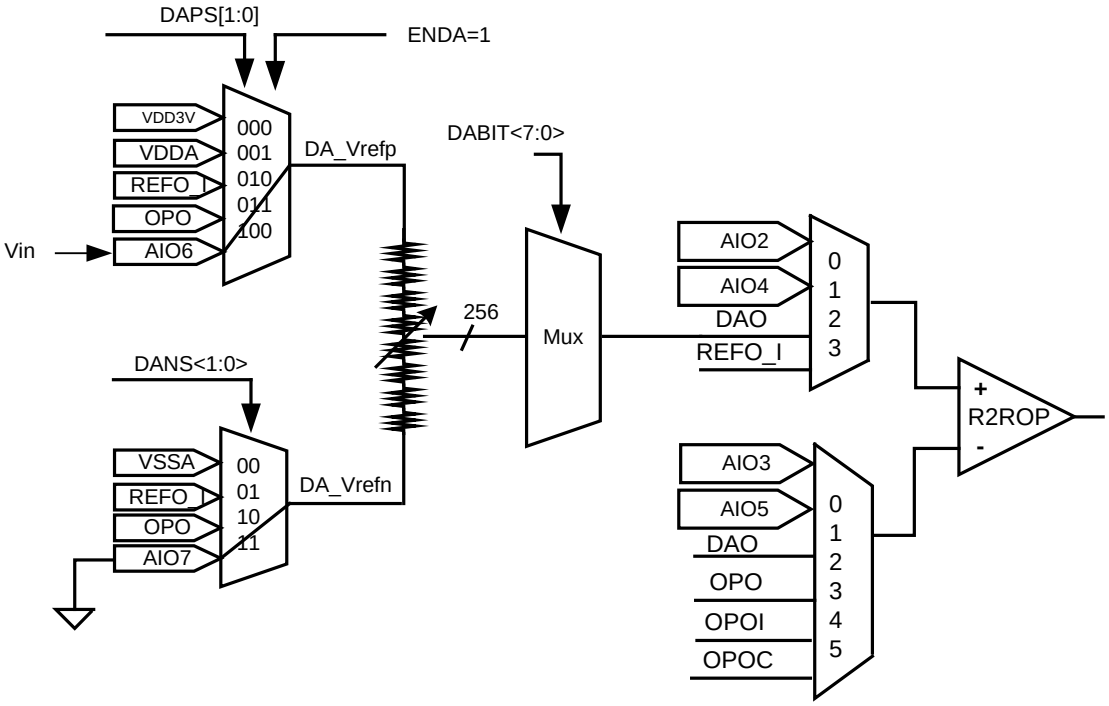
19.3.2. 8-BIT RESISTANCE LADDERS Control Register1

8bit Resistance Ladder Base Address + 0X00 (0X41704)		
Symbol	8bit Resistance Ladder 1(8bit Resistance Ladder Control Register 1)	
Bit	[31:16]	
Name	RSV	
RW	R-0	
Bit	[15:8]	[7:0]
Name	MASK	DABIT[7:0]
RW	R0W-0	RW-0

Bit	Name	Description
Bit[7~0]	DABIT	DABIT [7:0] buffer from MSB to LSB

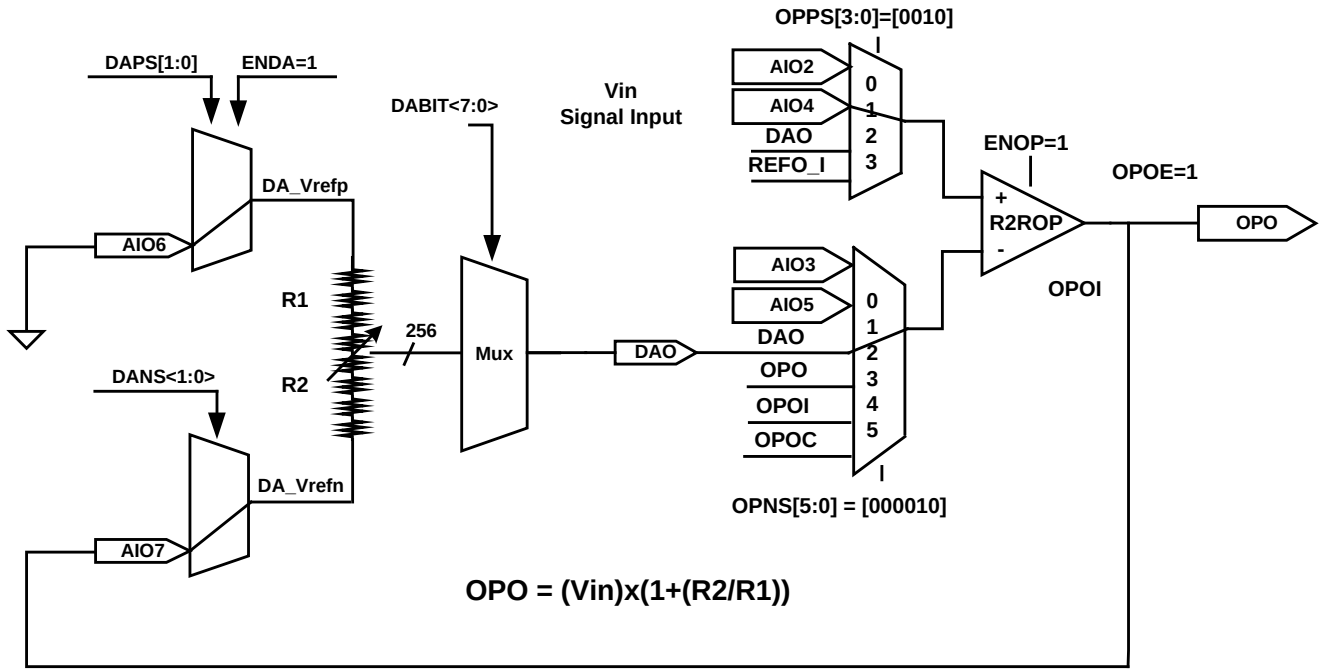
Application circuit function 01

Use DAO Output



Application circuit function 02

Use as Programmable Gain Amplifier



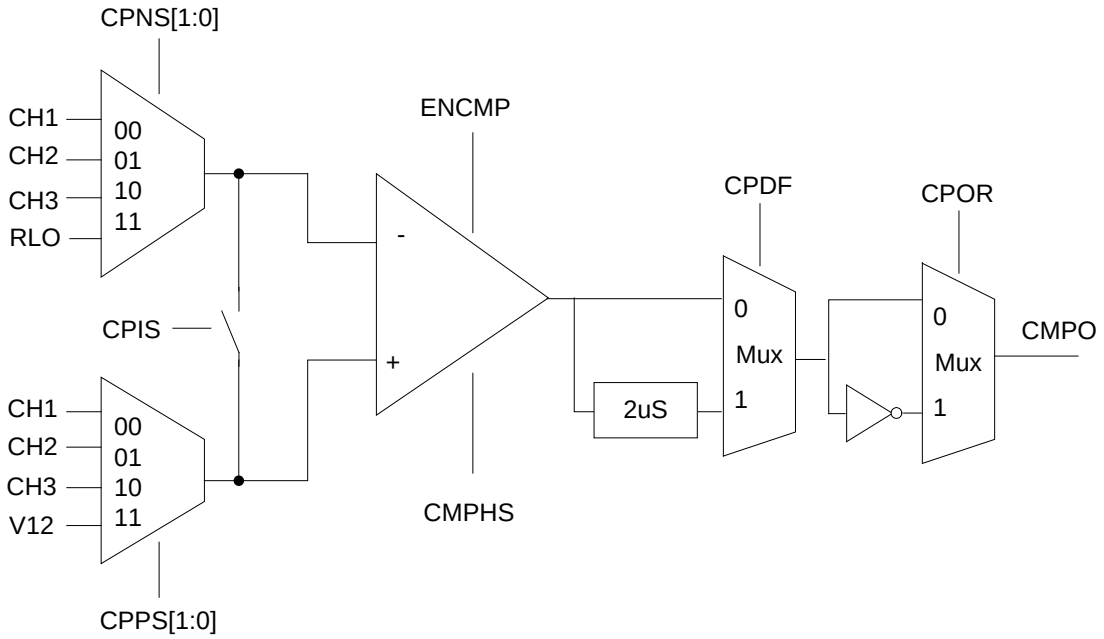
20. MULTIPLE FUNCTION COMPARATOR Network

20.1. Introduction

The chip has an embedded low-power, Rail-to-Rail multi-function comparator CMP for the comparing analog signals. It has the interrupt function; when the comparison result generates, the interrupt signal also generates; and it can increase the operability for users. It has different configuration settings for different applications.

Features of CMP include:

1. Rail-to-Rail input range
2. Low operating current
3. 2us peak pulse filter
4. Built-in 16 nodes 4-bit step resistor DAC with different comparison sets.
5. Change and discharge paths measured by touch buttons.
6. Interrupt signals can be generated, which belong to the interrupt vector HW3.



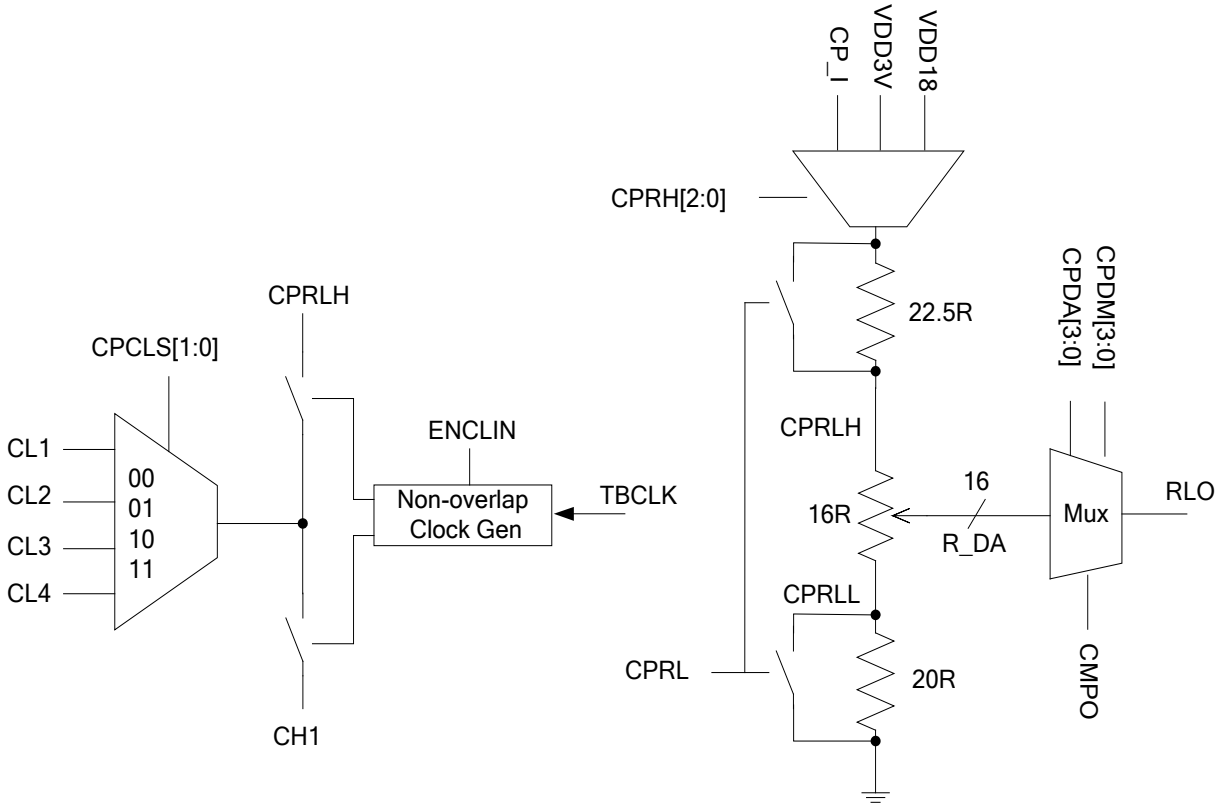
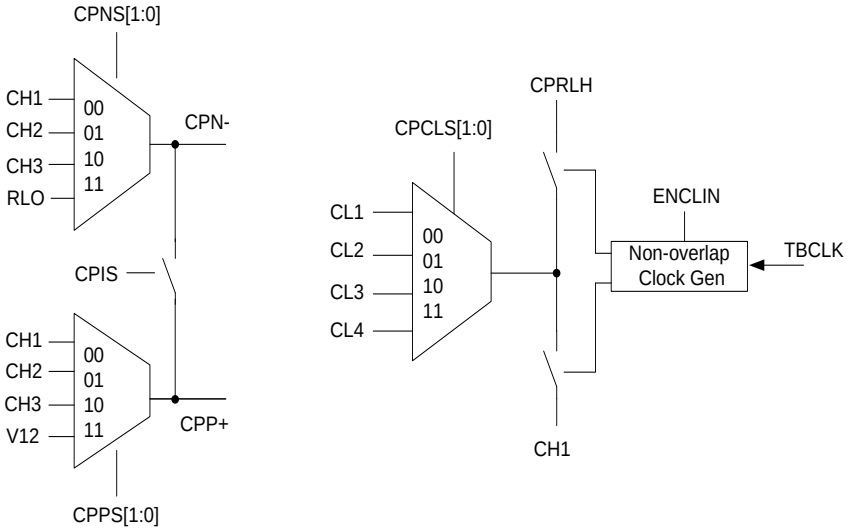


FIG. 20-1 CMP network diagram

20.1.1. Multiplexing input channel selector

The input channel of the comparator is composed two parts; one is the input channel of the comparator, which can be set by the controller CPPS [1:0]/CPNS [1:0] to respectively set the positive input channel and the negative input channel of the comparator; the other one is the touch button input channel, which can be set by the controller CPCLS [2:0]. Via proper configuration and the combination of the input channels of the two parts, the applications of the touch button can be realized. When using the comparator, the user can set the control bit CPIS as <1> to realize the short circuit between the positive input end and the negative input end; on the contrary, if the CPIS is set as <0>, the short-circuit will not be realized.



20.1.2. Built-in multi-node resistor and resistor node selection

The comparator has a built-in multi-node resistor, and the resistor includes three parts: 22.5R, 16R and 20R. The 16R resistor is connected to a 16-stage resistor node selector; the selector divides the 16R resistor into 16 nodes, which can be set by the controllers CPDA [3:0] and CPDM [3:0] to select different resistor nodes to output different voltages to the input channel RLO of the comparator. If the control bits CPRLH and CPRLL are set as <1>, the short circuit between the 22.5R resistor and 20R resistor can be achieved, which can adjust the resistor node voltage. The voltage sources of the multi-node resistor are VDD18/VDD3V/CP_I, and the controller CPRH [1:0] can be used to select different voltage sources to increase the output range of the node voltage.

The hysteresis controller CPDM [3:0] is linked up with the node selector CPDA [3:0]; each bit of the hysteresis controller CPDM [3:0] is corresponding to the control of the enablement and disablement of the each bit of the controller CPDA [3:0] respectively. When the corresponding bit of the hysteresis controller CPDM[3:0] is set as <1>, the hysteresis function of the corresponding bit of the node controller CPDA[3:0] will be enabled and the status of the bit is consistent with the output status of the comparator; that is CPDA[X]=CMPO. In this way, the node selector will be switched between the two nodes.

'u' means no change.

CPDM[3:0]	CMPO Output status	CPDA[3:0] Hysteresis switch period	CPDM[3:0]	CMPO Output status	CPDA[3:0] Hysteresis switch period
0000	0	uuuu	1000	0	0uuu
	1	uuuu		1	1uuu

0001	0	uuu0	1001	0	0uu0
	1	uuu1		1	1uu1
0010	0	uu0u	1010	0	0u0u
	1	uu1u		1	1u1u
0011	0	uu00	1011	0	0u00
	1	uu11		1	1u11
0100	0	u0uu	1100	0	00uu
	1	u1uu		1	11uu
0101	0	u0u0	1101	0	00u0
	1	u1u1		1	11u1
0110	0	u00u	1110	0	000u
	1	u11u		1	111u
0111	0	u000	1111	0	0000
	1	u111		1	1111

Table 20-1 Hysteresis control CPDM [3:0] configuration and values

20.1.3. Comparator output

The output of the comparator is digital output, and it will reach the IO pin PT1.7; therefore, the output of the comparator should set the IO to serve as the output mode. The output of the comparator can be set to pass through the 2us low-pass filter to eliminate the peak pulse interference. If the control bit CPDF is set as <1>, the output of the comparator will pass through the 2us low-pass filter; if the control bit CPDF is set as <0>, it will not pass through the filter. The polarity of the comparator can be set by the control bit CPOR. If the CPOR is set as <1>, the output of the comparator will be opposite in phase; if the CPOR is set as <0>, the output of the comparator will be normal.

20.1.4. Application of touch button

The comparator has a special function: measuring the touch button. The major principle is to set the comparison voltage via the multi-node resistor and then input which into the RLO; the multi-node resistor provides voltage to charge the touch button and then the charges of the touch button charges the external reference capacitor of the negative input channel CH1; next, the TMB counts the charge time that the voltage of the CH1 is higher than the voltage of the RLO and then determine the status that the touch button is touched or not according to the charge time.

Two switches need to be used to control the charging of the corresponding touch button and the charging of the touch button to the reference capacitor; besides, if one of the switches is close, the other one must be open. The comparator has a built-in non-overlap

controller to control the switches to ensure one of them is close and the other one is open. The operating frequency of the non-overlap controller is provided by the operating clock of the TMB. Therefore, if the function should be used, it is necessary to enable the counting function of the TMB and clear the counter register of the TMB.

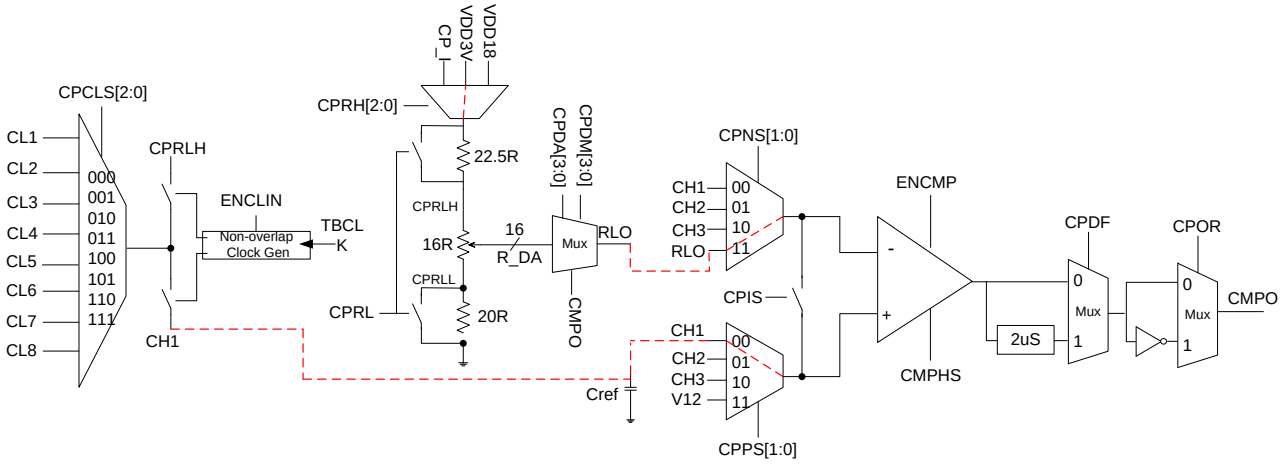


FIG. 20-4 Touch button connection diagram (One possible configuration)

20.1.5. Comparator operation initialization

The main function of the comparator is to compare the input signals; however, different modular combinations need different configurations to achieve different applications.

As a simple signal comparator:

1. Set the operating mode of the CMP to be low-power or normal.
2. Select the input channel, including the positive input channel, negative input channel;
3. If the RLO is selected as the positive input channel, the reference voltage source and the voltage node of the multi-node resistor should be set;
4. Enable the output function of the comparator;
5. Set whether the output passes through the low-pass filter and the output is opposite in phase;
6. If the CMP comparison interrupt vector is used, the interrupt function of the comparator should be enabled;
7. Enable the function of the comparator.

Touch button application initialization:

1. Set the TMB: set the operating mode of the TMB is mode 0, set the counting-trigger source is CMPO, set the TMB operating clock and overflow;
2. Set the CMP operating mode to be low-power or normal operating mode.
3. Select the input channel, including the positive input channel, negative input channel; the positive input channel is CH1 and the negative input channel is RLO;

4. Set the reference voltage source and the voltage node of the multi-mode resistor; and the resistor short-circuit switch of the resistor;
5. Enable the output function of the comparator;
6. Set whether the output passes through the low-pass filter and the output is opposite in phase;
7. If the CMP comparison interrupt vector is used, the interrupt function of the comparator should be enabled;
8. Enable the function of the comparator;
9. Release the charges of the touch button and the reference capacitor before charging;
10. Disable the non-overlap controller first, and then disable the reference voltage source of the non-overlap controller, and enable the resistor short-circuit switch of the resistor;
11. Enable the input end short-circuit switch; discharge from the reference capacitor of the CH1to ground via the resistor;
12. Set the corresponding IO pin of the touch button as the output mode and the output status is 0 to discharge from the touch button to ground;
13. Then enable the charging function;
14. Disconnect the input end short-circuit switch, disconnect the resistor short-circuit of the resistor and enable the reference voltage source of the resistor;
15. Disable the IO output mode of the touch button;
16. Clear the counter register of the TMB;
17. Enable the non-overlap function and select the touch button to be charged;
18. Read the counting value of the TMB after the charging is finished.

20.2. Register Address

CMP Register Address	31	24	23	16	15	8	7	0
CMP base address + 0x00 (0X41800)	-		REG0		MASK1		REG1	
CMP base address + 0x04 (0X41804)	MASK2		REG2		MASK3		REG3	

-Reserved

20.3. Register Functions

20.3.1. CMP Control Register0

CMP Base Address + 0X00 (0X41800)					
Symbol	CMPCR0 (CMP Control Register 0)				
Bit	[31:17]				[16]
Name	-				CMPO
RW	-				R-0
Bit	[15:08]	[7:6]	[5:4]	[3]	[2:0]
Name	MASK	CPPS[1:0]	CPNS[1:0]	CPRL	CPRH[2:0]
RW	R0W-0	RW-0			

Bit	Name	Description	
Bit[16]	CMPO	Comparator digital output	
		0	Negative input > positive input
		1	Positive input > negative input

Bit	Name	Description	
Bit[7~6]	CPPS	Comparator positive reference input selection	
		00	CH1
		01	CH2
		10	CH3
		11	V12
Bit[5~4]	CPNS	Comparator negative reference input selection	
		00	CH1
		01	CH2
		10	CH3
		11	RLO
Bit[3]	CPRL	Comparator resistor ladder short switch	
		0	Short-circuit switch opens. (Open=OFF)
		1	Short-circuit switch closes. (Closed=ON)
Bit[2~0]	CPRH	Comparator resistor ladder high voltage selection	
		000	OFF (high impendent)
		001	CP_I (charge pump output voltage)
		010	VDD3V (system power voltage)
		100	VDD (1.8V digital power voltage)

20.3.2. CMP Control Register1

CMP Base Address + 0X04 (0X41804)								
Symbol	CMPCR1 (CMP Control Register 1)							
Bit	[31:24]	[23:20]			[19:16]			
Name	MASK	CPDM[3:0]			CPDA[3:0]			
RW	R0W-0	RW-0						
Bit	[15:08]	[7]	[6]	[5]	[4]	[3:2]	[1]	[0]
Name	MASK	CPOR	CMPHS	CPIS	ENCLIN	CPCLS[1:0]	CPDF	ENCMP
RW	R0W-0	RW-0						

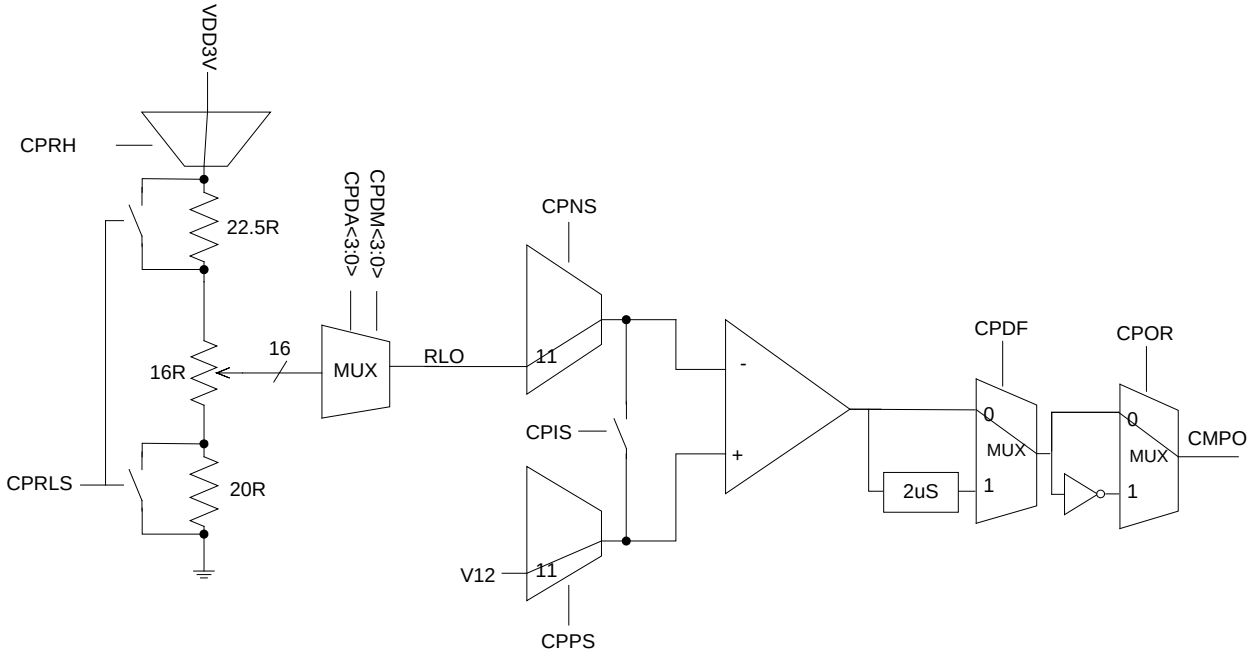
Bit	Name	Description	
Bit[23]	CPDM[3]	Determine if CPDA[3] is used for hysteresis and control by CMPO	
		0	Disable
		1	Enable, CPDA[3]=CMPO

Bit[22]	CPDM[2]	Determine if CPDA[2] is used for hysteresis and control by CMPO	
		0	Disable
		1	Enable, CPDA[2]=CMPO
Bit[21]	CPDM[1]	Determine if CPDA[1] is used for hysteresis and control by CMPO	
		0	Disable
		1	Enable, CPDA[1]=CMPO
Bit[20]	CPDM[0]	Determine if CPDA[0] is used for hysteresis and control by CMPO	
		0	Disable
		1	Enable, CPDA[0]=CMPO
Bit[19~16]	CPDA	Comparator internal resistor ladder control.	
		0000	0
		0001	1/16 (CPRLH – CPRLL)
		0010	2/16 (CPRLH – CPRLL)
		0011	3/16 (CPRLH – CPRLL)
		0100	4/16 (CPRLH – CPRLL)
		0101	5/16 (CPRLH – CPRLL)
		0110	6/16 (CPRLH – CPRLL)
		0111	7/16 (CPRLH – CPRLL)
		1000	8/16 (CPRLH – CPRLL)
		1001	9/16 (CPRLH – CPRLL)
		1010	10/16 (CPRLH – CPRLL)
		1011	11/16 (CPRLH – CPRLL)
		1100	12/16 (CPRLH – CPRLL)
		1101	13/16 (CPRLH – CPRLL)
		1110	14/16 (CPRLH – CPRLL)
		1111	15/16 (CPRLH – CPRLL)

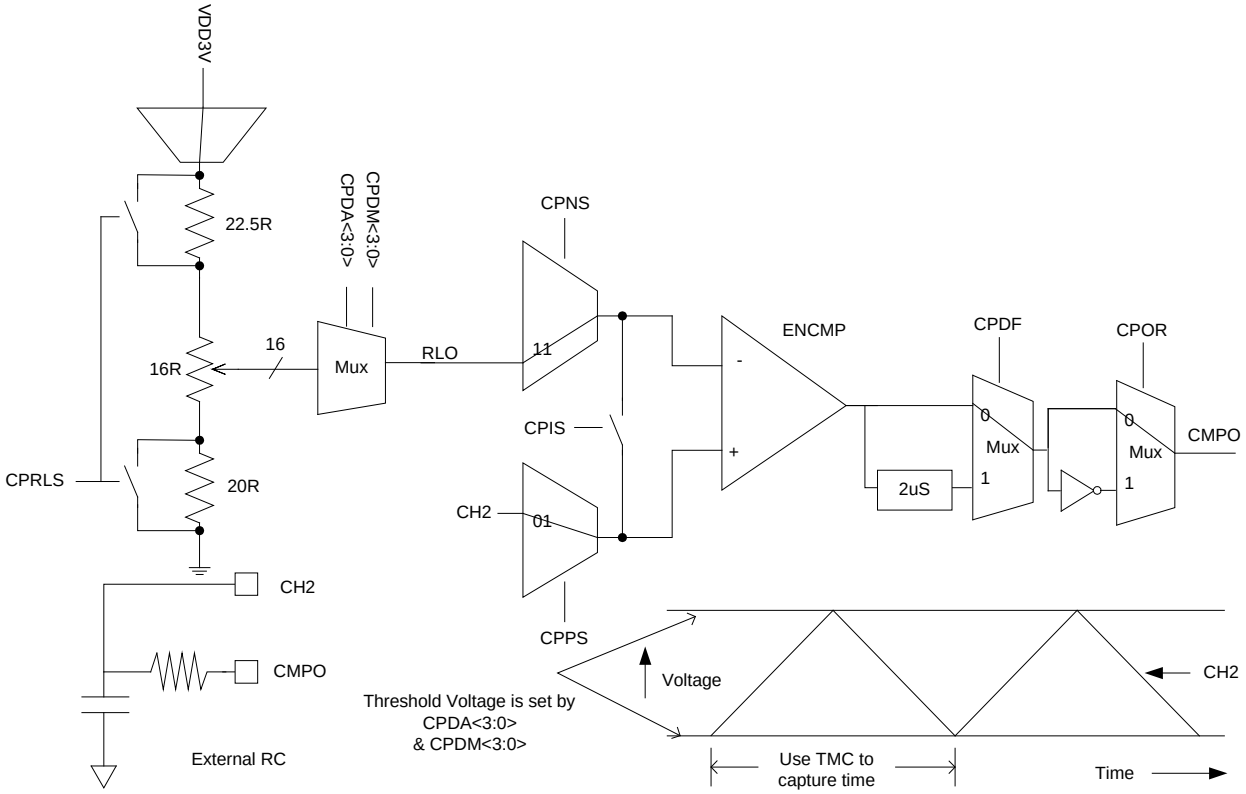
Bit	Name	Description	
Bit[7]	CPOR	Comparator digital output inverse control	
		0	Normal output
		1	Inversed output
Bit[6]	CMPHS	Comparator high speed mode enable	
		0	Low power mode
		1	High speed mode
Bit[5]	CPIS	Comparator input short switch	
		0	Open = OFF
		1	Close = ON
Bit[4]	ENCLIN	Enable the non-over lapping control. The input source is TBCLK	
		0	Disable, both switches are off
		1	Enable. Use TBCLK to generator non-over lapping control
Bit[3~2]	CPCLS	Comparator positive reference input selection	
		00	CL1
		01	CL2
		10	CL3
		11	CL4
Bit[1]	CPDF	Comparator output deglitch filter	
		0	Disable; the output of the comparator does not pass through the 2us low-pass filter.
		1	Enable; the output of the comparator passes through the 2us low-pass filter.
Bit[0]	ENCMP	Comparator enables control.	
		0	Disable (output 0)
		1	Enable

20.4. System example application circuit

20.4.1. CMP serves as low voltage detector



20.4.2. CMP is used to measure capacitors



21. SPI Management

21.1. Introduction

The HY16F18 series has a serial peripheral interface (SPI).
The SPI uses the synchronous serial data communication protocol, and works under the full-duplex mode.
It communicates with the 4-wire bidirectional interface and can work under the master/slave mode.
Under the master mode, it has several configurations to execute different client devices.

Functions:

(1) Full-duplex synchronous transmission.
(2) Support master mode operation or slave mode operation.
(3) Support transmitting MSB first or transmitting LSB first.
(4) The transmission frame is 4~32-bit and can provide programmable bit length setting.
(5) High-speed SPI bus busy-status flag.
(6) Programmable clock pulse rate.
(7) Support high/low potential slave end selection.
(8) Programmable clock polarity and phase

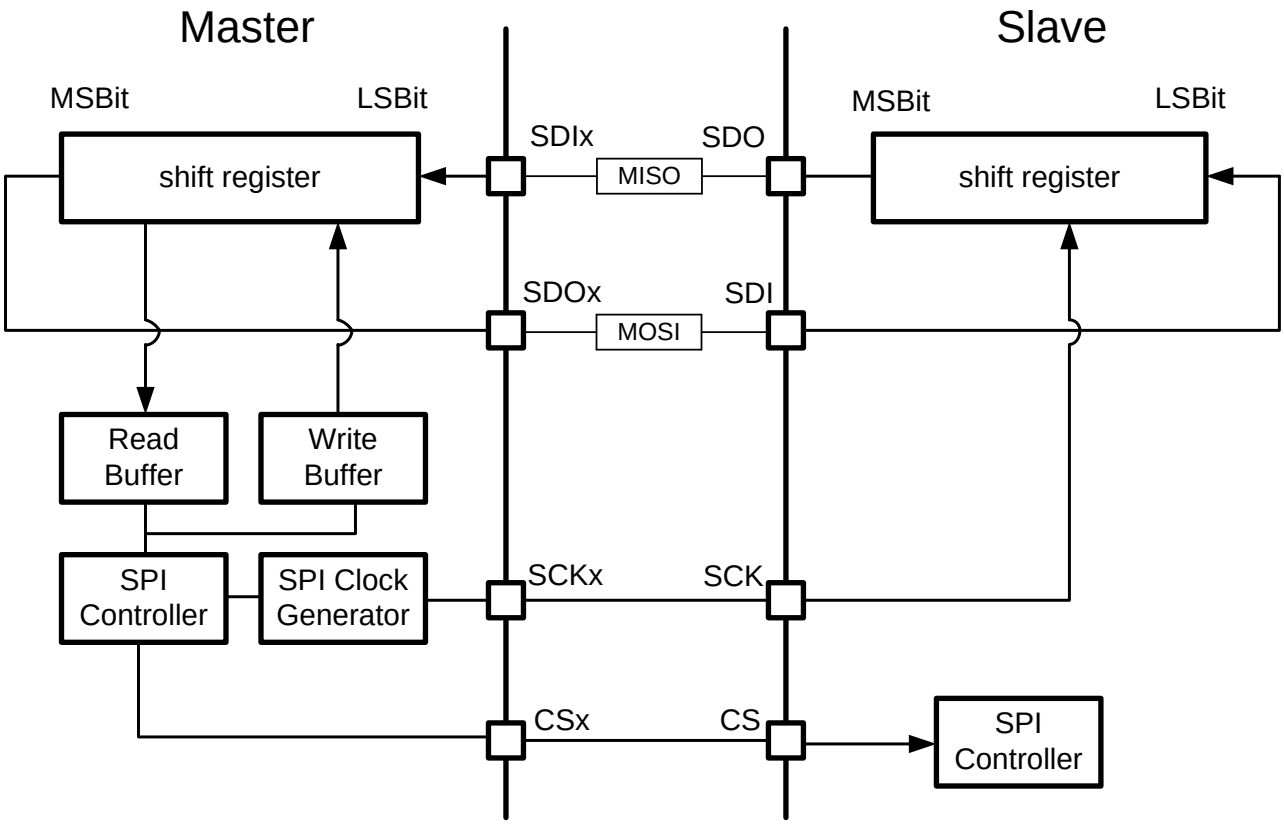


FIG. 21-1 Serial communication SPI structure diagram

The MISO pins are the input of the master device and the output of the slave device. The MOSI pins are the output of the master device and the input of the slave device. The SCK pin is from the serial communication clock output of the master device. The CS pin is from the chip selection of the master device to enable the SPI communication of the slave device. The MOSI/MISO/SCK/CS pins of the master device or the salve device are connected together to execute tasks.

The communication is always enabled by the master device. The master device transmits data to the slave device via the MOSI pins, and the slave device replies to the master device via the MISO pins. So, that is full duplex communication; the data input and output synchronously and use the same clock source.

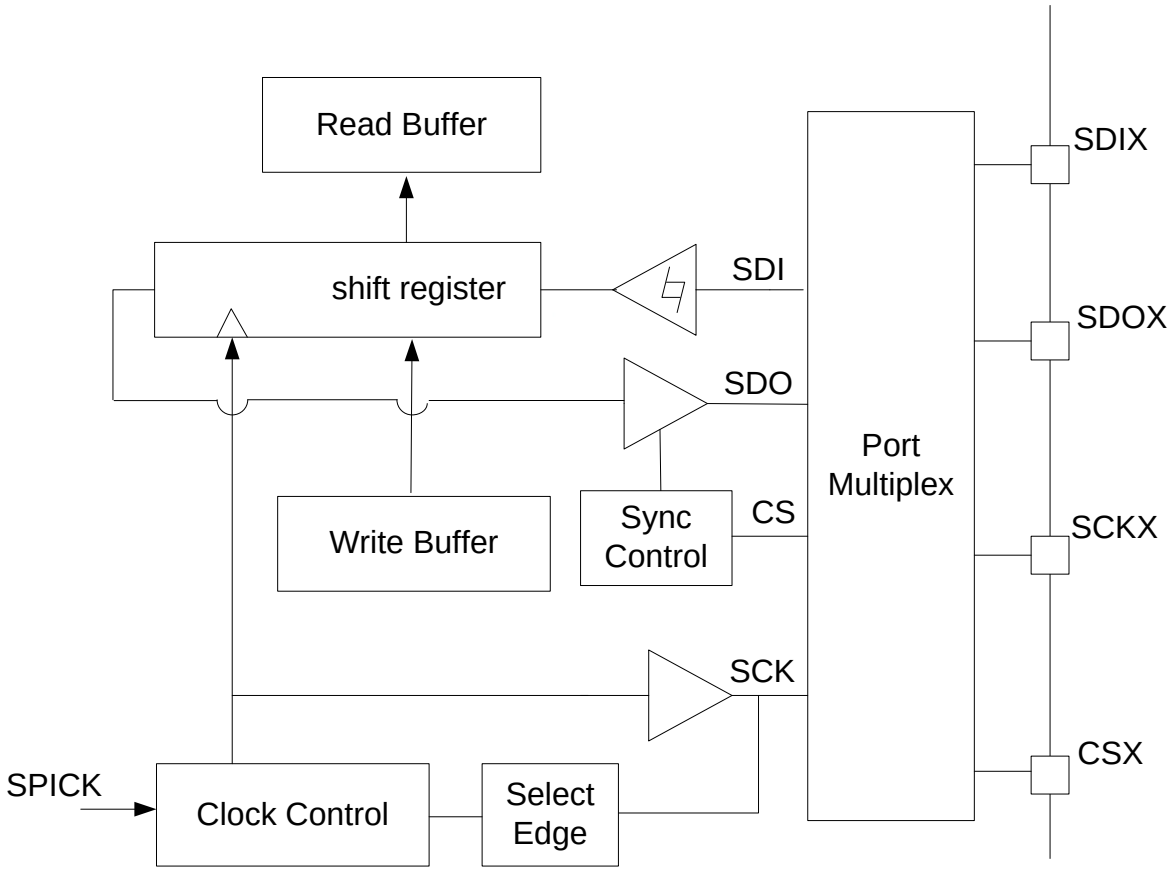


FIG. 21-2 SPI IO pin diagram

Function description: I/O pin setting:

The SPI pins can be programmed for different I/O pins.

Clock phase and clock polarity:

Four different clock types can be formed by software, and controlled by the CPOL and CPHA registers.

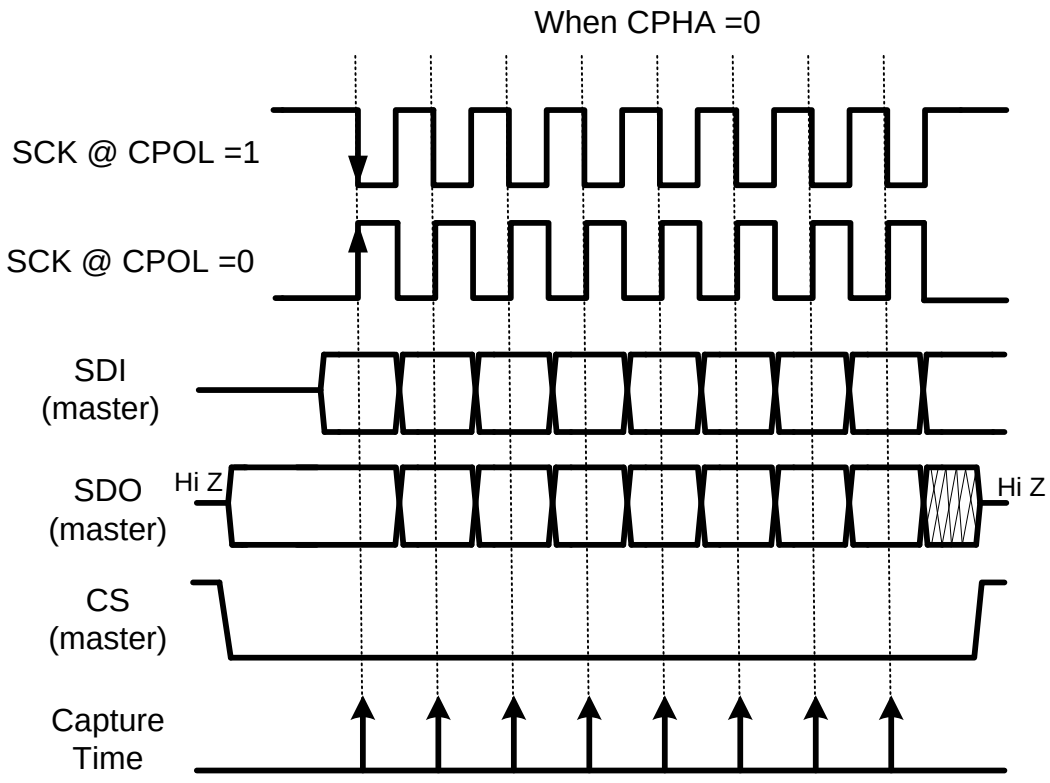
The CPOL (clock polarity) is to control the stable status value of the clock without any data transmission.

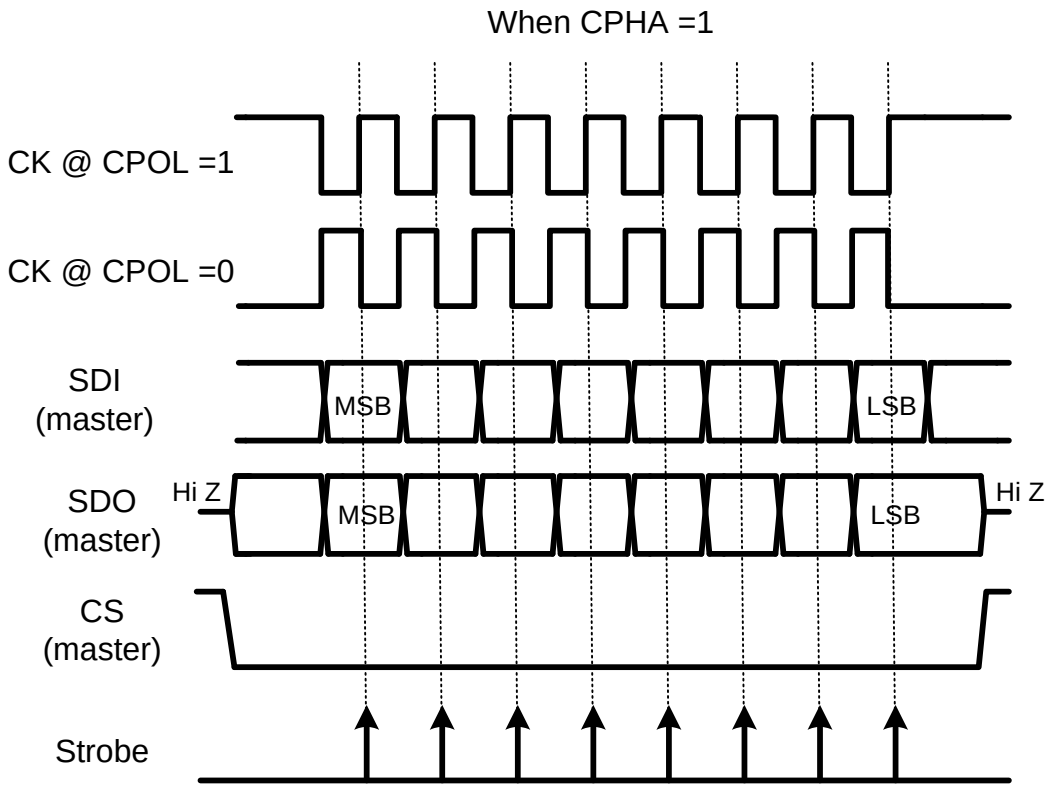
It can be used in the master mode and the slave mode. If the CPOL is 1(high potential), the SCK is 1 when the SPI is under the idle mode. On the other hand, if the CPOL is 0(low potential), the SCK is 0 when the SPI is under the idle mode (low potential).

The CPHA (clock phase) controls the capturing of the data clock edge of the SCK. If the CPHA is 1(high potential), the second clock edge of the SCK pin (If the CPOL is 1, it is the rising edge; if the CPOL is 0, it is the falling edge.) will capture the data of the MSB.

The data will be locked at the second clock edge of the SCK. On the other hand, if the CPHA is 0 (low potential), the first clock edge of the SCK pin (If the CPOL is 1, it is the falling edge; if the CPOL is 0, it is the rising edge.) will capture the data of the MSB.

The data will be locked at the first clock edge of the SCK. Therefore, the combination of the CPOL and the CPHA can control the data capturing and outputs of the clock edges.





Note: SPI Interface when working in Master Mode, SCK operating frequency SPICK / 2.

SPI Control Register 1:

(BL control bit) Data frame format:

The bit length of the transaction word for transmission and reception can be defined in the BL 0x40F04 [4:0]. The lowest bit length is 4 bits, and the highest bit length is 32 bits. The transmission format of the data of the shift register can be to transmit the MSB first or transmit the LSB first, which is defined by the LBF. If the LBF is 0, the data transmission format is to transmit the MSB of the shift register first. Then, the second MSB is transmitted; finally, the LSB is transmitted. If the LBF is 1, the data transmission format is to transmit the LSB of the shift register first.

(CSL control bit) Select the level from the slave device chip:

The CS pin can be defined as 0 or 1 (low potential or high potential) to enable the slave device. That is controlled by the CSL register. If the CSL of the master device is 0, the CS pin will output 0 (low potential) to enable the slave device. On the other hand, if the CSL is 1, the CS pin will output 1 (high potential) to enable the slave device. If the CSL of the slave device is 0, the slave device will be enabled after receiving the input 0 (low

potential) of the CS. On the other hand, if the CSL of the slave device is 1, the slave device will be enabled after receiving the input 1 (high potential) of the CS.
Note: When SPI Interface operates in 4-wire Master mode, CS pin control is a semi-automatic control of the way, For example, when CSL is set to <1>, CS pin will be pulled low, When the SPI Master to write data to the terminal when the SPI Device, CS pin will be automatically pulled to high potential, After the data transfer is complete, will automatically revert to low potential, that is, when Idle Low, Active is High.

(CSO control bit)
This control bit is only 3-wire SPI Slave mode will be used. This pin functions as Chip internal wake-up (CS) signal simulator control. SPI Slave before receiving data first set the CSO = <0> to receive data correctly. When data reception is completed, to read previous RXB Buffer, Must be set CSO = <1>, the received data can be read correctly. After reading the data need to set CSO = <0> ready to receive the next data. When the SPI Slave to return data to SPI Master, Also set CSO = <1>, Then transfers data written TXB Buffer, and then set the CSO = <0>, so that it can transfer data to the Master.

Note: When using a 3-wire SPI transfer if SPI Slave side has to complete initialization, and set CSO = 0, At this point if SPI Master before doing initialization, SPI Slave will cause the possibility of the first data received by mistake. Recommendation initialization process requires Handshake Protocol, confirming the initialization is complete before starting to make data transmission.

SPI Control Register 0**:**
(OVF control bit)
The OVF is the overflow flag of the SPI. When any additional SCK clock edge is inputted during the transmission period, it will be high potential (1). For example, if the bit length of a work is 16 bits and there are 17 clock pulses from the master device before CS changes to high (in this case, CSL is <0>), and when OVF receives the 17th clock edge, its value is 1. That means that errors occur during the transmission. If the 17th clock edge has occurred, it means that the data transmitted first are lost.

(ABF control bit)
The ABF is the interrupt flag of the SPI, which is only used in the slave mode. During the transmission, when the SCK clock edge inputs are insufficient, it will be high potential (1). For example, if the bit length of a word is 16 bits, there are 15 clock edges from the master device and the CS is changed to high potential (in this case, the CSL is 0), the ABF is 1. That means errors occur during the transmission. The transaction is not finished

and the transmitted data are updated to the read register. The transmission is stopped and lost.

(BUF control bit)

The BUF is the busy flag of the SPI. When the SPI is transmitting or receiving data, it is high potential (1). Under the master mode, when the SPI starts to transmit data, it is high potential (1). Once the SPI stops transmitting data or transmission is finished, it will be cleared automatically. Under the slave mode, when the SPI is ready to communicate with the master device, it is 1. Once the SPI stops transmitting data or transmission is finished, it will be cleared automatically.

SPI Interrupt Flag Control bit:

(1)STxIF: the flag STxIF is the transmission interrupt of the SPI. When the write-in register is loaded into the shift register, it is set as 1.

(2)SRxIF: the flag SRxIF is the reception interrupt of the SPI. When the shift register is loaded into the read register, it is set as 1

21.2. Register Address

SPI Register Address	31 24	23 16	15 8	7 0
SPI base address + 0x00(0X40F00)	SPIC2M	SPIC2	SPIC1M	SPIC1
SPI base address + 0x04(0X40F04)	SPIC0M	SPIC0	-	BL
SPI base address + 0x08(0X40F08)	RXB3	RXB2	RXB1	RXB0
SPI base address + 0x0C(0X40F0C)	TXB3	TXB2	TXB1	TXB0

-Reserved

21.3. Register Functions

21.3.1. SPI Register0

SPI Base Address + 0X00 (0X40F00)									
Symbol	SPICR0 (SPI Control Register 0)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	-	RXF	OVF	ABF	BUF	DCF	TXBF	RXBF
RW	R0W-0	-	R-0	RW0-0		R-0			
Bit	[15:08]	[7:4]				[3]	[2]	[1]	[0]
Name	MASK	-				CPHA	CPOL	M/S	EN
RW	R0W-0	-				RW-0			

Bit	Name	Description	
Bit[22]	RxF	Reception (Rx) register update flag	
		0	Normal

		1	The reception (RX) register is updated; the reception register cannot be read now.
Bit[21]	OVF	SPI bus data over-length flag	
		0	Normal
		1	The length of the received data length is higher than the set data length BL[4:0]; writing in 0 can clear the OVF flag.
Bit[20]	ABF	SPI bus data insufficient-length flag	
		0	Normal
		1	The length of the received data length is lower than the set data length BL[4:0]; writing in 0 can clear the ABF flag.
Bit[19]	BUF	SPI bus busy flag	
		0	SPI bus interface Idle Standby
		1	SPI bus interface busy status
Bit[18]	DCF	Data lost flag	
		0	Normal
		1	The reception register is full but still keeps receiving data; the old data will be lost and reading the reception register can clear the bit.
Bit[17]	TxBF	TX transmission register full flag	
		0	TX transmission register is empty and can transmit data.
		1	TX transmission register is full and keeping writing data in the register will overwrite old data.
Bit[16]	RxBF	Rx reception register full flag	
		0	RX reception register is empty.
		1	RX reception register is full (reading the reception can clear the bit.)
Bit[3]	CPHA	Clock phase configuration for the SPI bus capturing data	
		0	Capture data at the first clock edge of the SCK.
		1	Capture data at the second clock edge of the SCK.
Bit[2]	CPOL	SPI bus operating frequency polarity control	
		0	SCK low potential is idle.
		1	SCK high potential is idle.
Bit[1]	M/S	SPI operating mode configuration	
		0	Passive mode
		1	Active mode
Bit[0]	EN	SPI function enable control	
		0	Disable
		1	Enable

21.3.2. SPI Register1

SPI Base Address + 0X04 (0X40F04)						
Symbol	SPI CR1(SPI Control Register 1)					
Bit	[31:24]	[23:21]	[20]	[19]	[18]	[17:16]
Name	MASK	-	CSO	CSL	LBF	MD
RW	R0W-0	-	RW-0			
Bit	[15:05]	[04:00]				
Name	-	BL				
RW	-	RW-0				

Bit	Name	Description	
Bit[20]	CSO	Chip internal wake-up (CS) signal simulator control, applicable to the 3-wire mode	
		0	CS signal simulator works.
		1	CS signal simulator stands by.
Bit[19]	CSL	CS signal polarity configuration, for enabling devices, Suitable for 4-wire master end and from the end mode	
		0	Low-potential enablement
		1	High-potential enablement
Bit[18]	LBF	Data transmission order	
		0	Transmit MSB first
		1	Transmit LSB first
Bit[17-16]	MD	SPI interface operating mode configuration	
		00	SPI standard 4-wire communication interface mode
		01	SPI universal 3-wire interface mode
		10	TI mode
		11	TI mode
Bit[4~0]	SPIBL	SPI signal word length transmission configuration	
		00000	8 bits length
		00001	16 bits length
		00010	24 bits length
		00011	4 bits length
		00100	5 bits length
		00101	6 bits length
		00110	7 bits length
		00111	8 bits length
		01000	9 bits length
		01001	10 bits length
		01010	11 bits length

		01011	12 bits length
		01100	13 bits length
		01101	14 bits length
		01110	15 bits length
		01111	16 bits length
		10000	17 bits length
		10001	18 bits length
		10010	19 bits length
		10011	20 bits length
		10100	21 bits length
		10101	22 bits length
		10110	23 bits length
		10111	24 bits length
		11000	27 bits length
		11001	26 bits length
		11010	27 bits length
		11011	28 bits length
		11100	29 bits length
		11101	30 bits length
		11110	31 bits length
		11111	32 bits length

When the MD is set to three-wire mode, the original CS Pin become GPIO mode, you can generate the required by the User random wave type or use for other applications, but still need to CS SPI Interface as synchronization signals.

Three-wire mode of Master Mode:
Internal synchronization circuit itself without any special treatment.

Three-wire mode of Slave Mode:
Need to use the CSO Bit analog SPI Bus on the CS signal, are simulated using the CSO CS signal must be similar to the standard four-wire mode.

21.3.3. SPI Register2

SPI Base Address + 0X08 (0X40F08)	
Symbol	SPICR2 (SPI Control Register2)
Bit	[31:16]
Name	RXB31-16
RW	R-X
Bit	[15:0]
Name	RXB15-0
RW	RW-X

Bit	Name	Description
Bit[31~0]	SPIRB	SPIRB [31:0] is the 32-bit reception register.

Use the LBF bit to set whether the LSB or MSB is transmitted first.
If the LSB is set to be transmitted first, the position where the data are stored will be influenced, and the RXB effective data will be right-justified.
For example, if the BL is set to be under the 8-bit mode, the received data will be stored at the RXB [7:0]; if the BL is set to be under the 9-bit mode, the received data will be stored at the RXB [8:0], and so on.
If the MSB is set to be transmitted first, the RXB effective data will be left-justified.
For example, if the BL is set to be under the 8-bit mode, the received data will be stored at the RXB [31:24]; if the BL is set to be under the 9-bit mode, the received data will be stored at the RXB [31:23], and so on.

21.3.4. SPI Register3

SPI Base Address + 0X0C (0X40F0C)	
Symbol	SPICR3 (SPI Control Register 3)
Bit	[31:16]
Name	TXB31-16
RW	R-X
Bit	[15:0]
Name	TXB15-0
RW	RW-X

Bit	Name	Description
Bit[31~0]	SPITB	SPITB [31:0] is the 32-bit transmission register.

Use the LBF bit to set whether the LSB or MSB is transmitted first.
If the LSB is set to be transmitted first, the position where the data are stored will be influenced, and the TXB effective data will be right-justified.

For example, if the BL is set to be under the 8-bit mode, the received data will be stored at the TXB [7:0]; if the BL is set to be under the 9-bit mode, the received data will be stored at the TXB [8:0], and so on.

If the MSB is set to be transmitted first, the TXB effective data will be left-justified.

For example, if the BL is set to be under the 8-bit mode, the received data will be stored at the TXB [31:24]; if the BL is set to be under the 9-bit mode, the received data will be stored at the TXB [31:23], and so on.

22. UART Management

22.1. Introduction

Enhanced Universal Asynchronous Receiver Transmitter, EUART peripheral is usually called serial communications interface or SCI. The EUART can be configured as a full-duplex asynchronous system that can communicate with peripheral devices, such as CRT terminals and personal computers. It can also be configured as a half-duplex synchronous system that can communicate with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROM, etc.

The Enhanced EUART implements additional features, including Frame error detection and auto address identification. Frame error detection can determine whether a frame is effective or not through frame stop bit. Auto address identification function can compare address frame content with single chip address; serial interrupt can only be generated when matching. These 2 functions are implemented through hardware circuit and software respectively.

22.1.1. Baud Rate Generator, BRG

BRG is a dedicated 13 bit generator that supports asynchronous mode of the EUART. The following table shows the calculation of the serial transmission rate, but only for the master mode.

And in the case of a given target tandem transfer rate and a UART operating frequency source (URCK), we can calculate the approximate integer values Baud Rate using the formula in the following table, which can determine the serial transmission serial transmission rate error. It is recommended that after switching the internal crystal (HSRC) or external crystal (HSXT) operating frequency. Need to reset serial transmission rate or Use automatic transmission speed serial function, Recalibrate Baud Rate value. URCK frequency is selected from external HSXT or internal HSRC clock source, and it goes through UACD[3:0] divider. If UACD=1, URCK=HSXT(or HSRC). If UACD=2, URCK=HSXT/2(or HSRC/2) and so on.

Baud Rate Generator/EUART MODE	Baud Rate Equation
13 bit/asynchrony	URCK÷[4x(n+1)]
URCK= UART operating frequency source; n=BRGRH:BRGRL register correct value；	

For example: In the asynchronous mode, the operating frequency source of UART (assumed to 4MHz), and the target serial transmission rate of 9600bps, calculate the value of Baud Rate.

Baud Rate= ((URCK÷Target serial transmission rate) ÷4)-1
= ((4000000÷9600) ÷4)-1
= 103.1667
≈103

According to the above calculation Baud Rate:

Baud Rate = 4000000 ÷ (4x (103 + 1)) = 9615.38; so there is a certain error, the error are calculated as follows:

Error rate = (the actual calculation Baud Rate - the target Baud Rate) / the target Baud Rate
= (9615-9600) / 9600
= 0.16%

22.1.2. Communication IO pins

The EUART communication bus only uses two wires, TX/RX; the chip allocates 8 sets of communication IO pins (each set includes the TX/RX wires) for the EUART module for users to perform designs freely. But this is the IO port multiplexing function, through the GPIO Alternate Function Controller 0x40844's control bits PTUR and PTURE However, the reuse functions of the IO port can be used to conveniently select and enable the communication IO pins of the EUART via the controller PTUR [2:0]/PTURE; accordingly, when using the EUART, the IO communication pins should be enabled, and the corresponding IO pins should be set as the input mode or output mode. The distribution of the EUART communication IO pins is as shown in the following table.

PTUR[2:0]	PTURE	TX	RX	PTUR[2:0]	PTURE	TX	RX
000	1	PT1.0	PT1.1	100	1	PT2.0	PT2.1
001	1	PT1.2	PT1.3	101	1	PT2.2	PT2.3
010	1	PT1.4	PT1.5	110	1	PT2.4	PT2.5
011	1	PT1.6	PT1.7	111	1	PT2.6	PT2.7

Table 22-1 EUART communication IO pin distribution

22.1.3. Auto Baud Rate & Auto Baud rate setting process

UART modules support automatic detection and corrected serial transmission rate function, it is known as serial automatic transmission rate function. Its Auto-baud rate setting process is as follows:

1. UART initialization settings: Includes UART TX, RX Port and RX set .TX correspond to the GPIO pin needs to be set to the corresponding TX and RX Output to Input, and set ENSP = 1b.
2. Setting WUE = 0b, and automatic serial transmission rate control bit ENABD = 1b to start the Auto-baud rate function.

3. Before the automatic transmission speed serial function, to clear Baud Rate Generator register contents, and clears the RX Data Buffer and RX Flag set, clear finished, waiting to receive data 0x55.
4. Start automatic serial transmission rate detection (receiving data is 0x55), will be calculated at the completion of the automatic detection and correction after the result is written BRGRH [4: 0] and BRGRL [7: 0] register.
5. When the Baud Rate Generator register that is calculated over the contents of the 0000H 0FFFH to overflow, ABOVE the flag bit is set to 1, users can use of software way ABOVE set to 0 or by setting ENABD = 0 so ABDOVF = 0. In ABOVE = 1, the enable bit ENABLED state will remain 1.
6. Completion of Auto-baud rate settings. Final recommendations can be done after the Auto-baud rate, increasing the Hand hark process, the purpose is to confirm the auto-baud rate was correct.

22.1.4. EUART Asynchronous Mode

In this mode, the EUART uses standard "Non-Return-to-Zero, NRZ" format (one Start bit, eight or nine data bits and one Stop bit). The most common data format is 8 bit. An on-chip dedicated 13-bit Baud Rate Generator can be applied to derive standard baud rate frequencies from the oscillator.
Moreover, the EUART transmits and receives the last LSB. The transmitter and receiver are functionally independent but use the same data format and baud rate. Parity is supported by hardware and can be stored as the 9th data bit.

22.1.5. EUART TX transmission mode

EUART TRANSMIT BLOCK DIAGRAM

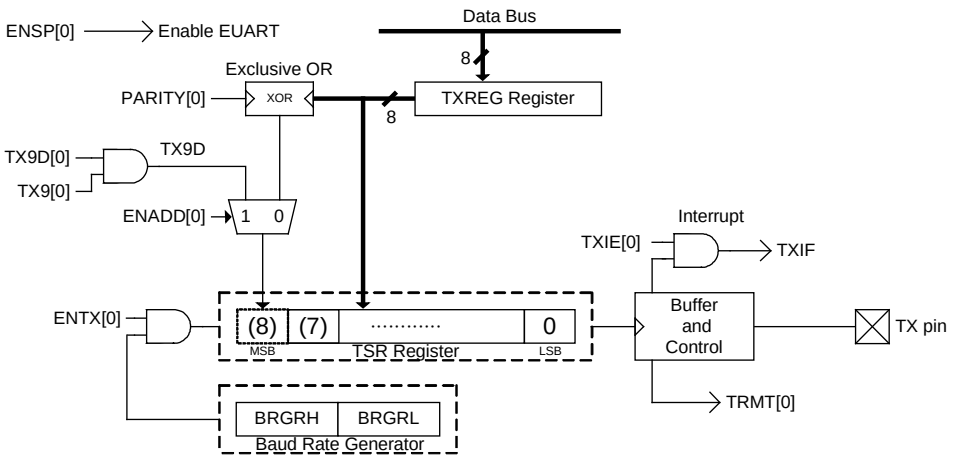


Figure 22-1 EUART Transmission Block Diagram

Figure 22-1 is the sequence of UART transmitter. The core of the transmitter is Transmit Shift Register, TSR), users cannot read/write TSR.

TSR obtains data from the Read/Write Transmit Buffer register, TXREG [7:0]. The TXREG [7:0] register is loaded with data in software. The TSR register is not loaded until the Stop bit has been transmitted from the previous load. Once the Stop bit is transmitted, the TSR is loaded with new data from the TXREG register (if available). At this point TXREG register becomes empty (current software no longer write data operation); at the same time UTXIF from 0 to 1. (When enabled ENTX, UTXIF to 1) Interrupts can be enabled or disabled by setting the UTXIE is 1 or 0; and regardless TXIE status, as long as the interrupt occurs, UTXIF will be from 1 to 0, and it is set in one instruction cycle after 1. If TSR register data has not been transmitted from the previous load and data has been written into TXREG register. TXIF is cleared in the second instruction period following the load instruction. TXIF will be configured as 1 again when Stop bit occurred.

Therefore, after the TXREG load new data instantly check UTXIF, its return value is not available for reference.UEXIF represents the current state of TXREG register, UTXIF = 1 indicates TXREG is empty, UTXIF = 0 indicates TXREG full. The Bit TRMT is showing the status of the TSR register, TRMT = 1 indicates TSR is empty, TRMT = 0 indicates TSR register full. TRMT and EUART interrupt no direct relationship, Users will need to determine whether the data is written again, can be determined by querying TRMT Bit state.

TX mode function EUART usage, TX function can query or interrupted manner.

When using must note the following points:

✓ UART actions are irrelevant to CPU instruction cycle except read and write action.

✓ TXIF and RXIF is for interrupt purpose, they are irrelevant to other events.

When using CPU to monitor peripheral components, be cautioned about the corresponding operating speed.

✓ 1. Reset (INTX = 0) default status: TRMT = 1, TXTIP = 0, UTXIF = 1.

✓ 2. Wait until the write TXREG: TRMT = 0, TXTIP = 1, UTXIF = 0.

✓ 3. Transfer TSR.

✓ 4. When the transfer 8/9 bit later, TRMT = (whether written TXREG) inverting, TXTIP = 0, UTXIF = 1.

✓ 5. Back to step 2, continue the next a data transmission; or set ENTX = 0, ENSP = 0, end of UART TX.

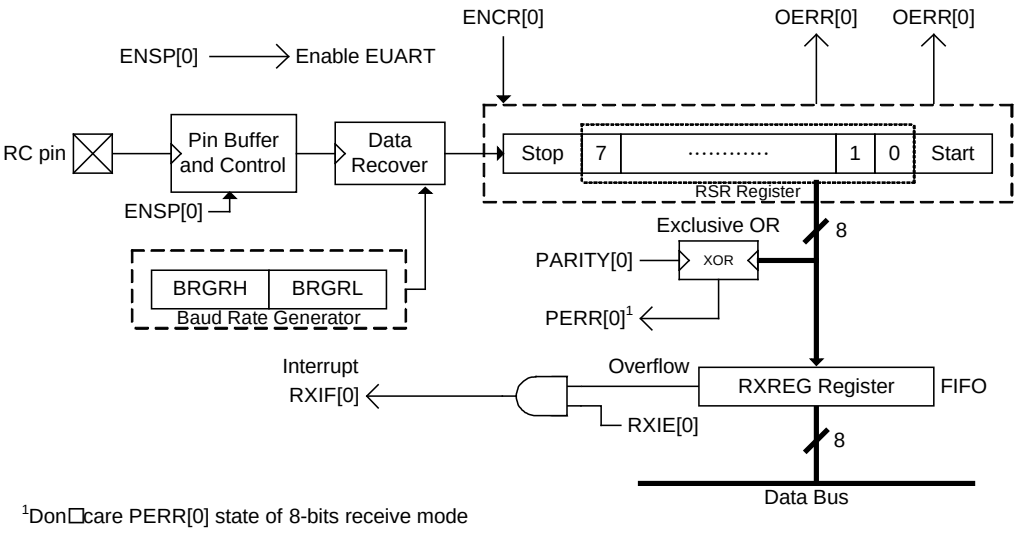
Interrupt ways TX mode function: Since UTXIF not only interrupt flag bit, or TXREG status flag bit on the power (reset default) when UTXIF = 1, so once UTXIE = 1 will enter the

interrupt vector and the corresponding interrupt, but UTXIF software cannot be cleared, it will have been entered interruption. therefore, use TX feature to note, when you need to send information to UTXIE set to 1, then enter the interrupt and then write data to the TXREG and disables interrupts TX namely UTXIE = 0. According to this mode of operation is repeatedly transmitted data can be implemented to transmit information through the interrupt.

Polling ways TX mode function is relatively simple and more, mainly after writing data, the TRMT Bit polling, polling status: TRMT = 1 is empty write data, TRMT = 0 is full, the wait has been sent . Repeated operation can be shown with the data sent.

22.1.6. EUART RX receive mode

EUART 8-BITs RECEIVE BLOCK DIAGRAM



[1]Don□care PERR[0] state of 8-bits receive mode

Figure 22-2 EUART 8-bits receiver block diagram

EUART 9-BITs RECEIVE BLOCK DIAGRAM

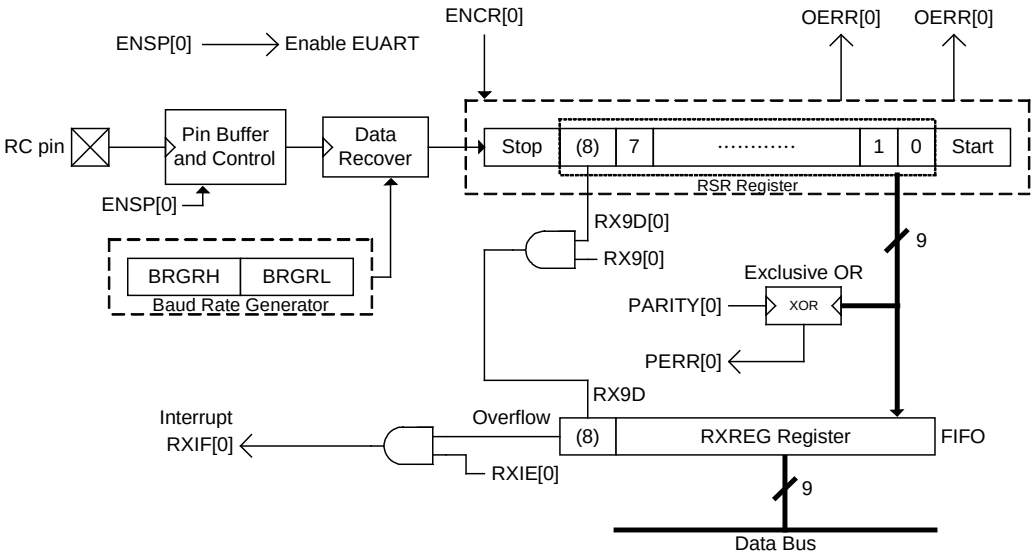


Figure 22-3 EUART 9-bits receiver block diagram

Figure 22-2 and Figure 22-3 receive mode UART functional block diagram. The data is received on the RC pin drives the data recovery circuit. Data recovery circuit is actually a high-speed shifter that operating at 13-bit auto baud rate, whereas the main receive serial shifter operates at baud rate or at OSC_RC2M. This mode is typically be used in RS-232 systems.

If RC pin does not receive complete byte (Start bit, 8(9) bit data, Close bit),
FERR bit will be set as 1 and it can be cleared by ENCR bit.
When RC pin has received two complete byte data, OERR bit will be configured as 1 when receiving the third complete byte data (have not read the data of RCREG register). OERR bit can be cleared by ENCR bit.
When complete data reception accomplished, RX's URXIF interrupt flag bit will be set, and URXIF software is not cleared, the operation can only be read by executing RCREG register to clear URXIF.
RCIDL bit the reaction is in the receiving state, Users can be done by polling this bit determine whether the received data.
When receiving data, hardware will conduct the received 8 bit data exclusive or. If RC9 is set as 1, the received RC9D data (9 bit) will be calculated by exclusive or. After operation, the result will be calculated again by exclusive or with PARITY bit and it will be displayed in PERR bit. If the received data is correct, PERR is configured as 0. Conversely, if the data received is incorrect, PERR will be set as 1. PERR bit cannot be cleared in software. PERR will be set as 0 whenever the next data is being correctly received.

RX Interrupt operation recommendations: after entering the RX interrupt, first read RCREG register, and then clear URXIF.

22.1.7. Automatic wake-up function

Under Sleep mode, all clocks to the EUART are suspended. As a result, the Baud Rate Generator is inactive and a correct byte reception cannot be conducted. The auto-wake-up function allows the controller to be awakened up when the activity on the RC line while the EUART is operating in Asynchronous mode. The auto-wake-up function is enabled by configuring the WUE bit of URCON register. After initiation, the typical receive sequence on RC is disabled and the EUART remains in an Idle state, monitoring for a wakeup event (it is not related with CPU Run mode).

A wake up event consists of a high state to low state transition on the RC line.

Followed by a wake up event, the module generates an URXIF interrupt. The interrupt is generated synchronously to the Q clock in normal operating mode. If the IC is in Sleep or Idle mode, it is asynchronously. The interrupt is cleared by reading RCREG register.

After wake up event, when low state to high state transition occurs on the RC line, WUE bit is automatically be cleared. At this time, EUART module returns to normal Run mode from idle mode.

Notice of Using Auto-Wake-Up Function

Due to the fact that auto-wake-up functions by sensing rising edge transitions on RC, information with any state changes before the Stop bit may output a false character and result in data or frame errors. Thus, the initial character in the transmission must be all "0" bit. This can be 00h (8 bit) for standard RS-232 ICs.

Oscillator start-up time must be considered as well, particularly in applying oscillators with longer start-up delay. The auto-wake-up character must be of sufficient length and of sufficient length of time interval to allow enough time for the selected oscillator to start and offer appropriate initialization of the EUART.

Notice of Using WUE Bit

Using WUE and URXIF event timing to determine the validity of received data may bring about some confusion. As noted, setting the WUE as 1 may place the EUART to a standby mode. The wake up event generates a receive interrupt and RCIF is placed 1. The WUE bit is cleared after a rising edge is seen on RC. The interrupt condition is cleared by reading the RCREG register.

Under normal condition, the data of RCREG after wake up is ineffective and should be discarded. The fact that WUE bit has been cleared (or is still set as 1) and URXIF flag is set should not be used as an indicator of the integrity of the data in RCREG. Users should consider deploying a firmware method to verify received data integrity. In order to assure no

effective data is lost, check the RCIDL bit to verify that a receive operation is not in progress. If a receive operation is not executed, the WUE can be placed 1, forcing the IC entering the Sleep mode.

22.2. Register Address

UART Register Address	31 24	23 16	15 8	7 0
EUART base address + 0x00(0X40E00)	-	-	URCONM	URCON
EUART base address + 0x04(0X40E04)	-	-	-	URSTA
EUART base address + 0x08(0X40E08)	-	-	BACONM	BACON
EUART base address + 0x0C(0X40E0C)	-	-	-	BRGRH
EUART base address + 0x10(0X40E10)	-	-	-	BRGRL
EUART base address + 0x14(0X40E14)	-	-	-	TXREG
EUART base address + 0x18(0X40E18)	-	-	-	RCREG

-Reserved

22.3. Register Functions

22.3.1. UART Register0

UART Base Address + 0X00 (0X40E00)								
Symbol	UARTCR0 (UART Control Register 0)							
Bit	[31:16]							
Name	RSV.							
RW	R-0							
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2:1]	[0]
Name	MASK	ENSP	ENTX	TX9	TX9D	PARITY	-	WUE
RW	R0W-0	RW-0					-	RW-0

Bit	Name	Description	
Bit[7]	ENSP	Enable UART control	
		0	Disable
		1	Enable
Bit[6]	ENTX	Enable UART to transmit the data	
		0	Disable
		1	Enable
Bit[5]	TX9	Control transmit 8-bit or 9-bit data	
		0	Transmit 8-bit data
		1	Transmit 9-bit data
Bit[4]	TX9D	Set the 9th state value of the transmit data	
		0	the transmit 9th bit data is 0
		1	the transmit 9th bit data is 1
Bit[3]	PARITY	Parity (none/even/odd) Selection bit	
		0	Even parity
		1	Odd parity
Bit[0]	WUE	Enable Wake up function	
		0	Disable
		1	Enable

22.3.2. UART Register1

UART Base Address + 0X04 (0X40E04)									
Symbol	UART1 (UART Control Register 1)								
Bit	[31:16]								
Name	RSV.								
RW	R-0								
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	RSV	-	RC9D	PERR	FERR	OERR	RCIDL	TRMT	ABDOCF
RW	R-0	-	R-0						

Bit	Name	Description	
Bit[6]	RC9D	If RC9 is enabled, then the received 9th bit data is stored here	
		0	the received 9th bit data is 0
		1	the received 9th bit data is 1
Bit[5]	PERR	Parity Error Status bit	
		0	Parity error has been detected for the current character
		1	Parity error has not been detected
Bit[4]	FERR	UART Receive Framing Error bit	
		0	Normal (No framing error)
		1	Framing error happened for receiving
Bit[3]	OERR	Overrun Error bit	
		0	No overrun error
		1	Overrun error
Bit[2]	RCIDL	Receiver Idle bit	
		0	Receiver is Idle
		1	Receiver is active
Bit[1]	TRMT	Transmit Shift Register Status bit	
		0	Transmit Shift Register full
		1	Transmit Shift Register empty
Bit[0]	ABDOVF	Auto-Baud Acquisition Rollover Status bit	
		0	No rollover has occurred
		1	A rollover has occurred during Auto-Baud Rate Detect mode (Must be cleared in software)

22.3.3. UART Register2

UART Base Address + 0X08 (0X40E08)						
Symbol	UARTCR2 (UART Control Register 2)					
Bit	[31:16]					
Name	RSV.					
RW	R-0					
Bit	[15:8]	[7:4]	[3]	[2]	[1]	[0]
Name	MASK	-	ENCR	RC9	ENADD	ENABD
RW	R0W-0	-	RW-0			

Bit	Name	Description	
Bit[3]	ENCR	Clear FERR Control	
		0	Normal
		1	Clear FERR, then return 0 automatically
Bit[2]	RC9	9-Bit Receive Enable bit	
		0	Selects 8-bit reception
		1	Selects 9-bit reception
Bit[1]	ENADD	Address Detect Enable bit(when RC9 = 1)	
		0	Enables address detection received 9 bit of all data as even and odd calibration function
		1	Disables address detection, enable interrupts and use the receive buffer,TX9D, RC9D can have data to analyze
Bit[0]	ENABD	Auto-Baud Rate Detect Enable bit	
		0	Disable Auto-Baud Rate or Detect are complete
		1	Enable Auto-Baud Rate Detect data 0X55 automatically cleared after completion

22.3.4. UART Register3

UART Base Address + 0X0C (0X40E0C)					
Symbol	UARTCR3 (UART Control Register 3)				
Bit	[31:16]				
Name	-				
RW	-				
Bit	[15:8]				[4:0]
Name	MASK	-			BRCR12-8
RW	R0W-0	-			RW-0

Bit	Name	Description
Bit[4~0]	BRGR12-8	Baud Rate Control Register MSB BIT

22.3.5. UART Register4

UART Base Address + 0X10 (0X40E10)		
Symbol	UARTCR4 (UART Control Register 4)	
Bit	[31:16]	
Name	RSV	
RW	R-0	
Bit	[15:8]	[7:0]
Name	MASK	BRCR7-0

RW	R0W-0	RW-0

Bit	Name	Description
Bit[7~0]	BRGR7-0	Baud Rate Control Register LSB BIT

22.3.6. UART Register5

UART Base Address + 0X14(0X40E14)		
Symbol	UARTCR5 (UART Control Register 5)	
Bit	[31:16]	
Name	RSV	
RW	R-0	
Bit	[15:8]	[7:0]
Name	RSV	TXREG
RW	R-0	RW-0

Bit	Name	Description
Bit[7~0]	TXREG	TXREG[7:0] buffer from MSB to LSB

22.3.7. UART Register6

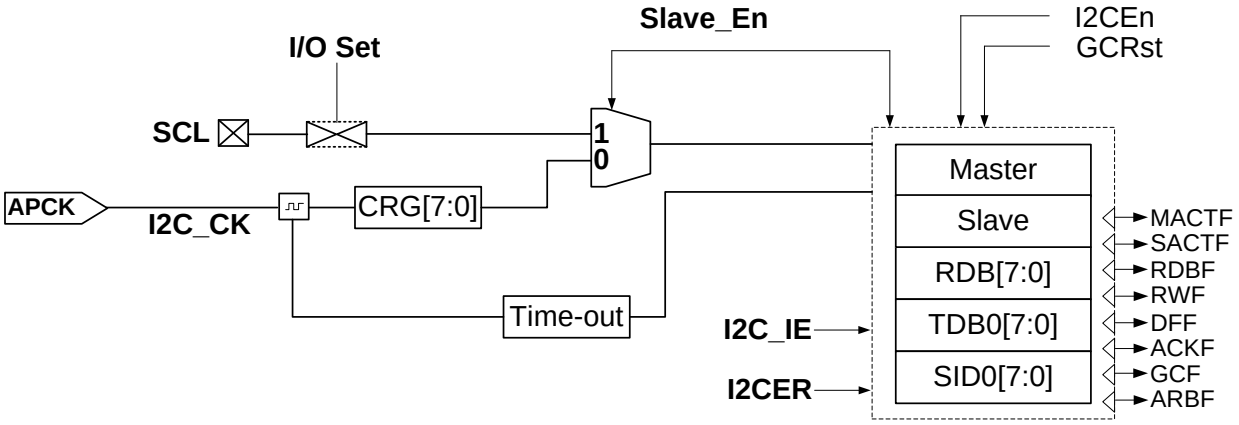
UART Base Address + 0X14(0X40E18		
Symbol	UARTCR6 (UART Control Register 6)	
Bit	[31:16]	
Name	RSV	
RW	R-0	
Bit	[15:8]	[7:0]
Name	RSV	RCREG
RW	R-0	RW-0

Bit	Name	Description
Bit[7~0]	RCREG	RCREG[7:0] buffer from MSB to LSB

22.4. I2C Network

22.5. Introduction

The Communication Interface
(Abbreviated CI) main types of I2C serial communication.
I2C serial interface, (Inter-Integrated Circuit Serial interface)
I2C communications interface contains the host (Master) and slave (Slave) two modes of operation.

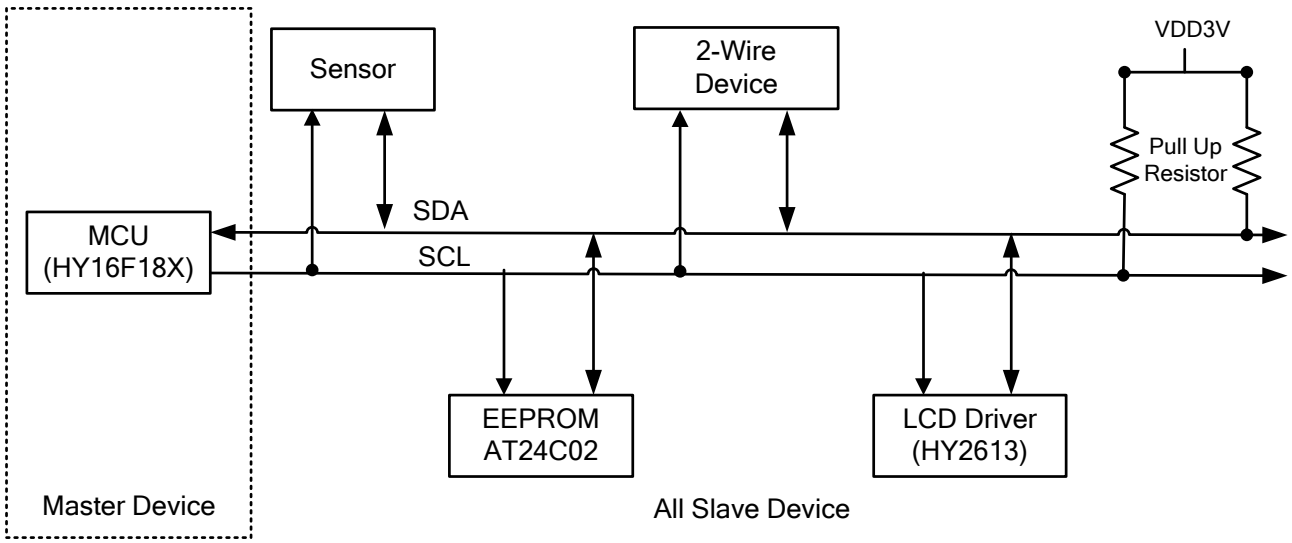


I2C serial interface features:

Standard I2C serial interface includes 2-pin for serial data (SDA), serial clock (SCL). Pin is Open Drain output structure, the need for external pull-up resistor, to ensure high-level output. Standard I2C serial interface can be configured as a master (Master), Slave (Slave) or master / slave mode. Programmable clock allows adjustment of I2C transfer rates.

Between master and slave data transmission is bidirectional.

I2C allows a large operating voltage range.I2C reference design uses a 7-bit long address space but retained the 16 addresses, so a group of bus and up to 112-node communication.



I2C serial interface signals:

Start signal (START):

Host SCL is high potential, the issue of SDA from high potential into a low potential to start data transfer.

Data (DATA) or address (ADDRESS) signal:

I2C serial interface protocol requires only when SCL is low potential, SDA can only be changed on the data.

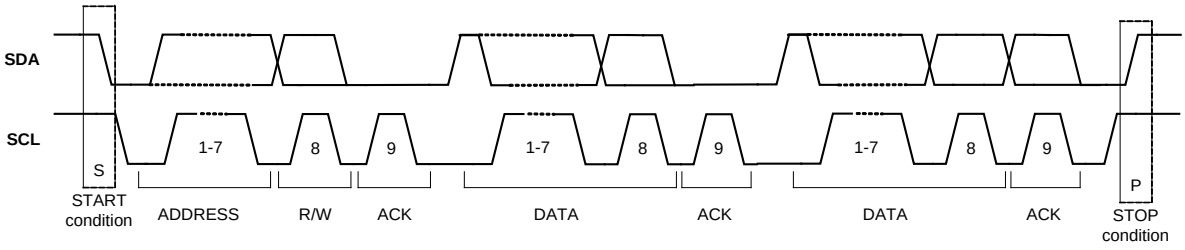
Response signal (Acknowledge):

Receiving data (slave) is received after the first eight bit,

Sending data to a device (host) sends a low potential, which means that data has been received.

Stop signal (STOP):

Host SCL is high potential, the issue of SDA from low potential to a high potential to end the data transfer.



Data transmission rate calculation:

I2C internal registers CRG [7:0] can control the host mode data transfer speed, CRG [7:0] value of the internal counter generates a host via the SCL pin signal, so the data transfer rate can be based on the I2C clock source I2C_CK frequency, using the following formula:

Data transfer on the I2C Bus SCL pin is a clock signal, which is determined on the SCL pin clock rate By I2C circuit clock source frequency I2CLK with CRG via the following formula:

(I2CK)Data Baud Rate = (APCK) / [4X (CRG + 1)]

Note:

I2C Master Mode and I2C Slave Mode under, SCL can support a maximum speed of 400 kHz.

Timing function (Time-Out):

Time-out control is to avoid I2C controller will lock I2C communication bus, I2C during operation in order to provide sufficient time to deal with MCU I2C controller needs, so I2C controller in response to each bit will be after pull SCL is Low, the Master cannot be heard next clock signal, that is, a communication delay (Clock Stretching). But when the MCU is too busy, or for any reason unable to respond to the needs of I2C controller when SCL I2C communication bus will likely be locked in Low.

In order to prevent this from happening, Time-out controller according to the user through the operating frequency divider DI2C [2:0] and time conditions controller I2CTLT [3:0], determine the state of SCL is Low Time-out conditions.

Conditional processing has the following states:
When the machine detects SCL are pulled Low of time to meet the conditions will force the SCL I2C controller let go and send an interrupt event to the CPU.

When the SCL does not meet Time-out time is released as the High, the Time-out controller internal counter will be reset, and then pulled at the next SCL is Low recount.

I2C communication pin

The I2C bus only has two wires, but the chip allocates 8 sets of communication IO pins for the I2C module (Each set of IO pins includes SCL/SDA), which is for the reuse functions of the IO port. In this way, users can conveniently select different communication pins. The corresponding communication pins can be selected and enabled via the controllers I2CPTS, I2CPTEN. When using the functions of the I2C, the communication IO pins should be enabled, and the corresponding IO pin should be set under the input mode or output mode. The following table is the communication pin distribution table.

I2CPTS[2:0]	I2CPTEN	SCL	SDA	I2CPTS[2:0]	I2CPTEN	SCL	SDA
000	1	PT1.0	PT1.1	100	1	PT2.0	PT2.1
001	1	PT1.2	PT1.3	101	1	PT2.2	PT2.3
010	1	PT1.4	PT1.5	110	1	PT2.4	PT2.5
011	1	PT1.6	PT1.7	111	1	PT2.6	PT2.7

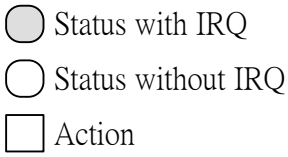
Table 23-1 I2C communication IO pin distribution

I2C serial interface terms

(SPIA): It means Action Register (ACT) giving instructions to the Action control register, where S is the Start instruction, and P is the Stop instruction, I is the interrupt flag and A is the Acknowledge instruction.

SPIA: It means Action Register(ACT) reading the value of the Action control register, which can be used to determine the interrupt flag or other instructions are finished or not.
STA: It means reading the value of the Status register, which is used to show the current operating status of the I2C circuit.

The following flow chart will respectively express the statuses of the I2C interface by (circular frame with gray background), (circular frame with white background) and (white rectangular frame):



Circular frame with gray background: it means the I2C status that the interrupt flag is established.
Circular frame with white background: it means the I2C status that the interrupt flag is not established and needs to be read actively by the MCU.
White rectangular frame: it means the instructions to the I2C should be given by the MCU.

22.5.1.1. Master TX flow

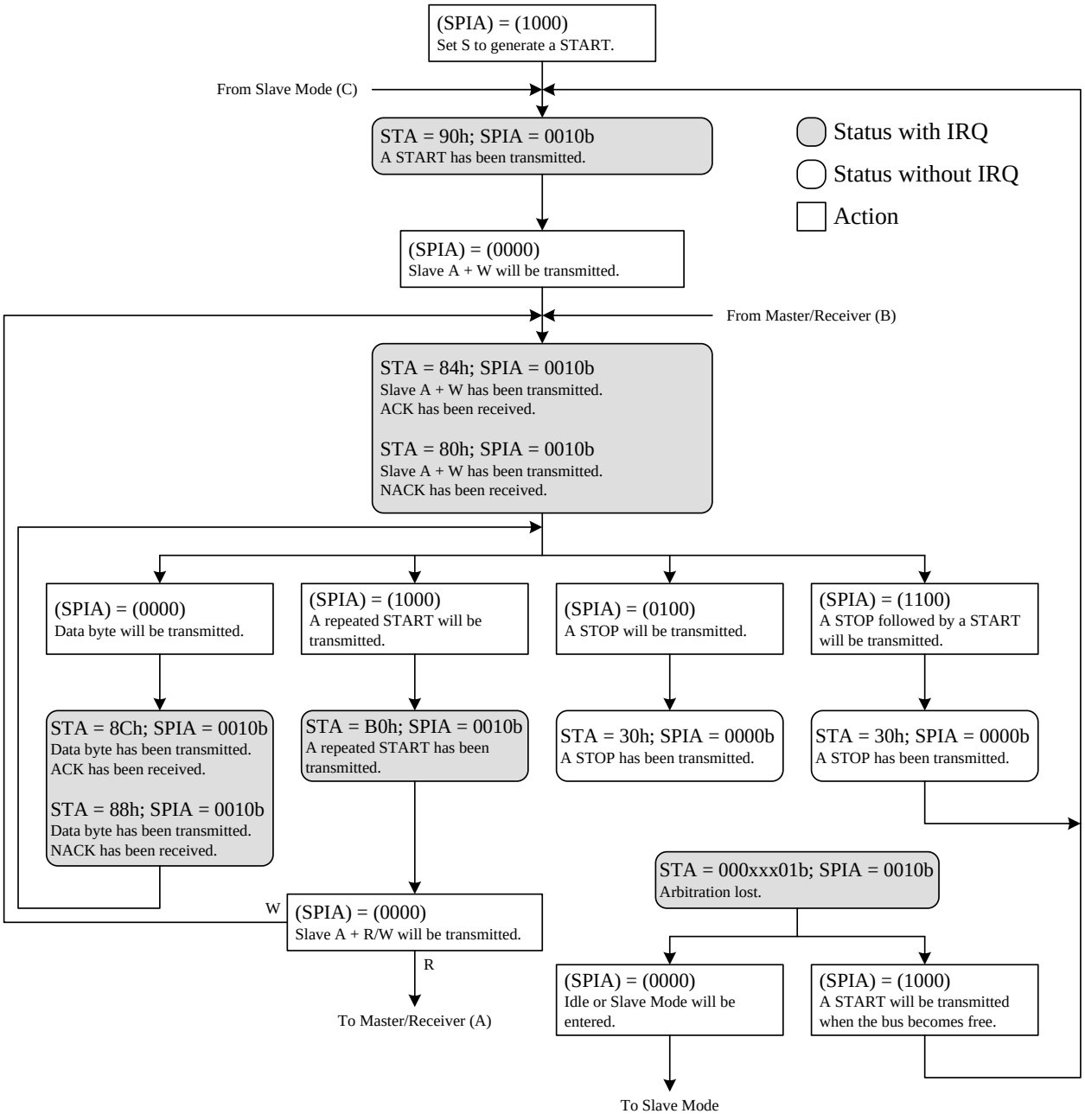


Fig 23-4 Master Transmitter Mode

22.5.1.2. Master RX flow

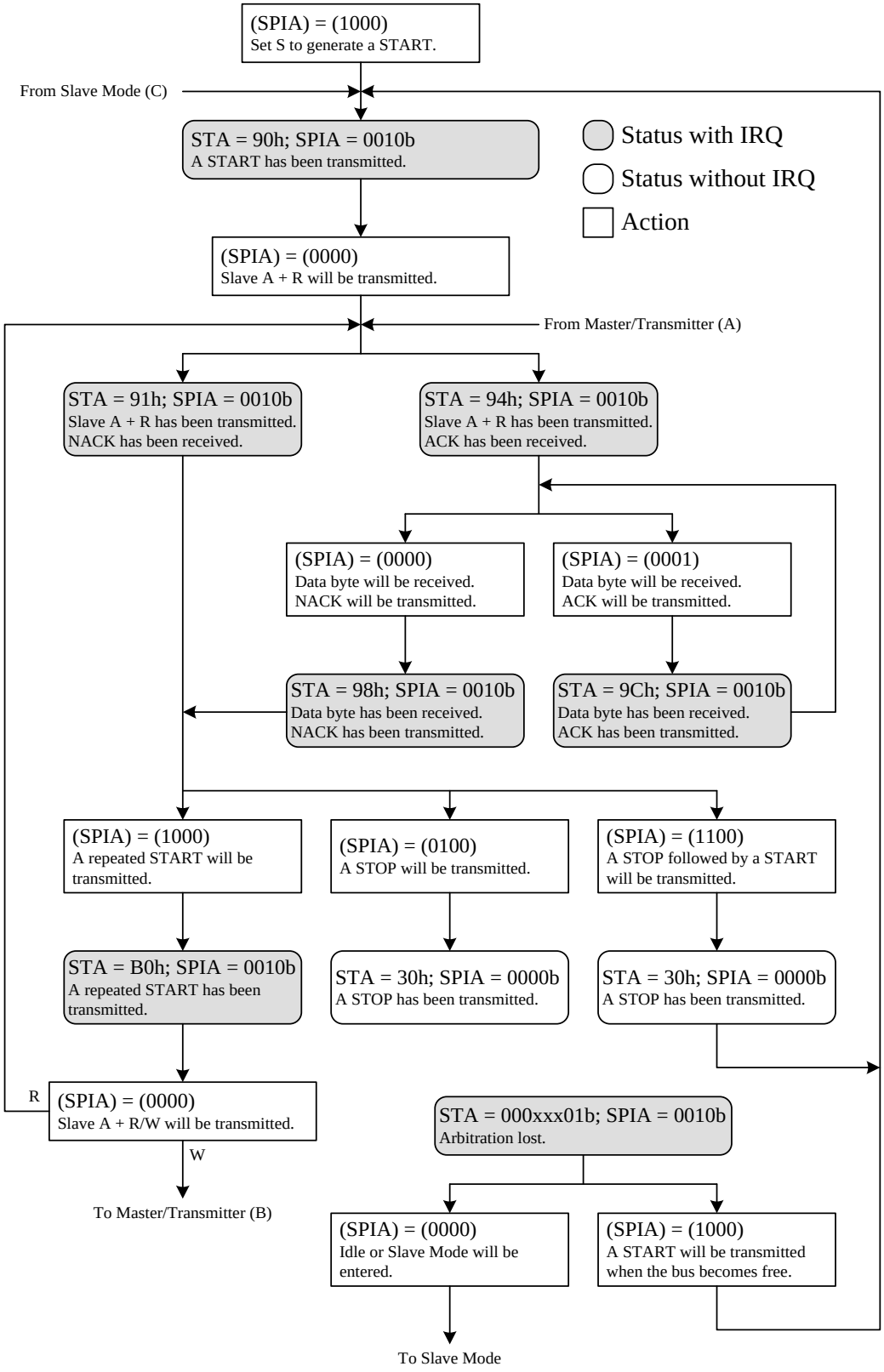


Fig 23-5 Master Receiver Mode

22.5.1.3. Slaver TX flow

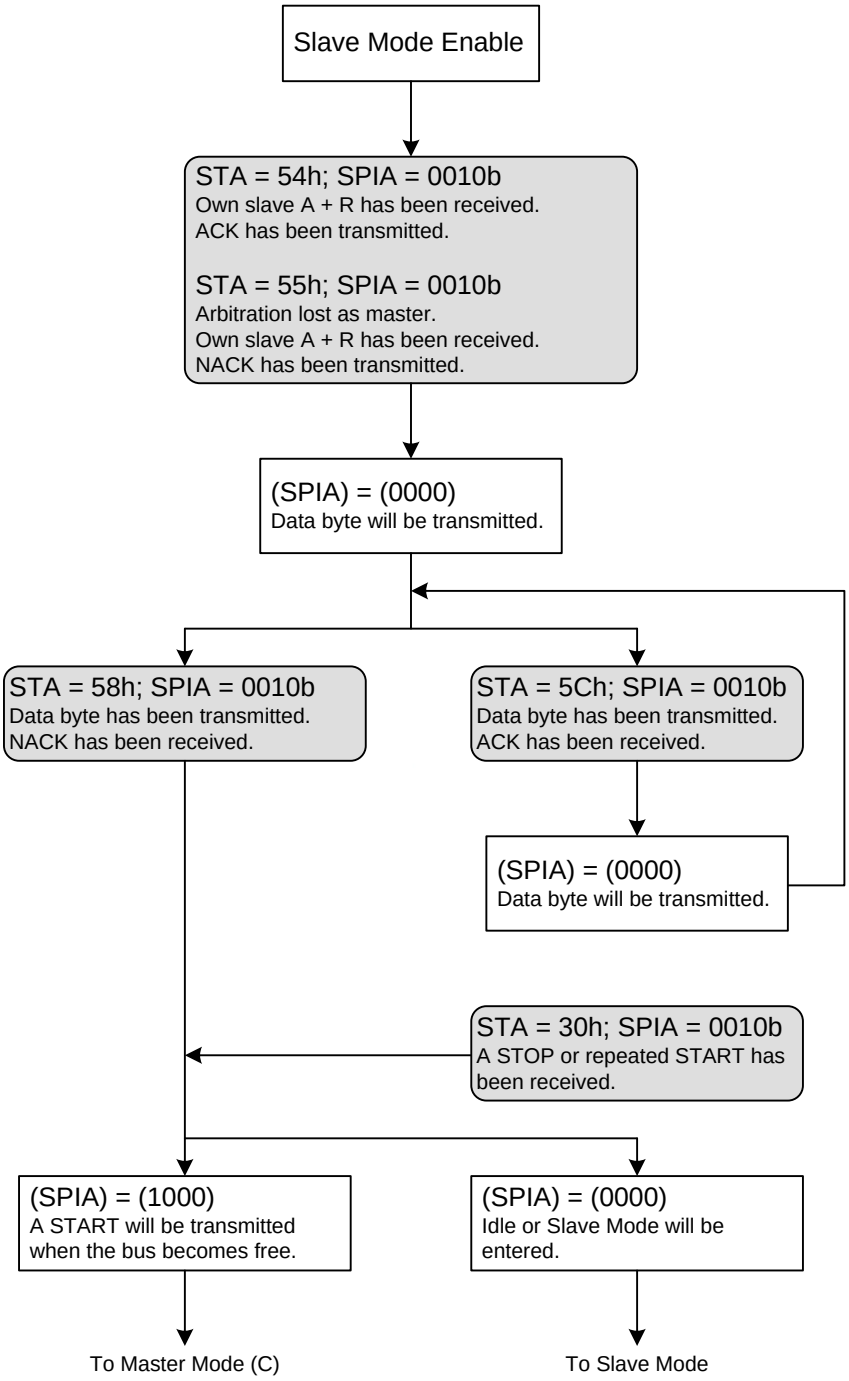


Fig 23-6 Slave Transmitter Mode

22.5.1.4. Slaver RX flow

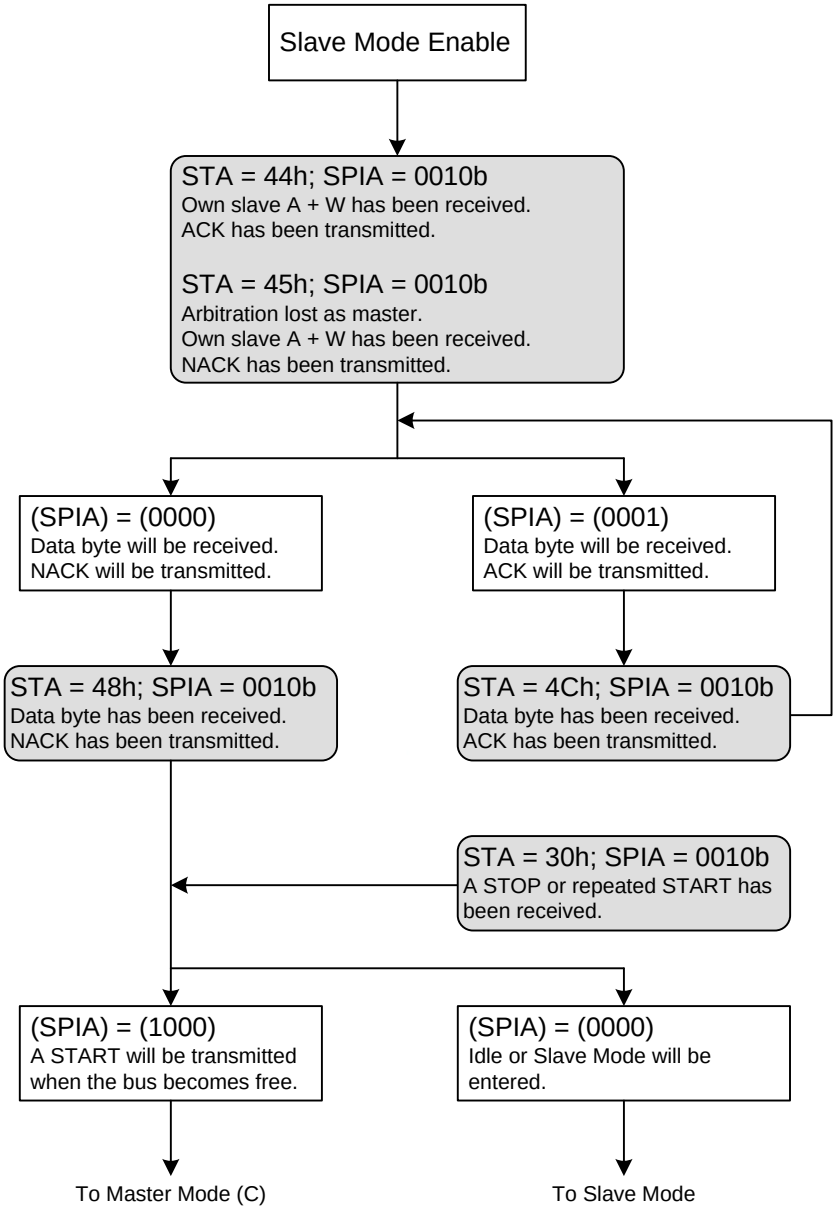


Fig 23-7 Slave Receiver Mode

22.5.1.5. General Call flow

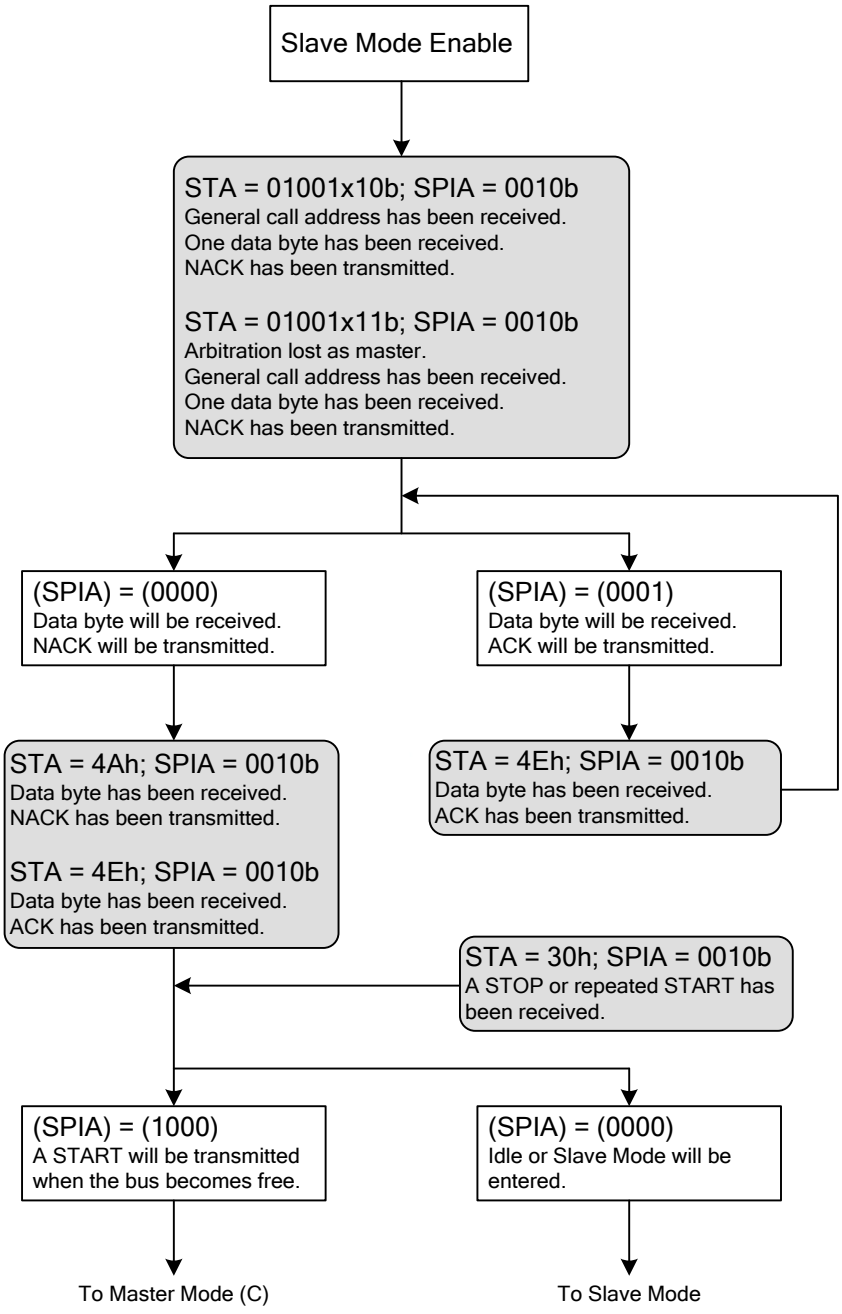


Fig 23-8 General Call Mode

22.6. Register Address

I2C Register Address	31 24	23 16	15 8	7 0
I2C base address + 0x00 (0X41000)	-	-	MASK0	I2C_CON0
I2C base address + 0x04 (0X41004)	MASK1	I2C_CON1	MASK2	I2C_CON2
I2C base address + 0x08 (0X41008)	MASK3	I2C_CON3	MASK4	I2C_CON4
I2C base address + 0x0C (0X4100C)	MASK5	MASK6	I2C_CON5	I2C_CON6
I2C base address + 0x10 (0X40010)	-	-	-	I2C_CON7
I2C base address + 0x14 (0X40014)	-	-	-	I2C_CON8

-Reserved

22.7. Register Functions

22.7.1. I2C Control Register0

Configuration Register (CFG)

I2C Base Address + 0X00 (0X41000)					
Symbol	I2CCR0 (I2C Control Register 0)				
Bit	[31:16]				
Name	RSV.				
RW	R-0				
Bit	[15:8]	[7:3]	[2]	[1]	[0]
Name	MASK	RSV.	GCRst	TOEn	I2CEn
RW	R0W-0	R-0	RW-0		

Bit	Name	Description	
Bit[02]	GCRst	General Call Reset Enable	
		0	Disable
		1	Enable
Bit[01]	TOEn	Time-out Function Enable	
		0	Disable
		1	Enable
Bit[00]	I2CEn	I2C Function Enable	
		0	Disable
		1	Enable

22.7.2. I2C Control Register1

Action Register (ACT)

I2C Base Address + 0X04 (0X41004)									
Symbol	I2CCR1 (I2C Control Register 1)								
Bit	[31:24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
Name	MASK	M_{Act}	S_{Act}	R_x P/S_r	R/W	DF	A/NA	GC	ARB
RW	R0W-0	R-0							
Bit	[15:08]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	SEn	10bEn	3BEn	EIRQFlag	START	STOP	IRQFlag	A/NA
RW	R0W-0	RW-0							

Bit	Name	Description	
Bit[23]	M_{Act}	Master Mode Active Flag	
		0	Inactive
		1	Active
Bit[22]	SAct	Slave Mode Active Flag	
		0	Inactive
		1	Active
Bit[21]	Rx P/Sr	Received Stop/Repeat-Start Flag	
		0	Normal
		1	Stop/Repeat-Start has been transmitted or received.
Bit[20]	R/W	Read/Write State Flag	
		0	Write Command has been transmitted or received.
		1	Read Command has been transmitted or received.
Bit[19]	DF	Data Field Flag	
		0	Normal
		1	I2C Data Byte has been transmitted or received.
Bit[18]	A/NA	Acknowledge Flag	
		0	No ACK has been transmitted or received.
		1	ACK has been transmitted or received.
Bit[17]	GC	General Call Flag	
		0	Normal
		1	Currently General Call Operation
Bit[16]	ARB	Arbitration Lost Flag	
		0	Normal
		1	Arbitration Lost

Bit	Name	Description	
Bit[07]	SEn	Slave Mode Enable	
		0	Disable
		1	Enable
Bit[06]	10bEn	Slave 10 Bit Address Mode Enable	
		0	Disable
		1	Enable Slave 10 Bit Addressing mode
Bit[05]	3BEn	Slave 3 Byte Data Mode Enable	
		0	Disable
		1	Enable Slave 3 Byte data transfer mode
Bit[04]	EIRQFlag	Error Interrupt Flag	
		0	Normal, write 0 to this bit makes this bit From 1 → 0 will drive the I2C down a state run.

		1	A time-out occurred or an unexpected start (stop) signal was received or arbitration failed
Bit[03]	START(S)	(S) Start Command Bit	
		0	No Command
		1	Start signal is generated in the I2C Bus
Bit[02]	STOP(P)	(P) Stop Command Bit	
		0	No Command
		1	Stop signal generated in the I2C Bus
Bit[01]	IRQFlag(I)	(I) Interrupt Flag	
		0	Normal, write 0 to this bit makes this bit From 1 → 0 will drive the I2C down a state run.
		1	Interrupt Pending
Bit[00]	A/NA(A)	(A) Acknowledge Return Bit	
		0	No ACK will be returned
		1	ACK will be returned.

22.7.3. I2C Control Register 2

Time-out Control Register (TOC)

I2C Base Address + 0X08 (0X41008)				
Symbol	I2CCR2 (I2C Control Register 2)			
Bit	[31:24]	[23:16]		
Name	MASK	CRG		
RW	R0W-0	RW-0		
Bit	[15:08]	[7]	[6:4]	[3:0]
Name	MASK	TOFlag	TOPS	TOLimit
RW	R0W-0	R-0	RW-0	

Bit	Name	Description	
Bit[23~16]	CRG	I2C Bus Data Baud Rate Control	
		0	Set 0
		1	Set 1

Data transfer on the I2C Bus SCL pin is a clock signal, which is determined on the SCL pin clock rate By I2C circuit clock source frequency I2CK with CRG via the following formula:

(I2CK)Data Baud Rate = (APCK) / [4X (CRG + 1)]

Bit	Name	Description	
Bit[7]	TOFlag	Time-out Flag	
		0	Normal
		1	I^2 C Bus Clock Stretching Time-out
Bit[6~4]	TOPS	Time-out Clock Pre-scale	
		111	$CLK_{PS} = I^2CLK / 128$
		110	$CLK_{PS} = I^2CLK / 64$
		101	$CLK_{PS} = I^2CLK / 32$
		100	$CLK_{PS} = I^2CLK / 16$
		011	$CLK_{PS} = I^2CLK / 8$

		010	$CLK_{PS} = I^2CLK / 4$
		001	$CLK_{PS} = I^2CLK / 2$
		000	$CLK_{PS} = I^2CLK / 1$

Bit	Name	Description	
Bit[3~0]	TOLimit	Time-out Limit, Time-out CLKPS occurrence is triggered count TOLimit 1 times	
		1111	16x CLK_{PS} Cycle
		1110	15x CLK_{PS} Cycle
		1101	14x CLK_{PS} Cycle
		1100	13x CLK_{PS} Cycle
		1011	12x CLK_{PS} Cycle
		1010	11x CLK_{PS} Cycle
		1001	10x CLK_{PS} Cycle
		1000	9x CLK_{PS} Cycle
		0111	8x CLK_{PS} Cycle
		0110	7x CLK_{PS} Cycle
		0101	6x CLK_{PS} Cycle
		0100	5x CLK_{PS} Cycle
		0011	4x CLK_{PS} Cycle
		0010	3x CLK_{PS} Cycle
		0001	2x CLK_{PS} Cycle
		0000	1x CLK_{PS} Cycle

22.7.4. I2C Control Register3

Slave ID0 (SID0)

I2C Base Address + 0X0C (0X4100C)				
Symbol	I2CCR3 (I2C Control Register 3)			
Bit	[31:24]		[23:16]	
Name	SID_1 MASK		SID_0 MASK	
RW	R0W-0		R0W-0	
Bit	[15:9]	[8]	[7:1]	[0]
Name	SID_1	VD1	SID_0	VD0
RW	RW-0		RW-0	

Bit	Name	Description	
Bit[31~24]	SID1 MASK	SID1 MASK	
		0	Disable
		1	Enable
Bit[23~16]	SID0 MASK	SID0 MASK	
		0	Disable
		1	Enable
Bit[15~9]	SID1	SID1 ID Number	
		0	Set 0
		1	Set 1
Bit[08]	Valid1	Slave ID_1 Valid Control	
		0	Slave ID0 Invalid
		1	Slave ID0 Valid
Bit[7~1]	SID0	SID0 ID Number	
		0	Set 0

		1	Set 1
Bit[00]	Valid0	Slave ID_0 Valid Control	
		0	Slave ID1 Invalid
		1	Slave ID1 Valid

22.7.5. I2C Control Register4

I2C Base Address + 0X10 (0X41010)			
Symbol	I2CCR4 (I2C Control Register 4)		
Bit	[31:16]		
Name	RSV.		
RW	R-0		
Bit	[15:8]	[7:1]	[0]
Name	RSV	Rx A7-1/D7-1	RW/D0
RW	R-0	R-X	

Bit	Name	Description	
Bit[7~1]	Rx A7-1/D7-1	Receiver Address/Data Buffer Bit 7-1	
		0	Set 0
		1	Set 1
Bit[0]	RW/D0	Receiver RW Field or Data Buffer Bit 0	
		0	Set 0
		1	Set 1

22.7.6. I2C Control Register5

Transmitter Data Buffer 0 (TXAD)

I2C Base Address + 0X14 (0X41014)			
Symbol	I2C 5 (I2C Control Register 5)		
Bit	[31:24]	[23:17]	[16]
Name	RSV.	TX2 A7-1/D7-1	Flag/D0
RW	R-0	RW-X	
Bit	[15:08]	[7:1]	[0]
Name	TX1 A7-0/D7-0	TX0 A7-1/D7-1	RW/D0
RW	RW-X		

Bit	Name	Description	
Bit[23~17]	TX2 A7-1/D7-1	TX2:Transmitter Address/Data Buffer Bit 7-1	
		0	Set 0
		1	Set 1
Bit[16]	Flag/D0	TX2:Transmitter RW Field or Data Buffer Bit 0	
		0	Set 0
		1	Set 1
Bit[15~8]	TX1 A7-0/D7-0	TX1:Transmitter Address/Data Buffer Bit 7-0	
		0	Set 0
		1	Set 1
Bit[7~1]	TX0 A7-1/D7-1	TX0:Transmitter Address/Data Buffer Bit 7-1	
		0	Set 0
		1	Set 1

Bit[00]	RW/D0	TX0:Transmitter RW Field or Data Buffer Bit 0	
		0	Set 0
		1	Set 1

Note:

(1) In the communication process when the unit is non-Address or Data transmission status register must be set to this 0XFF.

(2) Because TXAD of Bit 7 to 0 it is possible to SDA Bus lock on Low.

23. Real Time Clock Management

23.1. Introduction

The real time clock controller provides the real time clock and calendar.
The clock source of the RTC is from the external 32.768 KHz crystal connected to the I/O port or the internal 35 kHz LPO oscillator.
The RTC controller shows the time information about hour/minute/second by binary coded decimal (BDC) and the calendar information about year/month/day.
The controller has a programmable alert interrupt program and a periodically programmable wake-up interrupt program, such that the system can be automatically wakened to deal with the low power mode. The controller further has a 6-bit digital timing crystal oscillator offset compensation mechanism.

Function: The time information (hour/minute/second) and the date information (year/month/day) are stored in the register.
Alert register (year/month/day/hour/minute/second)
All time and date information are shown by the BCD format.
Leap automatic compensation (years: 2012~2099)
Week counter
6-bit digital timing crystal oscillator offset compensation
Support periodically wake up the CPU from the idle mode.
Support 8 periodical wake-up period options: 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, and 1
Support two time modes, 12/24 systems.

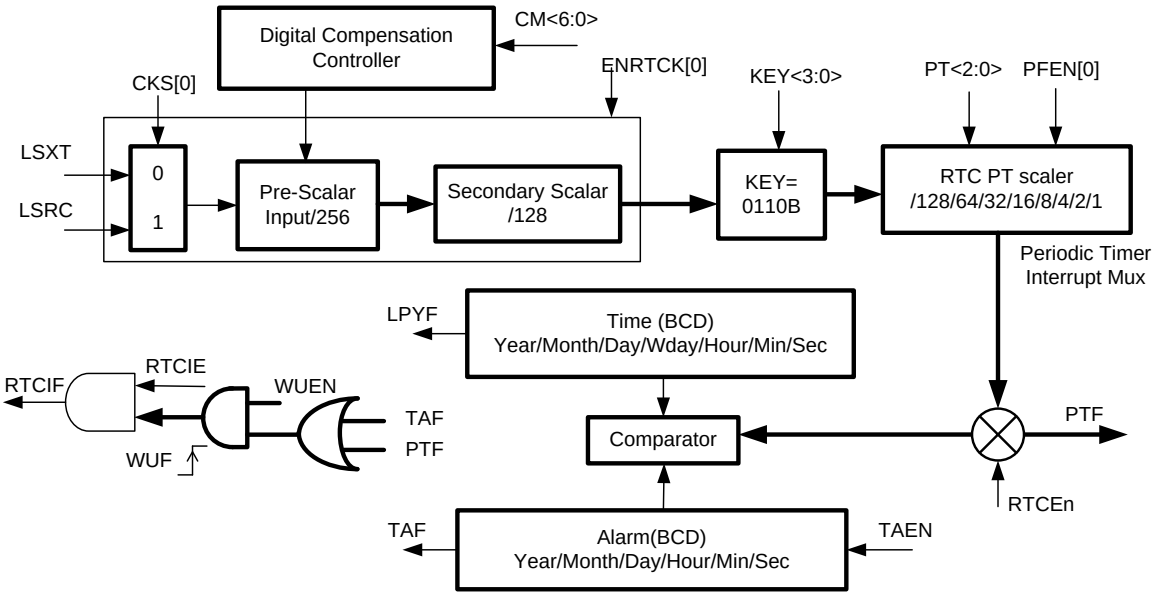


FIG. 24-1 RTC structure diagram

Access the RTC register:

The frequency of the RTC clock is different from that of the system clock; thus the register will be updated after two RTC clock pulses if the user has written new data in the register. The RTC data should be updated frequently.

A protection button for writing data in the register is provided.

When writing data in the RTC register, the RTKEY button should be set as <0110>, and other values of the RTKEY button will not allow any data to be written in the RTC register. Please note that the RTC will not check the data format written in the register; thus, the user should be extremely careful with the write-in operation.

Enable the RTC:

It is necessary to write <0110> in the KEY 0x41A00 [23:20] before writing data into the RTC register.

If the user wants to enable the RTC, the user should check whether the LSXT or LSRC can be used first. Then, set the RTCEN 0x41A00 [0] as <1>.

Frequency compensation:

The RTC allows the digital compensation for the clock input. The central frequency of the RTC is 32768Hz.

Any imperfect operations may result in the frequency offset. The digital compensation can be used to reduce the frequency offset.

The compensation method is to execute +/-2ppm at each step; the permissible maximal frequency change is +126ppm, and the permissible minimal frequency change is -126ppm. The maximal input frequency is 32772Hz, and the minimal input frequency is 32763Hz.

The maximal reference frequency that the user can input is 10MHz to measure the RTC clock during the manufacturing period.

The measurement value is calculated to obtain the compensation value. Then, the compensation value will be stored in the flash memory.

Once the system starts up, the compensation value will be loaded into the CM 0x41A04[22:16].

Time information:

The time information is stored in the 0x41A08 and 0x41A0C registers, which use BCD format.

The user can set the time as the 24 hour system or 12 hour (AM/PM) system.

The time default value is 00:00:00 (hour/minute/second), and it is 24 hour system.

Calendar information:

The calendar information is stored in the 0x41A10 and 0x41A14 registers, which use BCD format. The algorithm for leap year is performed by the hardware.

The effective year period is between 2012~2099. If the LPYF0x41A00 [19] is <1>, it is the leap year.

The year is expressed by two digits, which stands for 20xx year. The default date after the system is reset is 12/1/1 Sunday (January 2, 2012).

The maximal year is 99; and the year will become 00/1/1 after 99/12/31; but the leap year compensation will fail if the above condition takes place.

Week counter:

The RTC controller provides the information about one week. The WDA0x41A14 [2:0] value is defined from 0 to 6, which stands for Sunday to Saturday respectively.

TAF Clock Alert interrupts:

If the 0x41A08/0x41A0C/0x41A10/0x41A14registers, conform to the registers, 0x41A18/0x41A1C and the TAEN 0x41A00 [03] is 1, the TAF0x41A00 [16] interrupt flag will be set as <1> to MCU.

PTF Periodic timer interrupts:

The periodic timer has 8 periodic options for interrupt: 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.

Set the PTF 0x41A00 [18] as <1> to enable the periodic timer interrupt. These periodic options are controlled by the PT0x41A04 [2:0].

WUF System wake-up interrupt:

When the MCU enters the idle mode, it can be wakened by the system wake-up interrupt program.

There are two sources able to wake up the MCU: the periodic timer interrupt and alert interrupt. Set the WUF 0x41A00 [17] as <1> to enable the interrupt program.

23.2. Register Address

RTC Register Address	31 24	23 16	15 8	7 0
RTC base address + 0X00 (0X41A00)	RTKEY	RTCC1	RTCC0M	RTCC0
RTC base address + 0X04 (0X41A04)	RTCOM	RTCO	RTCPTM	RTPT
RTC base address + 0X08 (0X41A08)	-	-	RTHRM	RTHR
RTC base address + 0X0C (0X41A0C)	RTMIM	RTMI	RTSEM	RTSE
RTC base address + 0X00 (0X41A10)	RTYEM	RTYE	RTMOM	RTMO

RTC base address + 0X04 (0X41A14)	RTDAM	RTDA	RTWDM	RTWDA
RTC base address + 0X08 (0X41A18)	-	RCHR	RCMI	RCSE
RTC base address + 0X0C (0X41A1C)	-	RCYE	RCMO	RCDA

-Reserved

23.3. Register Functions

23.3.1. RTC Register0

RTC Base Address + 0X00 (0X41A00)								
Symbol	RTCCR0 (RTC Control Register 0)							
Bit	[31:24]	[23:20]			[19]	[18]	[17]	[16]
Name	MASK	KEY			LPYF	PTF	WUF	TAF
RW	R0W-0	RW-0			R-0	RW0-0	R-0	RW0-0
Bit	[15:08]	[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Name	MASK	-	PTEN	WUEN	TAEN	HRF	CKS	RTCEN
RW	R0W-0	-	RW-0					

Bit	Name	Description	
Bit[23-20]	KEY	The protection key for the RTC register	
		0110	Enable to change the RTC register value
		Others	Disable to change the RTC register value
Bit[19]	LPYF	Leap Year Flag	
		0	Current year is not leap year
		1	Current year is leap year
Bit[18]	PTF	Periodic Timer Flag	
		0	Normal
		1	The Periodic Timer Interrupt is triggered
Bit[17]	WUF	Wakeup Interrupt Flag	
		0	Normal
		1	The Wakeup Interrupt is triggered
Bit[16]	TAF	Alarm Flag	
		0	Normal
		1	The Alarm Interrupt is triggered
Bit[05]	PFEN	RTC periodic timer output enable control	
		0	Disable
		1	Enable
Bit[04]	WUFEN	RTC wake up flag enable control	
		0	Disable
		1	Enable
Bit[03]	TAEN	RTC alarm flag enable control	
		0	Disable
		1	Enable
Bit[02]	HRF	RTC hour format (24/12)	
		0	The hour format by 24
		1	The hour format by 12 (PM/AM)
Bit[01]	CKS	RTC clock input source	
		0	External low speed crystal source
		1	Internal low speed oscillator source
Bit[00]	RTCEN	Real timer clock enable control	
		0	Disable the RTC block
		1	Enable the RTC block

Precautions:

(1) RTC Clock Source Selection "CKS" has a foolproof protection under LSXT but if CKS select Enable LSXT not the case, the circuit will automatically switch to LSRC as clock source.

(2) When the RTC is set to work in 24-hour time, RTC hours (Hour) units ranges from 0 to 23 counts cycle count, when the RTC is set to work in 12-hour time, RTC hours (Hour) unit count range loop count is 0 to 11

(3) When the HRF control bit is set to <1> of time, that is working in 12-hour, then if you want to do a write operation to the RTC time, in hours (Hour) units, if more than the number 12 will cause RTC invalid write operation.

(4) RTC register data is written should be noted that, if set to <0> control bits in the HRF time, that is working in 24-hour format, writing in time if it is greater than 12 hours, information can be normal write into the RTC register. And then if then HRF control bit is set to <1> when the RTC registers will result in the hours count-up unit constantly up, this time, even set to work in 12-hour, hour units do not count will be the loop count from 0 to 11, there will be an exception condition occurs.

23.3.2. RTC Register1

RTC Base Address + 0X04 (0X41A04)					
Symbol	RTCCR1 (RTC Control Register 1)				
Bit	[31:24]	[23]	[22:16]		
Name	MASK	-	CM		
RW	R0W-0	-	RW-0		
Bit	[15:08]	[7:5]	[4]	[3]	[2:0]
Name	MASK	-	CKH	-	PT
RW	R0W-0	-	RW-0	-	RW-0

Bit	Name	Description	
Bit[22~16]	CM	It is clock divider frequency compensation register	
		0111111	+126 PPM to compensation crystal oscillator (max value)
		0111110	+124 PPM to compensation crystal oscillator
		…	STEP: +2 PPM to compensation crystal oscillator
		0000001	+2 PPM to compensation crystal oscillator
		0000000	0 PPM to compensation crystal oscillator
		1000000	0 PPM to compensation crystal oscillator
		1000001	-2 PPM to compensation crystal oscillator
		…	STEP: -2 PPM to compensation crystal oscillator
		1111110	-124 PPM to compensation crystal oscillator
		1111111	-126 PPM to compensation crystal oscillator (min value)
Bit[4]	CKH	RTC High Speed Clock Source Enable	
		0	Control by CKS
		1	CPU Clock
Bit[2~0]	PT	The periodic timer frequency selection	
		000	1/128 second
		001	1/64 second
		010	1/32 second

		011	1/16 second
		100	1/8 second
		101	1/4 second
		110	1/2 second
		111	1 second

23.3.3. RTC Register2

RTC Base Address + 0X08 (0X41A08)					
Symbol	RTCHRC (RTC Hour Control Register For calendar)				
Bit	[31:16]				
Name	RSV				
RW	R-0				
Bit	[15:08]	[7]	[6]	[5:4]	[3:0]
Name	MASK	-	PM	10HR	1HR
RW	R0W-0	-	RW-0		

Bit	Name	Description	
Bit[6]	HRPM	The indicator for am/pm format	
		0	AM or in 24 hour format
		1	PM (can be write 1 if RTHRF is set to 1)
Bit[5~4]	10HR	The ten digits for hour (BCD format)	
		00	0
		01	1
		10	2 (HRF when is 0) / Not available (HRF when is 1)
		11	Not available
Bit[3~0]	1HR	The single digits for hour (BCD format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Others	Not available

23.3.4. RTC Register3

RTC Base Address + 0X0C (0X41A0C)				
Symbol	RTCSMC (RTC seconds and min Control Register For calendar)			
Bit	[31:24]	[23]	[22:20]	[19:16]
Name	MASK	-	10MIN	1MIN
RW	R0W-0	-	RW-0	RW-0
Bit	[15:08]	[07]	[06:04]	[03:00]
Name	MASK	-	10SEC	1SEC
RW	R0W-0	-	RW-0	RW-0

Bit	Name	Description	
Bit[22~20]	10MIN	The ten digits for minute (BCD format)	
		000	0
		001	1
		010	2
		011	3
		100	4
		101	5
		110	6
		111	Not available
Bit[19~16]	1MIN	The single digits for minute (BCD format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Others	Not available
Bit[6~4]	10SEC	The ten digits for second (BCD format)	
		000	0
		001	1
		010	2
		011	3
		100	4
		101	5
		110	6
		111	Not available
Bit[3~0]	1SEC	The single digits for second (BCD format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Others	Not available

23.3.5. RTC Register4

RTC Base Address + 0X10 (0X41A10)				
Symbol	RTCYMC (RTC Year and Month Control Register For Calendar)			
Bit	[31:24]	[23:20]		[19:16]
Name	MASK	10YEAR		1YEAR
RW	R0W-0	RW-1		RW-2
Bit	[15:08]	[07:05]	[04]	[03:00]
Name	MASK	-	10MO	1MO
RW	R0W-0	-	RW-0	RW-1

Bit	Name	Description	
Bit[23~20]	10YEAR	The ten digits for year (BCD format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Others	Not available
Bit[19~16]	1YEAR	The single digits for year (BCD format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Others	Not available
Bit[4]	10MO	The ten digits for month (BCD format)	
		0	0
		1	1
Bit[3~0]	1MO	The single digits for month (BCD format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Others	Not available

23.3.6. RTC Register5

RTC Base Address + 0X14 (0X41A14)				
Symbol	RTCDWC (RTC Date and week Control Register For calendar)			
Bit	[31:24]	[23:22]	[21:20]	[19:16]
Name	MASK	-	10DAT	1DAT
RW	R0W-0	-	RW-0	RW-1
Bit	[15:08]	[07:03]		[02:00]
Name	MASK	-		WDA
RW	R0W-0	-		RW-0

Bit	Name	Description	
Bit[21~20]	10DAT	The ten digits for date (BCD format)	
		00	0
		01	1
		10	2
		11	3
Bit[19~16]	1DAT	The single digits for date (BCD format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Others	Not available
Bit[2~0]	WDA	The single digits for week day (BCD format)	
		000	Sunday
		001	Monday
		010	Tuesday
		011	Wednesday
		100	Thursday
		101	Friday
		110	Saturday
		111	Not available

23.3.7. RTC Register6

RTC Base Address + 0X18(0X41A18)							
Symbol	RTCHRA (RTC Hour and min and seconds Control Register for alarm)						
Bit	[31:24]			[23]	[22]	[21:20]	[19:16]
Name	RSV			-	CPM	10CHR	1CHR
RW	R-0			-	RW-0		
Bit	[15]	[14:12]	[11:8]	[7]	[6:4]	[3:0]	
Name	-	10CMI	1CM1	-	10CSE	1CSE	
RW	-	RW-0		-	RW-0		

Bit	Name	Description	
Bit[22]	CPM	Alarm The indicator for am/pm format	
		0	AM or in 24 hour format

		1	PM (can be write 1 if RTHRF is set to 1)
Bit[21~20]	10CHR	Alarm The ten digits for calendar hour (BCD format)	
		00	0
		01	1
		10	2 (RTHRF when is 0) / Not available (RTHRF when is 1)
		11	Not available
Bit[19~16]	1CHR	Alarm The single digits for hour (BCD format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Others	Not available
Bit[14~12]	10CMI	Alarm The ten digits for calendar minute (BCD format)	
		000	0
		001	1
		010	2
		011	3
		100	4
		101	5
		110	6
		111	Not available

Bit	Name	Description	
Bit[11~8]	1CMI	Alarm The single digits for minute (BCD format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Others	Not available
Bit[6~4]	10CSE	Alarm The ten digits for calendar second (BCD format)	
		000	0
		001	1
		010	2
		011	3
		100	4
		101	5
		110	6
		111	Not available
Bit[3~0]	1CSE	Alarm The single digits for second (BCD format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4

		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Others	Not available

23.3.8. RTC Register7

RTC Base Address + 0X1C(0X41A1C)						
Symbol	RTCYMDA (RTC Year /month/date Control Register For alarm)					
Bit	[31:24]			[23:20]		[19:16]
Name	RSV			10CYE		1CYE
RW	R-0			RW-1		RW-2
Bit	[15:13]	[12]	[11:8]	[07]	[06:04]	[03:00]
Name	-	10CMO	1CMO	-	10CDAT	1CDAT
RW	-	RW-0	RW-1	-	RW-0	RW-1

Bit	Name	Description	
Bit[23~20]	10CYE	The ten digits for calendar year (BCD format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Others	Not available
Bit[19~16]	1CYE	The single digits for calendar year (BCD format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Others	Not available
Bit[12]	10CMO	The ten digits for calendar month (BCD format)	
		0	0
		1	1

Bit	Name	Description	
Bit[11~8]	1CMO	The single digits for calendar month (BCD format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4

		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Others	Not available
Bit[5~4]	10CDAT	The ten digits for calendar date (BCD format)	
		00	0
		01	1
		10	2
		11	3
Bit[3~0]	1CDAT	The single digits for calendar date (BCD format)	
		0000	0
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001	9
		Others	Not available

24. HYCON Note 32

Type	Description	Initial
-	No Use	
RSV.	Reserve	
X	Unknown	
W	Write	
R	Read	
R0	Only Read 0	
R1	Only Read 1	
W0	Only Write 0	
W1	Only Write 0	
RW-0	Read/ Write	Initial 0
RW-1	Read/ Write	Initial 1
R0W-0	Read 0/ Write	Initial 0
R1W-1	Read 1/ Write	Initial 1
R-X	Read	Initial 1 or 0 Unknown

25. Revision History

The following describes the files are quite different places, and punctuation and font changes not described ranges.

Version	Page	Summary of Changes	Date
V01	ALL	First edition	20130520
V02	ALL	ADD Wait Mode at CH4	20130930
	ALL	Chinese version release	20130930
V03	ALL	8-BIT RESISTANCE LADDERS unified correct name for the 8-bit Resistance Ladders (digital resistor)	20131007
	ALL	HSXT external oscillator amended highest range of 16MHz	
V04	CH5	Figure 5.1 is a functional block diagram describes REFOI correct name REFO_I	20140310
	CH7	Strengthening instructions for interrupt vector priority level	
V05	CH17	ADC input network OPO corrected to OPOI, REFO corrected as REFO_I	20150609
	CH18	OPAMP network OPNS [3] corrected to OPOI, OPNS [4] corrected to OPO, R2ROP output Description Correction	
V06	CH19	8-bit Resistance Ladders network input REFO corrected to REFO_I	20150911
	CH22	Parity bit function description revised, enhance description of ENADD bit function	
V07	CH24	Revised HRF control bit description of Chapter. RTC, and add using notices	20151116
V08	1 9 15~19	1. Change the title to HY16F184/HY16F187/HY16F188 User's Guide. 2. CH2 IC IO pin function table Delete PT4.0. 3. Correct the Power Management description.	20160322
V09	 21	1. Add HAO calibration method description. 2. Modify the WDT profile and description	20160524
V10	38~39 76~81 82~86 116 114 93 45&51 43 143 144 All 100 56	1. Modify Ch12 GPIO PT1 Management 2. Modify Ch12 GPIO PT2 Management 3. Modify Fig 18-1 OPAMP function block diagram 4. Add Power Mode (Enter Sleep) description. 5. Add Chapter 14.4 Analog to digital multiplexing function Switchover Considerations description. 6. Modify Timer A & Timer B description 7. Modify the 8.3.1 WDT register description 8. Modify SPI Diagram 9. Modify CPHA description 10. Remove the sample program description 11. Modify CH17 Power Mode description. 12. Modify PWM initialize operation description 13. Modify CH5 Power Management block diagram	20170213

	17 39	14. Modify CH8 WDT block diagram	
V11	ALL	1. Remove the GPIO multiplex function of the PT3.2 / PT3.3 pin, which only retains the AIO4 / AIO5 analog function. 2. Modify the PWMA to PWMG description to PWM Duty Cycle = (PWM Duty) * (PWM Period) 3. Modify the TPS initialization settings and calculation methods. 4. Added ADC input impedance (R_{ADC}) description, ADC network diagram (ADCLK renamed ADCK). 5. Added RTC / WDT / TMA / TMB / TMC0 / TMC1 interrupt request flag trigger condition description. 6. Modify R_{PU}=85k (internal pull high resistor) description. 7. Modify 8-bit Resistance Ladder figure 19-2 block diagram. 8. Modify CH5.3.1 ENRFO control bit description.	20171006