



# **HY-ADC ENOB Test User's Manual**

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## 1. ENOB and Noise Free Description

$$\text{ENOB} = \log_2 \left( \frac{\text{FSR}}{\text{RMS Noise}} \right) = \frac{\ln \left( \frac{\text{FSR}}{\text{RMS Noise}} \right)}{\ln(2)} \quad \text{Equation 1}$$

$$\text{Noise Free Bits} = \log_2 \left( \frac{\text{FSR}}{\text{Peak - to - Peak Noise}} \right) = \frac{\ln \left( \frac{\text{FSR}}{\text{Peak - to - Peak Noise}} \right)}{\ln(2)} \quad \text{Equation 2}$$

RMS Noise that generated from Sigma Delta ADC is the minimum voltage value of distinguishable sampling signal. Hence, ENOB (Effective Number of Bits) is calculated by RMS Noise and Full Scale Range ratio. However, RMS Noise must be calculated by many average times. Insufficient sampling times can only represent RMS Noise for a specific period of time instead of the RMS Noise of the entire ADC operation. Therefore, RMS Noise operation times cannot be less than 1024 times.

However, Noise Free Bit represents that ADC output value count is not rolling. Noise Free Bits are stable ADC output performance. Bit operation is defined as Peak-to-Peak Noise and Full Scale Range ratio.

RMS Noise Calculation:

$$\text{Average Counts} \rightarrow \text{Average} = \frac{\sum_{k=1}^n \text{ADC}[k]}{n} \quad \text{Equation 3}$$

n = Total ADC sampling times.

$$\text{RMS Noise} = \frac{V_{\text{REF}} \times \sqrt{\frac{\sum_{k=1}^n (\text{ADC}[k] - \text{Average})^2}{n}}}{2^{\text{Scale}}} \quad \text{Equation 4}$$

Scale = Total ADC Output Bits

Peak-to-Peak Noise Calculation:

$$\text{Peak - to - Peak Noise} = \frac{V_{\text{REF}} \times (\text{ADC}_{\text{Max}} - \text{ADC}_{\text{Min}})}{2^{\text{Scale}}} \quad \text{Equation 5}$$

ADCMax = Maximum ADC value of total sample

ADCMin = Minimum ADC value of total sample

## 2. Software Description

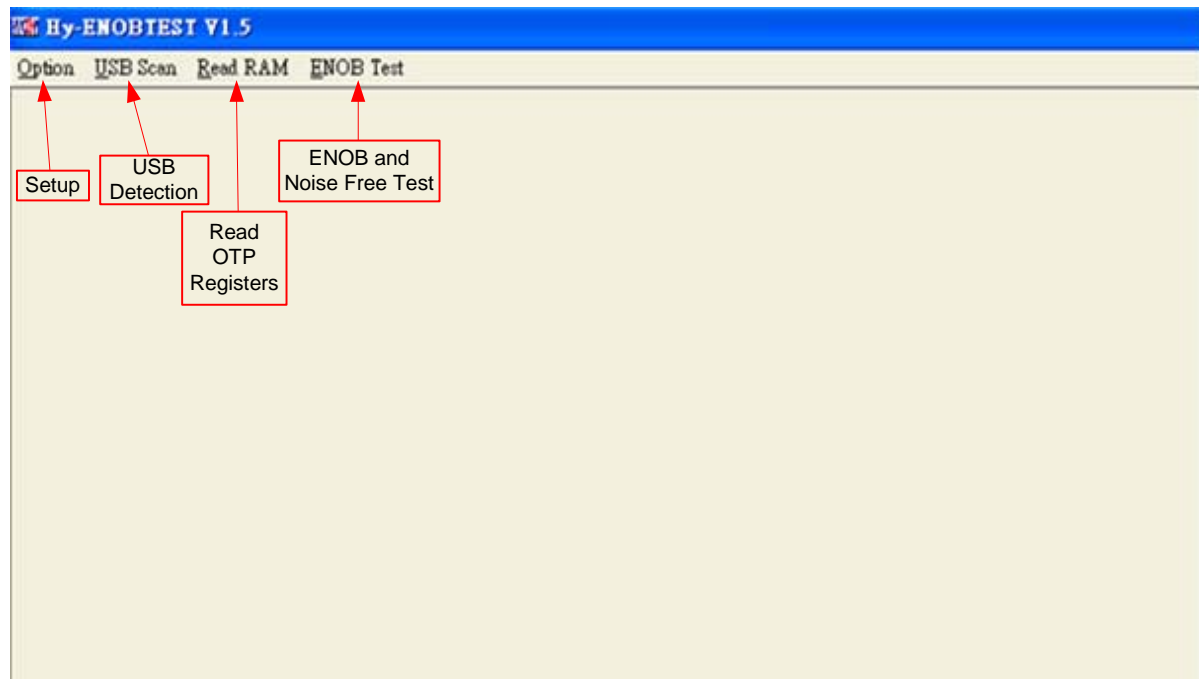


Figure 1

### 2.1 Option

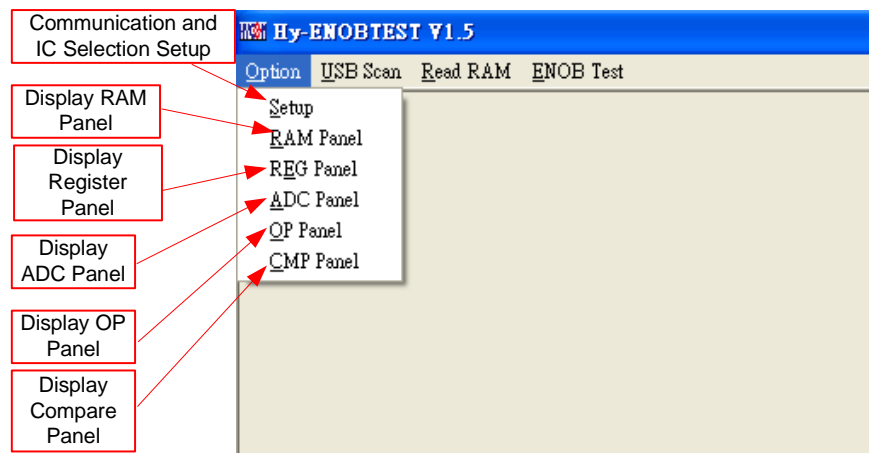


Figure 2

## 2.1.1 Setup

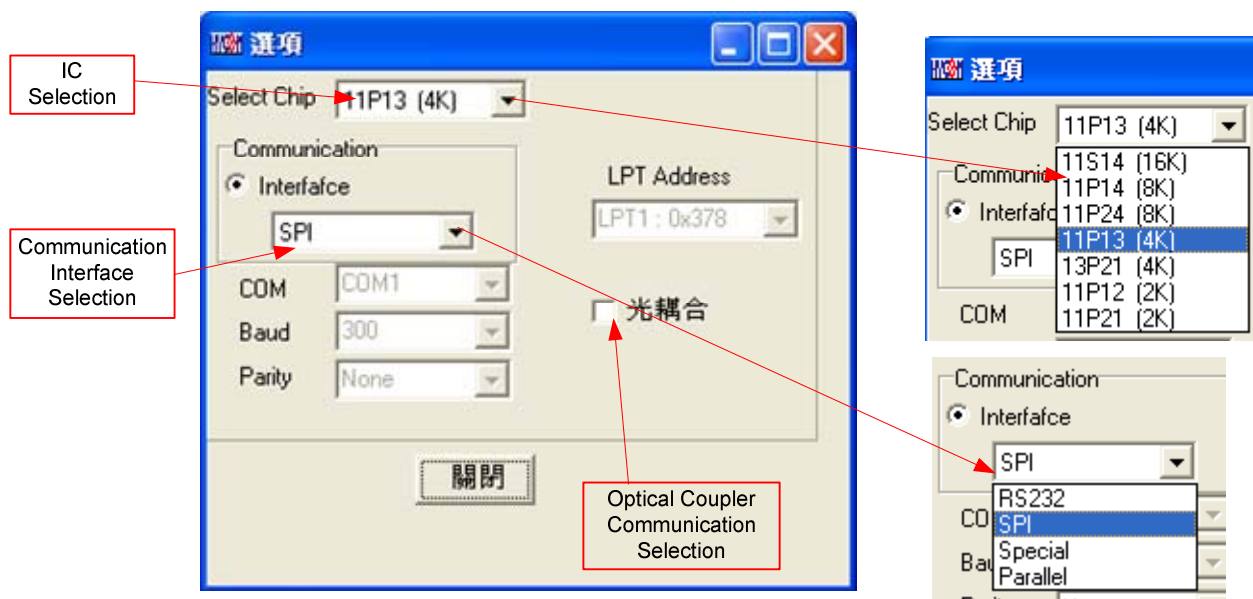


Figure 3

### 1. IC Selection

Choose OTP IC, OTP IC program needs to add-in SPI or Special communication program.

### 2. Communication Interface Selection

Only SPI or Special is selectable. The function is not supportive for other interface.

### 3. Optical coupler Selection

The option used when choosing optical coupler as isolator of communication interface.

## 2.1.2 RAM Panel

記憶體 - 11P13 (4K)																
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000	02	02	02	02	02	02	06	06	02	02	-	-	-	-	-	00
010	10	00	92	-	-	-	07	3C	04	-	00	00	-	09	7A	7D
020	60	00	18	4A	04	-	00	00	-	00	01	01	10	17	02	-
030	E0	01	01	08	02	02	00	00	-	EE	74	CF	9E	05	E0	6C
040	4C	C0	86	00	FF	00	00	FF	00	00	FF	FF	FF	FF	-	30
050	-	FF	DC	60	00	7A	5B	7B	7A	7D	10	00	00	00	83	-
060	00	00	-	-	-	-	-	-	-	-	-	-	-	99	20	00
070	DF	00	04	-	1F	E0	-	1F	00	00	-	-	-	-	-	-
080	95	92	8B	0A	00	10	00	03	09	05	03	00	01	03	00	00
090	00	00	00	8C	08	00	00	00	00	00	00	00	00	00	00	00
0A0	00	00	0E	0E	05	00	01	00	3C	00	00	00	00	06	EE	D2
0B0	74	EE	A6	73	FF	00	A0	00	00	00	00	00	00	00	00	00
0C0	00	00	00	00	01	00	00	00	00	00	00	00	AA	00	00	00
0D0	00	00	50	FD	98	74	EE	98	74	EE	99	74	EE	B8	74	EE
0E0	D5	74	EE	CF	74	EE	D4	74	EE	07	75	EE	00	04	00	00
0F0	08	00	A6	73	01	13	FF	00	F8	00	C0	3D	95	00	95	00

Figure 4

Please refer to Chapter 3.2 RAM Window Operation of HY-IDE Software User's Manual.

## 2.1.3 REG Panel

**寄存器 - 11P13 (4K)**

IND0: M[010] = 10    Program Counter: 0  
 IND1: M[092] = 00    Work: 00    Cycle: FE9C0000

Byte								
INDF0	POINC0	PODEC0	PRINC0	PLUSW0	INDF1	POINC1	PODEC1	PRINC1
02	02	02	02	02	02	06	06	02
PLUSW1	WREG	BSR	ADCORH	ADCCORM	ADCCORL	TMAR	PRC	TMCR
02	00	01	EE	74	CF	86	FF	00
PWMR	SSPBUF	LCD0	LCD1	LCD2	LCD3	LCD4	LCD5	LCD6
FF	00	00	7A	5B	7B	7A	7D	10
LCD7	LCD8	LCD9						
00	00	00						

Word								
FSR0	FSR1	TOS	PCLAT	TBLPTR	TBLD	PROD	TMBR	CCP0R
0010	0092	073C	0000	097A	7D60	0018	FF00	FFFF
CCP1R								
FFFF								

PAGE1		PAGE2		PAGE3	
STKPTR	STKFL	STKUN	STKOV	STKPRT3	STKPRT2
INTIE1	GIE	ADICIE	TMCIE	TMAIE	E1IE
INTIE2	-	-	-	-	SSPIE
INTF1	-	ADCIF	TMCIF	TMBIF	WDTIF
INTF2	-	-	-	-	SSPIF
STATUS	-	-	-	C	DC
PSTAUTS	PD	TO	IDLEB	POR	SVS
SVSCN	ENPOR	SVSFG	SVSOP	SVSON	VLDX3
SBMSET1	SKRST	NORADC	RCFTR5	RCFTR4	RCFTR3
PWRCN	ENVDDA	VDDAX1	VDDAX0	ENREF	-
MCKCN1	ADCS2	ADCS1	ADCS0	ADCSK	XTHSP
MCKCN2	-	-	LSCK	HSS1	HSS0
MCKCN3	LCD\$2	LCD\$1	LCD\$0	-	PERCK

Figure 5

Please refer to Chapter 3.3 Register Window Operation of HY-IDE Software User's Manual.

## 2.1.4 ADC Panel

**ADC - 11P13 (4K)**

IN[2:0] = 011    LS\_OK    ENADC    VDDA = 2.40 V

ADCS[2:0] = 000    INH[1:0] = 01    INIS    INX[1:0] = 01    INL[2:0] = 011

ADCCK    VDDA    OSR[2:0] = 111    ADC Output Rate    ADC\_CK / 32768    EE74CF

ADC out mode    ADC out bits    HEX    24    Read ADC

Block Diagram Details:

- Inputs: AI2, AI6, AI4, AI0, VDD, REFO, -TPSH, INH, INIS, INL, AI3, AI7, AI5, AI1, OP00, VSS, -TPSL.
- Internal Blocks: S-1/4 SD16 Chopper on OPAMP-L,  $\Sigma \Delta$  AD, VERBUFF, VERH, VRL.
- Registers: DCSET[2:0] = 101, ADGN[2:0] = 110, PGAGN[1:0] = 11, VRH[1:0] = 10, VRL[1:0] = 10.
- Outputs: VERH, VRL.

Figure 6

Please refer to Chapter 3.6 ADC Window Operation of HY-IDE Software User's Manual.

## 2.1.5 OP Panel

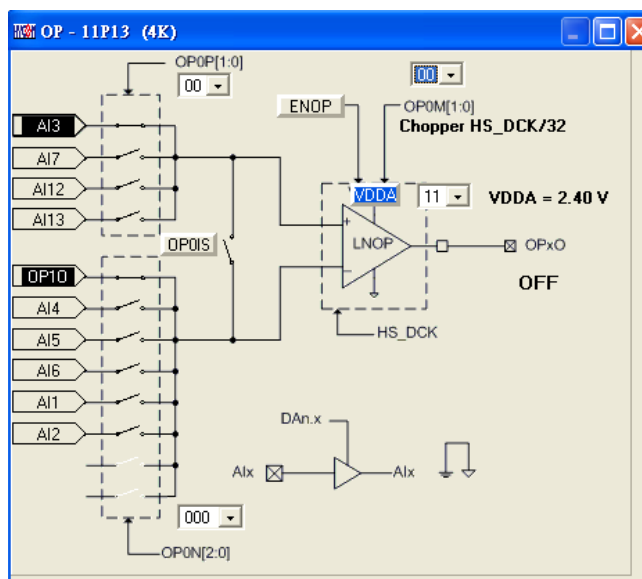


Figure 7

Please refer to Chapter 3.7 OP Window Operation of HY-IDE Software User's Manual.

## 2.1.6 CMP Panel

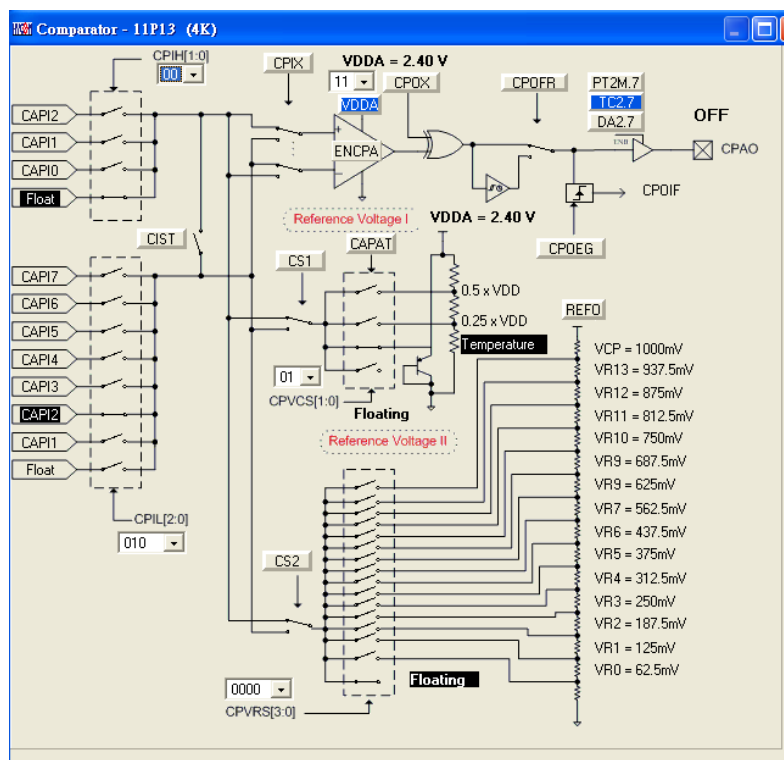


Figure 8

Please refer to Chapter 3.8 Comparator Window Operation of HY-IDE Software User's Manual.

## 2.2 USB Scan

USB scan function help to detect whether USB scan communication port is connected to ENOB Control Board. If it is connected, the status, USB On Line, will be shown in left corner, as Figure 9

displayed.

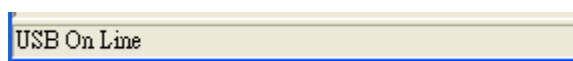


Figure 9

If it is not connected, the status, USB not Connect, will be shown in left corner, as Figure 10 displayed.



Figure 10

PC program will scan once in every minute.

## 2.3 Read RAM

After USB Scan is executed, make sure USB is On Line. Then executes Read RAM, OTP Chip RAM and Registers at this moment, will be written into PC buffer. This will influence RMS Noise and Peak-to-Peak Noise operation of ENOB Test.

## 2.4 ENOB Test

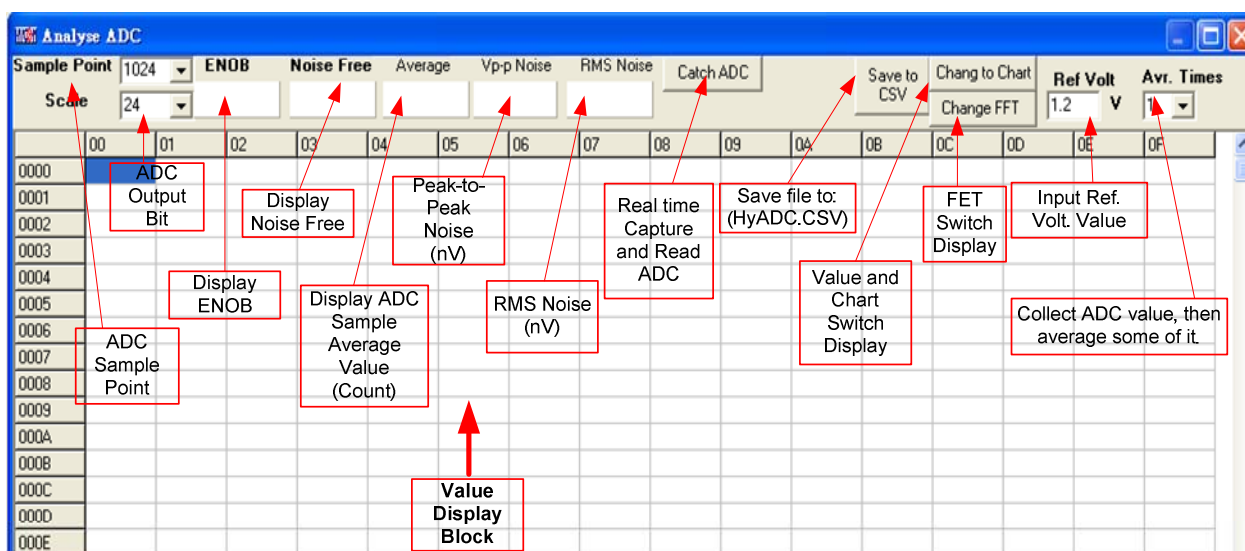


Figure 11

### 1. Sample Point

"Catch ADC" and "Ca.Flash" function of ADC sample point. The minimum OTP ADC sampling output amount is 256, the maximum is 1024.

### 2. Scale

ADC output bits. The minimum of ADC output is 8-bit, maximum is 24-bit.

### 3. ENOB

Display ENOB (Effective Number of Bits). The Calculation is shown as Equation 1. The unit is Bit.

### 4. Noise Free

Display Noise Free Bits. The Calculation is shown as Equation 2. The unit is Bit.

### 5. Average



Display ADC sampling average value. The Calculation is shown as Equation 3. The unit is Count.

6. Vp-p Noise

Display Peak-to-Peak Noise. The Calculation is shown as Equation 3. The unit is nV.

7. RMS Noise

Display RMS Noise. The Calculation is shown as Equation 4. The unit is nV.

8. Catch ADC

Real time catch and display ADC value in sequence in value display block.

9. Save to CSV

Save the value of display block into HyADC.CSV file, including ENOB, Noise Free, Average, Vp-p Noise and RMS Noise.

10. Change To Chart

Change to display chart and value in value display block.

11. Change FFT

Chart switch, displaying frequency domain and time domain.

12. Ref Volt

Input Reference Voltage value (unit is V).

13. Avr. Times

Select software average. Values in the value display block will be averaged based on the selected times, then to be shown in the block.



PIN 6 → VSS

PIN 7 → ICEIRQ\_Q, signal line for detecting whether HYCON OTP writing into Flash Memory is accomplished.

## 2. J4, J5, J8 : Optical Coupler Communication Port

### J4 Description

PIN 1 → VP supplies power to optical coupler IC (U9~U13).

J5 & J8 open → thoroughly separate the power of optical coupler IC and HYCON OTP.

J5 & J8 short → optical coupler IC and HYCON OTP uses the same power

PIN 2 → SPIDI\_Q, DI signal line of optical coupler.

PIN 3 → SPICK\_Q, CK signal line of optical coupler.

PIN 4 → SPIDO\_Q, DO signal line of optical coupler.

PIN 5 → SPICS\_Q, CS signal line of optical coupler.

PIN 6 → VSSP, optical coupler ground.

PIN 7 → SPIIRQ\_Q, signal line (optical coupler) for detecting whether HYCON OTP writing into Flash Memory is accomplished.

## 3. J9, J10, J11 and U8

U8 is Flash Memory that capacitates 512K byte memory.

J10 and J11 is Flash Memory power source.

J10 & J11 pin1-2 short → powered by External (J5-pin1 and J8-pin2)

J10 & J11 pin2-3 short → power is regulated from U3 (J5-pin2 and J8-pin1)

### J9 Description:

PIN 1 → VDD\_X, supplying U8 power.

PIN 2 → FLDI, controlling DI signal line of U8.

PIN 3 → FLCK, controlling CK signal line of U8.

PIN 4 → FLDO, controlling DO signal line of U8.

PIN 5 → FLCS, controlling CS signal line of U8.

PIN 6 → VSS\_X, U8 ground.

## 4. JP1, JP2, J6 and U3

JP1 and JP2 supplies external power to U3 in order to generate VDD power

J6 open → using external power (5V) that inputted from JP1 and JP2.

J6 short → using USB power.

The regulator composed by U3, R1, R2 and R3 generates VDD power. The output voltage can be amended through R1, R2 and R3. The equation is described in below:

$$VDD = 1.240V \times \left(1 + \frac{R1 + R2}{R3}\right)$$

## 4. Revision History

Major differences are stated thereafter:

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Version	Page	Revision Summary
V01	ALL	First edition
V02	9	Delete 2.5 Switch test information.
	ALL	Update all the figures