HY17P60B
Datasheet

8-Bit RISC-like Mixed Signal Microcontroller
Embedded 19-Bit ΣΔADC
With Low Noise OPAMP & 4x20 LCD

Table of Contents

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1. Features

- **8-Bit RISC-like Mixed Signal Microcontroller**
  - 71 high performance H08D instruction sets
  - Hardware Lookup table
  - Power On/ Brown Out 1/ Brown Out 2
  - WDT/MCLR Reset
  - Support Assembly & C compiler environment
- **Operating Voltage and Temperature Range**
  - Digital Circuit: 2.2V ~ 5.5V
  - Analog Circuit: 2.4V ~ 4.5V
  - Operating Temperature: - 40°C ~ 85°C
- **8k Word OTP (One Time Programmable)**
  - Program memory, 512Byte data memory
- **High resolution ΣΔADC**
  - Max. Sampling Frequency up to 1MHz
  - Oversampling Freq. setting:32~61440
  - Second/third order comb filter with conversion frequency of 30.72ksps
  - ADC Gain: x1/2, x1, x2, x4, x8
  - Zero input/output voltage
  - High input impedance (built-in input buffer)
  - Built-in absolute temperature sensor
- **Built-in digital signal processing (DSP) realizes digital AC RMS, Peak Hold and other digital calculation functions**
- **Multi-functional comparator**
  - LVD low voltage detection function with multi-stage detection voltage setting and external input voltage detection function
  - Equipped with delay and latch function, reducing glitch
- **OPA (Low Noise Operational Amplifier)**
  - Combined with external components to achieve AC rectifier filter circuit
- **Analog voltage (VDDA) source equipping with 10mA regulated voltage source output ability, quick start function**
- **1.2V internal analog circuit common-ground voltage source**
- **4x20 LCD driver**
  - 1/4 Duty、1/3 Bias
  - Built-in charge pump regulated circuit, providing multiple LCD bias voltage
  - There are 2 LCD ports with digital input and output ports
- **3 sets of 24-bit programmable counters for frequency and duty cycle measurement.**
- **8-bit Timer A1**
- **16-bit Timer B module with PWM function**
- **UART、I^2C(Master/Slave) module**
- **Built-In EPROM (BIE) ,Built-in 2.75V low voltage programming control circuit**
- **Built-in Brownout and Watch dog timer to prevent the CPU into the crash mode**
- **External Crystal oscillator: 32768Hz or 1M~16MHz.Built-in HAO oscillator, four HAO frequency can be selected: 4.9152MHz, 9. 8304MHz.Mode multiple CPU clock switching options, allowing users to achieve the best power saving plan**
  - Operation mode
  - Idle mode: LPO 14.5kHz
  - Sleep mode
- **Support 8 stack levels.**
- **Package Type**
  - LQFP64
  - QFN32
- **Applications**
  - 2000 Counts DMM
  - Measurement Device
  - Infrared temperature measurement
  - Weighing

2. Pin Definition

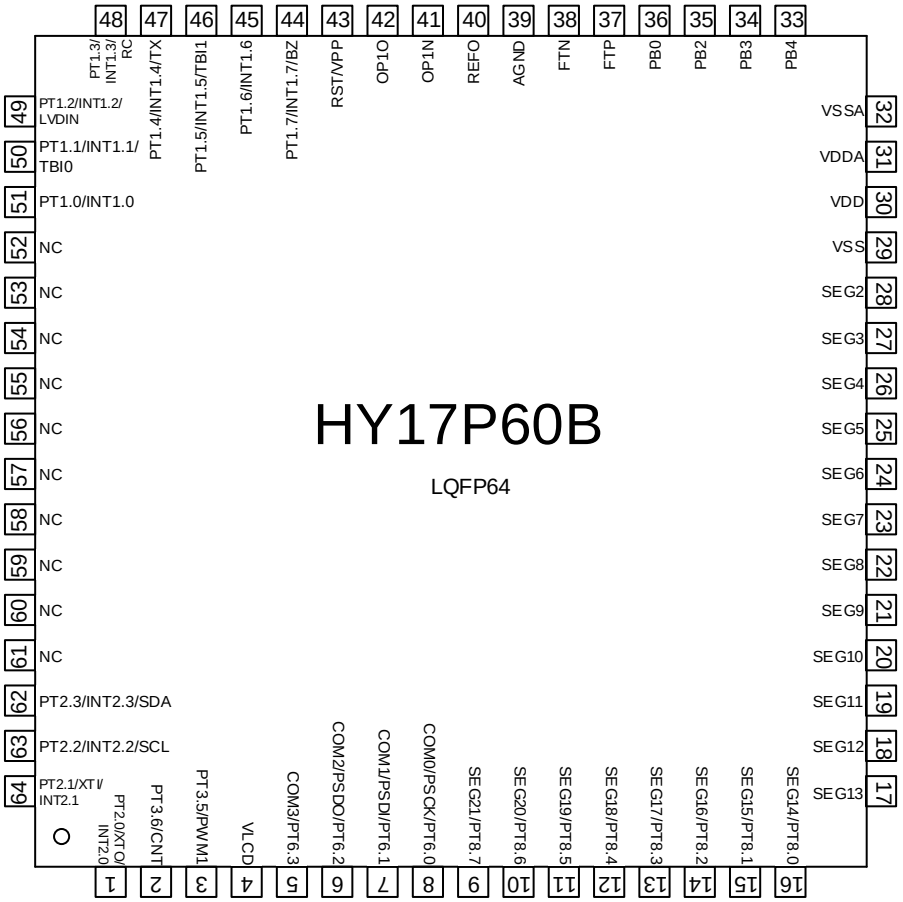


Figure2-1 HY17P60B LQFP64 pin diagram

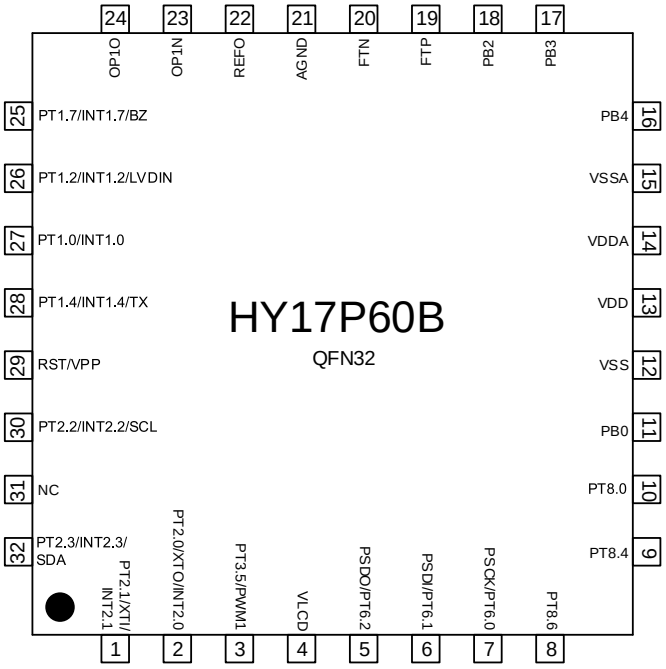


Figure2-2 HY17P60B QFN32 pin diagram

2.1. Pin Description

"I/O" Input/Output, "I" Input, "O" Output, "S" Schmitt Trigger, "C" CMOS, "P" Power, "A" Analog

Pin No.		Name	Characteristic		Description
LQFP64	QFN32		I/O	Type	
1	2	PT2.0/XTO/INT2.0			
		PT2.0	I/O	S/C	Digital input/output
		XTO	A	A	Output port of external oscillator
		INT2.0	I	S	Interrupt source INT2.0
2	-	PT3.6/CNT			
		PT3.6	I/O	S/C	Digital input/output
		CNT	I	S	Input port of frequency counter
3	3	PT3.5/PWM1			
		PT3.5	I/O	S/C	Digital input/output
		PWM1	O	C	PWM1 output port
4	4	VLCD	P	P	Voltage source of LCD ，1~10uF need. (Source: VDD)
5	-	COM3/PT6.3			
		COM3	O	A	COM3 output of LCD
		PT6.3	I/O	S/C	Digital input/output
6	5	COM2/PSDO/PT6.2			
		COM2	O	A	COM2 output of LCD
		PSDO	O	S	PSDO of OTP read/write interface
		PT6.2	I/O	S/C	Digital input/output
7	6	COM1/PSDI/PT6.1			
		COM1	O	A	COM1 output of LCD
		PSDI	I	S	PSDI of OTP read/write interface
		PT6.1	I/O	S/C	Digital input/output
8	7	COM0/PSCK/PT6.0			
		COM0	O	A	COM0 output of LCD
		PSCK	I	S	PSCK of OTP read/write interface
		PT6.0	I/O	S/C	Digital input/output
9	-	SEG21/PT8.7			
		SEG21	O	A	Segment output of LCD
		PT8.7	I/O	S/C	Digital input/output
10	8	SEG20/PT8.6			
		SEG20	O	A	Segment output of LCD
		PT8.6	I/O	S/C	Digital input/output

Pin No.		Name	Characteristic		Description
LQFP64	QFN32		I/O	Type	
11	-	SEG19/PT8.5 SEG19 PT8.5	 O I/O	 A S/C	 Segment output of LCD Digital input/output
12	9	SEG18/PT8.4 SEG18 PT8.4	 O I/O	 A S/C	 Segment output of LCD Digital input/output
13	-	SEG17/PT8.3 SEG17 PT8.3	 O I/O	 A S/C	 Segment output of LCD Digital input/output
14	-	SEG16/PT8.2 SEG16 PT8.2	 O I/O	 A S/C	 Segment output of LCD Digital input/output
15	-	SEG15/PT8.1 SEG15 PT8.1	 O I/O	 A S/C	 Segment output of LCD Digital input/output
16	10	SEG14/PT8.0 SEG14 PT8.0	 O I/O	 A S/C	 Segment output of LCD Digital input/output
17	-	SEG13	O	A	Segment output of LCD
18	-	SEG12	O	A	Segment output of LCD
19	-	SEG11	O	A	Segment output of LCD
20	-	SEG10	O	A	Segment output of LCD
21	-	SEG9	O	A	Segment output of LCD
22	-	SEG8	O	A	Segment output of LCD
23	-	SEG7	O	A	Segment output of LCD
24	-	SEG6	O	A	Segment output of LCD
25	-	SEG5	O	A	Segment output of LCD
26	-	SEG4	O	A	Segment output of LCD
27	-	SEG3	O	A	Segment output of LCD
28	-	SEG2	O	A	Segment output of LCD
29	12	VSS	P	P	Ground end of IC operation voltage source
30	13	VDD	P	P	Voltage source of IC operation · 1~10uF need.

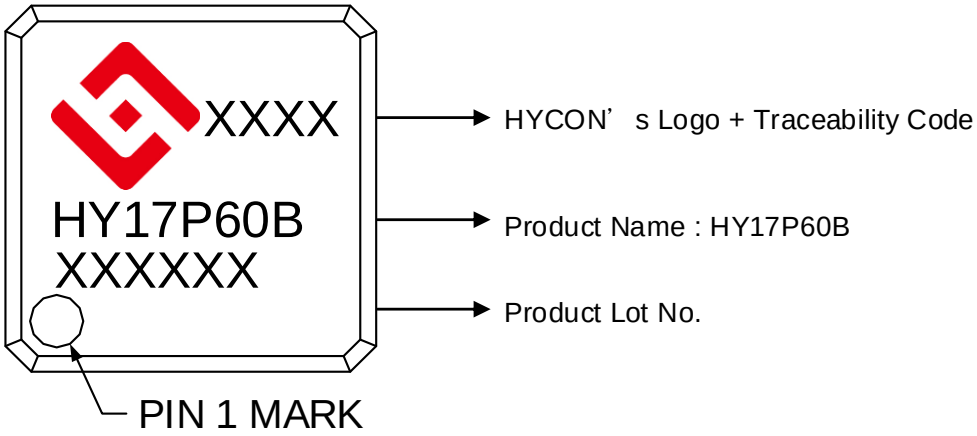
Pin No.		Name	Characteristic		Description
LQFP64	QFN32		I/O	Type	
31	14	VDDA	P	P	Analog circuit voltage source (source: VDD)
32	15	VSSA	P	P	Ground end of IC operation voltage source
33	16	PB4	I	A	Analog input channel
34	17	PB3	I	A	Analog input channel
35	18	PB2	I	A	Analog input channel
36	11	PB0	I	A	Analog input channel
37	19	FTP	I/O	A	Capacitor connect port of pre-filter
38	20	FTN	I/O	A	Capacitor connect port of pre-filter
39	21	AGND	P	P	Analog power ground end (source: VDDA)
40	22	REFO	P	P	Voltage reference port (source: VDDA)
41	23	OP1N	I	A	OPAMP(OP1) negative input terminal
42	24	OP1O	O	A	OPAMP(OP1) output terminal
43	29	RST/VPP			
		RST	I	S	Reset IC (Low active)
		VPP	P	P	EPROM read/write voltage source
44	25	PT1.7/INT1.7/BZ			
		PT1.7	I/O	S/C	Digital input/output
		INT1.7	I	S	Interrupt source INT1.7
		BZ	O	C	Buzzer output port
45	-	PT1.6/INT1.6			
		PT1.6	I/O	S/C	Digital input/output
		INT1.6	I	S	Interrupt source INT1.6
46	-	PT1.5/INT1.5/TBI1			
		PT1.5	I/O	S/C	Digital input/output
		INT1.5	I	S	Interrupt source INT1.5
		TBI1	I	S	TimerB CPI Source Input pin
47	28	PT1.4/INT1.4/TX			
		PT1.4	I/O	S/C	Digital input/output
		INT1.4	I	S	Interrupt source INT1.4
		TX	O	C	UART communication Transfer pin

Pin No.		Name	Characteristic		Description
LQFP64	QFN32		I/O	Type	
48	-	PT1.3/INT1.3/RC			
		PT1.3	I/O	S/C	Digital input/output
		INT1.3	I	S	Interrupt source INT1.3
		RC	I	S	UART communication Receiver Pin
49	26	PT1.2/INT1.2/LVDIN			
		PT1.2	I/O	S/C	Digital input/output
		INT1.2	I	S	Interrupt source INT1.2
		LVDIN	A	A	LVD external signal input port
50	-	PT1.1/INT1.1/TBI0			
		PT1.1	I/O	S/C	Digital input/output
		INT1.1	I	S	Interrupt source INT1.1
		TBI0	I	S	TimerB CPI Source Input pin
51	27	PT1.0/INT1.0			
		PT1.0	I/O	S/C	Digital input/output
		INT1.0	I	S	Interrupt source INT1.0
52~61	31	NC	-	-	Unused (not connectable)
62	32	PT2.3/INT2.3/SDA			
		PT2.3	I/O	S/C	Digital input/output
		INT2.3	I	S	Interrupt source INT2.3
		SDA	I/O	S	SDA of I^2C communication interface
63	30	PT2.2/INT2.2/SCL			
		PT2.2	I/O	S/C	Digital input/output
		INT2.2	I	S	Interrupt source INT2.2
		SCL	I/O	S	SCL of I^2C communication interface
64	1	PT2.1/XTI/INT2.1			
		PT2.1	I/O	S/C	Digital input/output
		XTI	A	A	Input port of external oscillator
		INT2.1	I	S	Interrupt source INT2.1

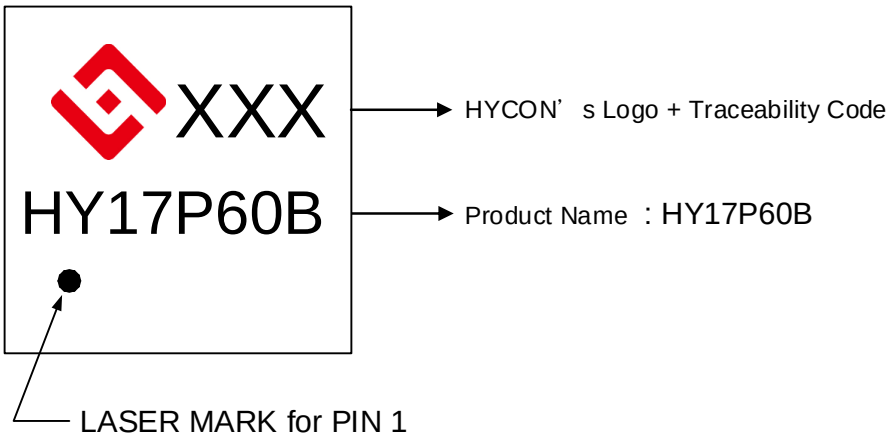
Table 2-1 Pin Definition and Pin Description

2.2. Package marking information

2.2.1. HY17P60B LQFP Package marking information



2.2.2. HY17P60B QFN Package marking information



3. Application Circuit

3.1. 2000 counts manual range DMM

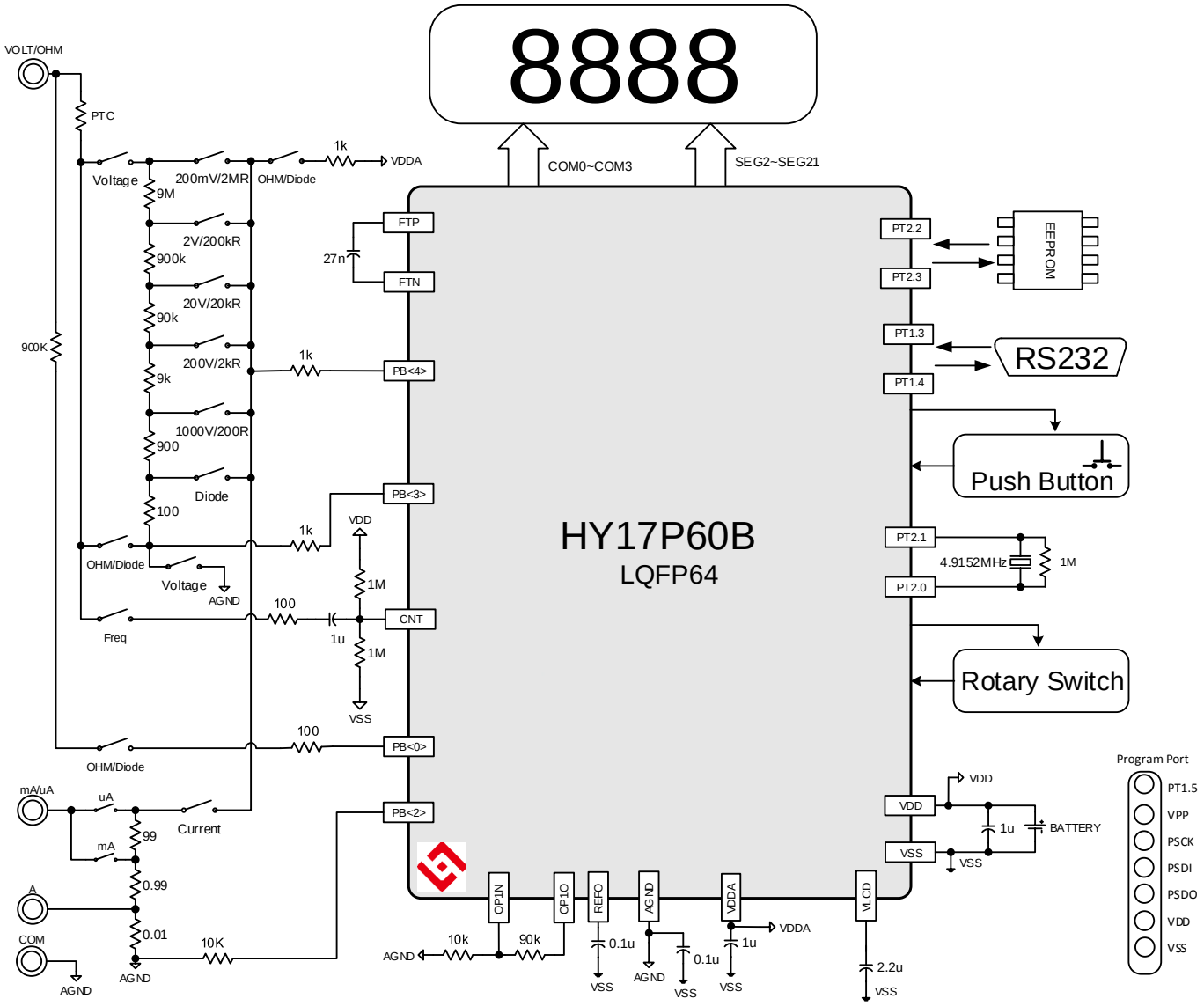


Figure 3-1 HY17P60B 2000 Counts manual range DMM application circuit

3.2. HY17P60B Infrared sensor application circuit

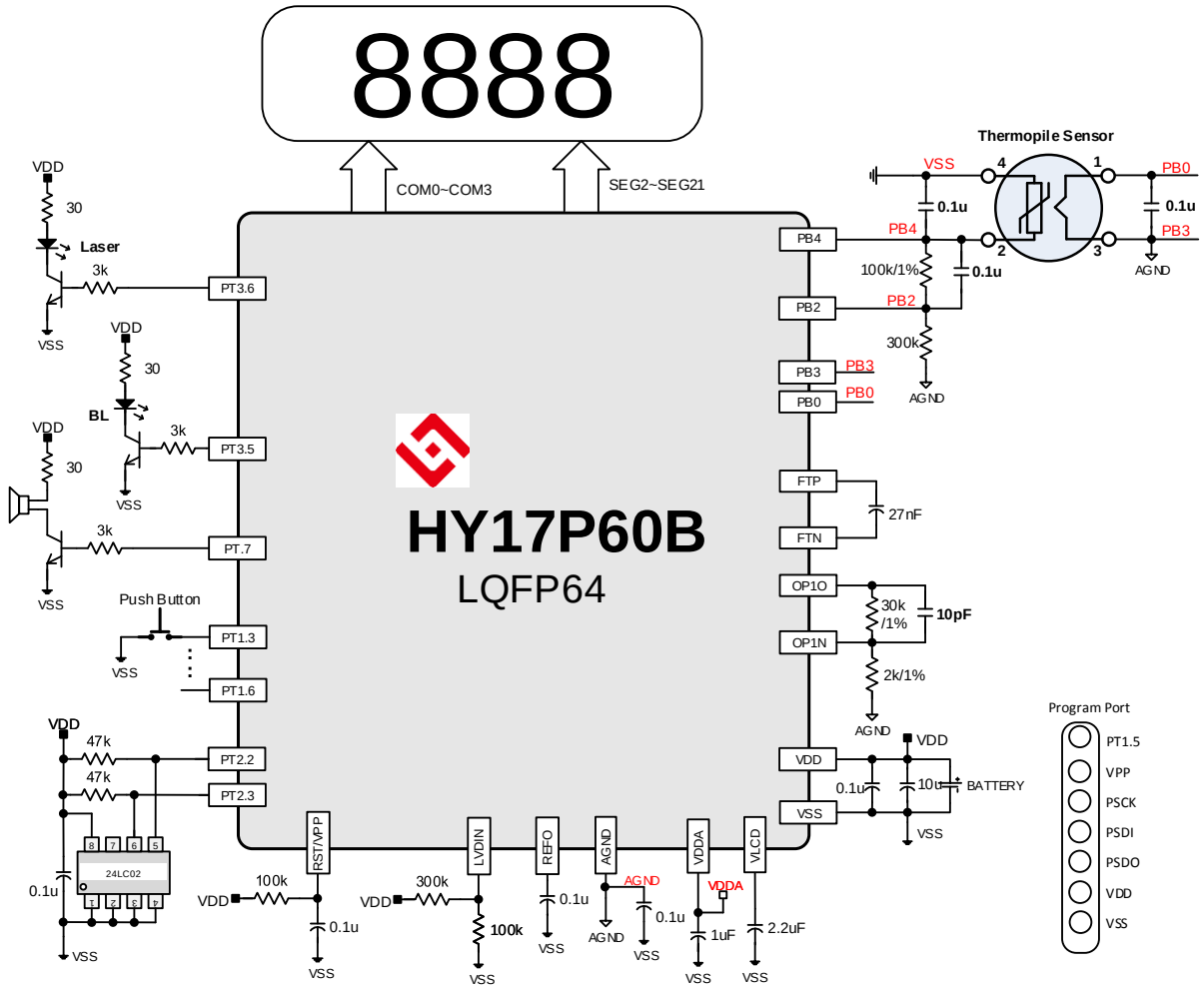


Figure 3-2 HY17P60B Infrared sensor application circuit

4. Function Outline

4.1. Internal Block Diagram

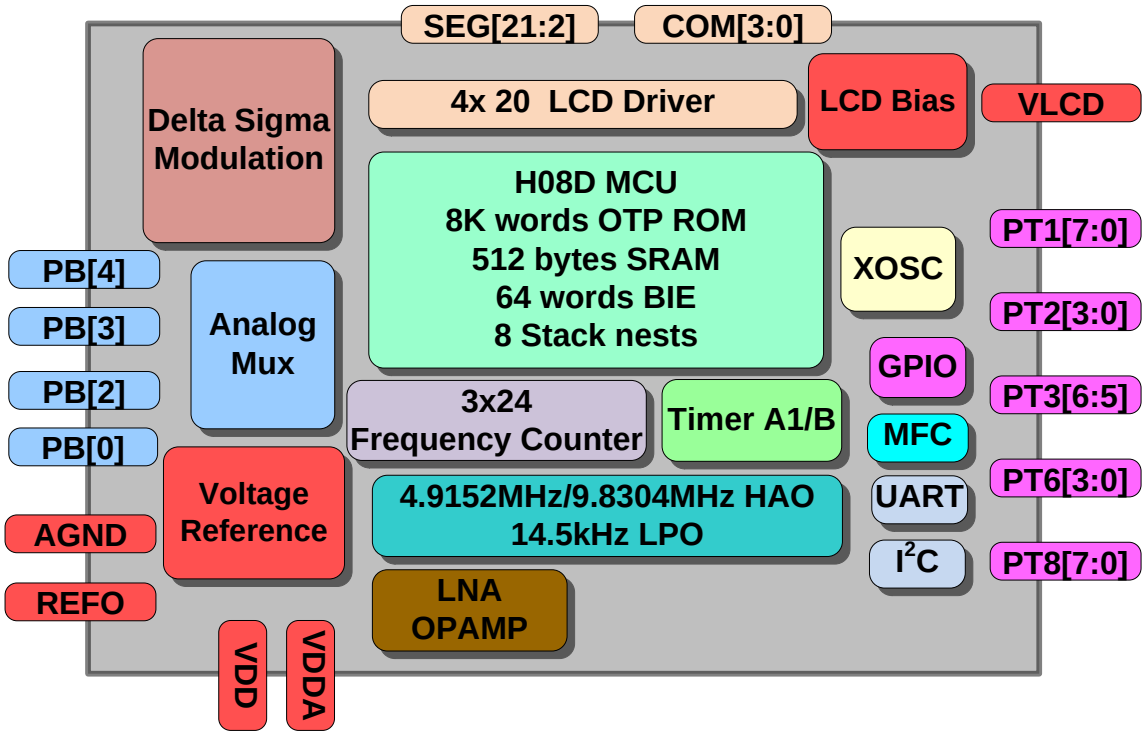


Figure 4-1 Internal Block Diagram

4.2. Related Manuals and Supporting Documents

IC Function Related Instruction Manual

DS-HY17P60B	HY17P60B Data Sheet
UG-HY17S68	HY17S68 User's Manual
APD-CORE005	H08D Instruction Set User's Manual

Development Tool Related Instruction Manual

APD-HY17PIDE001	HY17P Series Development Tool Software Instruction Manual
APD-HY17PIDE006	HY17S68-DK02 IDE Hardware Instruction Manual
APD-HYIDE013	Integrated Writer User's Manual
APD-HYIDE014	HY10000-WK08C Integrated Writer Online Update Manual
APD-OTP005	OTP programming pin information

Product Production Related Instruction Manual

APD-HY17PIDE004	HY17P Series HexLoader User's Manual

4.3. ADC Network

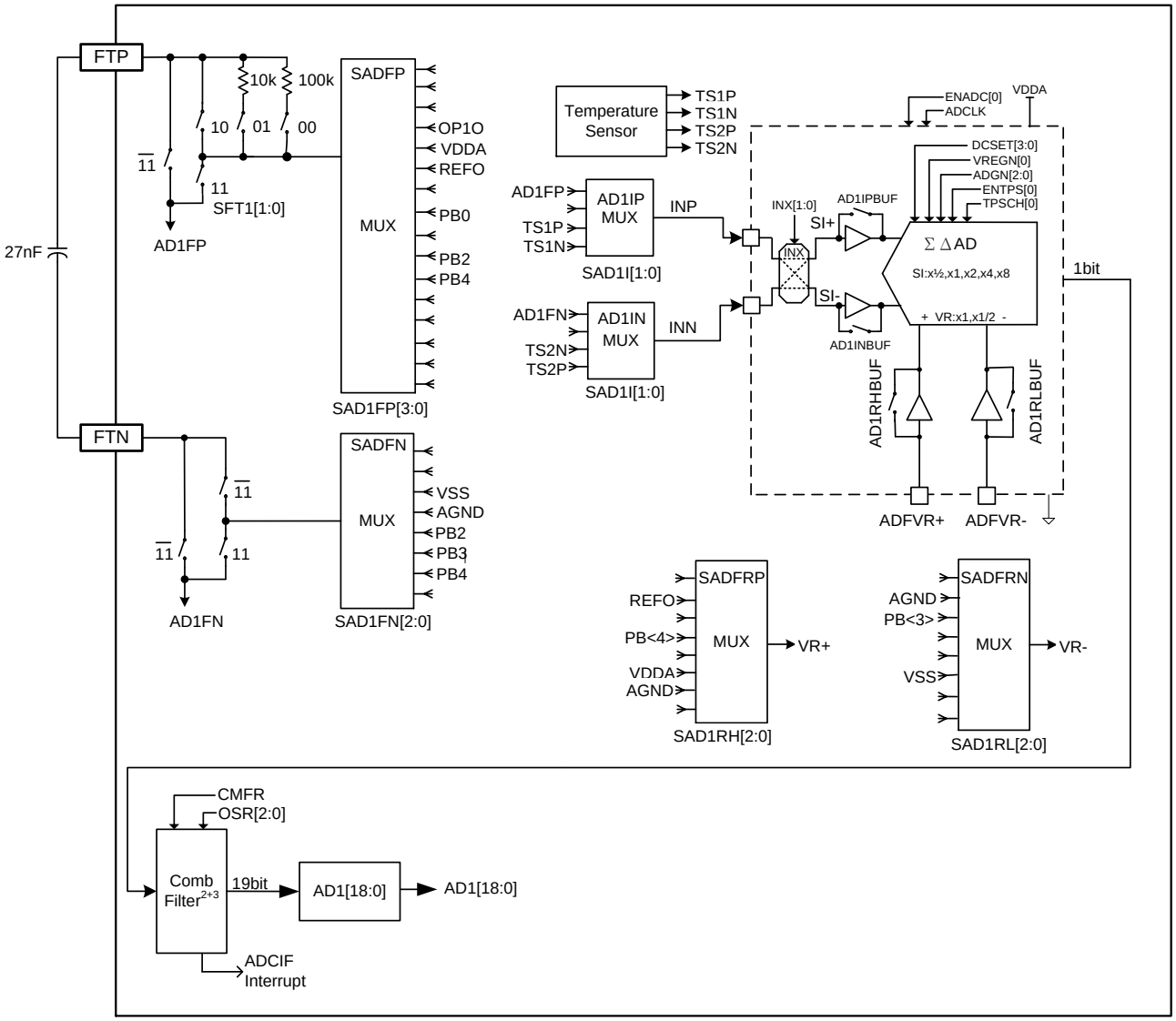


Figure 4-1 ΣΔADC Network block diagram

4.4. Digital Signal Processing(DSP)

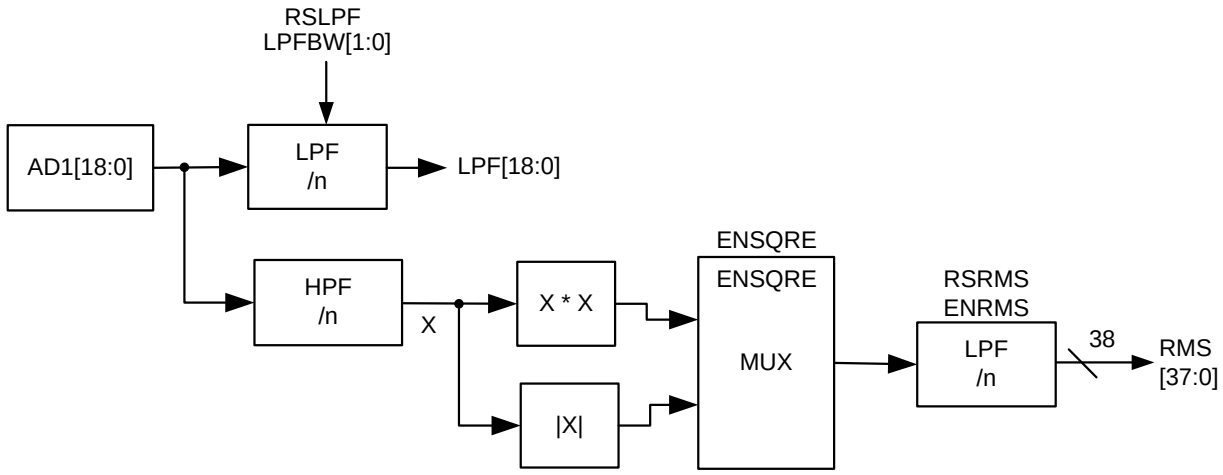


Figure 4-2 Digital Signal Processing(DSP) block diagram

4.5. Analog Input Network

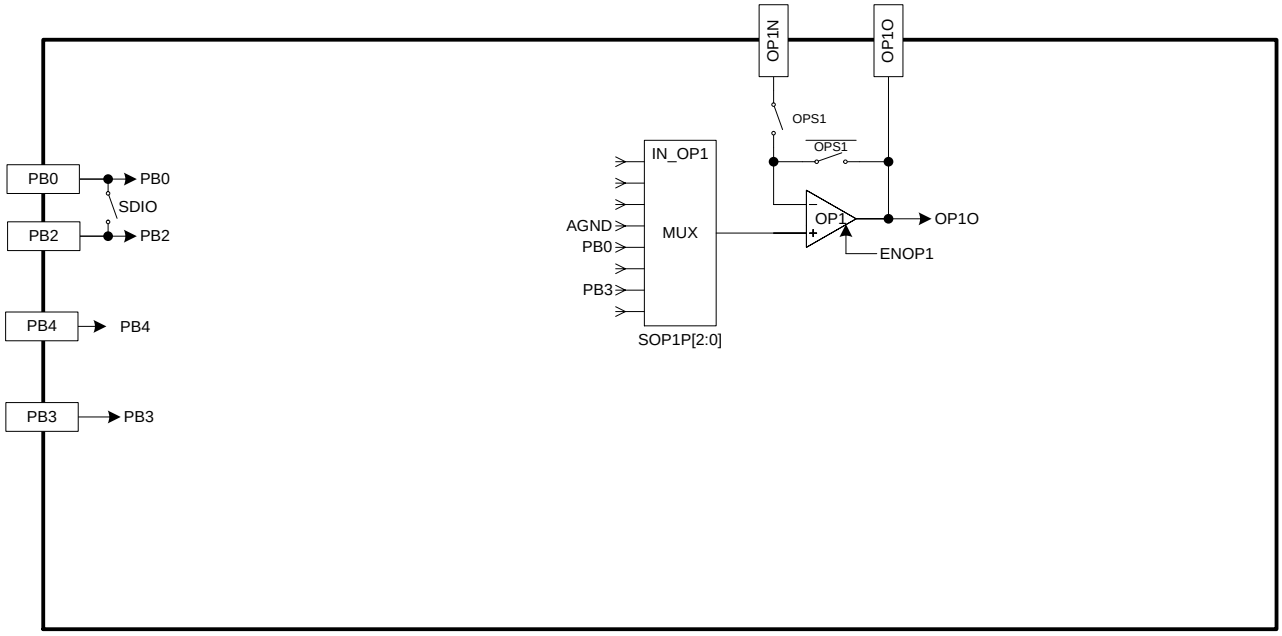


Figure 4-3 Analog Input Network block diagram

4.6. Clock System

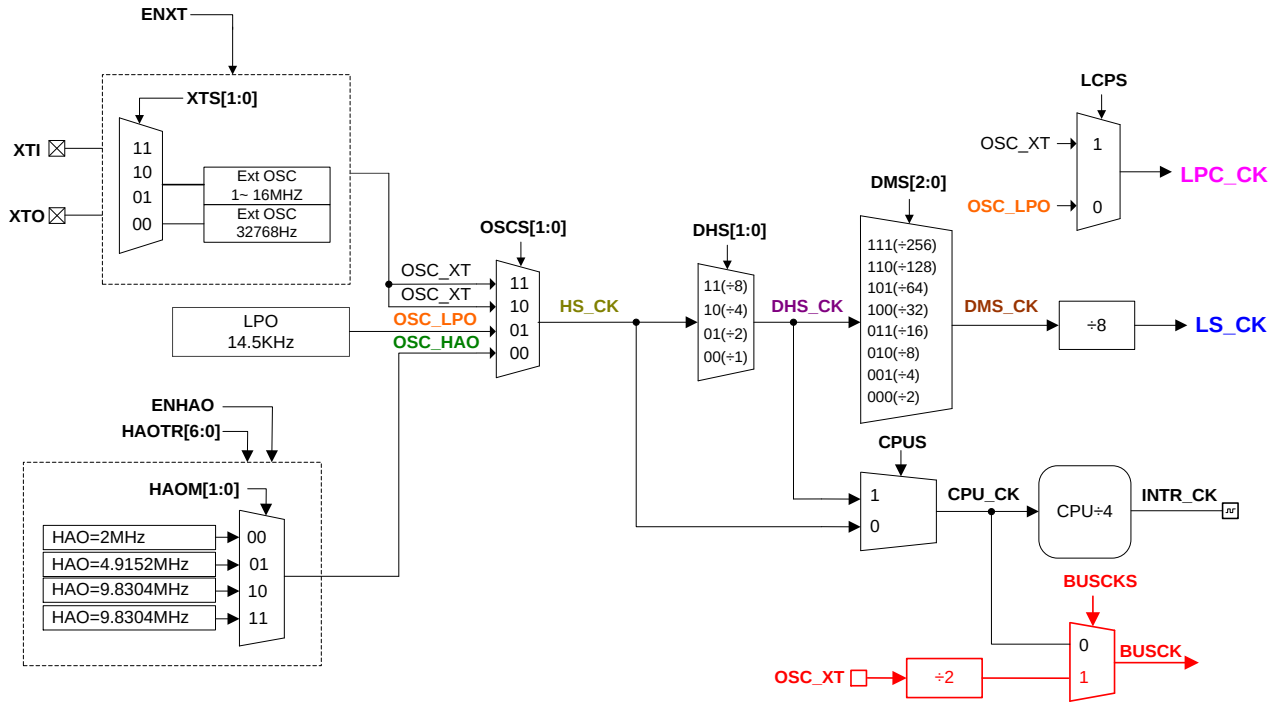


Figure 4-4 HY17P60B Clock System block diagram (一)

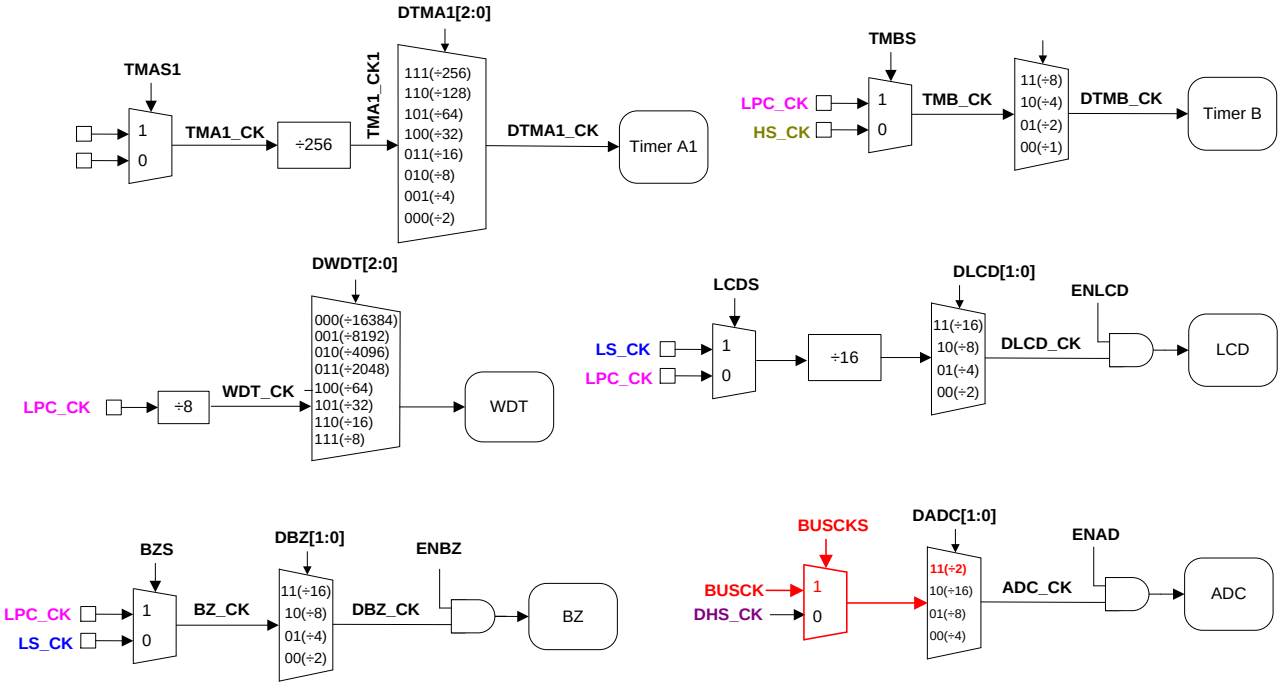
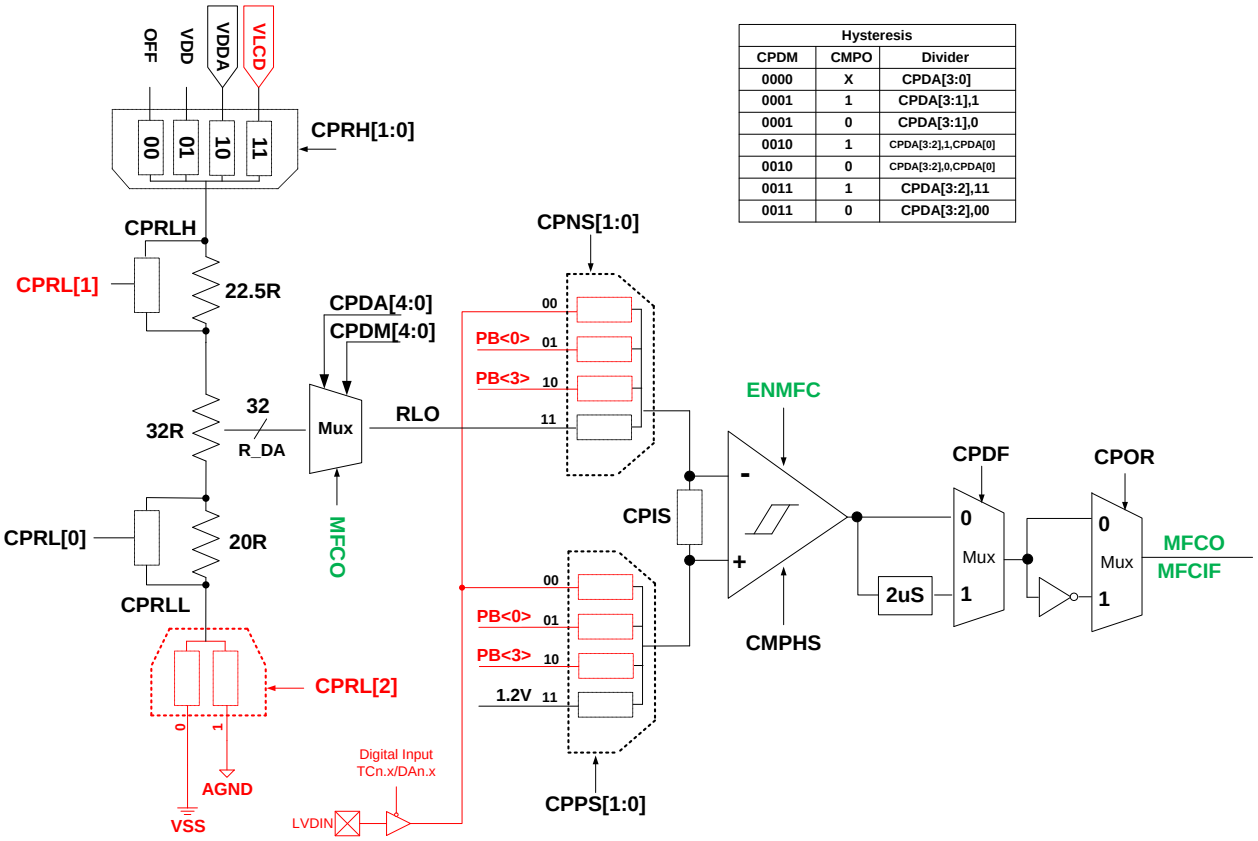


Figure 4-5 HY17P60B Clock System block diagram (二)

4.7. Multi-function Comparator



Hysteresis		
CPDM	CMPO	Divider
0000	X	CPDA[3:0]
0001	1	CPDA[3:1],1
0001	0	CPDA[3:1],0
0010	1	CPDA[3:2],1,CPDA[0]
0010	0	CPDA[3:2],0,CPDA[0]
0011	1	CPDA[3:2],11
0011	0	CPDA[3:2],00

Figure 4-6 Multi-function Comparator block diagram

4.8. Reset

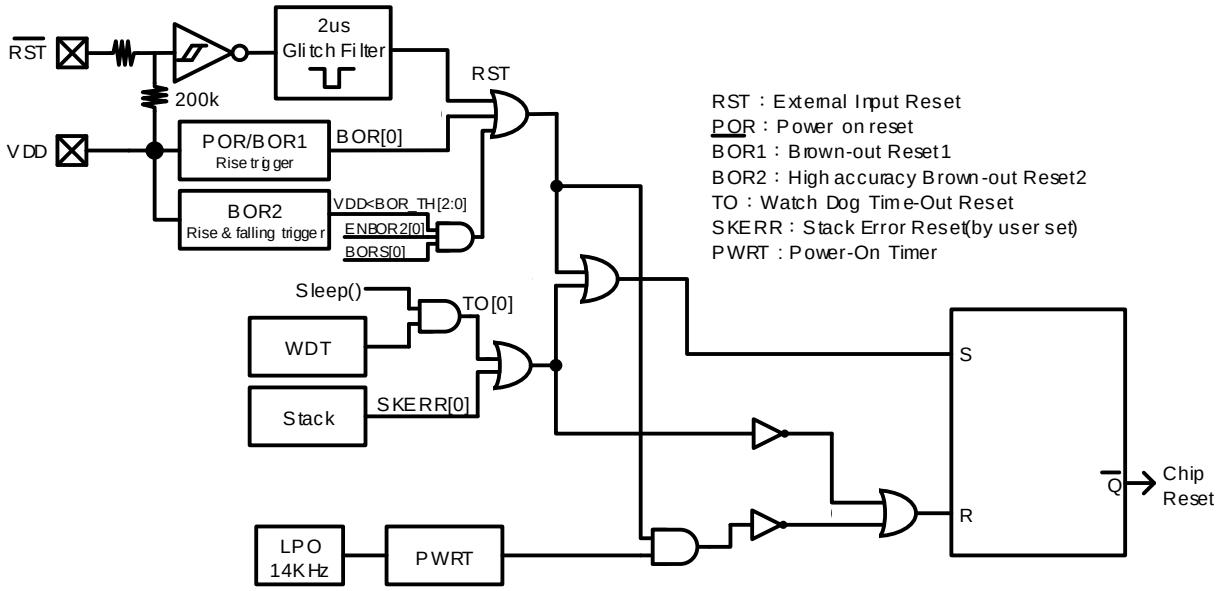


Figure 4-7 Reset block diagram

4.9. Power Diagram

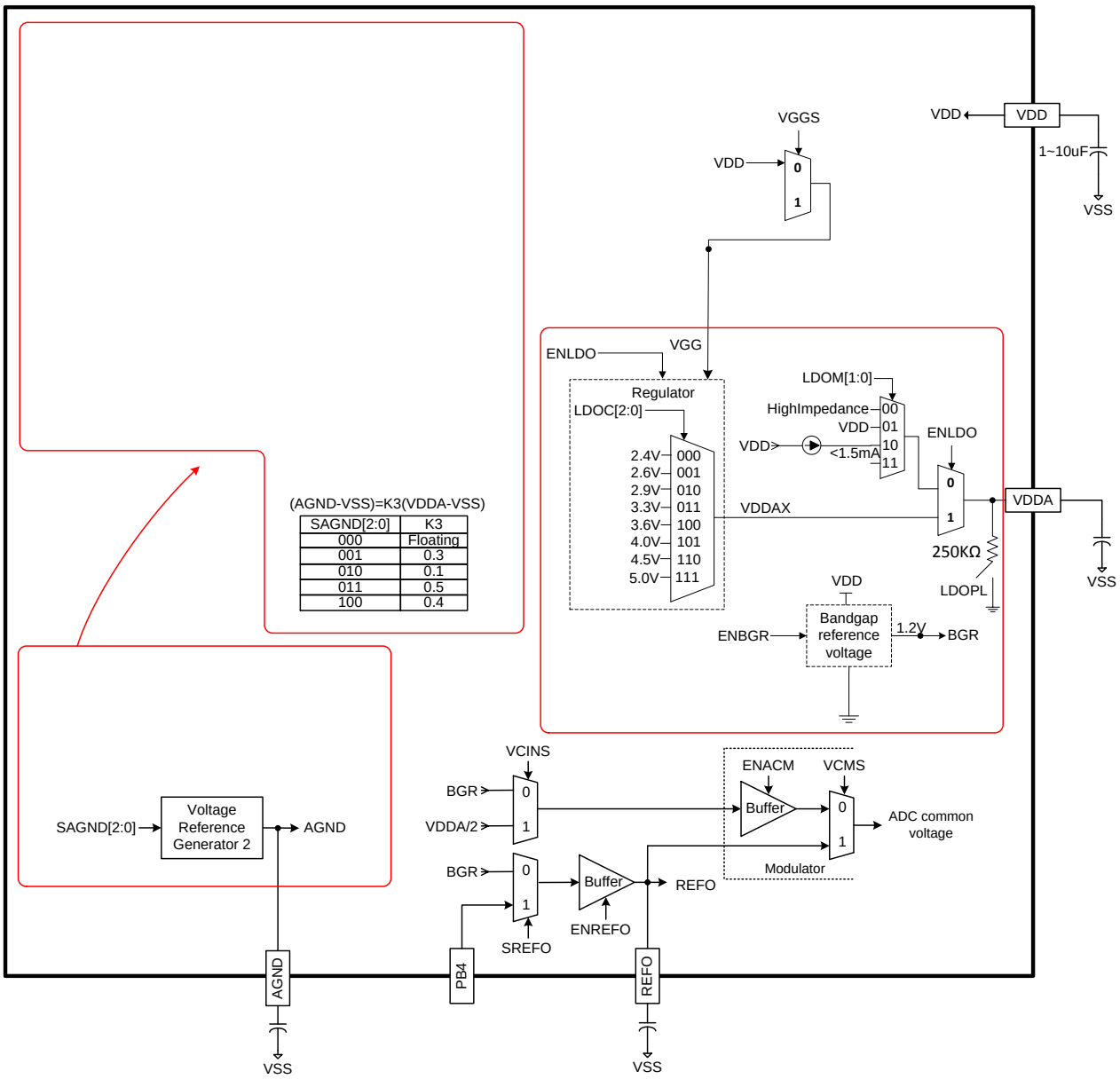


Figure 4-8 Power System block diagram

4.10. Frequency Counter、CNT Pin

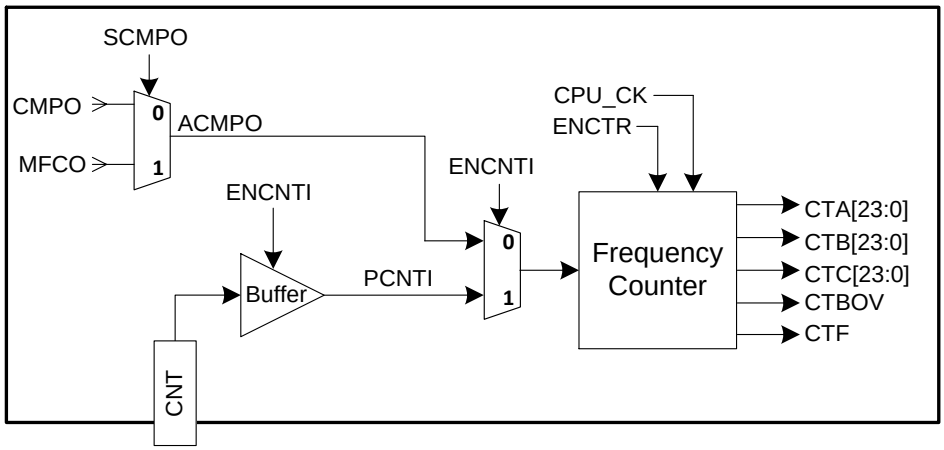


Figure 4-90 Frequency Counter block diagram

4.11. GPIO PORT1~3

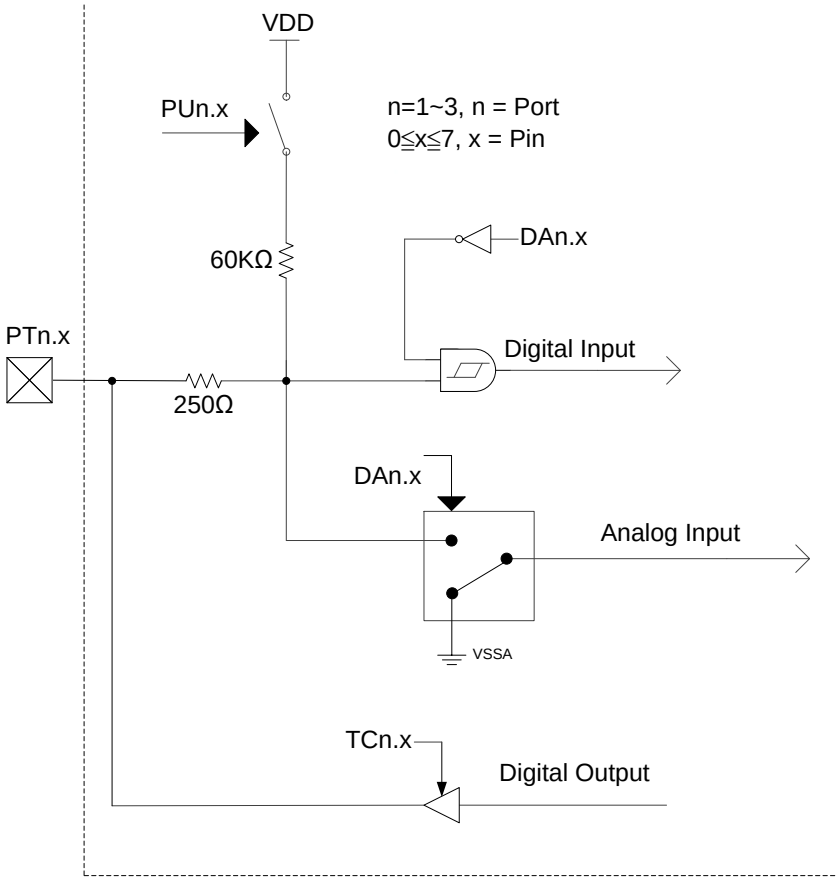


Figure 4-101 GPIO PORT1~3 block diagram

4.12. Watch Dog

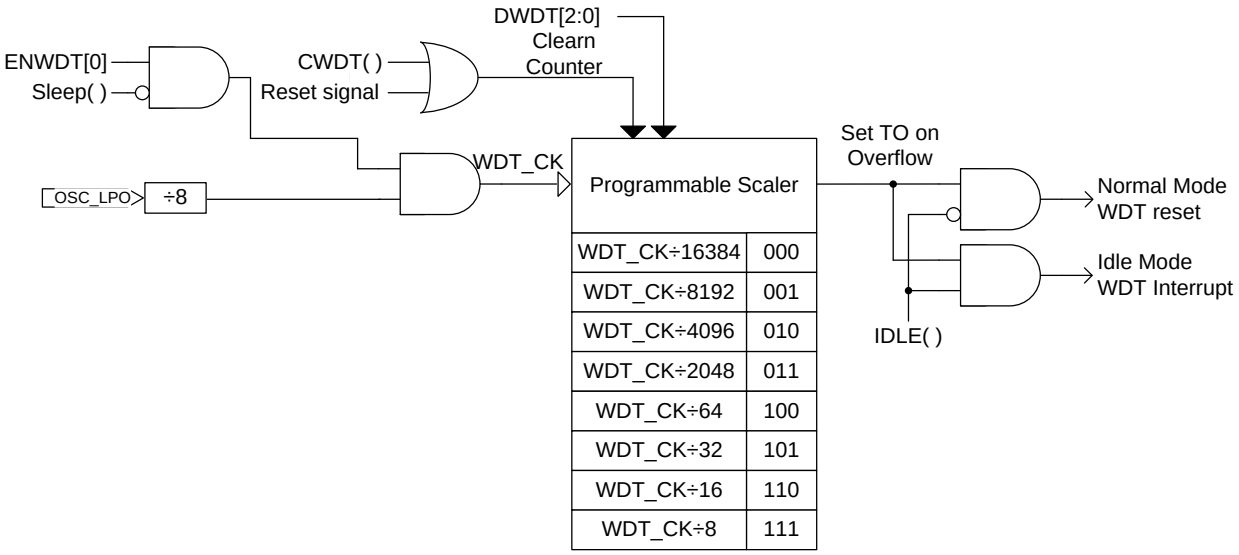


Figure 4-112 Watch Dog block diagram

4.13. 8-bit Timer A1

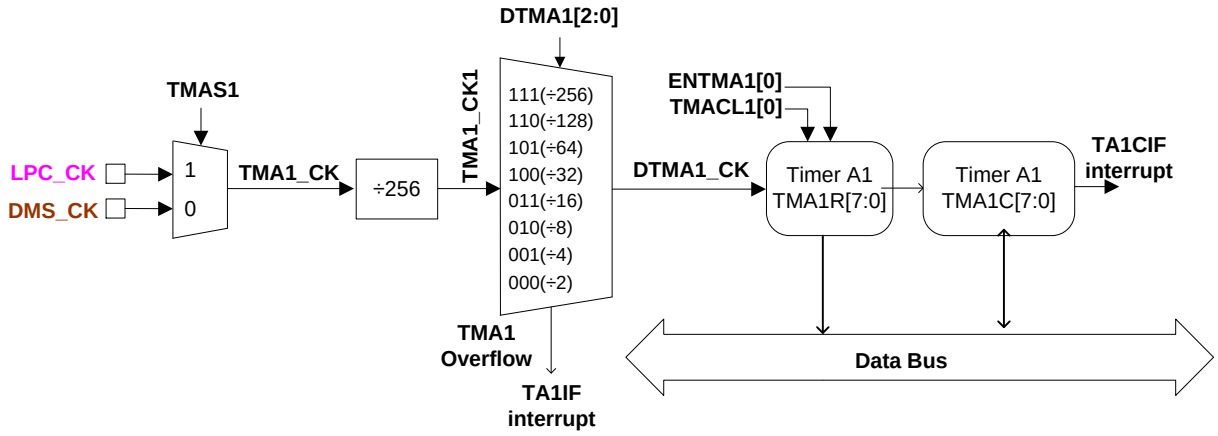


Figure 4-123 8-bit Timer A1 block diagram

4.14. 16-bit Timer B

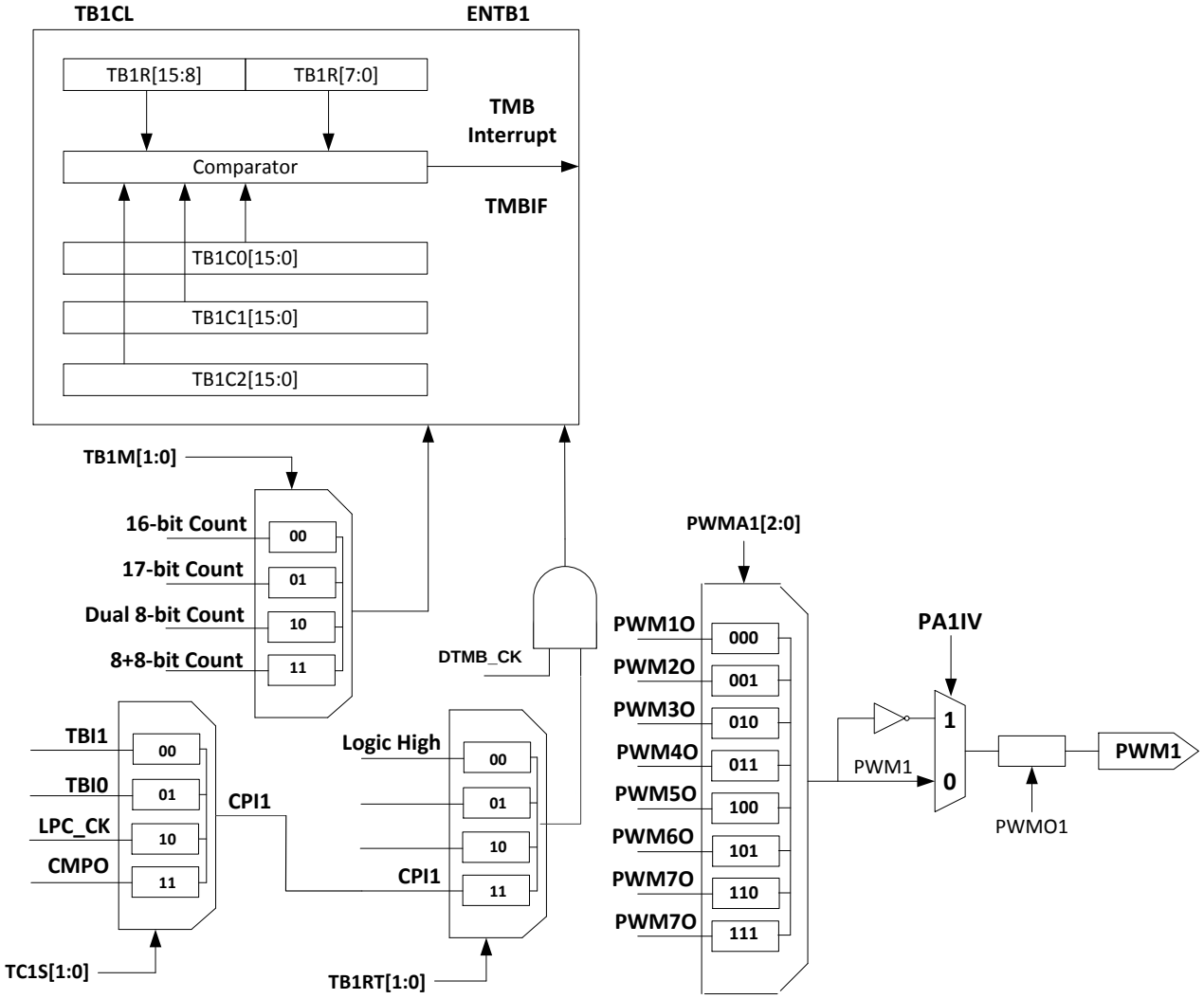


Figure 4-134 16-bit Timer B block diagram

4.15. LCD

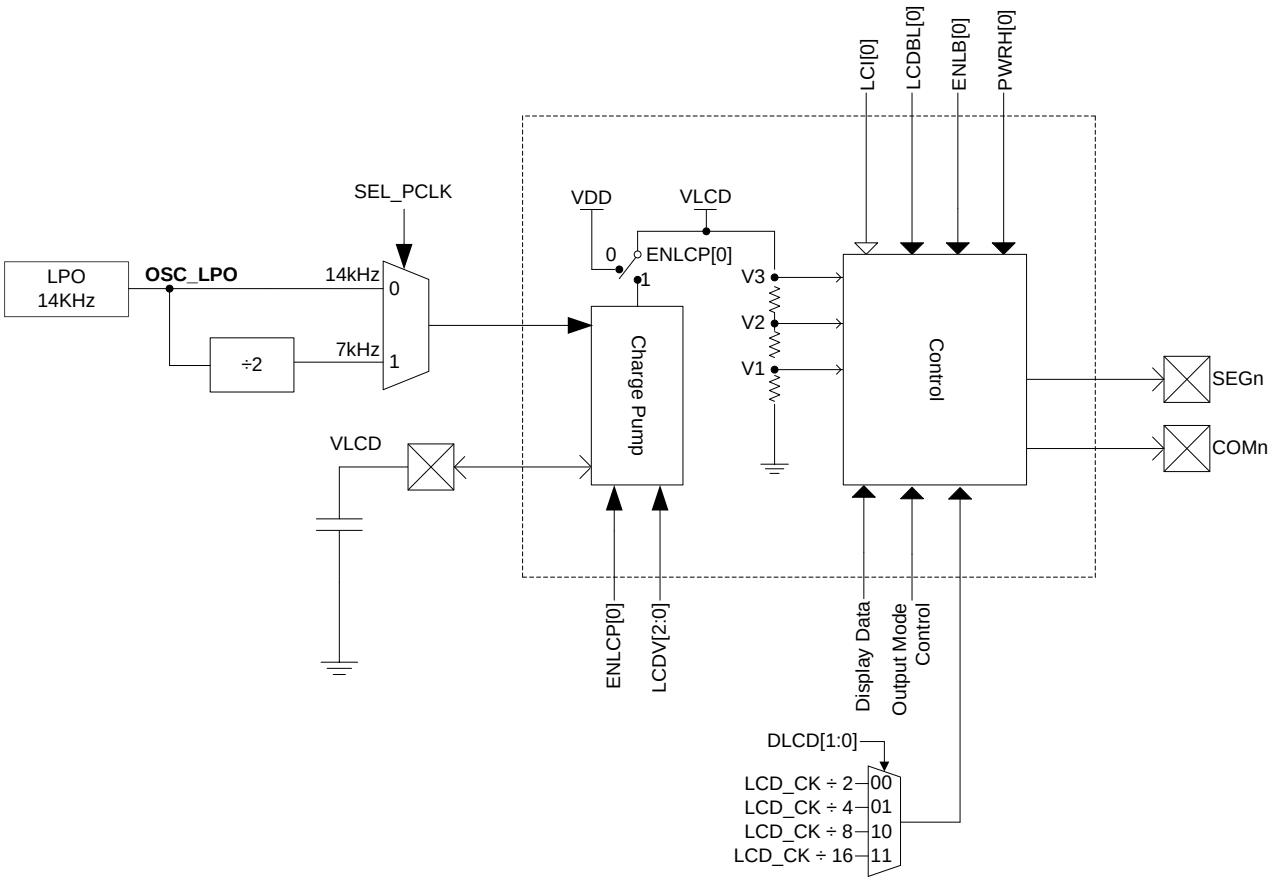


Figure 4-145 LCD block diagram

4.16. EUART

EUART TRANSMIT BLOCK DIAGRAM

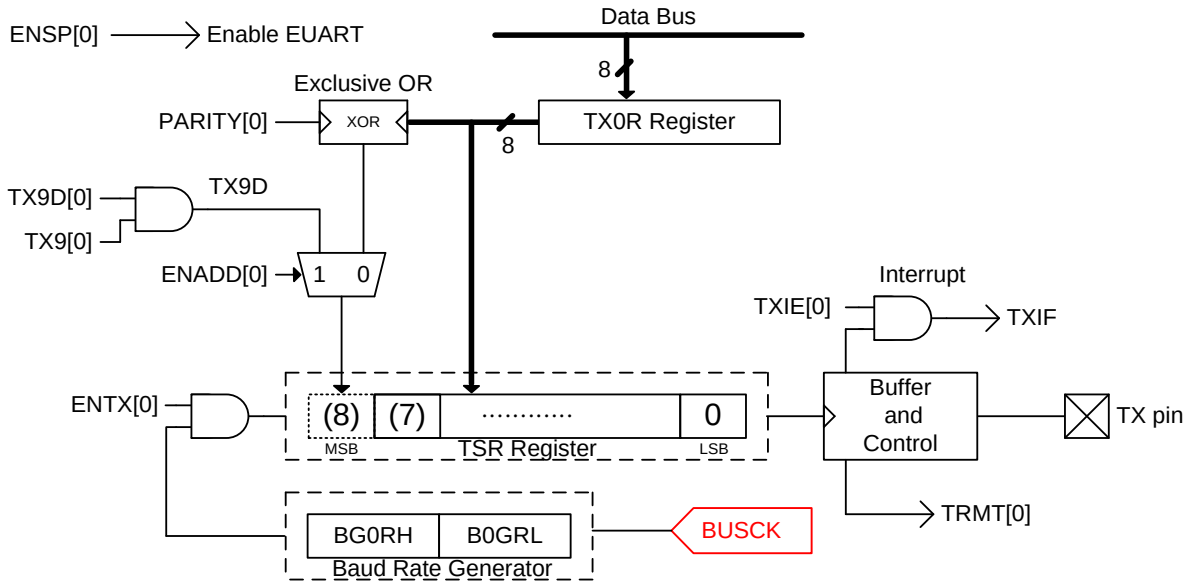
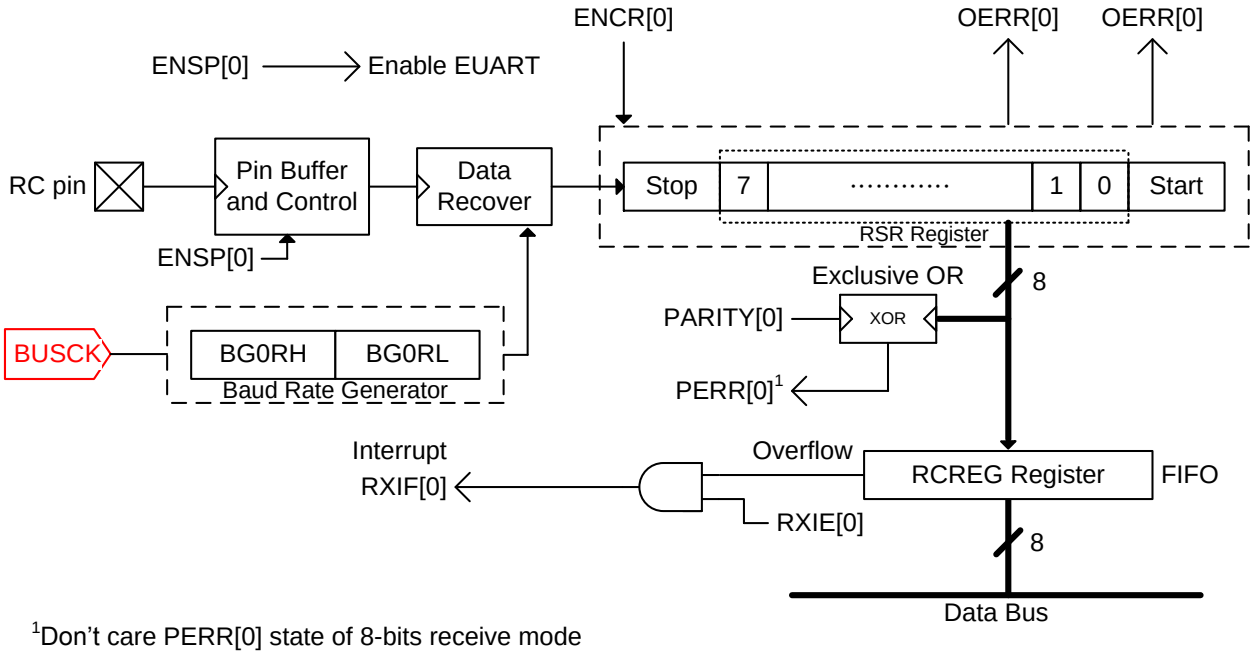


Figure 4-156 EUART transmit block diagram

EUART 8-BITs RECEIVE BLOCK DIAGRAM



[1]Don't care PERR[0] state of 8-bits receive mode

Figure 4-167 EUART 8-bits receive block diagram

4.17. I²C

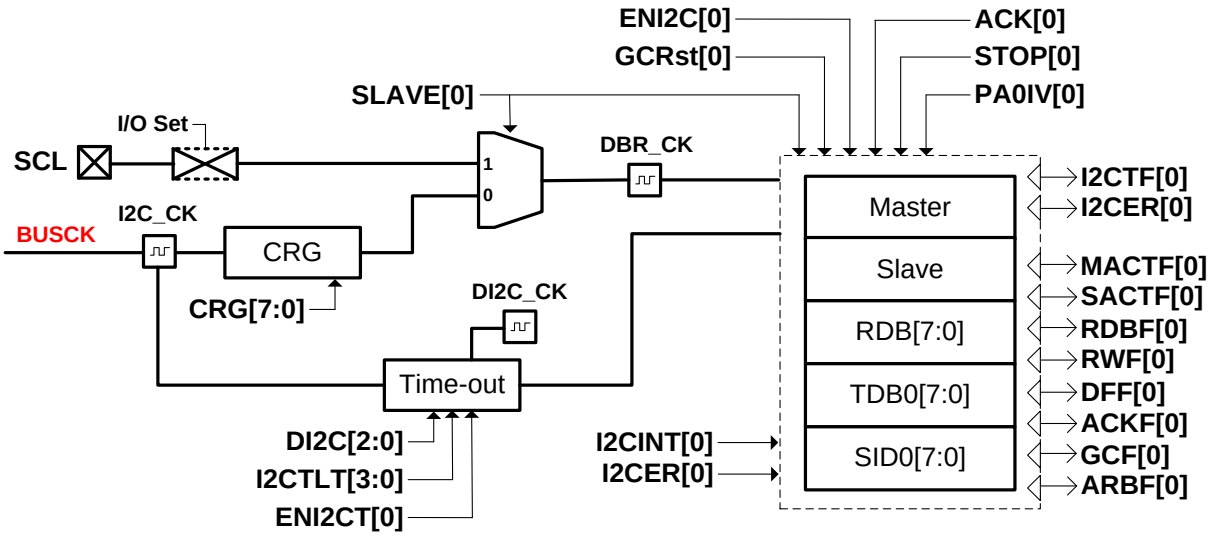


Figure 4-178 I²C block diagram

5. Register List

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
000H	INDF0	Contents of FSR0 to address data memoryvalue of FSR0 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
001H	POINC0	Contents of FSR0 to address data memoryvalue of FSR0 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
002H	PODEC0	Contents of FSR0 to address data memoryvalue of FSR0 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
003H	PRINC0	Contents of FSR0 to address data memoryvalue of FSR0 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
004H	PLUSW0	Contents of FSR0 to address data memoryvalue of FSR0 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
005H	INDF1	Contents of FSR1 to address data memoryvalue of FSR1 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
006H	POINC1	Contents of FSR1 to address data memoryvalue of FSR1 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
007H	PODEC1	Contents of FSR1 to address data memoryvalue of FSR1 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
008H	PRINC1	Contents of FSR1 to address data memoryvalue of FSR1 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
009H	PLUSW1	Contents of FSR1 to address data memoryvalue of FSR1 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00AH	INDF2	Contents of FSR2 to address data memoryvalue of FSR2 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00BH	POINC2	Contents of FSR2 to address data memoryvalue of FSR2 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00CH	PODEC2	Contents of FSR2 to address data memoryvalue of FSR2 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00DH	PRINC2	Contents of FSR2 to address data memoryvalue of FSR2 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00EH	PLUSW2	Contents of FSR2 to address data memoryvalue of FSR2 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00FH	FSR0H	-	-	-	-	-	-	FSR0[9:8]		 xxxx	.... .uuu	-,-,-,-,-,-,*,*
010H	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
011H	FSR1H	-	-	-	-	-	-	FSR1[9:8]		xxx	.... .uuu	-,-,-,-,-,-,*,*
012H	FSR1L	Indirect Data Memory Address Pointer 0 Low Byte,FSR1[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
013H	FSR2H	-	-	-	-	-	-	FSR2[9:8]		xxx	.... .uuu	-,-,-,-,-,-,*,*
014H	FSR2L	Indirect Data Memory Address Pointer 0 Low Byte,FSR2[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
015H	TOSU	-	-	-	-	-	-	-	-	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
016H	TOSH			-	Top-of-Stack High Byte (TOS[12:8])					.xxx xxxx	..uu uuuu	-,*,*,*,*,*,*,*
017H	TOSL	Top-of-Stack Low Byte (TOS[7:0])								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
018H	SKCN	SKFL	SKUN	SKOV	SKPRT[4:0]					0000 0000	u$$$ $$$$	rw0,rw0,rw0,*,*,*,*
019H	PCLATU	-	-	-	-	-	-	-	-	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
01AH	PCLATH			-	PC High Byte for PC[12:8]					..00 0000	..00 0000	*,*,*,*,*,*,*,*
01BH	PCLATL	PC Low Byte for PC[7:0]								0000 0000	0000 0000	*,*,*,*,*,*,*,*
01CH	TBLPTRU	-	-	-	-	-	-	-	-	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
01DH	TBLPTRH	-	-	-	Program Memory Table Pointer High Byte (TBLPTR<13:8>)					..xx xxxx	..uu uuuu	-,-,*,*,*,*,*,*
01EH	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR[7:0])								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
01FH	TBLDH	Program Memory Table Latch High Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
020H	TBLDL	Program Memory Table Latch Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
021H	PRODH	Product Register of Multiply High Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
022H	PRODL	Product Register of Multiply Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
023H	INTE0	GIE	TA1CIE	ADIE	WDTIE	TB1IE	CTIE	E1IE	E0IE	0000 0000	0uuu uuuu	*,*,*,*,*,*,*,*
024H	INTE1	TA1IE	-	TXIE	RCIE	I2CERIE	I2CIE	E3IE	E2IE	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
025H	INTE2	MFCIE	-	-	-	CTBOVE	RMSIE	LPFIE	BOR2IE	.000 0000	.uuu uuuu	*,*,*,*,*,*,*,*
026H	INTF0	-	TA1CIF	ADIF	WDTIF	TB1IF	CTF	E1IF	E0IF	.000 0000	.uuu uuuu	*,*,*,*,*,*,*,*
027H	INTF1	TA1IF	-	TXIF	RCIF	I2CERIF	I2CIF	E3IF	E2IF	0000 0000	uuuu uuuu	*,*,*,* r,r,*,*
028H	INTF2	MFCIF	-	-	-	CTBOV	RMSF	LPFF	BOR2IF	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
029H	WREG	Working Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
02AH	BSRCN	-	-	-	-	-	BSR[2:0]			 xxxx	.... uuuu	-,-,-,-,-,*,*,*
02BH	MSTAT	-	-	-	C	DC	N	OV	Z	...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
02CH	PSTAT	BOR	PD	TO	IDL	RST	SKERR	BOR2LV	GCRstIF	$000 $000	uu$u u$uu	rw0,rw0,rw0,rw0 rw0,rw0,r,rw0
02DH	BIECN	1	BLKSEL	-	ENBVD	VPPHV	ENBCP	BIEWR	BIERD	1.00 $000	1.00 $uuu	r1,-,*,* r,*,*,*
02EH	BIEARH	-	-	BIE High Byte Address Register as BIEA[13:8]						0.xx xxxx	u.uu uuuu	*,-,*,*,*,*,*,*
02FH	BIEARL	BIE Low Byte Address Register as BIEA[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
030H	BIEDRH	BIE High Byte Data Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
031H	BIEDRL	BIE Low Byte Data Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
032H	PWRCN	ENBGR	LDOC[2:0]			LDOM[1:0]		ENLDO	CSFON	1000 0000	1uuu u00u	*,*,*,*,*,wr0,wr0,*
033H	PWRCN1	ENREFO	ENCMP	ENCNTI	ENCTR	ENVS	SAGND[2:0]			0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
034H	PWRCN2	-	VGGS	CHPCKS[1:0]		ENFIR	LDOPL	ENTPS	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
035H	OSCCN0	OSCS[1:0]		DHS[1:0]		DMS[2:0]			CUPS	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
036H	OSCCN1	CCOPT	LCPS	DADC[1:0]		DTMB[1:0]		TMBS	LCDS	0000 0000	uuuu uuu.	*,*,*,*,*,*,*,-
037H	OSCCN2	DLCD[1:0]		ENXT	XTS[1:0]		HAOM[1:0]		ENHAO	0000 0001	uuuu uuu1	*,*,*,*,*,*,*,*

Table 5-1 Register List

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
038H	CSFCN0	SKRST	HAOTR[6:0]							.1..	....	*,*,*,*,*,*,*,*
039H	CSFCN1	BUSCKS	-	-	BOR_TH[2:0]			BORS	ENBOR2	0000 0011	uuuu uuuu	*,*,*,*,*,*,*,*
03AH	WDTCN	ENBZ	BZS	BZ[1:0]		ENWDT	DWDT[2:0]			0000 0000	uuuu $000	-,*,*,* rw1,*,*,*
03BH	AD1CN0	ENAD1	ENCH	ENINXCH	VREGN	OSR[2:0]			CMFR	000. 0000	uuu. uuuu	*,*,*,*,*,*,*,*
03CH	AD1CN1	ENACM	VCMS	VCINS	TPSCP	TPSCH	ADGN[2:0]			xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
03DH	AD1CN2	FilterN[1:0]		-	DAFM	DCSET[3:0]				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
03EH	AD1CN3	SAD1FP[3:0]				-	SAD1FN[2:0]			xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
03FH	AD1CN4	AD1RHBUF	AD1RLBUF	AD1IPBUF	AD1INBUF	INX[1:0]		VRIS	INIS	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
040H	AD1CN5	SAD1RH[2:0]			SAD1RL[2:0]			SAD1I[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
041H	RMSCN	ENRMS	ENLPF	ENSQRE	LPFBW[1:0]		-	RSLPF	RSRMS	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
042H	NET0	SDIO	SREFO	SFT1[1:0]		-	-	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
045H	NET3	-	-	-	SCMPO	-	-	-	CNTI_IF	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
04CH	CTAU	CTA[23:16]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
04DH	CTAH	CTA[15:8]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
04EH	CTAL	CTA[7:0]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
04FH	CTBU	CTB[23:16]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
050H	CTBH	CTB[15:8]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
051H	CTBL	CTB[7:0]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
052H	CTCU	CTC[23:16]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
053H	CTCH	CTC[15:8]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
054H	CTCL	CTC[7:0]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
05BH	RMSDATA4	RMS[37:30]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
05CH	RMSDATA3	RMS[29:22]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
05DH	RMSDATA2	RMS[21:14]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
05EH	RMSDATA1	RMS[13:6]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
05FH	RMSDATA0	RMS[5:0]						-	-	xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
060H	LPFDATAU	LPF[18:11]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
061H	LPFDATAH	LPF[10:3]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
062H	LPFDATAL	LPF[2:0]			-	-	-	-	-	xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
063H	AD1DATAU	AD1[18:11]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
064H	AD1DATAH	AD1[10:3]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
065H	AD1DATAL	AD1[2:0]			-	-	-	-	-	xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
066H	OP1CN0	ENOP1	SOP1P[2:0]			-	-		OPS1	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
068H	TMA1CN	ENTMA1	TMACL1	TMAS1	DTMA1[2:0]			-	-	0000 00.0	u0uu uu.u	*,rw1,*,*,*,-,*
069H	TMA1R	TMA1 counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
06AH	TMA1C	TMA1C counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
06BH	PT1	PT1.7	PT1.6	PT1.5	PT1.4	PT1.3	PT1.2	PT1.1	PT1.0	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
06CH	PT1IN	IN1.7	IN1.6	IN1.5	IN1.4	IN1.3	IN1.2	IN1.1	IN1.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
06DH	TRISC1	TC1.7	TC1.6	TC1.5	TC1.4	TC1.3	TC1.2	TC1.1	TC1.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
06EH	PT1PU	PU1.7	PU1.6	PU1.5	PU1.4	PU1.3	PU1.2	PU1.1	PU1.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
06FH	PT1M1	-	-	-	-	INTEG1[1:0]		INTEG0[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
070H	PT1INT	INTEG7	INTEG6	INTEG5	INTEG4	INTEG3	INTEG2	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
071H	PT1INTE	INTE1.7	INTE1.6	INTE1.5	INTE1.4	-	-	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
072H	PT1INTF	INTF1.7	INTF1.6	INTF1.5	INTF1.4	-	-	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
073H	PT2	-	-	-	-	PT2.3	PT2.2	PT2.1	PT2.0	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
074H	PT2IN	-	-	-	-	IN2.3	IN2.2	IN2.1	IN2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
075H	TRISC2	-	-	-	-	TC2.3	TC2.2	TC2.1	TC2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
076H	PT2PU	-	-	-	-	PU2.3	PU2.2	PU2.1	PU2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
077H	PT2INT	-	-	-	-	INTG2.3	INTG2.2	INTG2.1	INTG2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
078H	PT2INTE	-	-	-	-	INTE2.3	INTE2.2	INTE2.1	INTE2.0	0000 0000	uuuu uuuu	
079H	PT2INTF	-	-	-	-	INTF2.3	INTF2.2	INTF2.1	INTF2.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
07AH	MFCN0	CPRH[1:0]		MFCO	CPIS	CPOR	CPDF	CMPHS	ENMFC	0000 0000	uuuu uuuu	*,*,r,*,*,*,*,*
07BH	MFCN1	CPRL[2:0]			-	CPPS[1:0]		CPNS[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
07CH	MFCN2	-	-	-	CPDA[4:0]					0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
07DH	MFCN3	-	-	-	CPDM[4:0]					0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*

Table 5-2 Register List

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
180H	LCDCN1	ENLCP	LCDV[2:0]			ENLB	SELPCLK	LCDBL	ENLCD	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
182H	LCDCN3	SCM3[1:0]		SCM2[1:0]		SCM1[1:0]		SCM0[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
183H	LCDCN4	SSG21	SSG20	SSG19	SSG18	SSG17	SSG16	SSG15	SSG14	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
185H	LCDCN6	SSG5[1:0]		SSG4[1:0]		SSG3[1:0]		SSG02[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
186H	LCDCN7	SSG9[1:0]		SSG8[1:0]		SSG7[1:0]		SSG6[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
187H	LCDCN8	SSG13[1:0]		SSG12[1:0]		SSG11[1:0]		SSG10[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
18BH	LCD0	LCD SEG3[4:7] data				LCD SEG2[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18CH	LCD1	LCD SEG5[4:7] data				LCD SEG4[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18DH	LCD2	LCD SEG7[4:7] data				LCD SEG6[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18EH	LCD3	LCD SEG9[4:7] data				LCD SEG8[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
18FH	LCD4	LCD SEG11[4:7] data				LCD SEG10[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
190H	LCD5	LCD SEG13[4:7] data				LCD SEG12[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
191H	LCD6	LCD SEG15[4:7] data				LCD SEG14[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
192H	LCD7	LCD SEG17[4:7] data				LCD SEG16[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
193H	LCD8	LCD SEG19[4:7] data				LCD SEG18[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
194H	LCD9	LCD SEG21[4:7] data				LCD SEG20[3:0] data				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
19FH	PT3	-	PT3.6	PT3.5	-	-	-	-	-	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1A0H	PT3IN	-	IN3.6	IN3.5	-	-	-	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A1H	TRISC3	-	TC3.6	TC3.5	-	-	-	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A2H	PT3PU	-	PU3.6	PU3.5	-	-	-	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1A8H	PT6	-	-	-	-	PT6.3	PT6.2	PT6.1	PT6.0	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1A9H	PT6IN	-	-	-	-	IN6.3	IN6.2	IN6.1	IN6.0	0000 xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1AAH	TRISC6	-	-	-	-	TC6.3	TC6.2	TC6.1	TC6.0	0000 xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1ABH	PT6PU	-	-	-	-	PU6.3	PU6.2	PU6.1	PU6.0	0000 xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1B0H	PT8	PT8.7	PT8.6	PT8.5	PT8.4	PT8.3	PT8.2	PT8.1	PT8.0	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1B1H	PT8IN	IN8.7	IN8.6	IN8.5	IN8.4	IN8.3	IN8.2	IN8.1	IN8.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1B2H	TRISC8	TC8.7	TC8.6	TC8.5	TC8.4	TC8.3	TC8.2	TC8.1	TC8.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1B3H	PT8PU	PU8.7	PU8.6	PU8.5	PU8.4	PU8.3	PU8.2	PU8.1	PU8.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1C3H	CFG0	-	-	-	-	-	GCRst	ENI2CT	ENI2C	0000 0000	.... .uuu	-,-,-,- -,*,*,*
1C4H	ACT0	SLAVE	-	-	I2CER	START	STOP	I2CINT	ACK	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1C5H	STA0	MACTF	SACTF	RDBF	RWF	DFF	ACKF	GCF	ARBF	0001 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1C6H	CRG0	CRG[7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1C7H	TOC0	I2CTF	DI2C[2:0]			I2CTLT[3:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1C8H	RDB0	RDB[7:1]							RDB[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1C9H	TDB0	TDB0[7:1]							TDB0[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1CAH	SID0	SID0[7:1],The corresponding address of the 7-bit mode							SID0V[0]	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1CBH	UR0CN	ENSP	ENTX	TX9	TX9D	PARITY	-	-	WUE	0000 0..0	uuuu u..u	*,*,*,*,-,-,*
1CCH	UR0STA	-	RC9D	PERR	FERR	OERR	RCIDL	TRMT	ABDOVF	.000 0010	.uuu uuuu	-,r,r,r r,r,r,rw0
1CDH	BA0CN	-	-	-	-	ENCR	RC9	ENADD	ENABD	 0000	.... uuuu	-,-,-,- *,*,*,*
1CEH	BG0RH	-	-	-	Baud Rate Generator Register High Byte					...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
1CFH	BG0RL	Baud Rate Generator Register Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1D0H	TX0R	UART Transmit Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1D1H	RC0REG	UART Receive Register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
1D2H	TB1Flag		PWM7A	PWM6A	PWM5A	PWM4A	PWM3A	PWM2A	PWM1A	.000 0000	.uuu uuuu	-,r,r,r r,r,r,r
1D3H	TB1CN0	ENTB1	TB1M[1:0]		TB1RT[1:0]		TB1CL	PWMO1	PWMO0	0000 0000	uuuu u0uu	*,*,*,*,rw1,*,*
1D4H	TB1CN1	PA1IV	PWMA1[2:0]			PA0IV	PWMA0[2:0]			0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
1D5H	TB1RH	TimerB1 counter Register [15:8]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
1D6H	TB1RL	TimerB1 counter Register [7:0]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
1D7H	TB1C0H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1D8H	TB1C0L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1D9H	TB1C1H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1DAH	TB1C1L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1DBH	TB1C2H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1DCH	TB1C2L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
1E2H	FILTER	FreSpect		Frebit	ENSpect	-	-	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
080h ~ 0FFh		SRAM as 128Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*
100h ~ 17Fh		SRAM as 128Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*
200h ~ 2FFh		SRAM as 256Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*

Table 5-3 Register List

6. Electrical Characteristics

Absolute Maximum Ratings:

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at V_{DD} to V_{SS} . . . . −0.2 V to 6.0 V

Voltage applied to any pin . . . . −0.2 V to V_{DD} + 0.3 V

Voltage applied to RST/VPP pin . . . . −0.2 V to 8.75 V

Diode current at any device terminal . . . . ±2 mA

Storage temperature, Tstg: (unprogrammed device) . . . . −55℃ to 125℃

(Programmed device) . . . . −40℃ to 85℃

Total power dissipation. 0.5W

Maximum output current sink by any I/O pin 20mA

6.1. Recommended operating conditions

T_A = -40℃ ~ 85℃,unless otherwise noted

Sym.	Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		All digital peripherals and CPU V_{DD} = 2.2V~5.5V, Frequency<=9.6MHz, V_{DD} = 3.6V~5.5V, Frequency<=16MHz,		2.2		5.5	V
V_{DDA}	Supply Voltage		Analog peripherals		2.4		4.5	V
V_{SS}	Supply Voltage				0		0	V
XT	External Oscillator Frequency	Watch crystal	V_{DD} = 2.5V~5.5V, ENXT[0]=1	XTS[1:0]=0x		32768		Hz
XT	External Oscillator Frequency	Ceramic resonator, Crystal	V_{DD} = 2.5V~5.5V, ENXT[0]=1	XTS[1:0]=10	450K		4M	Hz
XT	External Oscillator Frequency	Ceramic resonator, Crystal	V_{DD} = 2.5V~5.5V, ENXT[0]=1	XTS[1:0]=11	1M		8M	Hz
XT	External Oscillator Frequency	Ceramic resonator, Crystal	V_{DD} = 3.6V~5.5V, ENXT[0]=1	XTS[1:0]=11	450K		16M	Hz

6.2. Internal RC Oscillator

T_A = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1, HAOM[1:0]=01	-20%	4.9152	+20%	MHz
HAO	High Speed Oscillator frequency	ENHAO[0]=1, HAOM[1:0]=11	-20%	9.8304	+20%	MHz
LPO	Low Power Oscillator frequency	VDD supply voltage be enable LPO	-20%	14.5	+20%	kHz

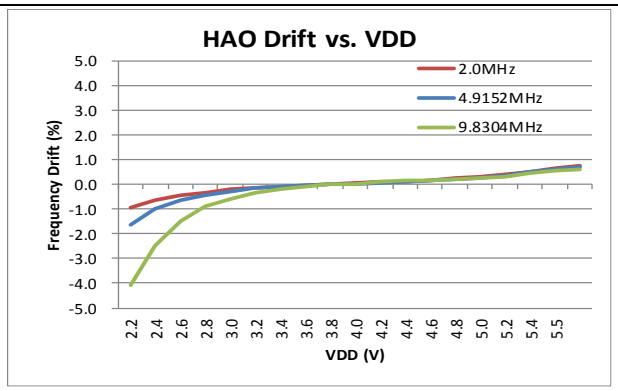


Figure 6.2-1 HAO vs. VDD

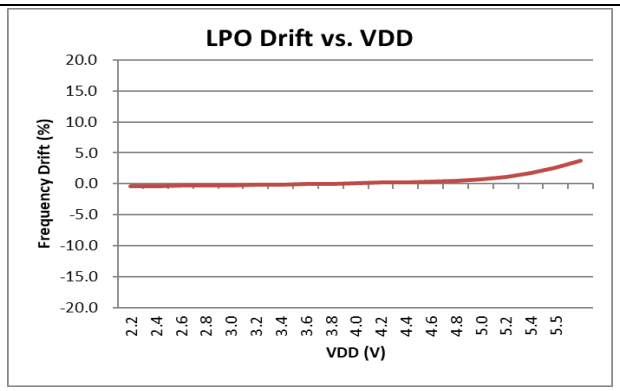


Figure 6.2-2 LPO vs. VDD

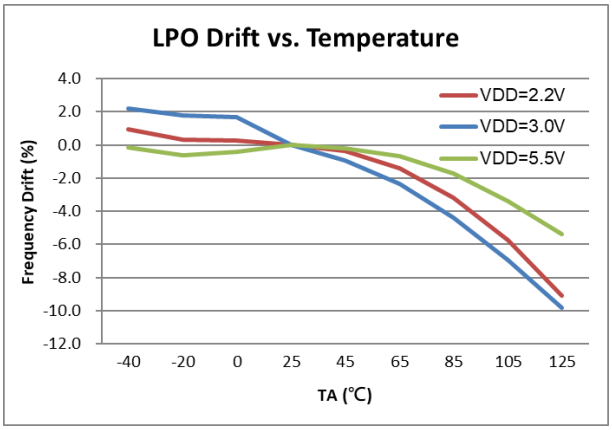


Figure 6.2-3 LPO vs. Temperature

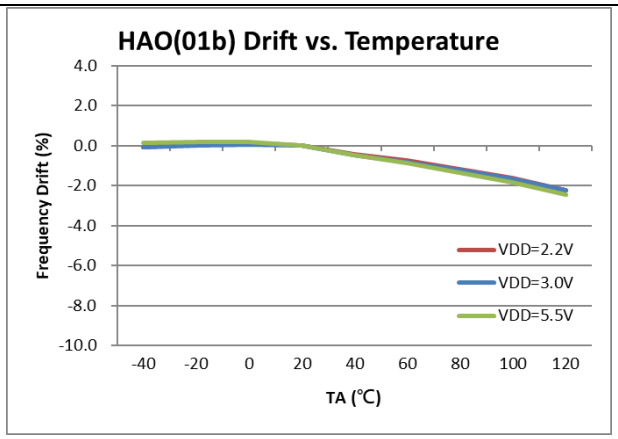


Figure 6.2-4 HAO(4.9152MHz) vs. Temperature

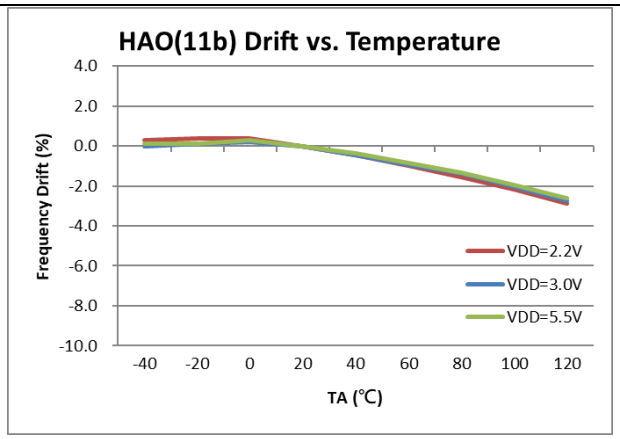


Figure 6.2-5 HAO(9.8304MHz) vs. Temperature

6.3. Supply current into VDD excluding peripherals current

T_A = 25℃,V_{DD} = 3.0V,OSC_LPO = 14.5KHz,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{AM1}	Active mode 1	OSC_CY = off, OSC_HAO = 9.8304MHz, CPU_CK = 9.8304MHz		600	1000	uA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO = 4.9152MHz, CPU_CK = 4.9152MHz		320	650	uA
I_{LP1}	Low Power 1	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO,		2	5	uA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		1.0	2.5	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.25	1.0	uA
I_{LP4}	Low Power 4	OSC_CY =32768Hz, OSC_HAO = off, CPU_CK =32768Hz, Idle state		1.8	3.6	uA

OSC_CY：External Oscillator frequency.

OSC_HAO：Internal High Accuracy Oscillator frequency.

CPU_CK：CPU core work frequency.

T_A = 25℃,V_{DD} = 5.5V,OSC_LPO = 14.5KHz,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{AM1}	Active mode 1	OSC_CY = off, OSC_HAO = 9.8304MHz, CPU_CK = 9.8304MHz		1200	1800	uA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO = 4.9152MHz, CPU_CK = 4.9152MHz		720	1200	uA
I_{LP1}	Low Power 1	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO,		4	10	uA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		2.5	5	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.4	2	uA

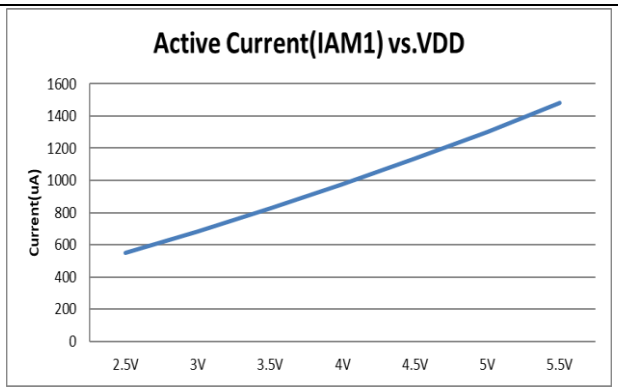


Figure 6.3-1 I_{AM1} vs. VDD

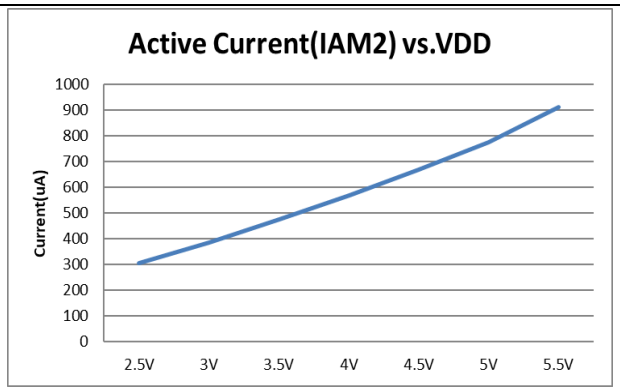
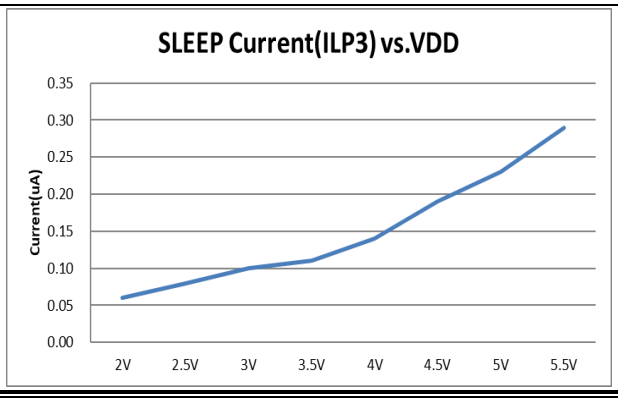


Figure 6.3-2 I_{AM2} vs. VDD



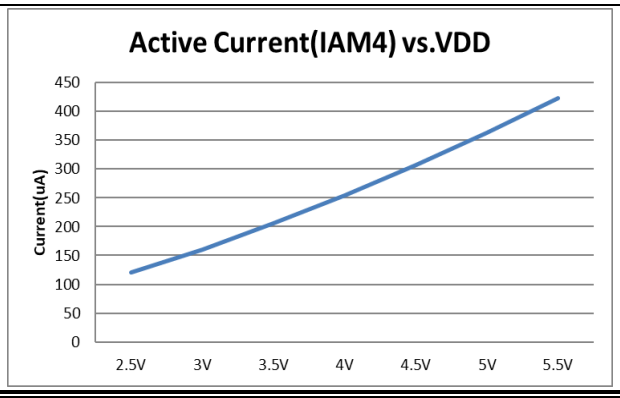


Figure 6.3-3 I_{AM3} vs. VDD

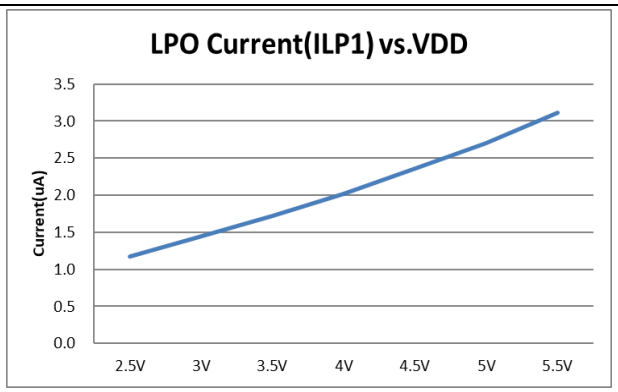


Figure 6.3-4 I_{AM4} vs. VDD

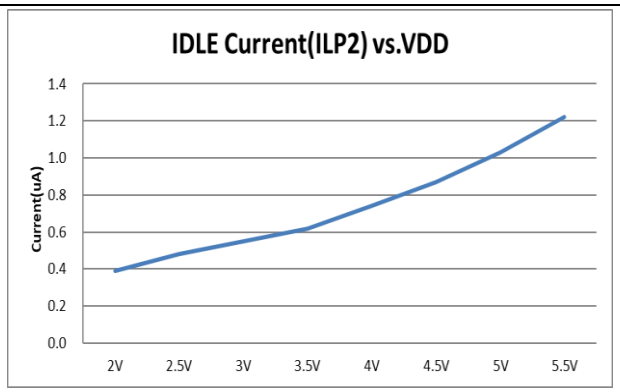


Figure 6.3-5 I_{LP1} vs. VDD

Figure 6.3-6 I_{LP2} vs. VDD

Figure 6.3-7 I_{LP3} vs. VDD

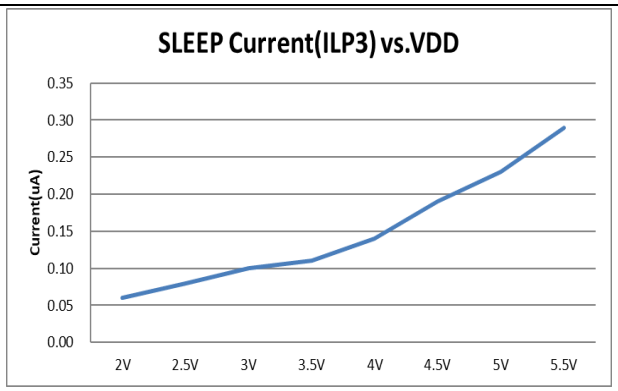
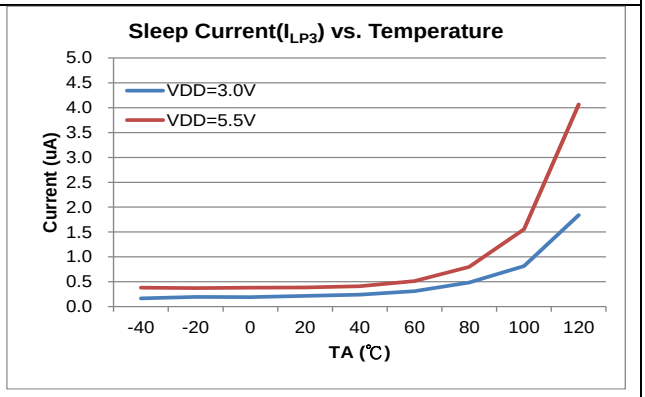


Figure 6.3-8 I_{LP3} vs. Temperature



6.4. Port 1,2,3,6,8

T_A = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				0.7*V_{DD}	V
V_{IL}	Low-Level input voltage		0.3*V_{DD}			
V_{hys}	Input Voltage hysteresis(V_{IH} - V_{IL})			0.3*V_{DD}		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance			60		kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	VDD=3V, I_{OH}=-10mA,	V_{DD} -0.4			V
		VDD=5V, I_{OH}=-15mA,	V_{DD} -0.4			
V_{OL}	Low-level output voltage	VDD=3V, I_{OL}=10mA			V_{SS} +0.4	
		VDD=5V, I_{OL}=15mA			V_{SS} +0.4	

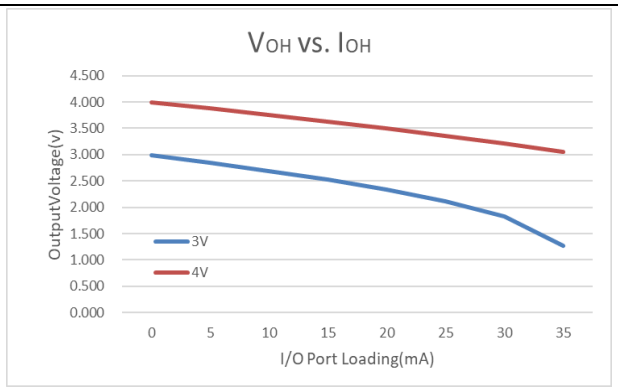


Figure 6.4-1 V_{OH} vs. I_{OH}

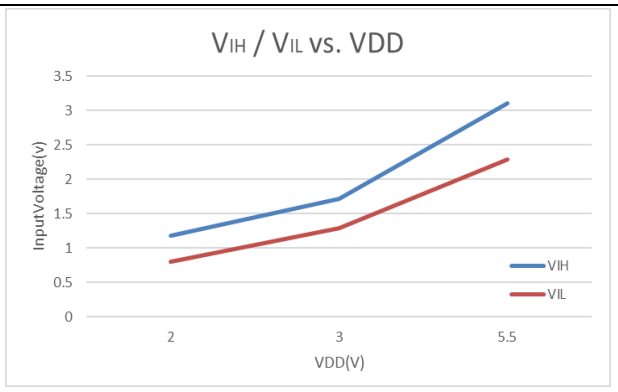


Figure 6.4-2 V_{IH}/V_{IL} vs. VDD

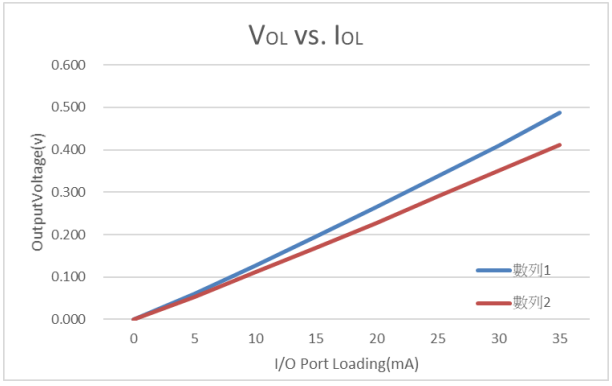


Figure 6.4-3 V_{OL} vs. I_{OL}

6.5. Reset(Brownout)

T_A = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
BOR1	Pulse length needed to accepted reset internally, t_{d-LVR1}			2			uS
	V_{DD} Start Voltage to accepted reset internally (L➔H),V_{HYS1}			1.0	1.35	1.65	V
	BOR1 current, I_{BOR1}				0.2	0.5	uA
	Temperature Drift				5		%
BOR2	Pulse length needed to accepted reset internally, t_{d-LVR2}			2			uS
	V_{DD} Start Voltage to accepted reset internally (L➔H),V_{HYS2}, and BOR_TH[2:0]:		000b	-8%	1.73	+8%	V
			001b	-8%	2.0	+8%	
			010b	-8%	2.22	+8%	
			011b	-8%	2.5	+8%	
			100b	-8%	2.72	+8%	
			101b	-8%	3.0	+8%	
			110b	-10%	3.63	+10%	
			111b	-10%	4.0	+10%	
	V_{DD} Start Voltage to accepted reset internally (H➔L),V_{LVR2}, and BOR_TH[2:0]:		000b	-8%	1.67	+8%	V
			001b	-8%	1.96	+8%	
			010b	-8%	2.17	+8%	
			011b	-8%	2.44	+8%	
			100b	-8%	2.69	+8%	
			101b	-8%	2.96	+8%	
			110b	-10%	3.58	+10%	
			111b	-10%	3.94	+10%	
	Hysteresis, $V_{HYS2-LVR2}$			25	60	90	mV
	BOR2 current, I_{BOR2}				10	15	uA
	Temperature Drift				3	5	%
RST	Pulse length needed as RST/VPP pin to accepted reset internally, t_{d-RST}			2			uS
	Input Voltage to accepted reset voltage				1.1		V
	Reset release voltage				2		V

BOR1/BOR2：Brownout Reset 1/2

LVR：Low Voltage Reset of BOR

RST：External Reset pin

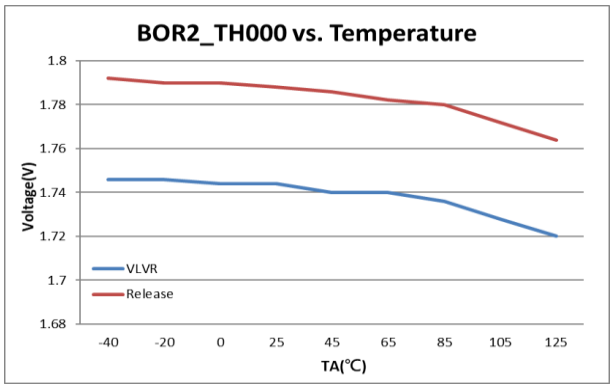
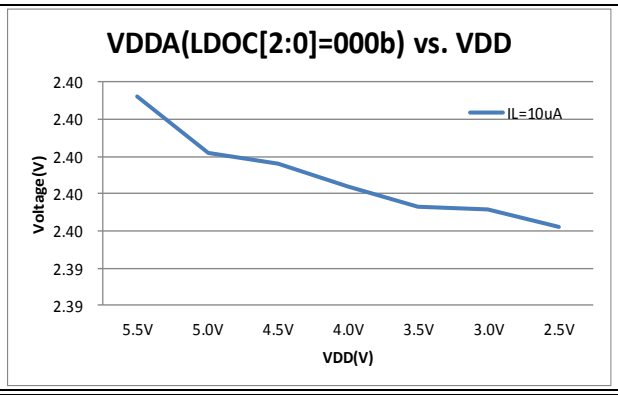


Figure 6.5-1 BOR vs. Temperature

6.6. Power System

T_A = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
VDDA	VDDA operation current, I_{VDDA}	I_L = 0mA	LDOC[2:0]=000b		20		uA
	Select VDDA output voltage	I_L = 0.1mA, VDD≧ VDDA+0.25V	LDOC [2:0]=000b	-5%	2.4	+5%	V
			LDOC [2:0]=001b		2.6		V
			LDOC [2:0]=010b		2.9		V
			LDOC [2:0]=011b		3.3		V
			LDOC [2:0]=100b		3.6		V
			LDOC [2:0]=101b		4.0		V
			LDOC [2:0]=110b		4.5		V
	Dropout voltage	I_L = 10mA	LDOC [2:0]=000b		250		mV
	Temperature drift	LDOC [2:0]=000b I_L = 0.1mA	T_A=-40℃~85℃		50		PPM/℃
	V_{DD} Voltage drift	LDOC [2:0]=000b	V_{DD}=2.2V~5.5V		±0.2		%/V
AGND	AGND operation current, I_{Agnd}	SAGND≠000b	I_L = 0mA		400		uA
	Output voltage ,V_{Agnd}	SAGND=001b	I_L = 0uA	-5%	VDDA*0.3	-5%	V
		SAGND=010b	I_L = 0uA	-5%	VDDA*0.1	-5%	V
		SAGND=011b	I_L = 0uA	-5%	VDDA*0.5	-5%	V
		SAGND=100b	I_L = 0uA	-5%	VDDA*0.4	-5%	V
REFO	REFO operation current, I_{AREFO}		I_L = 0uA		260		uA
	V(REFO,VSS)		I_L = 0uA	-3%	1,2	-3%	V
	Temperature drift		T_A=-40℃~85℃		100		ppm/℃
	RMS Noise				60		uVrms
VDDA：Adjust Voltage Regulator,							



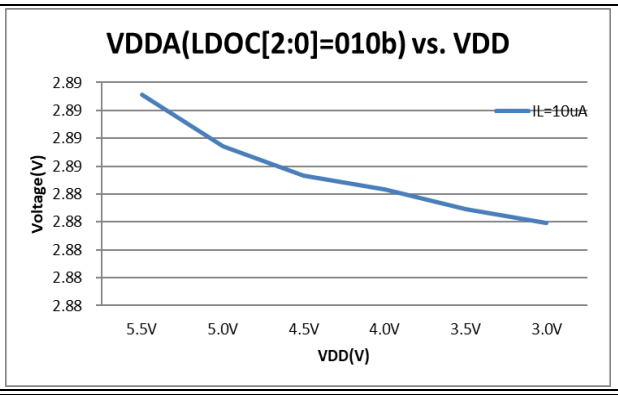


Figure 6.6-1 VDDA(000b) vs. VDD

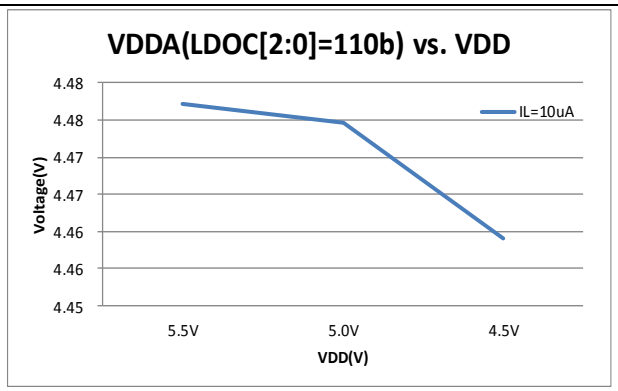


Figure 6.6-2 VDDA(010b) vs. VDD

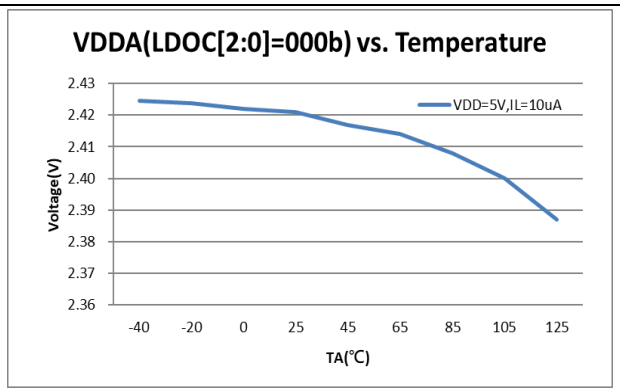


Figure 6.6-3 VDDA(110b) vs. VDD

Figure 6.6-4 VDDA(000b) vs. Temperature

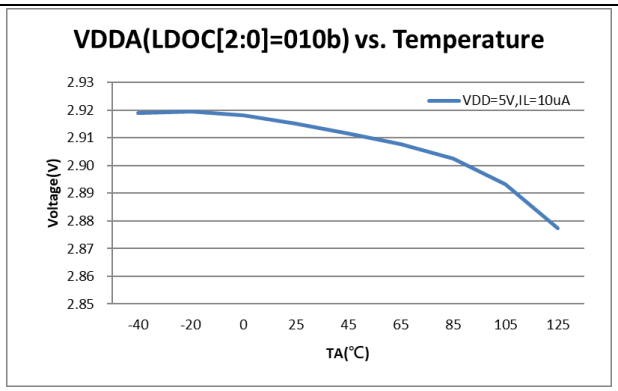


Figure 6.6-5 VDDA(010b) vs. Temperature

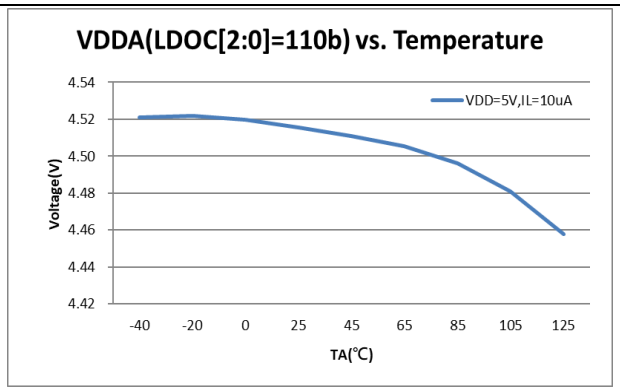


Figure 6.6-6 VDDA(110b) vs. Temperature

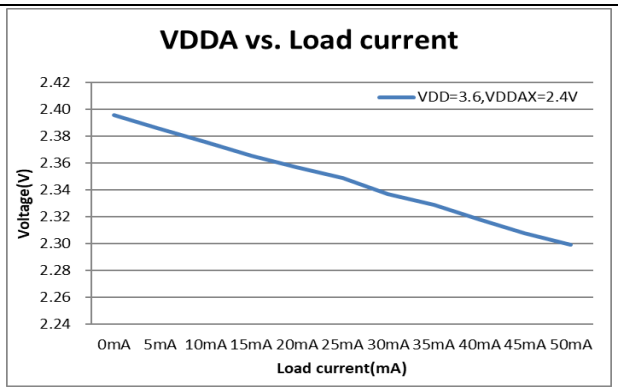


Figure 6.6-7 VDDA vs. Load current

6.7. Multi-Function Comparator

TA = 25℃,VDD = 3.0V, unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
IMC	Operation supply current	ENCMP[0]=1, CMPHS[0]=1b		5		uA
	Low Power Mode	ENCMP[0]=1, CMPHS [0]=0b		1		
VIC	Common-mode input voltage		0		VDD-1	V
VOS	Offset voltage		-5		5	mV
Vhys	Input hysteresis		0	0.7	1.5	mV
Vaccy	Reference Voltage	ENLDO[0]=1b, CPPS[1:0]=11b, VRSEL[0]=1b	1.15	1.2	1.25	V
	Temperature Drift			50		ppm/℃
	VDD Voltage drift			±0.2		%/V
IR	Multi-node resistor current	CPRL[0]=0b		10		uA
		CPRL[0]=1b		30		
	ENLDO[0]=1b,CPPS[1:0]=11b,CPRH[1:0]=01b,CPRL[0]=0b.	CPDA[4:0]=00011b	-5%	3.89	5%	V
		CPDA[4:0]=00100b		3.73		
		CPDA[4:0]=00101b		3.58		
		CPDA[4:0]=00110b		3.44		
		CPDA[4:0]=00111b		3.31		
		CPDA[4:0]=01000b		3.19		
		CPDA[4:0]=01001b		3.08		
		CPDA[4:0]=01010b		2.98		
		CPDA[4:0]=01011b		2.88		
		CPDA[4:0]=01100b		2.79		
		CPDA[4:0]=01101b		2.71		
		CPDA[4:0]=01110b		2.63		
		CPDA[4:0]=01111b		2.55		
		CPDA[4:0]=10000b		2.48		
		CPDA[4:0]=10001b		2.42		
		CPDA[4:0]=10010b		2.35		
		CPDA[4:0]=10011b		2.29		
		CPDA[4:0]=10100b		2.24		
		CPDA[4:0]=10101b		2.18		
		CPDA[4:0]=10110b		2.13		
		CPDA[4:0]=10111b		2.08		
		CPDA[4:0]=11000b		2.03		
		CPDA[4:0]=11001b		1.99		
		CPDA[4:0]=11010b		1.94		

		CPDA[4:0]=11011b		1.90		
		CPDA[4:0]=11100b		1.86		
		CPDA[4:0]=11101b		1.82		
	CPDA[4:0]=00000b~00010b, and 11110b~11111b (reserved)					

LVD：Low Voltage Detect.

6.8. LCD

T_A = 25℃,V_{DD} = 3.3V, C_{VLCD} =4.7uF,unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{LCD}	Operation supply current with output buffer.(all segment turn on, No load)	ENLCP[0]=1	V_{DD} = 3.0V		8		uA
VLCD	Supply Voltage at VLCD pin	ENLCP [0]=0		2.4		5	V
	Embedded Charge Pump output voltage at VLCD pin	V_{DD} = 3.3V, ENLCP [0]=1, C_{VLCD} =4.7uF	LCDV[2:0]=111b	-10%	2.45	+10%	V
			LCDV[2:0]=110b	-10%	2.70	+10%	
			LCDV[2:0]=101b	-10%	2.85	+10%	
			LCDV[2:0]=100b	-10%	3.10	+10%	
			LCDV[2:0]=011b	-10%	3.30	+10%	
			LCDV[2:0]=010b	-10%	4.10	+10%	
			LCDV[2:0]=001b (VDD>2.4V mode)	-10%	4.55	+10%	
			LCDV[2:0]=000b (VDD>2.75V)	-10%	5.1	+10%	
	VDD Voltage drift	ENLCP [0]=1, CV_{LCD} =4.7uF, LCDV[2:0]>010b,VDD=2.2V~ 5.5V; LCDV[2:0]=001b,VDD>2.4V; LCDV[2:0]=000b,VDD>2.75V;			4		%/V
Z_{LCD}	Output impedance with LCD buffer	f_{LCD} =128Hz,VLCD=3.05V			10		kΩ

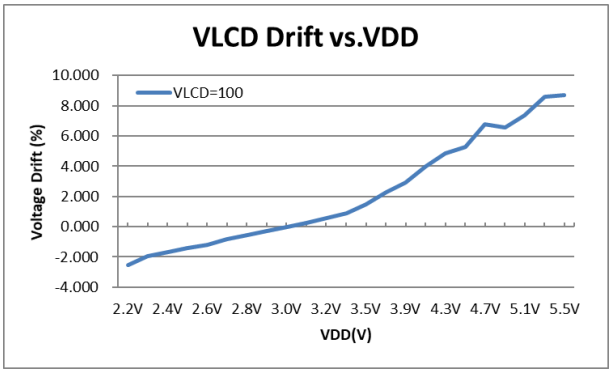


Figure 6.8-1 VLCD(LCDV=100b) vs. VDD

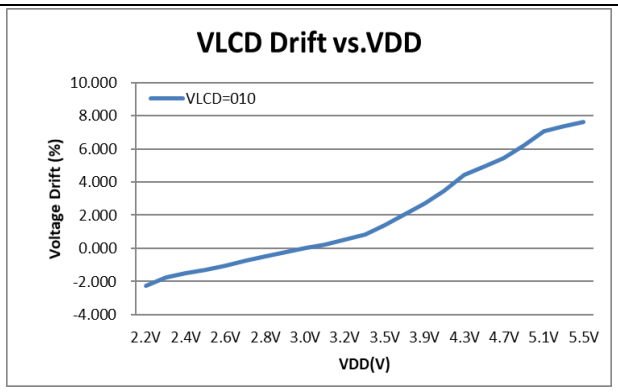


Figure 6.8-2 VLCD(LCDV=010b) vs. VDD

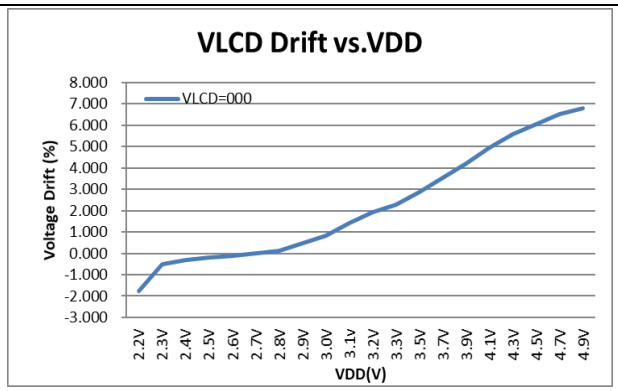
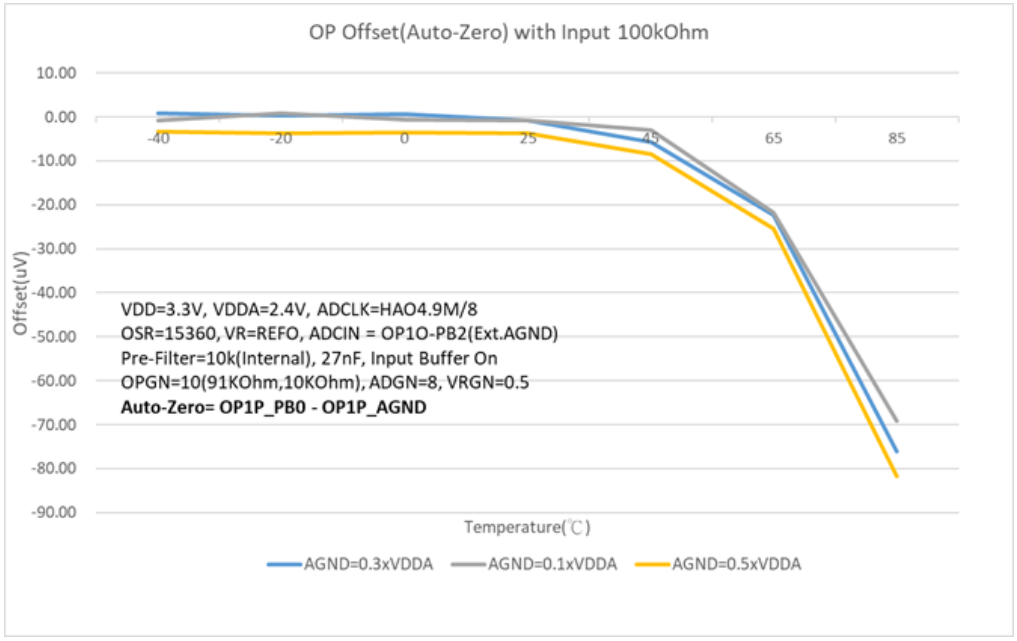


Figure 6.8-3 VLCD(LCDV=000b) vs. VDD

6.9. OPAMP

TA = 25℃,VDD = 3.3V, VDDA=2.4V, AGND=0.3VDDA, Input buffer on unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{os-op}	Input offset voltage	OP Gain=10, ADGN=8, VRGN=0.5 Pre-Filter=10K(Inside) / 27nF(Outside)			800	uV
	Input offset voltage with Auto-Zero	Auto-Zero(OP1P_PB0-OP1P_AGND) OP Gain=10, ADGN=8, VRGN=0.5 Pre-Filter=10K(Inside) / 27nF(Outside)		-2		uV
V_{os-td}	OP Input offset temperature drift	with chopper, TA=-40℃ ~ 85℃		0.64		uV/℃
CMVR	Common-mode voltage input range		VSS+0.1		VDDA - 1.1	V



6.10. ΣADC, Power Supply and recommended operating conditions

TA = 25℃,VDD = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{SD18}	Supply Voltage at VDDA	ENLDO[0]=0		2.4		5.5	V
$I_{\Sigma\Delta ADC}$	Operation supply current	Input gain =1, input buffer on			254		uA
$f_{\Sigma ADC}$	Modulator sample frequency, ADC_CK				1		MHz
	Over Sample Ratio, OSR			32		61440	
Eos	Input offset voltage	Chopper on OSR=61440	Input gain=1, reference gain=1		1		uV
Vrms	Input RMS Noise	Chopper on, OSR=61440, input gain=1 reference gain=1			3.5		uV
		Chopper off, OSR=32, input gain=1 reference gain=1			350		uV
NM	Normal Rejection ratio	Chopper On OSR=61440	Input gain=1, reference gain=1. Vin=200mVrms 50/60Hz		60		dB
AC_{bw}	AC Measurement Bandwidth	OSR=32, LPFBW=1024 Without Voltage Divider	0.5% error	20		4k	Hz
			3dB				
			Square wave, 0.5% error			0.3k	
			Triangle wave, 0.5% error				

		A/D Clock=1MHz	*ENOB(RMS) with OSR/GAIN at A/D Clock=0.5MHz, VDD=3.3V, VDDA=2.4V, AGND=0.3VDDA, VREF=1.2,Vin=Ext.Short, Chopper Off;*						
Max. Vin(mV) =0.9*VREF[1]	**OSR**	**32**	**64**	**128**	**256**	**7680**	**15360**	**30720**	**61140**
	Output rate(Hz)	**31250**	**7813**	**3906**	**1953**	**65**	**33**	**16**	**8**
	Gain								
±2160	**0.5**	**12.63**	14.09	14.78	15.3	17.96	18.39	18.7	19
±1080	**1**	**12.77**	14.09	14.66	15.13	17.9	18.24	18.57	18.87
±540	**2**	**12.66**	14.01	14.62	15.13	17.68	18.01	18.29	18.41
±270	**4**	**12.53**	13.81	14.53	15.12	17.28	17.7	17.57	18.06
±135	**8**	**12.29**	13.46	14.17	14.77	16.78	16.8	16.97	16.98

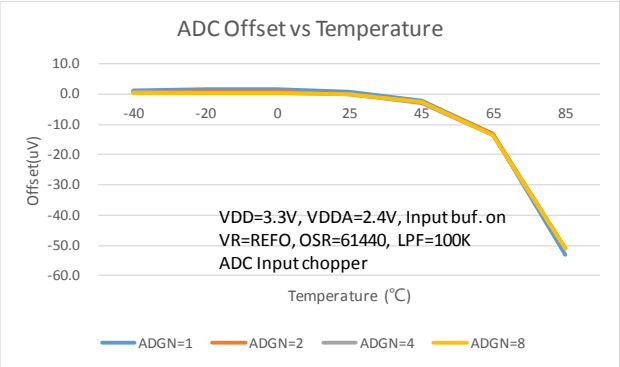
		A/D Clock=1MHz	*RMS Noise(uV) with OSR/GAIN at A/D Clock=0.5MHz, VDD=3.3V, VDDA=2.4V, AGND=0.3VDDA, VREF=1.2,Vin=Ext.Short, Chopper Off;*						
Max. Vin(mV) =0.9*VREF[1]	OSR	32	64	128	256	7680	15360	30720	61140
	Output rate(Hz)	31250	7813	3906	1953	65	33	16	8
	Gain								
±2160	0.5	759.55	276.19	170.49	118.99	18.77	13.94	11.24	9.16
±1080	1	344.59	137.19	92.75	66.86	9.80	7.75	6.17	5.02
±540	2	185.38	72.84	47.80	33.52	5.72	4.54	3.75	3.44
±270	4	101.38	41.88	25.35	16.90	3.77	2.82	3.08	2.19
±135	8	59.82	26.70	16.28	10.74	2.66	2.62	2.34	2.33

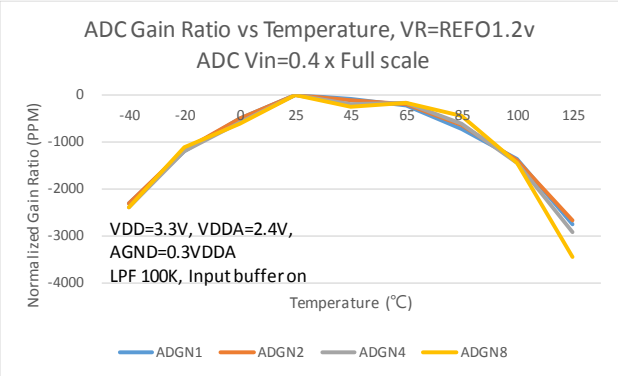
Table 6.10-1(a) SD18, Chopper Off, ENOB and RMS Noise Table

ENOB(RMS) with OSR/GAIN at A/D Clock=0.5MHz, VDD=3.3V, VDDA=2.4V, AGND=0.3VDDA, VREF=1.2,Vin=Ext.Short, Chopper On ;								
Max. Vin(mV) =0.9*VREF[1]	**OSR**	**64**	**128**	**256**	**7680**	**15360**	**30720**	**61140**
	Output rate(Hz)	**3906**	**1953**	**977**	**33**	**16**	**8**	**4**
	Gain							
±2160	**0.5**	14.71	15.27	15.88	18.5	18.85	19.2	19.47
±1080	**1**	14.74	15.32	15.79	18.42	18.83	19.14	19.45
±540	**2**	14.6	15.13	15.57	18.36	18.75	19.03	19.32
±270	**4**	14.48	15.08	15.76	18.09	18.43	18.74	18.86
±135	**8**	14.05	14.77	15.33	17.56	17.9	18.03	18.18

RMS Noise(uV) with OSR/GAIN at A/D Clock=0.5MHz, VDD=3.3V, VDDA=2.4V, AGND=0.3VDDA, VREF=1.2,Vin=Ext.Short, Chopper On;								
Max. Vin(mV) =0.9*VREF[1]	**OSR**	**64**	**128**	**256**	**7680**	**15360**	**30720**	**61140**
	Output rate(Hz)	**3906**	**1953**	**977**	**33**	**16**	**8**	**4**
	Gain							
±2160	**0.5**	179.26	121.63	79.58	12.92	10.16	7.97	6.61
±1080	**1**	87.63	58.69	42.32	6.85	5.14	4.17	3.34
±540	**2**	48.37	33.37	24.68	3.56	2.73	2.24	1.83
±270	**4**	26.26	17.36	10.85	2.15	1.70	1.37	1.26
±135	**8**	17.66	10.71	7.31	1.55	1.23	1.12	1.01

Table 6.10-1(b) SD18, Chopper On, ENOB and RMS Noise Table





6.10.1. ΣADC,Temperature Sensor

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TC_S	Sensor temperature drift			173		uV/℃
KT	Absolute Temperature Scale 0°K			284		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~85℃		±2		℃

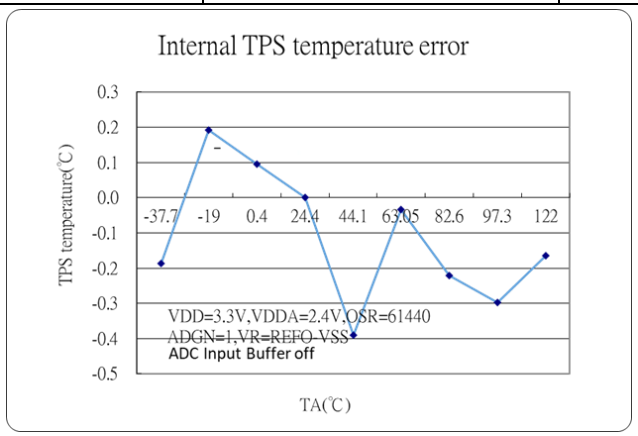


Figure 6.10-2 ADC Temperature Error

6.11. Analog input and switch performance

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V AGND=0.5VDDAunless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{AL}	Analog Input Leakage Current	AGND=0.5 VDDA		10	100	pA
		AGND=0.3VDDA		10	100	
		AGND=0.1VDDA		100	500	

6.12. Build-In EPROM(BIE)

T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{BIE}	Supply Voltage at VPP PIN			8.5	8.75	V
I_{BIE}	Operation supply current			3		mA
V_{SS}	Supply Voltage			0		V
When connecting to the external V_{BIE} power source to program the BIE block, users can use the instruction to program the words one by one into the BIE block.						

6.13. Build-In EPROM(BIE) Low voltage control circuit

T_A = 25℃,V_{DD} = 3.05V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
T_O	Operation temperature range		0	25	40	℃
V_{DD}	Operation supply Voltage		2.75		5.5	V
V_{SS}	Supply Voltage			0		V
When the 2.75V low voltage programming control circuit is activated, users can program the BIE block without connecting to the external V_{BIE} power source.						

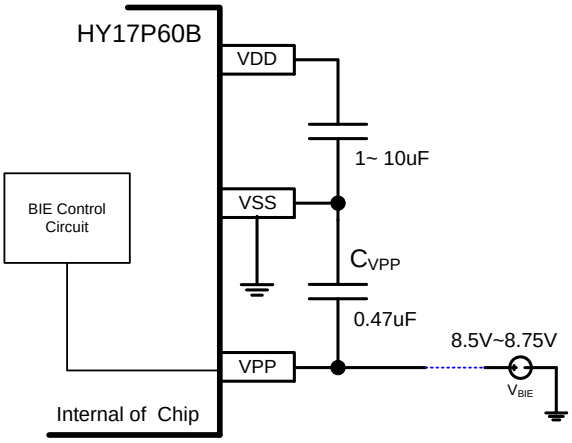


Figure 6.13-1 BIE typical application block diagram

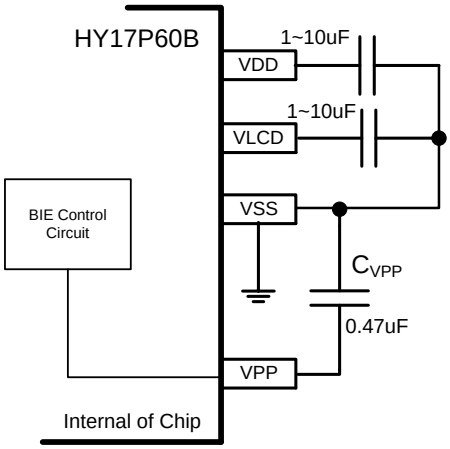


Figure 6.13-2 BIE typical application use low voltage control circuit block diagram

7. Ordering Information

Device[1]	Package Type	Pins	Package Drawing		Code[2]	Shipment Packing Type	Unit Q'ty	Material Composition	MSL3
HY17P60B-D000	Die	-	D	000	000	Tray	250	Green[4]	-
HY17P60B-L064	LQFP	64	L	064	000	Tray	250	Green[4]	MSL-3
HY17P60B-NS32	QFN	32	N	S32	000	Tape & Reel	5000	Green[4]	MSL-3

[1] **Device No.: Model No. – Package Type Description – Code** (Blank Code/ Standard/ Customized Programming Code)

Ex: Your customized programming code is 001 and you require die shipment.

The device No. will be HY17P60B-D000-001.

Ex: You request blank code in die package.

The device No. will be HY17P60B-D000.

Ex: You request blank code in LQFP 64 package.

The device No. will be HY17P60B-L064.

And please clearly indicate the shipment packing type when placing orders.

Ex: Your customized programming code is 008 and you require products in LQFP 64 package.

The device No. will be HY17P60B-L064-008.

And please clearly indicate the shipment packing type when placing orders.

[2] **Code :**

"001"~ "999" is standard or customized programming code. Blank code does not have these numbers.

[3] **MSL:**

The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization.

The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

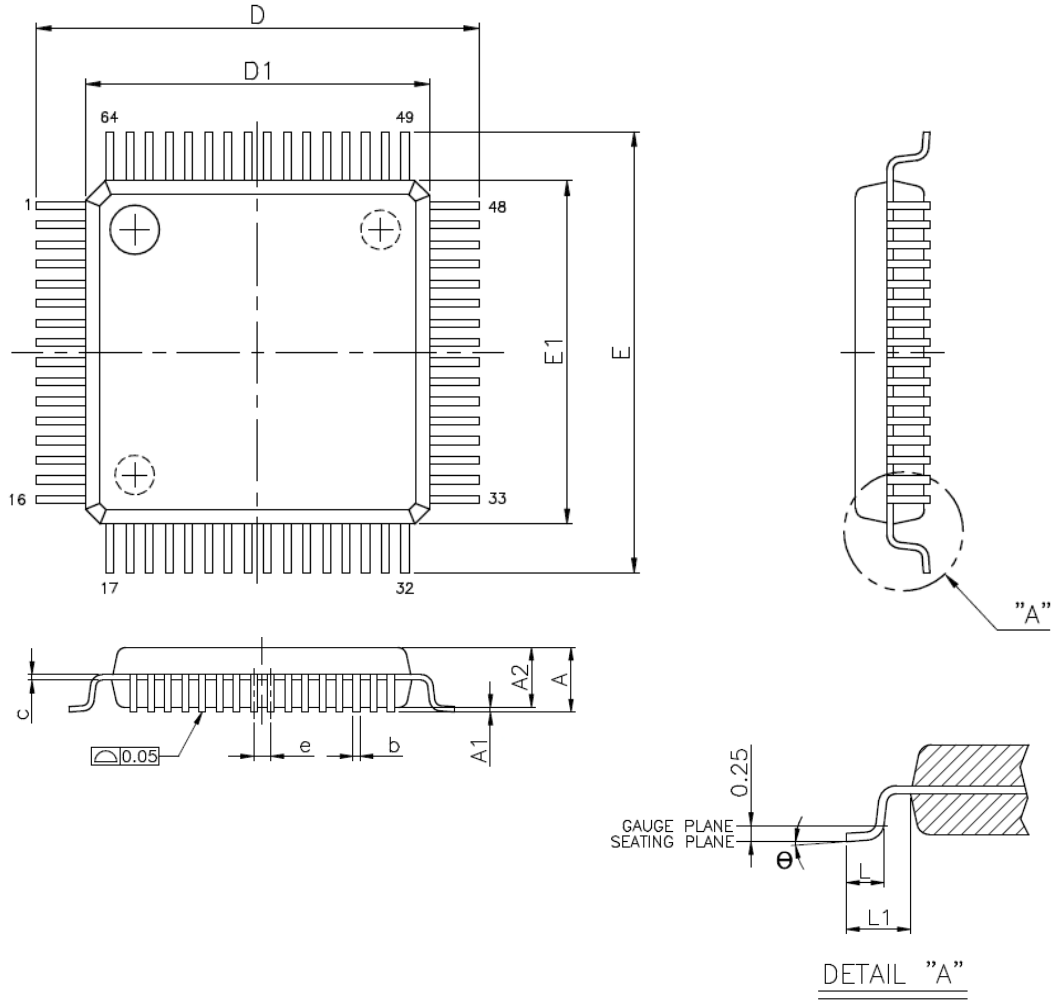
[4] **Green (RoHS & no Cl/Br):**

HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br<900ppm or Cl<900ppm or (Br+Cl)<1500ppm).

8. Package Information

8.1. LQFP64(L064)

8.1.1. Package Dimensions LQFP64(7x7)

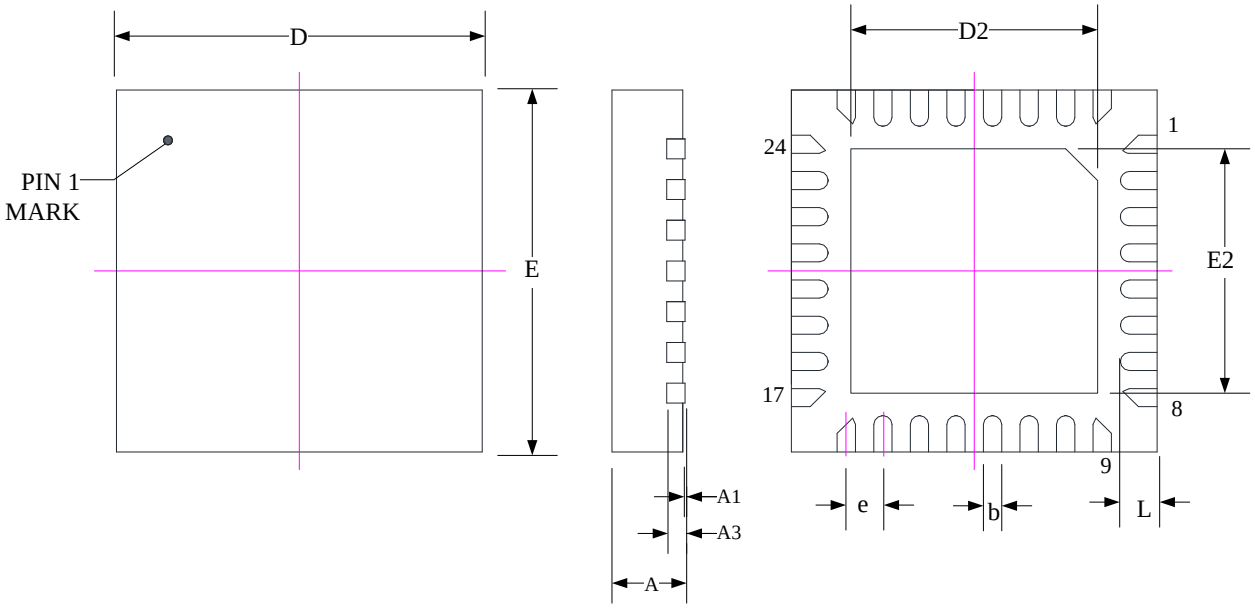


SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Note:
1. All dimensions refer to JEDEC OUTLINE MS-026.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

8.2. QFN32(NS32)

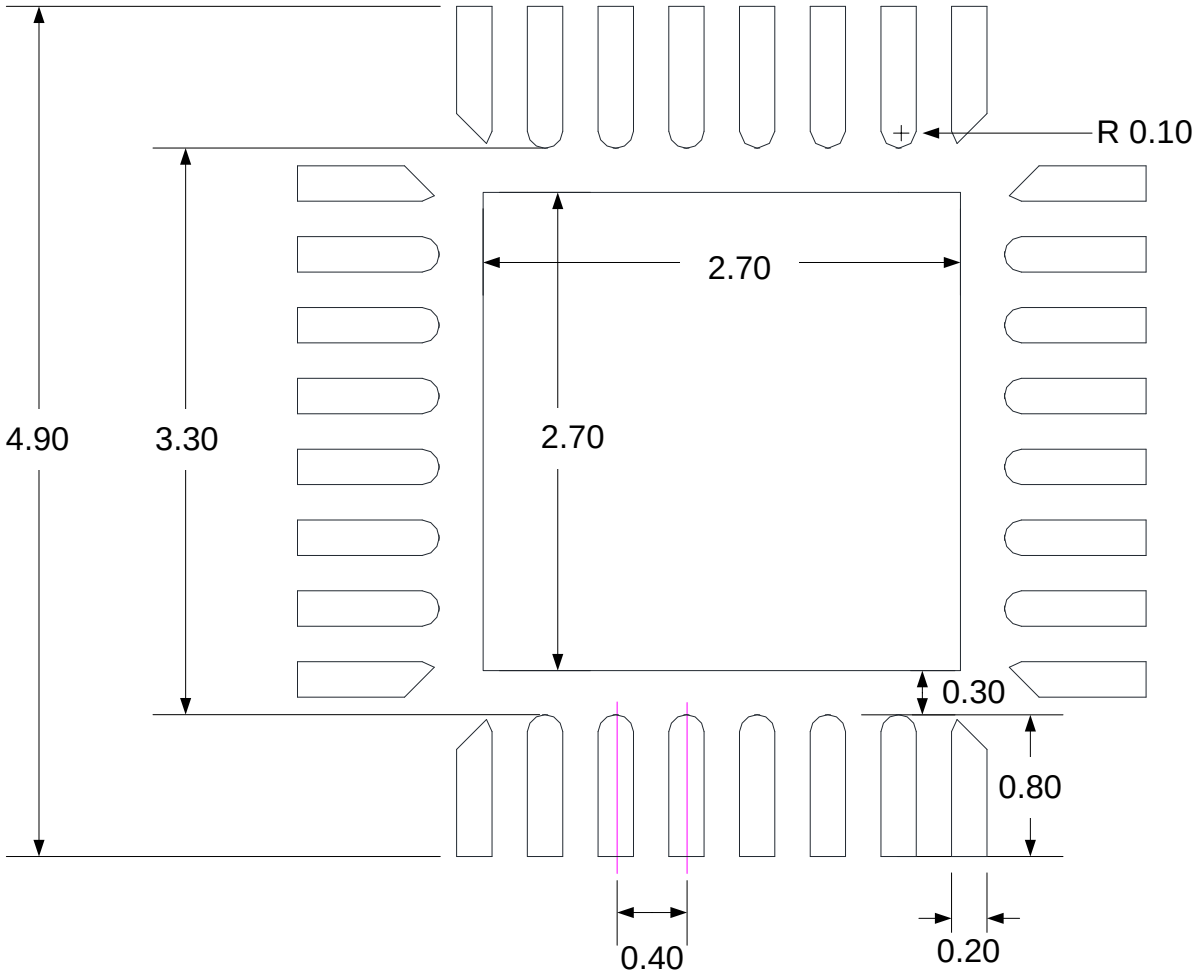
8.2.1. Package Dimensions QFN32(4x4x0.55)



SYMBOLS	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	0.15 REF.		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.65	2.70	2.75
E2	2.65	2.70	2.75
L	0.25	0.30	0.35
e	0.40 BASIC		

Note:
1. All dimensions refer to JEDEC OUTLINE MO-220.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.
4. https://www.hycontek.com/hy_mcu/QFN_DFN_PCB_EN.pdf

8.2.2. Land Pattern Design Recommendations

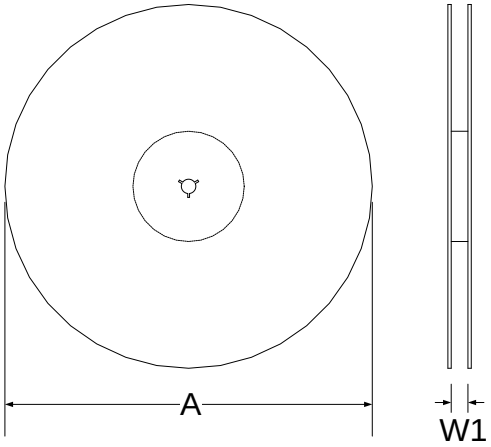


Note:
1. Publication IPC-7351 is recommended for alternate designs.
2. https://www.hycontek.com/wp-content/uploads/QFN_DFN_PCB_EN.pdf
3. Unit: mm.

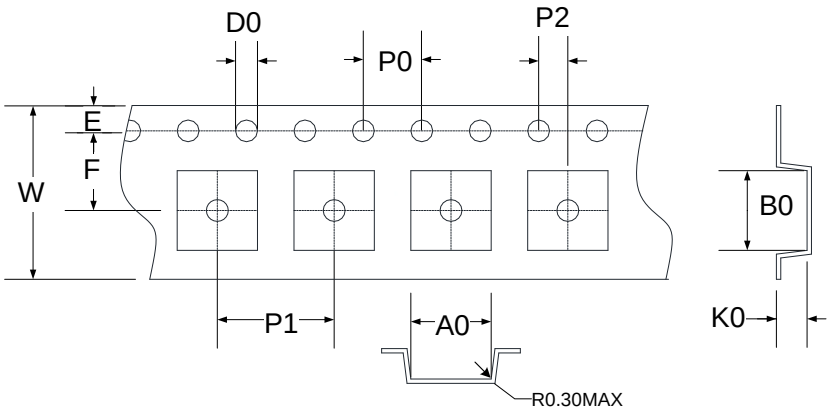
8.2.3. Tape & Reel Information

8.2.3.1. Reel Dimensions

Unit: mm



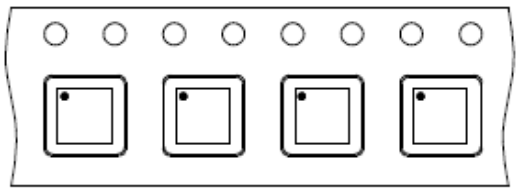
8.2.3.2. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	4.35	4.35	1.10	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

8.2.3.3. Pin1 direction



9. Revision Record

Major differences are stated thereinafter:

Version	Page	Date	Revision Summary
V01	All	2021/09/22	First edition
V02	46	2022/03/21	Update the unit quantity of Die & QFN32 package type
	48	2022/03/21	Update the package dimensions of QFN32 package type to 4x4x0.55