HY17M24
Datasheet

8-Bit RISC-like Mixed Signal Microcontroller
Embedded 24-Bit ΣΔADC
Rail to Rail OPAMP

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注意：

1、 本說明書中的內容，隨著產品的改進，有可能不經過預告而更改。請客戶及時到本公司網站下載更新 http://www.hycontek.com。

2、 本規格書中的圖形、應用電路等，因第三方工業所有權引發的問題，本公司不承擔其責任。

3、 本產品在單獨應用的情況下，本公司保證它的性能、典型應用和功能符合說明書中的條件。當使用在客戶的產品或設備中，以上條件我們不作保證，建議客戶做充分的評估和測試。

4、 請注意輸入電壓、輸出電壓、負載電流的使用條件，使 IC 內的功耗不超過封裝的容許功耗。對於客戶在超出說明書中規定額定值使用產品，即使是瞬間的使用，由此所造成的損失，本公司不承擔任何責任。

5、 本產品雖內置防靜電保護電路，但請不要施加超過保護電路性能的過大靜電。

6、 本規格書中的產品，未經書面許可，不可使用在要求高可靠性的電路中。例如健康醫療器械、防災器械、車輛器械、車載器械及航空器械等對人體產生影響的器械或裝置，不得作為其部件使用。

7、 本公司一直致力於提高產品的品質和可靠度，但所有的半導體產品都有一定的失效概率，這些失效概率可能會導致一些人身事故、火災事故等。當設計產品時，請充分留意冗餘設計並採用安全指標，這樣可以避免事故的發生。

8、 本規格書中內容，未經本公司許可，嚴禁用於其他目的之轉載或複製。

1. 特點

- **8-Bit RISC-like 微控制器**
  - 具有 71 條高性能指令集 H08D
  - 硬體查表器
  - Power On/ Brown Out 1/ Brown Out 2
  - WDT/MCLR Reset
- **工作電壓與操作溫度範圍**
  - VDD = 1.9V ~ 5.5V 數位電路
  - VDDA = 2.4V ~ 5.5V 類比電路
  - - 40°C ~ 85°C 工作溫度
- **記憶體**
  - 4K words MTP 程式記憶體(燒錄次數 100 次)
  - 32 bytes EEPROM 資料記憶體(燒錄次數 3K 次)
  - 256 bytes SRAM ■ 6L 堆疊
- **24-Bit ΣΔADC 類比數位轉換器**
  - 最高取樣頻率達 1MHz
  - 超取樣頻率設置 64～65536
  - 二/三階梳狀濾波器，轉換頻率 15.6Ksps
  - 信號放大 x1/4, x1/2, x1,x2,x4,x8,x16
  - 全差動輸入信號與測量範圍的零點調整
  - 低溫飄係數與內置絕對溫度傳感器
- **低功耗與低溫飄係數電源系統**
  - VDDA 線性穩壓電源
    - 供應類比電路或外部傳感器電壓源
    - 採可外灌輸入電壓設計
    - 可設置穩壓輸出 2.4V/2.6V/2.9V/3.3V /3.6V /4.0V/4.5V/5.0V
    - 支援不須外掛穩壓電容驅動線路
  - REFO 參考電壓源
    - 可設置輸出 1.2V
    - 採可外灌輸入電壓設計
- **Rail to Rail 運算放大器**
  - 積分器電路
- **12-BIT 可編程數位電阻器**
  - 可編程電阻分壓計
- **通訊介面**
  - I^2C、EUART、2 線式 ICE 與燒錄引腳
- **計時器**
  - Watch Dog
  - 8-bit Timer
  - 16-bit Timer
    - 16-Bit PWM ◆ 8-bit+8-bit PWM
- **低功耗特性**
  - 休眠模式 0.25uA@3.0V
  - 待機模式 1uA@3.0V
- **工作頻率**
  - 外接石英震盪器 32768Hz ~ 16MHz
  - 內置 HAO 震盪器，共有四種頻率可選：1.843MHz、4.147MHz、8.755MHz、17.51MHz
  - 內置低功耗 LPO 震盪器 14.5KHz
- **封裝**
  - SSOP28、QFN24、SSOP24、SOP16
- **應用領域**
  - 煙霧感測、氣體感測
  - PM2.5、紅外感測
  - 溫度感測、類比信號收集器

功能列表

Model No.	VDD (V)	Internal Clock (Hz)	System Clock (Hz)	Program Memory (word)	SRAM (byte)	Built-In EEPROM (byte)	ADC ENOB (bit x ch)	Sample Rate (sps)	I/O	Timer (bit x ch)	PWM (bit x ch)	Serial Interface (I/F x ch)	Package
HY17M24	1.9~5.5	14.5K 1.843M 4.147M 8.755M 17.51M	14.5K~16M	4K	256	32	21-bit x11	8~15.6K	9xIO	8-bit x 1 16-bit x 1	8-bit x 2 16-bit x 1	EUART x 1 I^2C x 1	SOP16
							21-bit x15		17xIO				SSOP24 QFN24 SSOP28

2. 引腳與定義

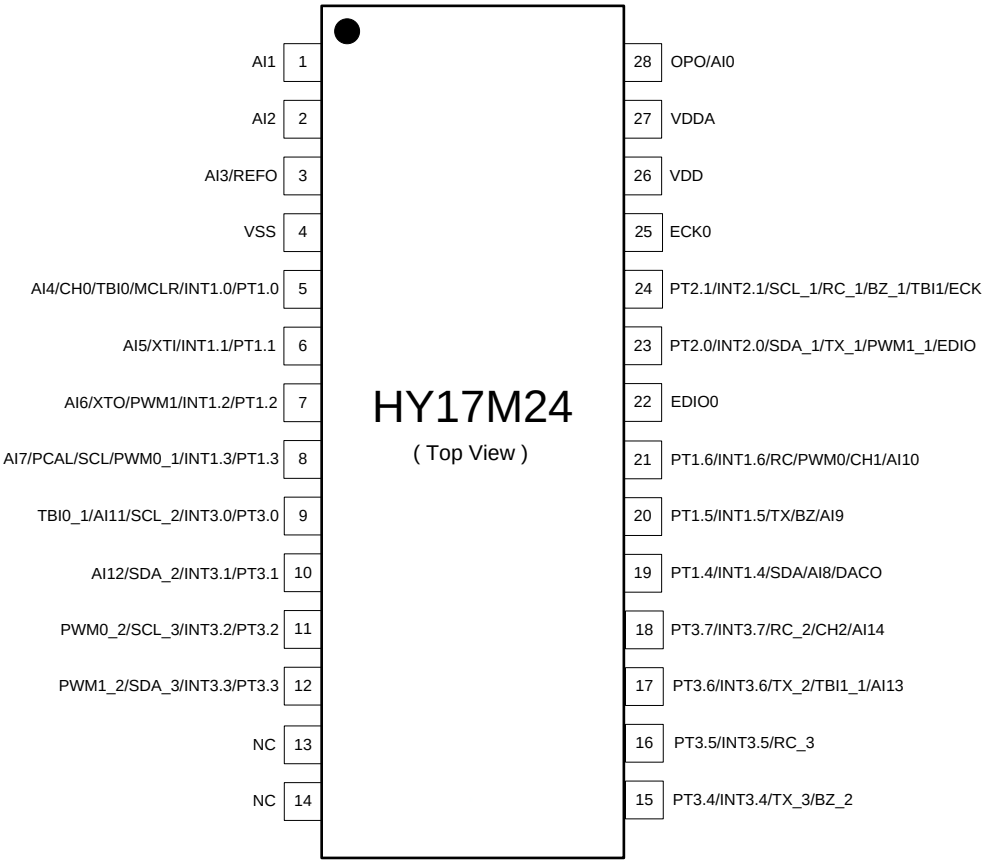


圖 2-1 引腳圖 SSOP28

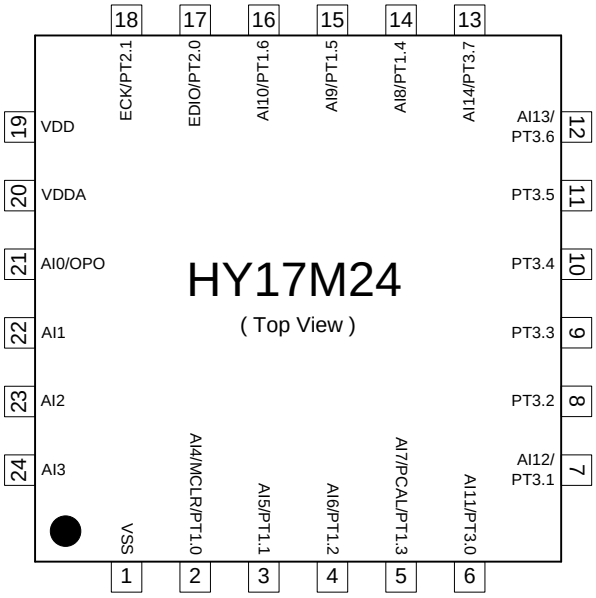


圖 2-2 引腳圖 QFN24

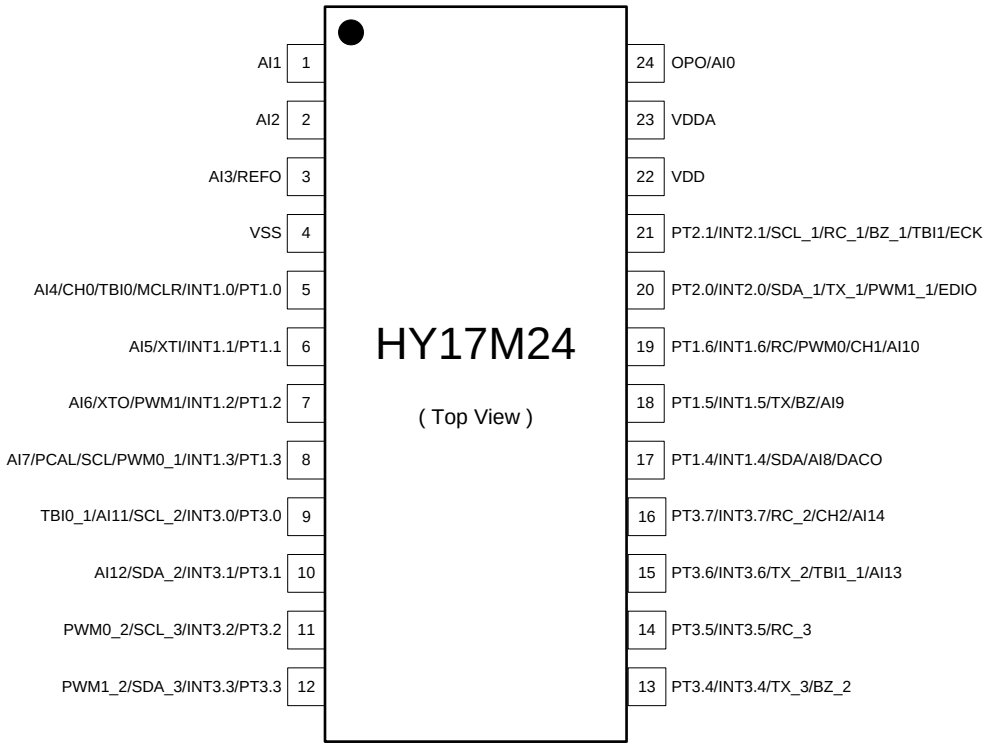


圖 2-3 引腳圖 SSOP24

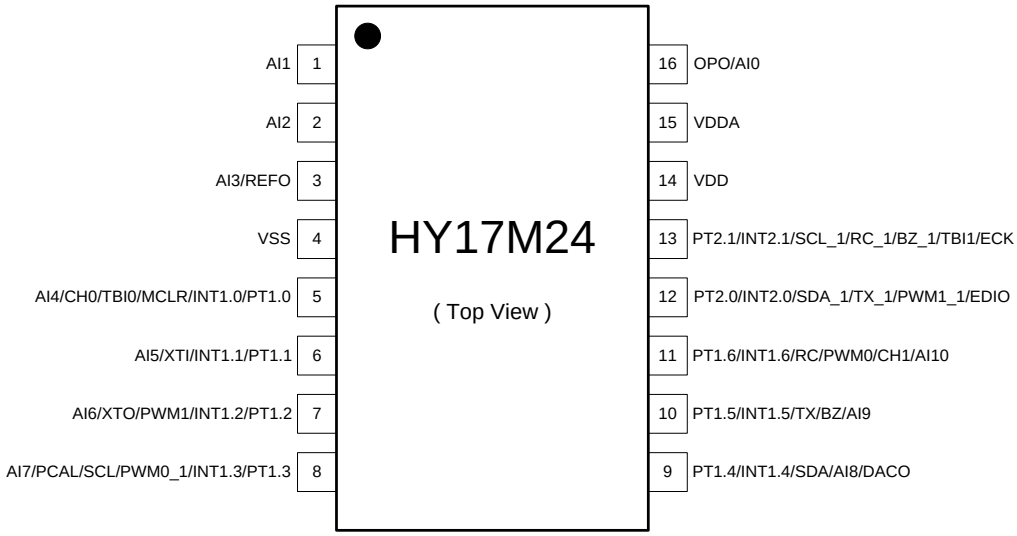


圖 2-4 引腳圖 SOP16

2.1. HY17M24 引腳定義說明

封裝 / 編號 / 腳位				設計			描述
SSOP28	QFN24	SSOP24	SOP16	名稱/功能	型式	緩衝	
1	22	1	1	AI1	A	A	類比輸入通道 1
2	23	2	2	AI2	A	A	類比輸入通道 2
3	24	3	3	AI3	A	A	類比輸入通道 3
				REFO	P	P	參考電壓引腳
4	1	4	4	VSS	P	P	晶片工作電壓源接地端引腳
5	2	5	5	PT1.0	I	S	數位輸入引腳
				INT1.0	I	S	外部中斷源 INT1.0
				MCLR	I	S	低電位有效，帶內部上拉電阻
				TBI0	I	S	TimerB CPI 輸入選擇源
				CH0	A	A	比較器輸入通道 0
				AI4	A	A	類比輸入通道 4
6	3	6	6	PT1.1	I/O	S/C	數位輸入 / 輸出引腳
				INT1.1	I	S	外部中斷源 INT1.1
				XTI	A	A	外接震盪器輸入端
				AI5	A	A	類比輸入通道 5
7	4	7	7	PT1.2	I/O	S/C	數位輸入 / 輸出引腳
				INT1.2	I	S	外部中斷源 INT1.2
				PWM1	O	C	PWM1 輸出
				XTO	A	A	外接震盪器輸出端
				AI6	A	A	類比輸入通道 6
8	5	8	8	PT1.3	I/O	S/C/N	數位輸入 / 輸出引腳
				INT1.3	I	S	外部中斷源 INT1.3
				PWM0_1*[2]	O	C	PWM0 輸出
				SCL	I/O	S/C	I²C 通訊時鐘信號
				PCAL*[1]	O	C	燒錄用之頻率校正輸出引腳
				AI7	A	A	類比輸入通道 7
9	6	9	-	PT3.0	I/O	S/C/N	數位輸入 / 輸出引腳
				INT3.0	I	S	外部中斷源 INT3.0
				SCL_2*[2]	I/O	S/C	I²C 通訊時鐘信號
				AI11	A	A	類比輸入通道 11
				TBI0_1	I	S	TimerB CPI 輸入選擇源
10	7	10	-	PT3.1	I/O	S/C/N	數位輸入 / 輸出引腳
				INT3.1	I	S	外部中斷源 INT3.1

封裝 / 編號 / 腳位				設計			描述
SSOP28	QFN24	SSOP24	SOP16	名稱/功能	型式	緩衝	
				SDA_2*[2]	I/O	S/C	I²C 通訊數據信號
				AI12	A	A	類比輸入通道 12
11	8	11	-	PT3.2	I/O	S/C/N	數位輸入 / 輸出引腳
				INT3.2	I	S	外部中斷源 INT3.2
				SCL_3*[2]	I/O	S/C	I²C 通訊時鐘信號
				PWM0_2*[2]	O	C	PWM0 輸出
12	9	12	-	PT3.3	I/O	S/C/N	數位輸入 / 輸出引腳
				INT3.3	I	S	外部中斷源 INT3.3
				SDA_3*[2]	I/O	S/C	I²C 通訊數據信號
				PWM1_2*[2]	O	C	PWM1 輸出
15	10	13	-	PT3.4	I/O	S/C/N	數位輸入 / 輸出引腳
				INT3.4	I	S	外部中斷源 INT3.4
				TX_3*[2]	O	C	UART 通訊傳送信號
				BZ_2*[2]	O	C	蜂鳴器輸出端
16	11	14	-	PT3.5	I/O	S/C/N	數位輸入 / 輸出引腳
				INT3.5	I	S	外部中斷源 INT3.5
				RC_3*[2]	O	C	UART 通訊傳送信號
17	12	15	-	PT3.6	I/O	S/C/N	數位輸入 / 輸出引腳
				INT3.6	I	S	外部中斷源 INT3.6
				TX_2*[2]	O	C	UART 通訊傳送信號
				TBI1_1	I	S	TimerB CPI 輸入選擇源
				AI13	A	A	類比輸入通道 13
18	13	16	-	PT3.7	I/O	S/C/N	數位輸入 / 輸出引腳
				INT3.7	I	S	外部中斷源 INT3.7
				RC_2*[2]	O	C	UART 通訊傳送信號
				CH2	A	A	比較器輸入通道 2
				AI14	A	A	類比輸入通道 14
19	14	17	9	PT1.4	I/O	S/C/N	數位輸入 / 輸出引腳
				INT1.4	I	S	外部中斷源 INT1.4
				SDA	I/O	S/C	I²C 通訊數據信號
				AI8	A	A	類比輸入通道 8
				DACO	A	A	Resistance Ladder 電壓輸出通道
20	15	18	10	PT1.5	I/O	S/C	數位輸入 / 輸出引腳
				INT1.5	I	S	外部中斷源 INT1.5
				TX	O	C	UART 通訊傳送信號
				BZ	O	C	蜂鳴器輸出端

封裝 / 編號 / 腳位				設計			描述
SSOP28	QFN24	SSOP24	SOP16	名稱/功能	型式	緩衝	
				AI9	A	A	類比輸入通道 9
21	16	19	11	PT1.6	I/O	S/C	數位輸入 / 輸出引腳
				INT1.6	I	S	外部中斷源 INT1.6
				RC	I	S	UART 通訊接收信號
				PWM0	O	C	PWM0 輸出
				CH1	A	A	比較器輸入通道 1
				AI10	A	A	類比輸入通道 10
22	-	-	-	EDIO0	I/O	S/C	仿真及燒錄之通訊數據腳 EDIO0
23	17	20	12	PT2.0	I/O	S/C/N	數位輸入 / 輸出引腳
				INT2.0	I	S	外部中斷源 INT2.0
				SDA_1*[2]	I/O	S/C	I²C 通訊數據信號
				TX_1*[2]	O	C	UART 通訊傳送信號
				PWM1_1*[2]	O	C	PWM1 輸出
				EDIO*[1]	I/O	S/C	仿真及燒錄之通訊數據腳 EDIO
24	18	21	13	PT2.1	I/O	S/C/N	數位輸入 / 輸出引腳
				INT2.1	I	S	外部中斷源 INT2.1
				SCL_1*[2]	I/O	S/C	I²C 通訊時鐘信號
				RC_1*[2]	I	S	UART 通訊接收信號
				BZ_1*[2]	O	C	蜂鳴器輸出端
				TBI1	I	S	TimerB CPI 輸入選擇源
				ECK*[1]	I	S	仿真及燒錄之通訊時鐘腳 ECK
25	-	-	-	ECK0	I	S	仿真及燒錄之通訊時鐘腳 ECK0
26	19	22	14	VDD	P	P	晶片工作電壓源接正端引腳, 需外接 10uF 電容至 VSS.
27	20	23	15	VDDA	P	P	LDO 線性穩壓電源輸出引腳,啟動 輸出時需外接 1uF 電容至 VSS.
28	21	24	16	AI0	A	A	類比輸入通道
				OPO	A	A	OPAMP 輸出通道

[1] 仿真 ICE 與燒錄時用的引腳，該模式下 GPIO 複用功能無法使用。

[2] 經由晶片內部設置，可規劃複用引腳功能在該引腳輸出或輸入。*表示為複用選擇的腳位。

表 2-1 引腳編號與說明

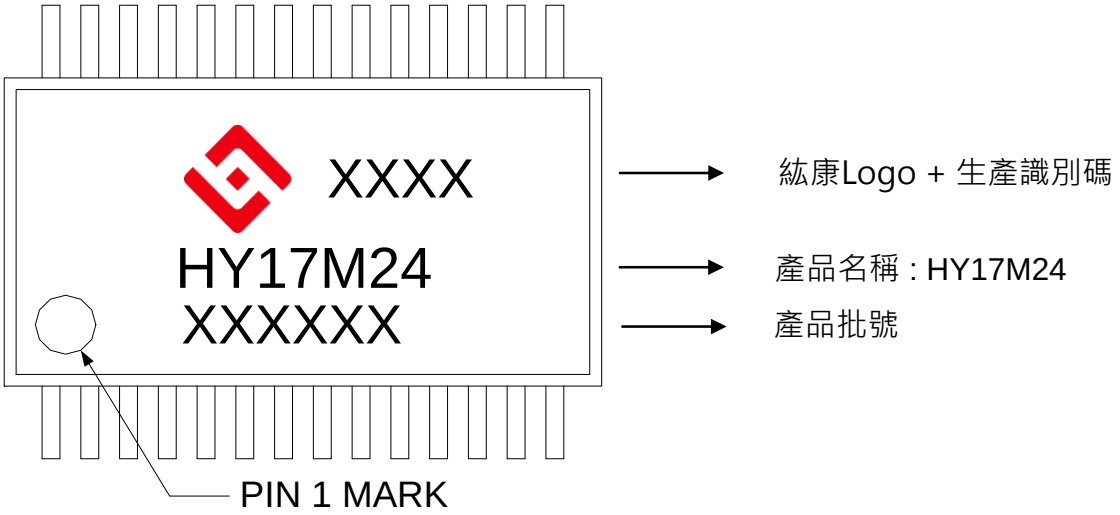
2.2. 復用引腳定義說明

Function	I/O Type	INT	Internal Pull high	Special Function	Buzzer	Timer B Enable	I²C	UART	Comparator	Analog	PWM
PT1.0	DAI	INT1.0	PU1.0	MCLR		TBI0			CH0	AI4	
PT1.1	DAI/O	INT1.1	PU1.1	XTI						AI5	
PT1.2	DAI/O	INT1.2	PU1.2	XTO						AI6	PWM1
PT1.3	DAI/O	INT1.3	PU1.3	PCAL			SCL			AI7	PWM0_1
PT1.4	DAI/O	INT1.4	PU1.4	DACO			SDA			AI8	
PT1.5	DAI/O	INT1.5	PU1.5		BZ			TX		AI9	
PT1.6	DAI/O	INT1.6	PU1.6					RC	CH1	AI10	PWM0
ECK0	DI/O			ECK0							
EDIO0	DI/O			EDIO0							
PT2.0	DI/O	INT2.0	PU2.0	EDIO			SDA_1	TX_1			PWM1_1
PT2.1	DI/O	INT2.1	PU2.1	ECK	BZ_1	TBI1	SCL_1	RC_1			
AI0	AIO			OPO						AI0	
AI1	AI									AI1	
AI2	AI									AI2	
AI3	AIO			REFO						AI3	
PT3.0	DAI/O	INT3.0	PU3.0			TBI0_1	SCL_2			AI11	
PT3.1	DAI/O	INT3.1	PU3.1				SDA_2			AI12	
PT3.2	DI/O	INT3.2	PU3.2				SCL_3				PWM0_2
PT3.3	DI/O	INT3.3	PU3.3				SDA_3				PWM1_2
PT3.4	DI/O	INT3.4	PU3.4		BZ_2			TX_3			
PT3.5	DI/O	INT3.5	PU3.5					RC_3			
PT3.6	DAI/O	INT3.6	PU3.6			TBI1_1		TX_2		AI13	
PT3.7	DAI/O	INT3.7	PU3.7					RC_2	CH2	AI14	

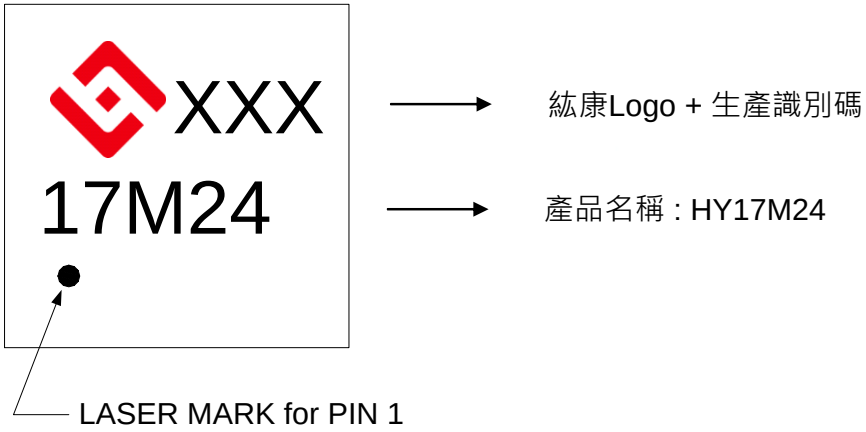
表 2-2 引腳編號與說明

2.3. 封裝片標記信息

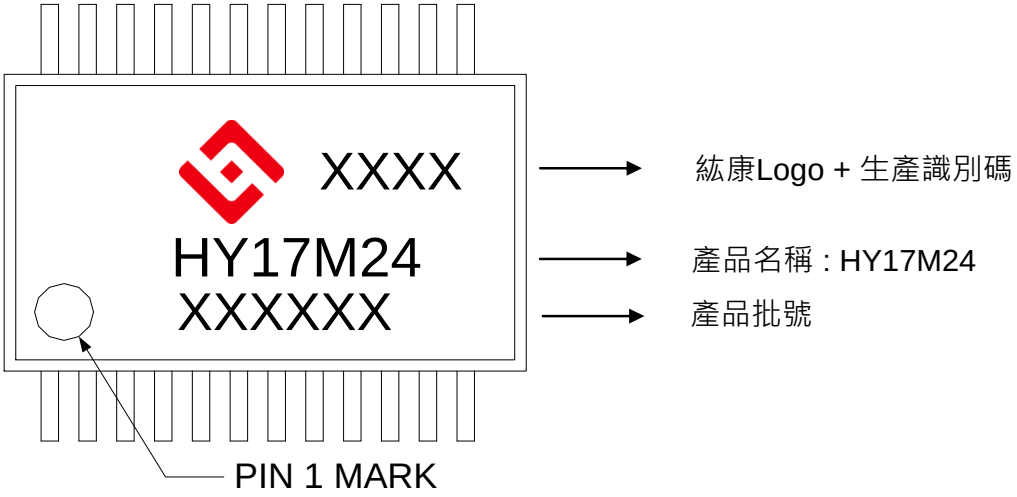
2.3.1. SSOP28 封裝片標記信息



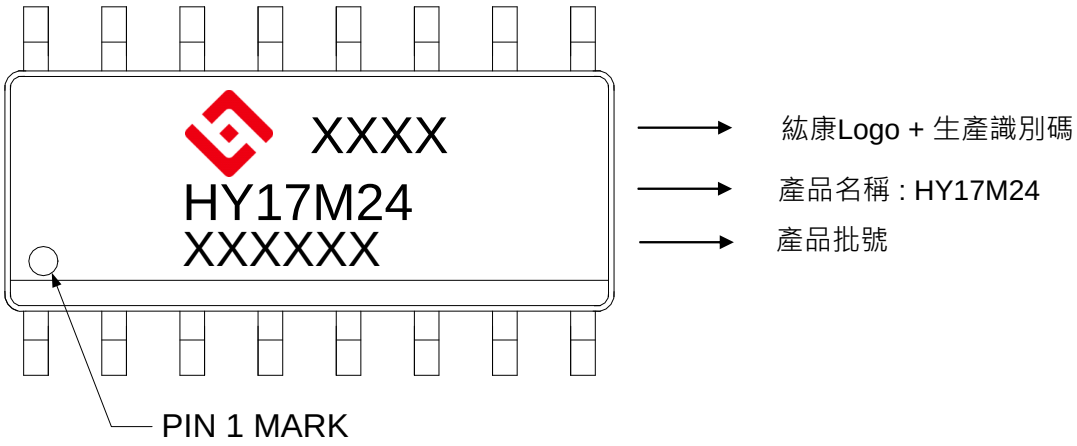
2.3.2. QFN24 封裝片標記信息



2.3.3. SSOP24 封裝片標記信息



2.3.4. SOP16 封裝片標記信息



3. 應用參考電路

3.1. 獨立型煙霧傳感器應用(光學傳感器)

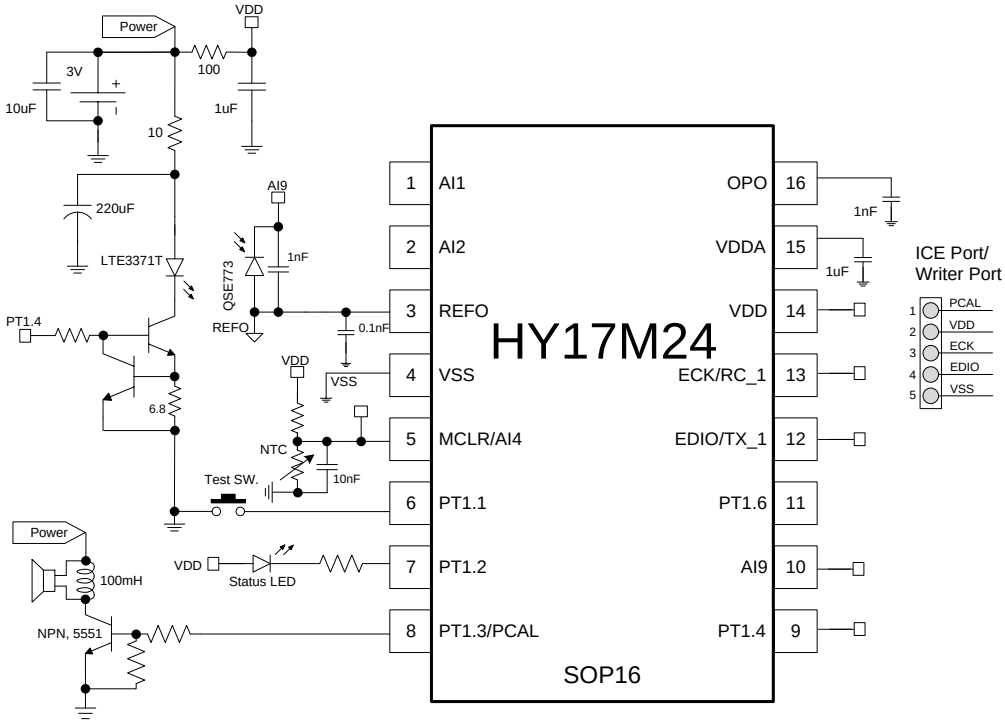


圖 3-1 煙霧傳感器應用參考電路

3.2. 聯網型煙霧傳感器應用(光學傳感器)

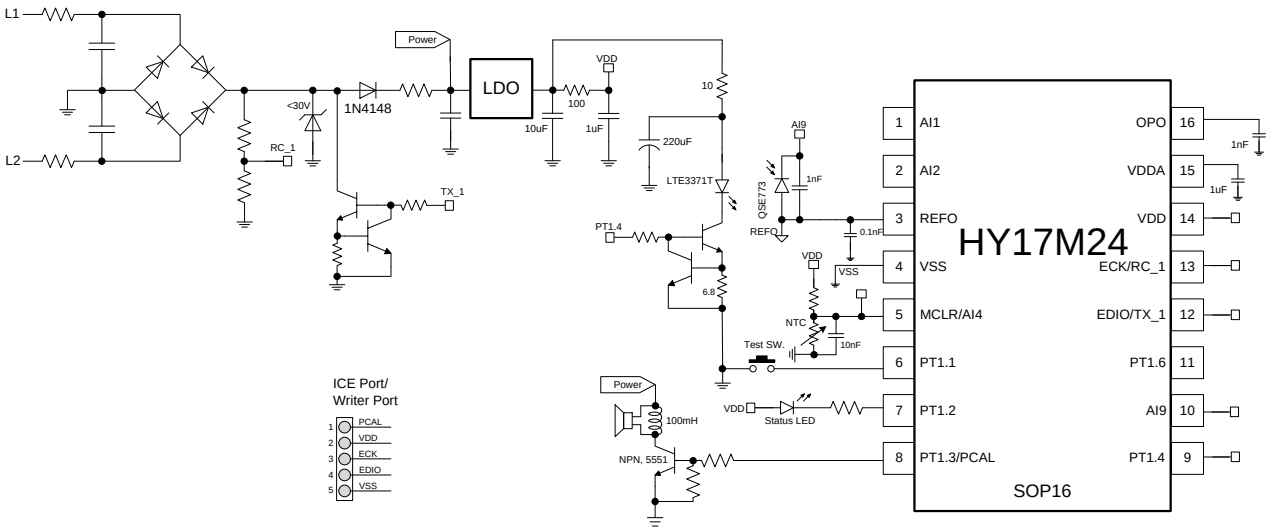


圖 3-2 煙霧傳感器應用參考電路

3.3. 電化學試紙應用

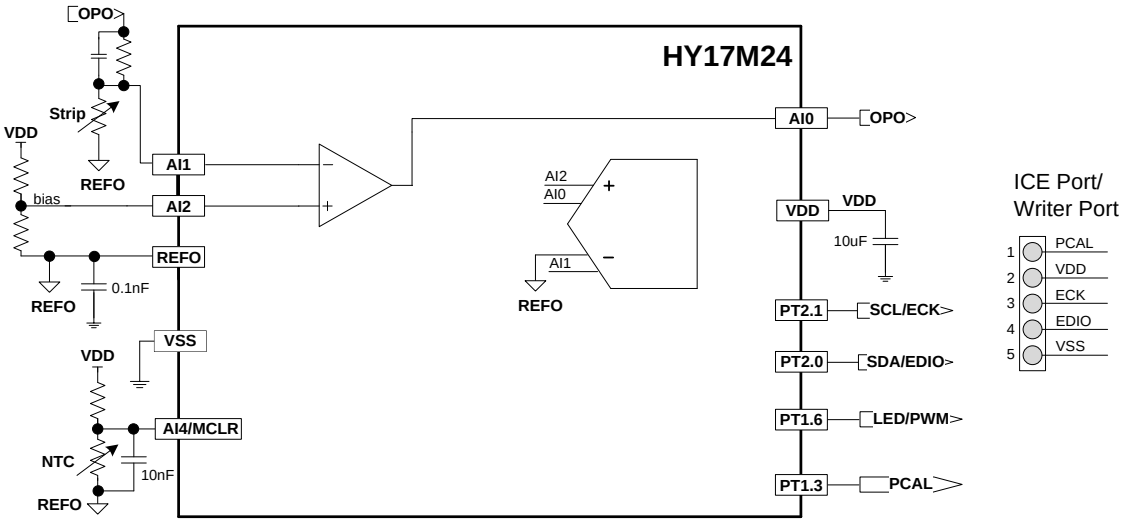


圖 3-3 電化學試紙應用參考電路

3.4. 電壓電流偵測及充放電控制應用

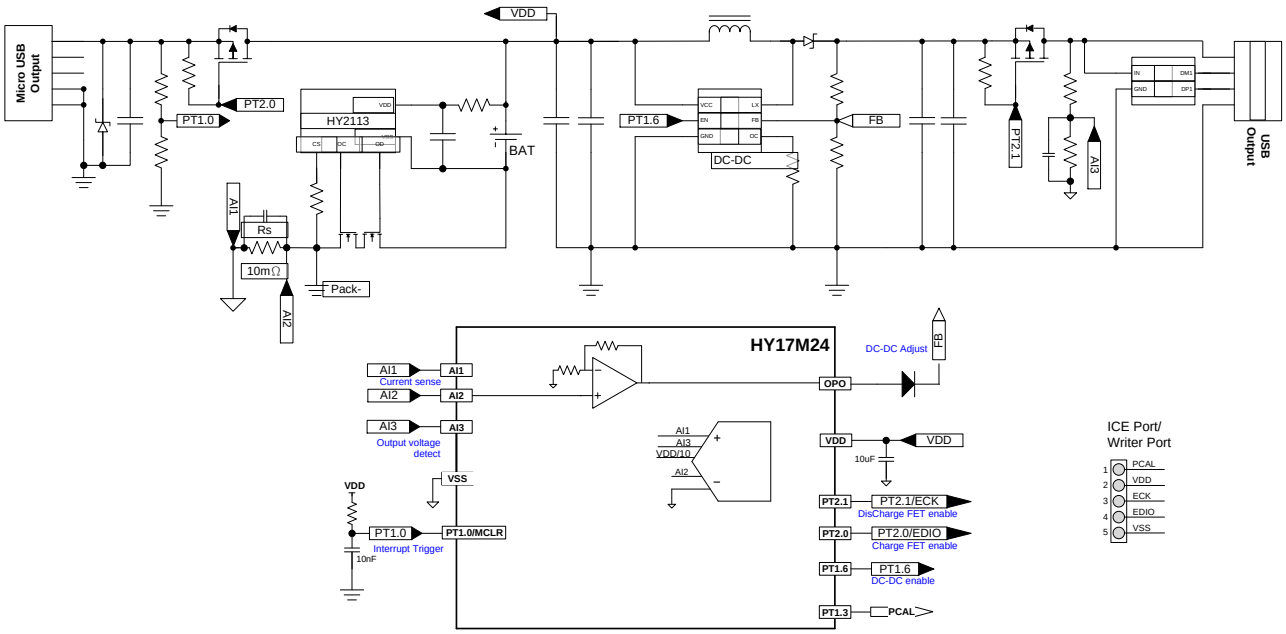


圖 3-4 電壓電流偵測及充放電控制應用參考電路

4. 功能概述

4.1. 內部方塊圖

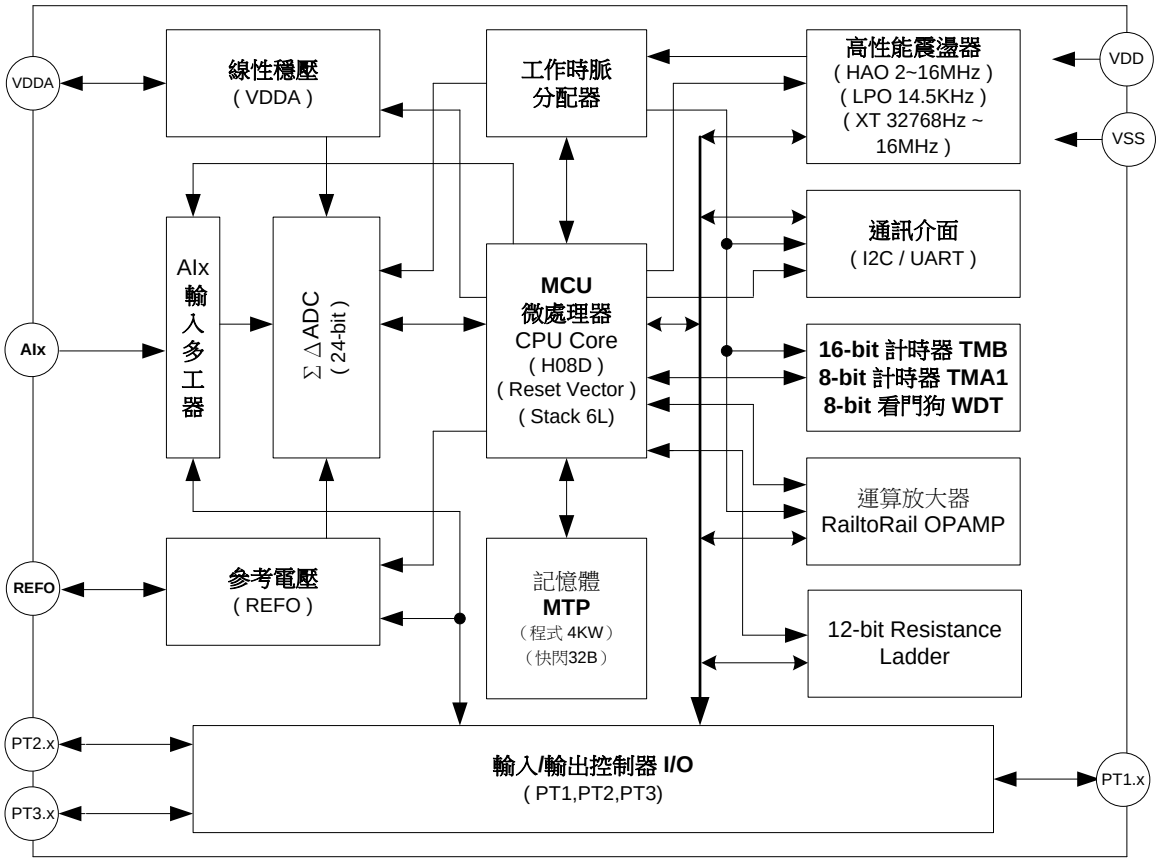


圖 4-1 內部方塊圖

4.2. 相關說明與支援文件

晶片功能相關使用說明書

DS-HY17M24	HY17M24 規格說明書
UG-HY17M24	HY17M24 使用說明書
APD-CORE002	H08A、H08C、H08D 組合語言指令集說明書

開發工具相關使用說明書

APD-HY17MIDE001	HY17M24 開發工具軟體使用說明書
APD-HY17MIDE002	HY17M24 開發工具硬體使用說明書
APD-HY17MIDE003	HY17M24 ENOB 工具使用說明書

產品生產相關使用說明書

APD-HY17MIDE0xx	HY17M24 生產線專用燒錄器說明書

4.3. Clock System

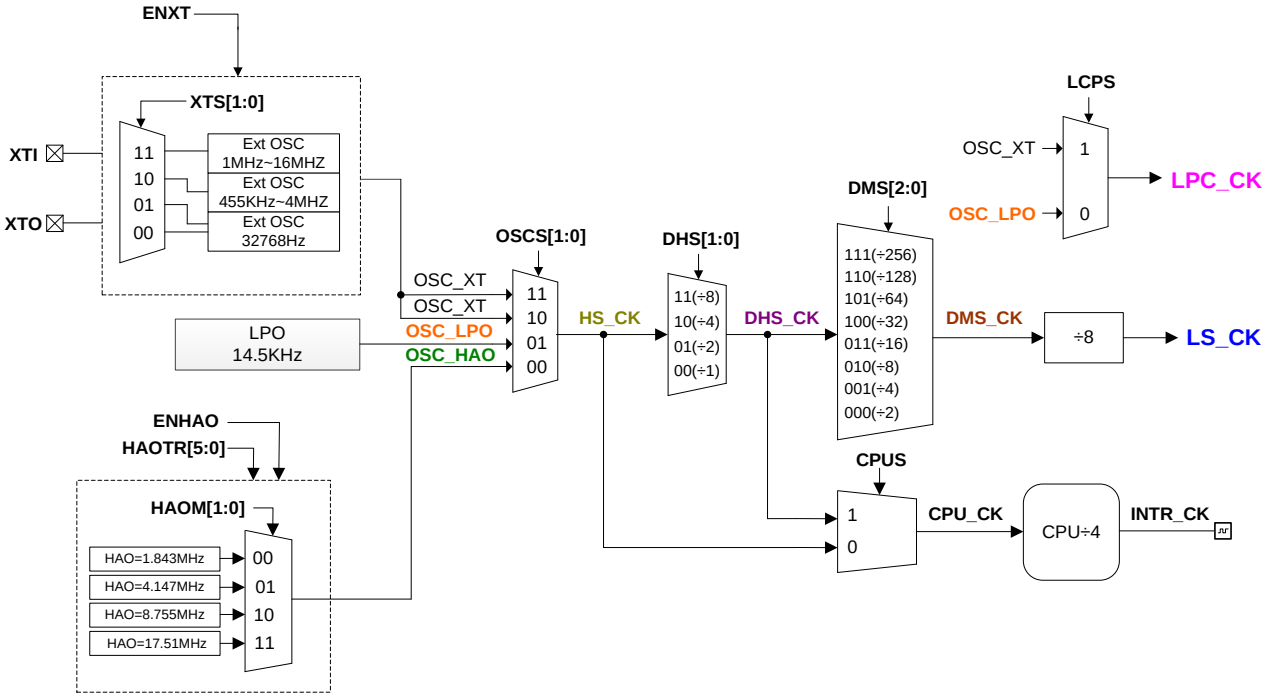


圖 4-2 Clock System(一)

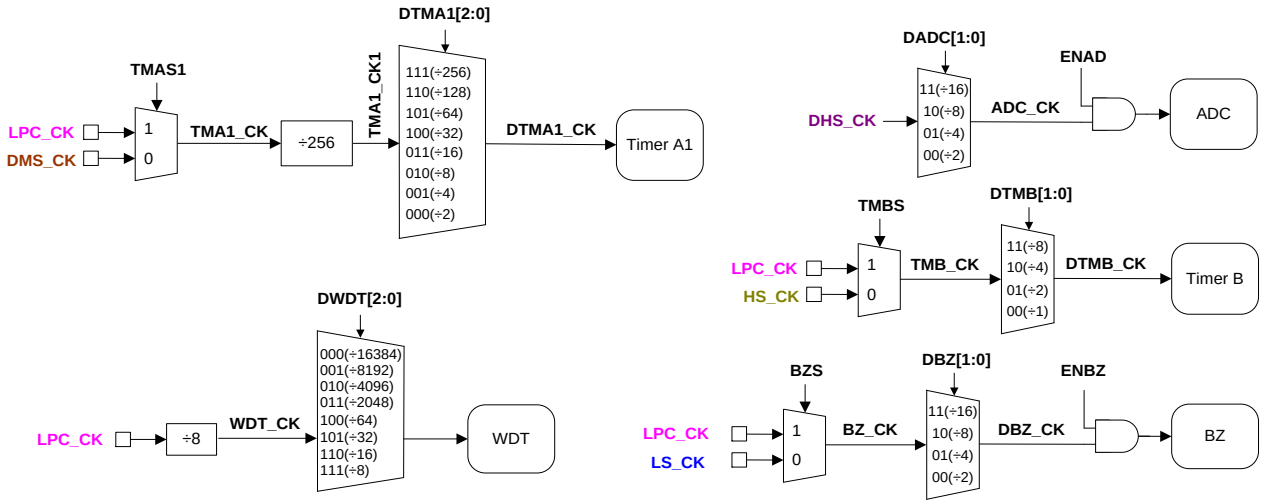


圖 4-3 Clock System(二)

4.4. GPIO PT1.0 System

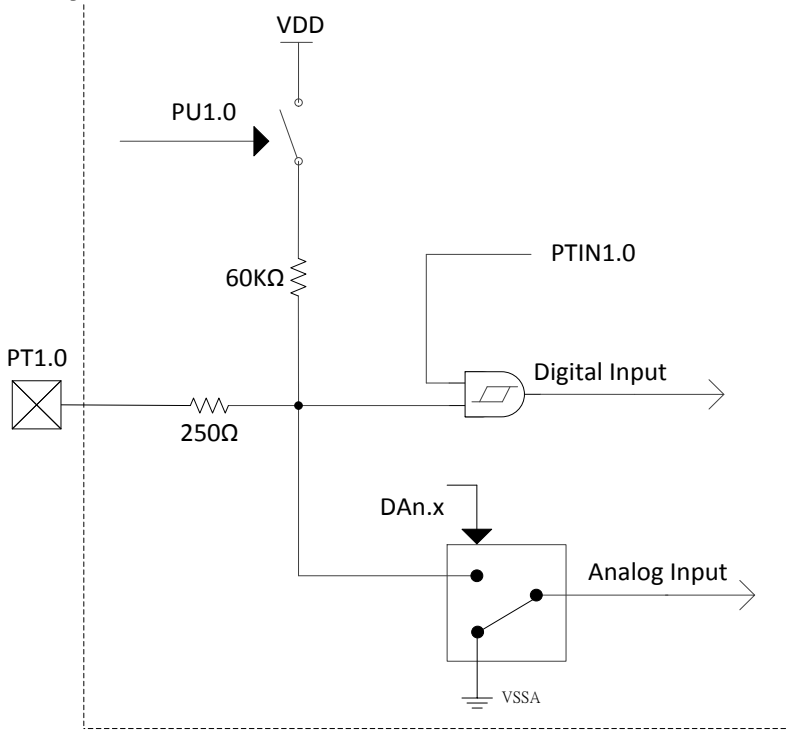


圖 4-4 GPIO PT1.0 System

4.5. GPIO PT1~PT3 System

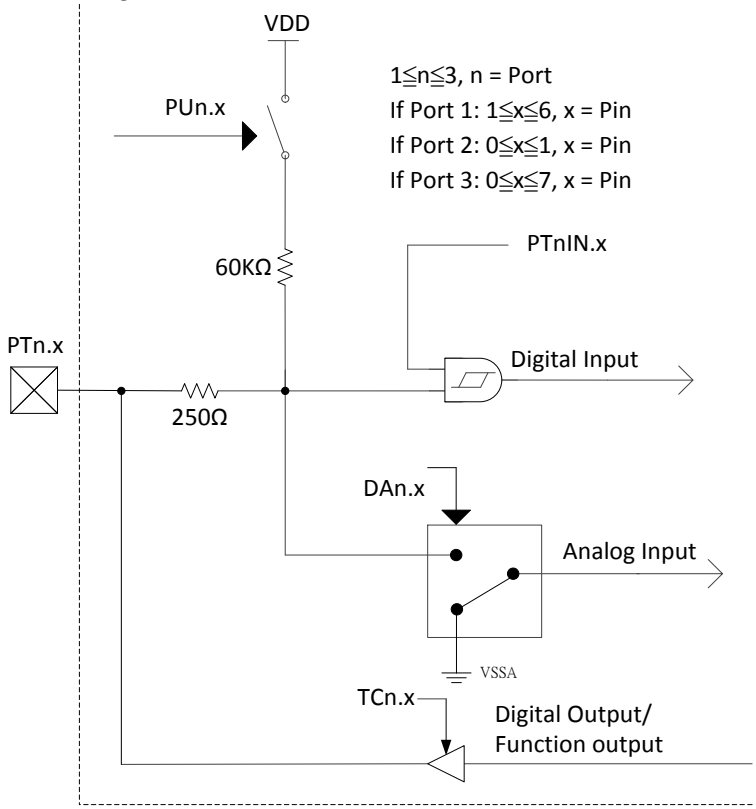


圖 4-5 GPIO PT1~PT3 System

4.6. Reset System

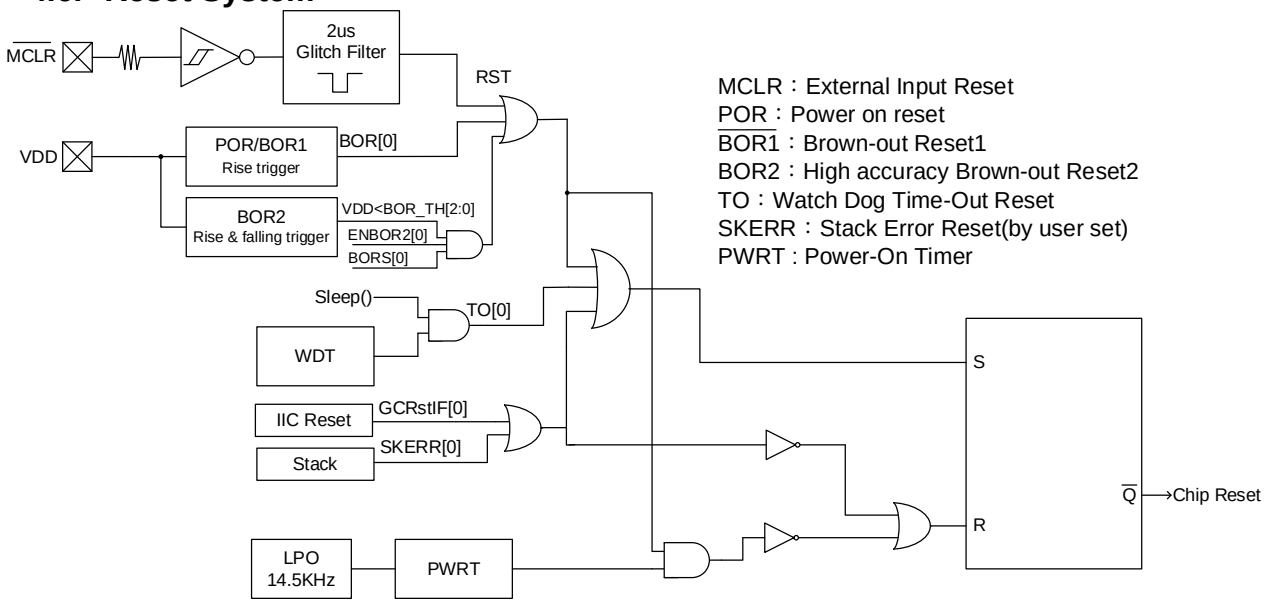


圖 4-6 Reset

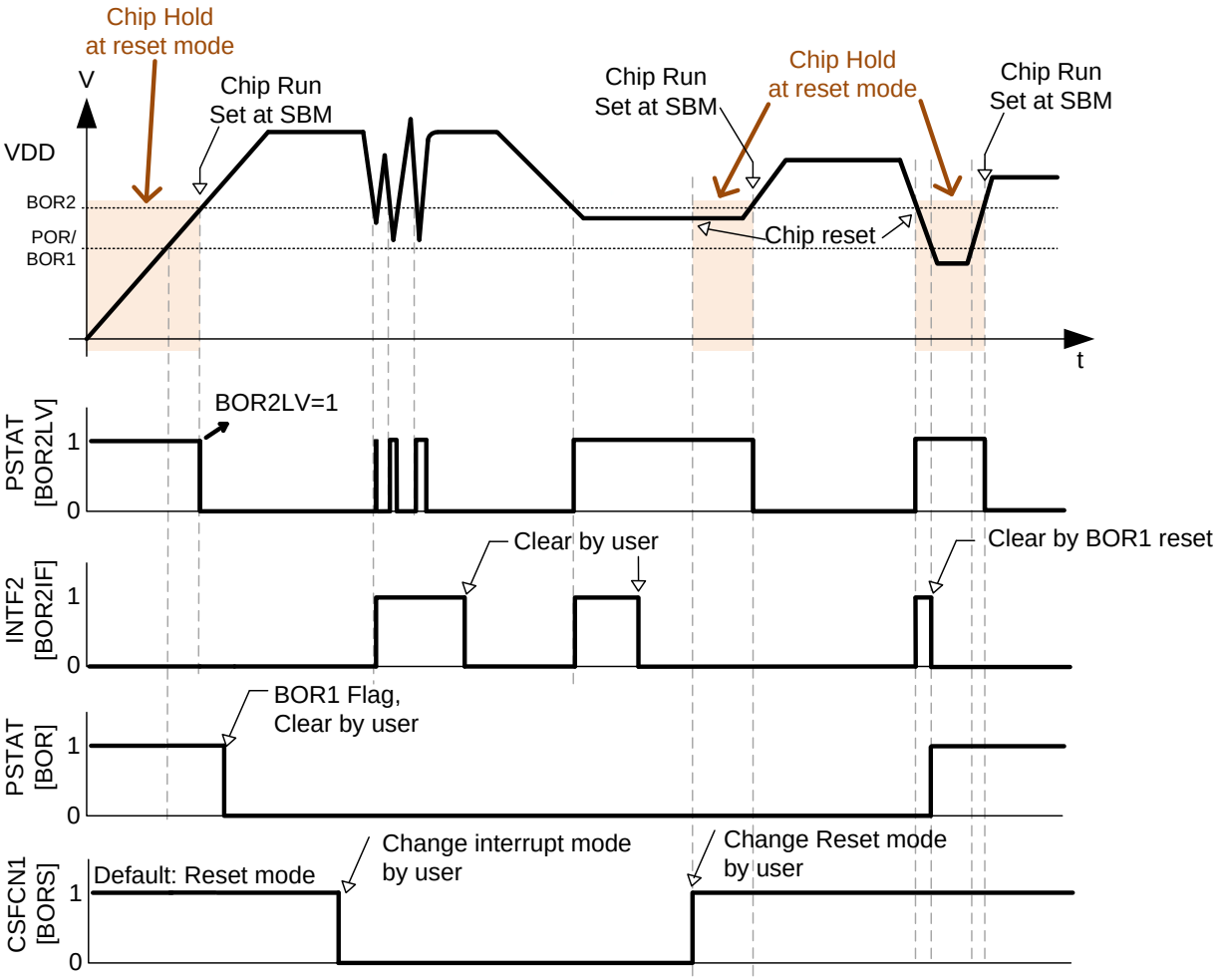


圖 4-7 BOR1 and BOR2 Chart

4.7. Power System

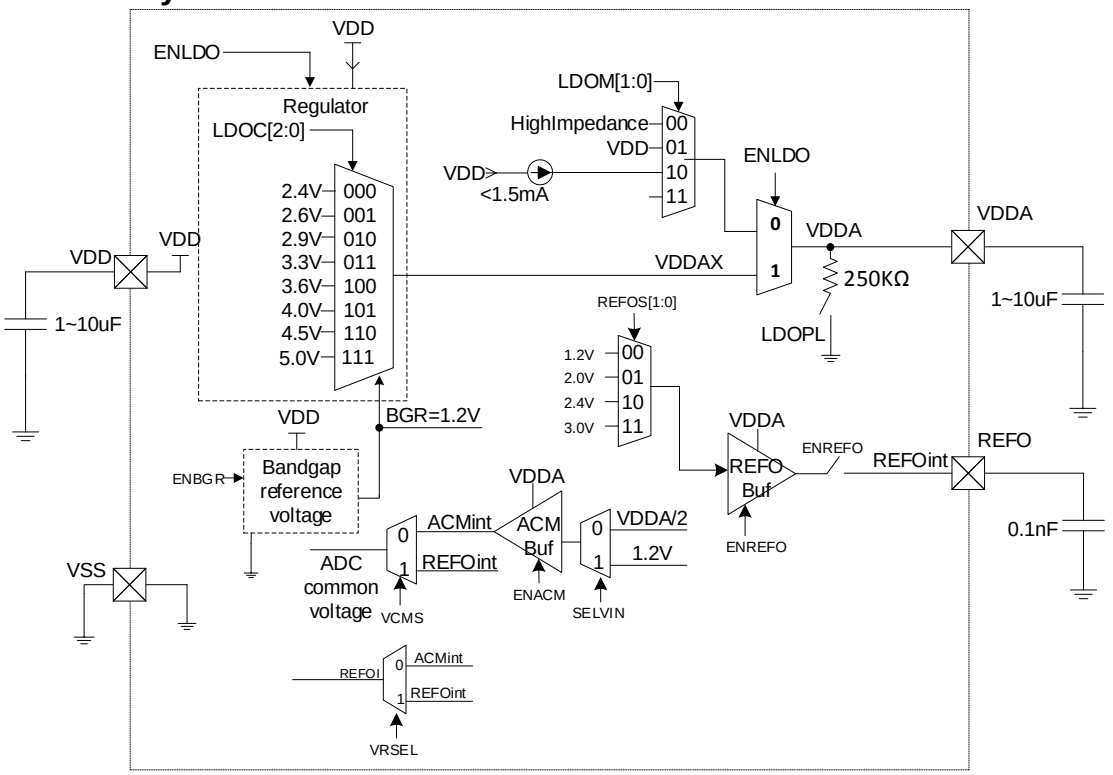
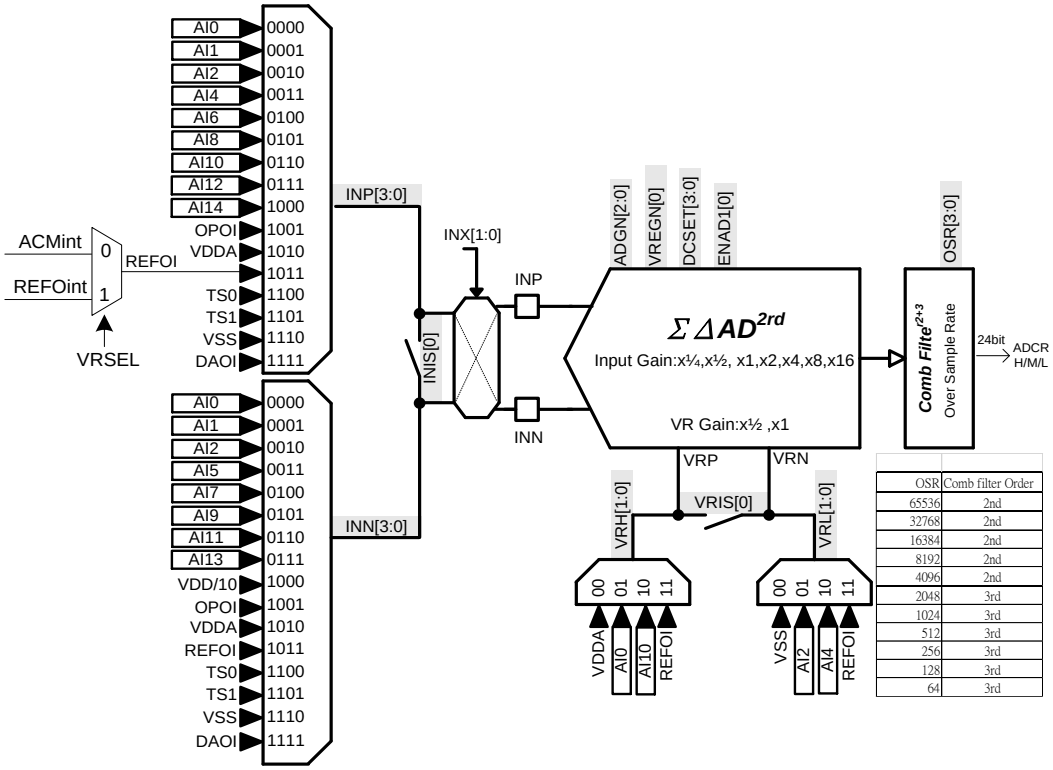


圖 4-8 Power System

4.8. ADC Network



OSR	Comb filter Order
65536	2nd
32768	2nd
16384	2nd
8192	2nd
4096	2nd
2048	3rd
1024	3rd
512	3rd
256	3rd
128	3rd
64	3rd

圖 4-9 ADC Network

4.9. 12-bit Resistance Ladder Network

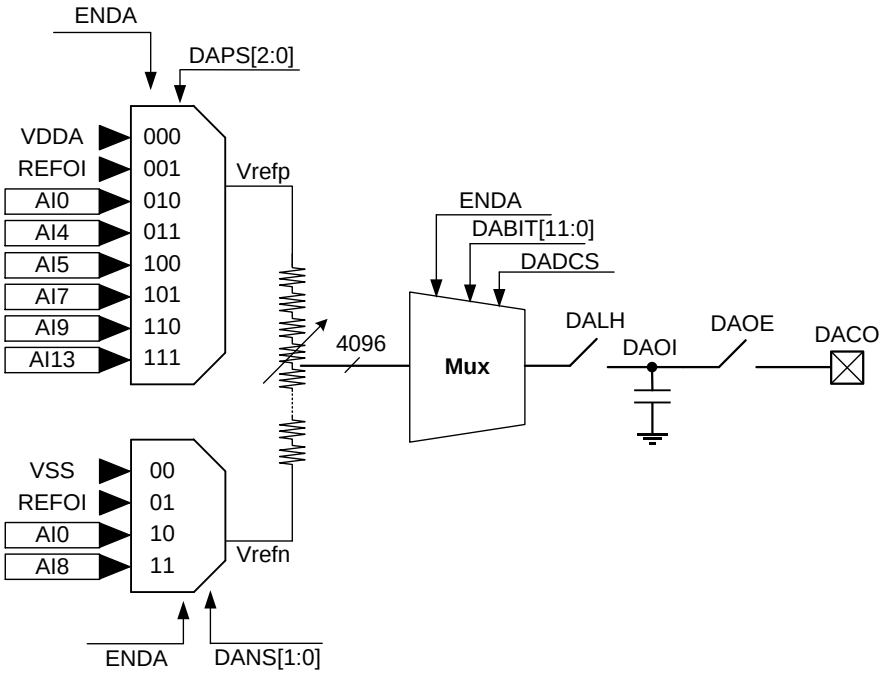


圖 4-10 12-bit Resistance Ladder Network

4.10. Rail to Rail OPAMP Network

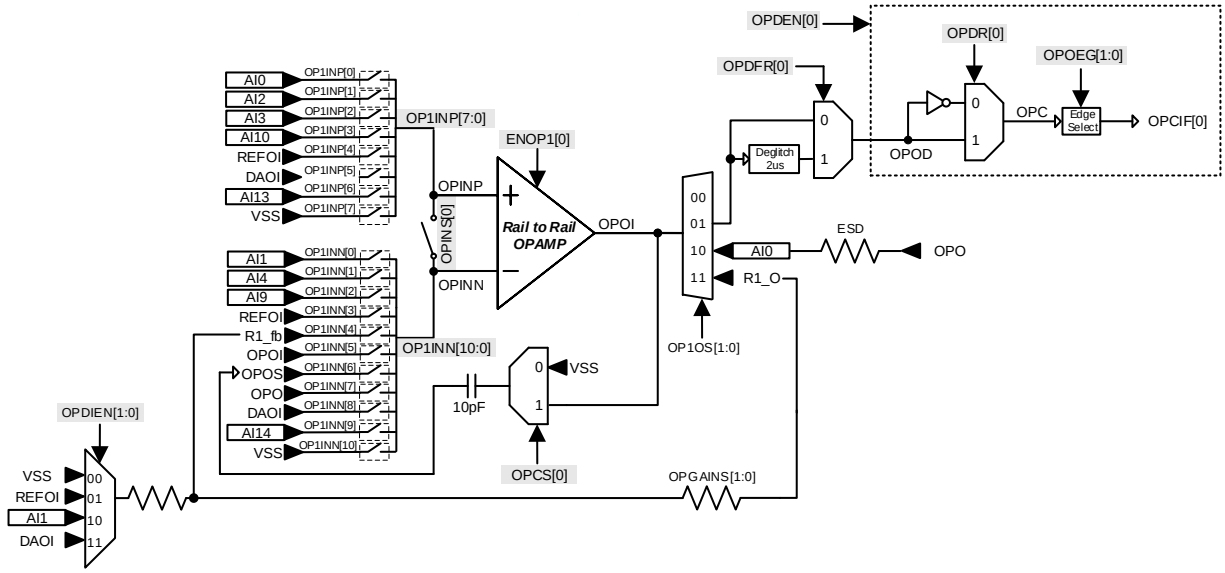


圖 4-11 Rail to Rail OPAMP Network

4.11. Comparator Network

Hysteresis		
CPDM	CMPO	Divider
00000	X	CPDA[4:0]
00001	1	CPDA[4:1],1
00001	0	CPDA[4:1],0
00010	1	CPDA[4:2],1,CPDA[0]
00010	0	CPDA[4:2],0,CPDA[0]
00011	1	CPDA[4:2],11
00011	0	CPDA[4:2],00

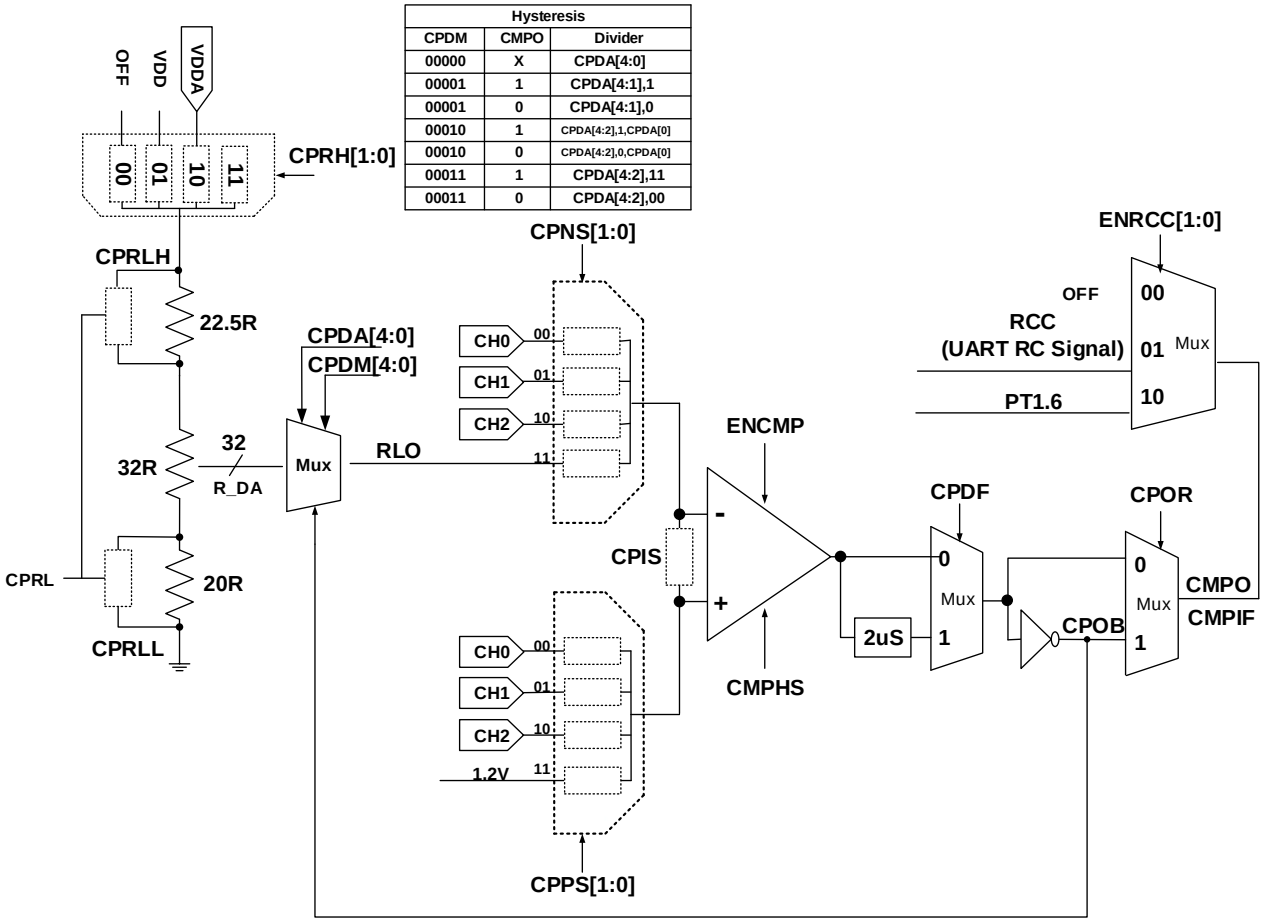


圖 4-12 Comparator Network

4.12. Watch Dog System

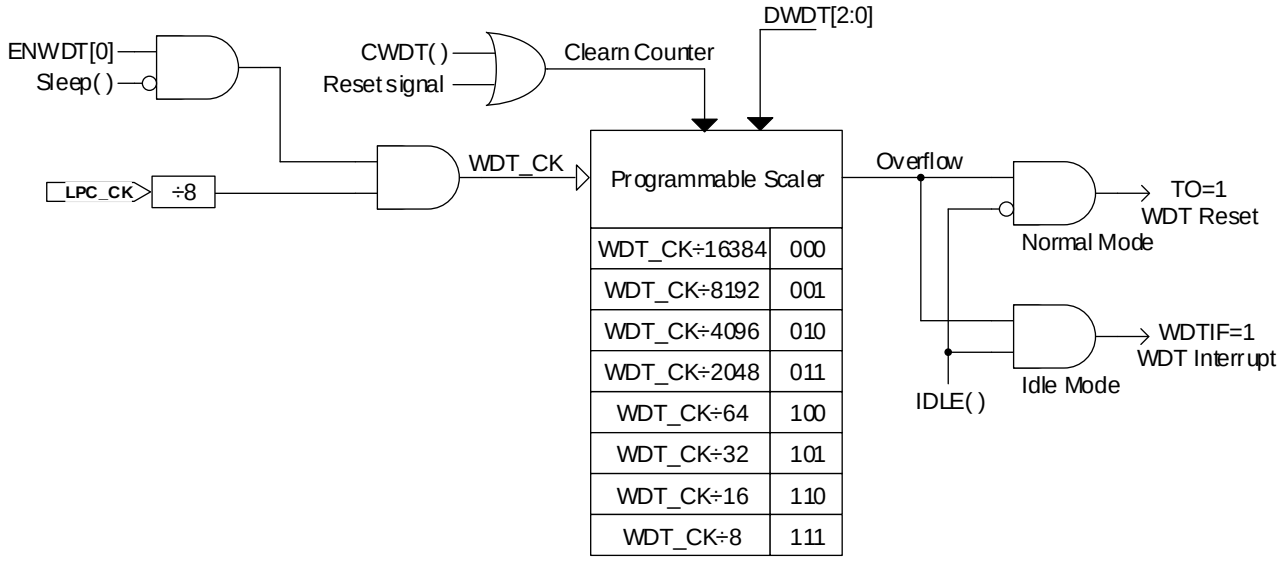


圖 4-13 Watch Dog System

4.13. 8-bit Timer A1 System

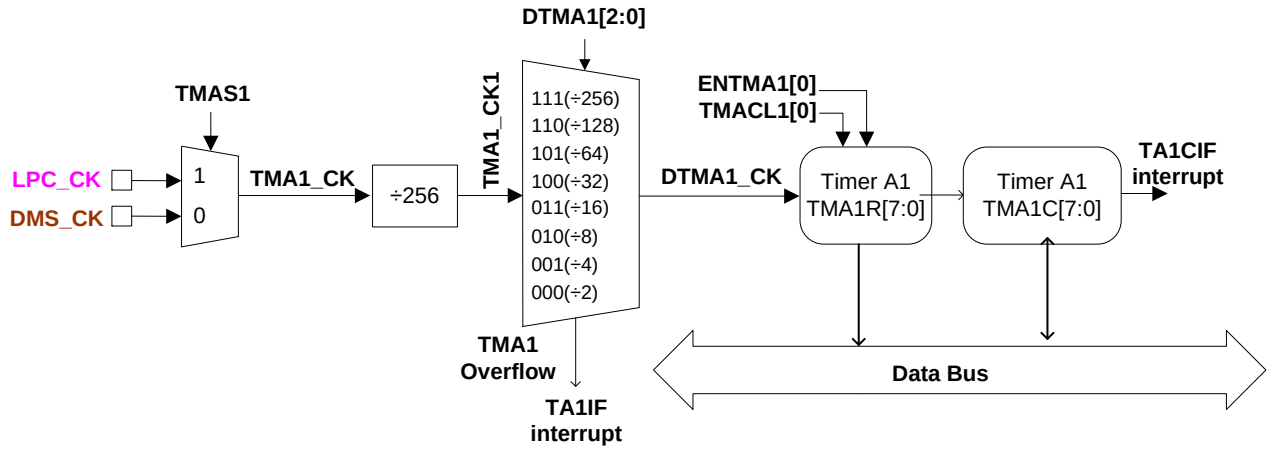


圖 4-14 Timer A1 System

4.14. 16-bit Timer B System

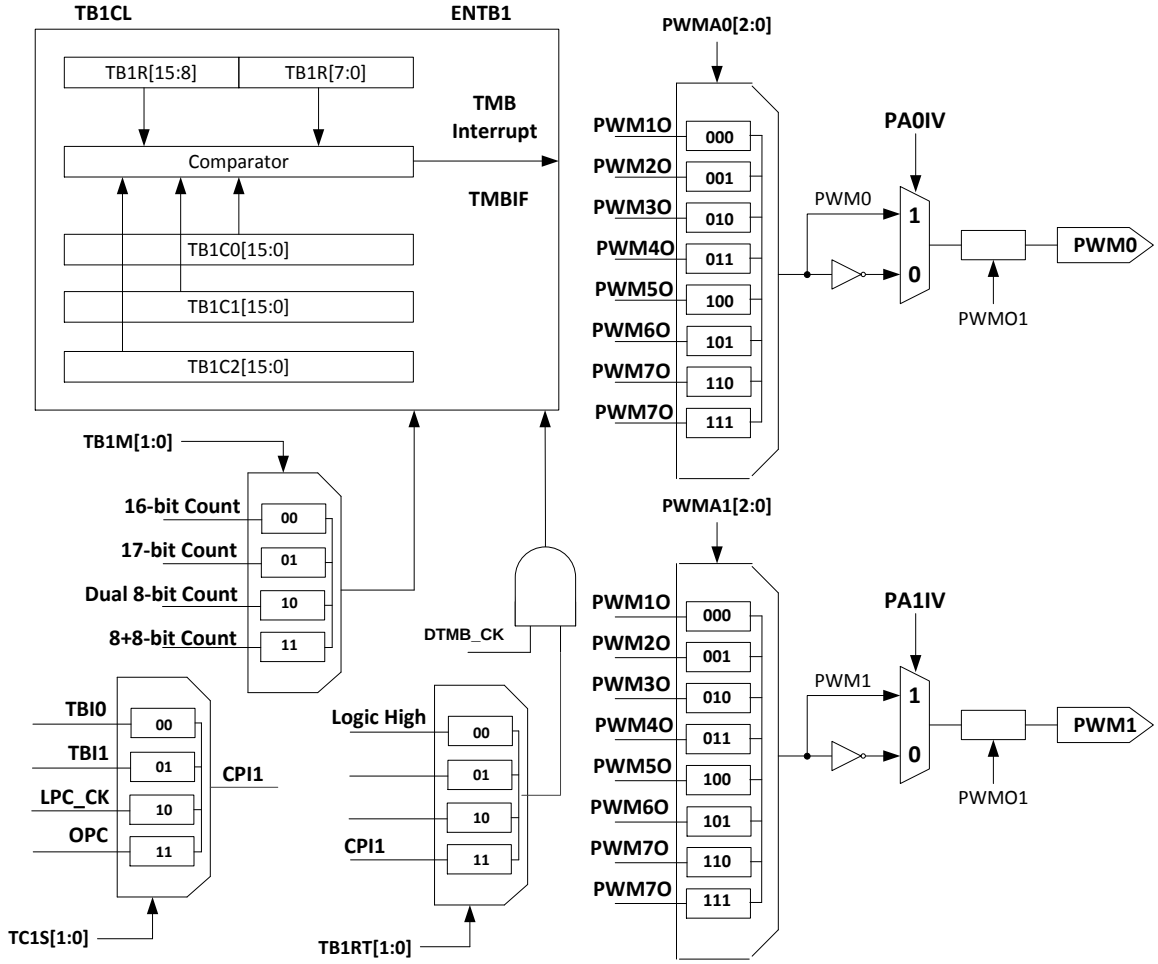


圖 4-15 Timer B System

4.15. I²C

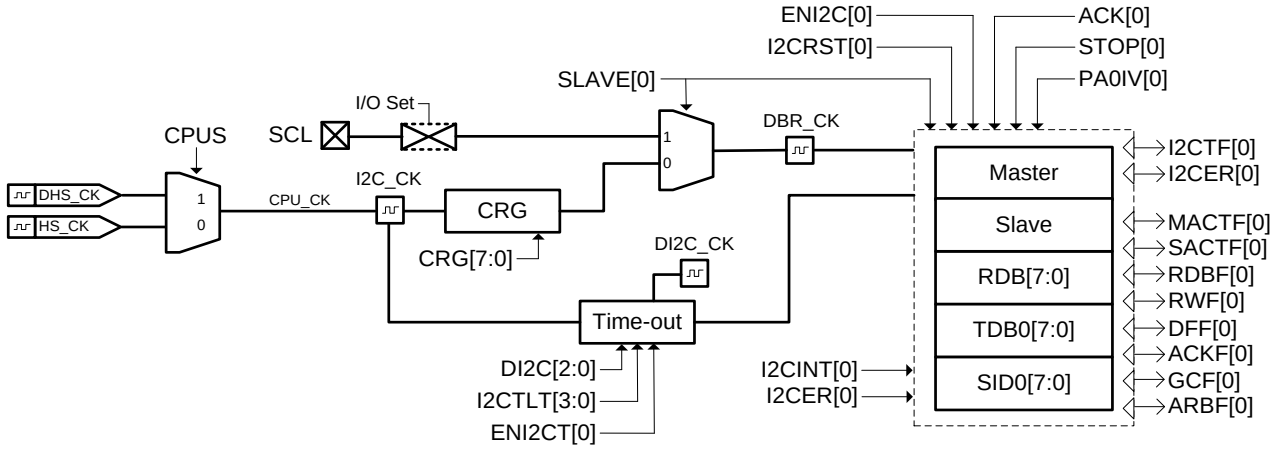


圖 4-16 I²C 方塊圖

4.16. EUART

EUART TRANSMIT BLOCK DIAGRAM

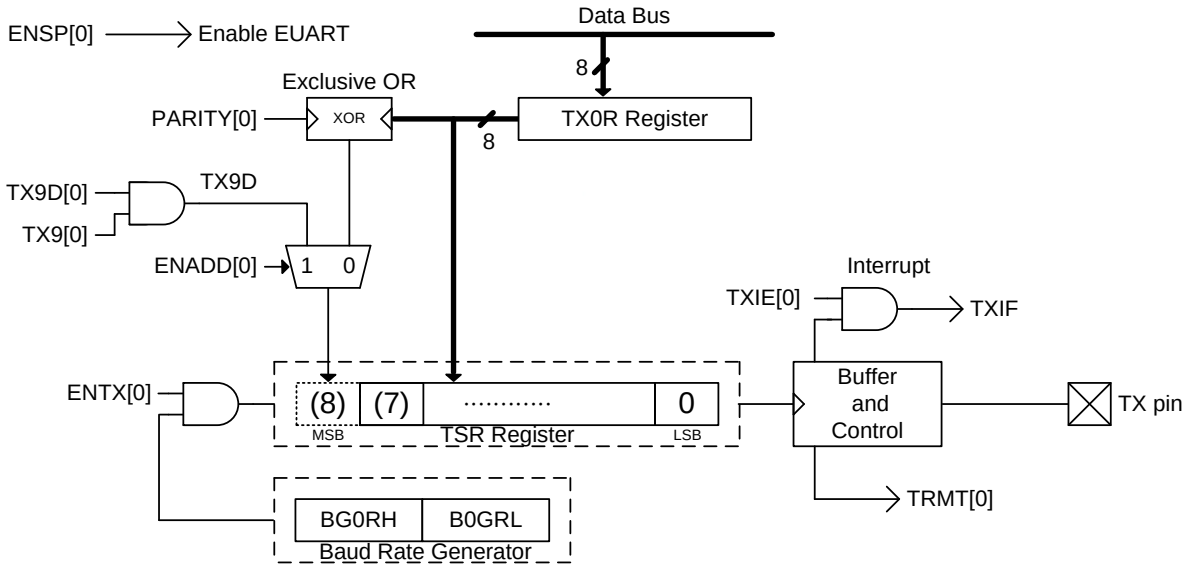
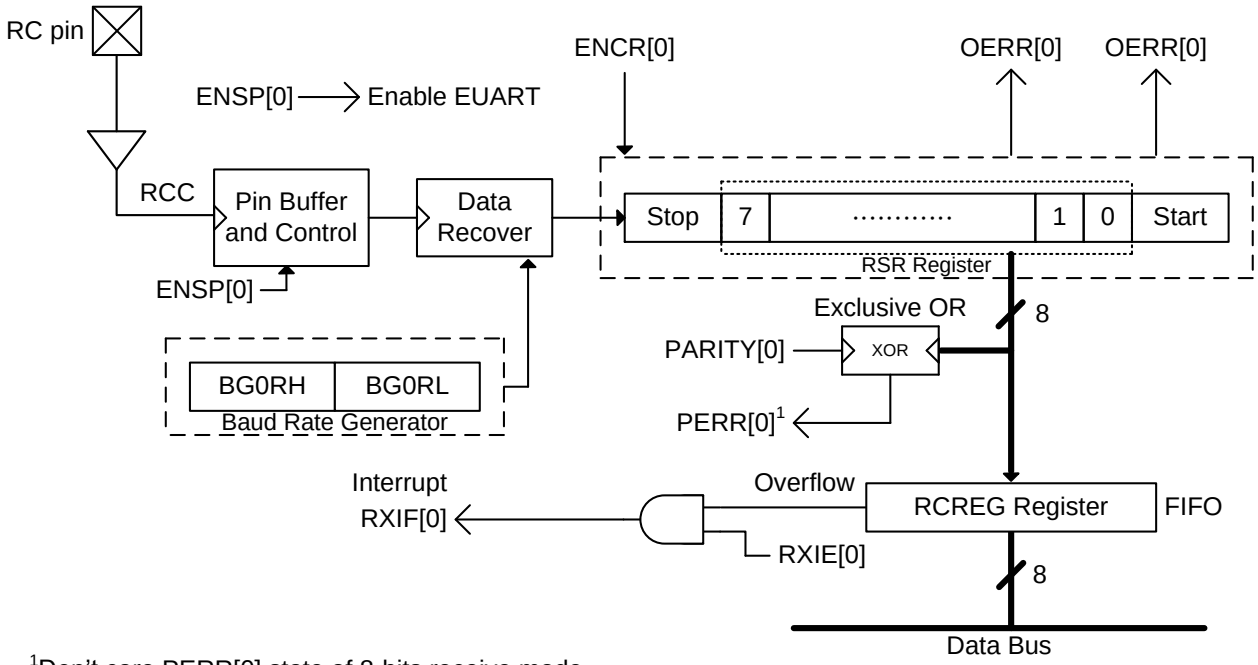


圖 4-17 EUART 傳送方塊圖

EUART 8-BITs RECEIVE BLOCK DIAGRAM



[1]Don't care PERR[0] state of 8-bits receive mode

圖 4-18 EUART 8-bits 接收方塊圖

5. 暫存器列表

"-"no use,"*"read/write,"w"write,"r"read,"r0"onlyread 0,"r1"onlyread 1,"w0"onlywrite 0,"w1"omlywrite 1

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
000h	INDF0	Contents of FSR0 to address data memoryvalue of FSR0 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
001h	POINC0	Contents of FSR0 to address data memoryvalue of FSR0 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
002h	PODEC0	Contents of FSR0 to address data memoryvalue of FSR0 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
003h	PRINC0	Contents of FSR0 to address data memoryvalue of FSR0 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
004h	PLUSW0	Contents of FSR0 to address data memoryvalue of FSR0 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
005h	INDF1	Contents of FSR1 to address data memoryvalue of FSR1 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
006h	POINC1	Contents of FSR1 to address data memoryvalue of FSR1 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
007h	PODEC1	Contents of FSR1 to address data memoryvalue of FSR1 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
008h	PRINC1	Contents of FSR1 to address data memoryvalue of FSR1 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
009h	PLUSW1	Contents of FSR1 to address data memoryvalue of FSR1 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Ah	INDF2	Contents of FSR2 to address data memoryvalue of FSR2 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Bh	POINC2	Contents of FSR2 to address data memoryvalue of FSR2 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Ch	PODEC2	Contents of FSR2 to address data memoryvalue of FSR2 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Dh	PRINC2	Contents of FSR2 to address data memoryvalue of FSR2 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Eh	PLUSW2	Contents of FSR2 to address data memoryvalue of FSR2 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
00Fh	FSR0H	-	-	-	-	-	-	-	FSR0[8]	…. ...x	…. ...u	-,-,-,- -,-,-,*
010h	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
011h	FSR1H	-	-	-	-	-	-	-	FSR1[8]	…. ...x	…. ...u	-,-,-,- -,-,-,*
012h	FSR1L	Indirect Data Memory Address Pointer 0 Low Byte,FSR1[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
013h	FSR2H	-	-	-	-	-	-	-	FSR2[8]	…. ...x	…. ...u	-,-,-,- -,-,-,*
014h	FSR2L	Indirect Data Memory Address Pointer 0 Low Byte,FSR2[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
016h	TOSH	-	-	-	-	TOS[11:8]				…. xxxx	…. uuuu	-,-,-,- *,*,*,*
017h	TOSL	Top-of-Stack Low Byte (TOS<7:0>)								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
018h	SKCN	SKFL	SKUN	SKOV	-	-	SKPRT[2:0]			000. .000	u$$. .$$$	rw 0,rw 0,rw 0,- -,*,*,*
01Ah	PCLATH	-	-	-	-	PC[11:8]				…. 0000	…. 0000	-,-,-,- *,*,*,*
01Bh	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	*,*,*,*,*,*,*,*
01Ch	TBLPTRU	-	-	-	-	-	-	-	-	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
01Dh	TBLPTRH	-	-	-	-	TBLPTR[11:8]				…. xxxx	…. uuuu	-,-,-,- *,*,*,*
01Eh	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
01Fh	TBLDH	Program Memory Table Latch High Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
020h	TBLDL	Program Memory Table Latch Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
021h	PRODH	Product Register of Multiply High Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
022h	PRODL	Product Register of Multiply Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
023h	INTE0	GIE	TA1CIE	ADIE	WDTIE	TB1IE		E1IE	E0IE	0000 0.00	0uuu uuuu	*,*,*,*,*,*,*,*
024h	INTE1	TA1IE		TXIE	RCIE	I2CERIE	I2CIE	E3IE	E2IE	0.00 0000	uuuu uuuu	*,*,*,*,*,*,*,*
025h	INTE2						CMPIE	OPCIE	BOR2IE	…. ...0	uuuu uuuu	*,*,*,*,*,*,*,*
026h	INTF0	-	TA1CIF	ADIF	WDTIF	TB1IF	TMAIF	E1IF	E0IF	.000 0000	.uuu uuuu	*,*,*,*,*,*,*,*
027h	INTF1	TA1IF		TXIF	RCIF	I2CERIF	I2CIF	E3IF	E2IF	0.00 0000	uuuu uuuu	*,*,*,*,*,*,*,*
028h	INTF2						CMPIF	OPCIF	BOR2IF	…. ...0	uuuu uuuu	*,*,*,*,*,*,*,*
029h	WREG	Working Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
02Ah	BSRCN	-	-	-	-	-	-	-	BSR[0]	…. ...x	…. ...u	-,-,-,- -,-,-,*
02Bh	MSTAT	-	-	-	C	DC	N	OV	Z	…x xxxx	...u uuuu	-,-,-,*,*,*,*,*
02Ch	PSTAT	BOR	PD	TO	IDL	RST	SKERR	BOR2LV	GCRstIF	$000 $000	uu$u u$uu	rw0,rw0,rw0,rw0 rw0,rw0,r,rw0
02Eh	PWRCN	ENBGR	LDOC[2:0]			LDOM[1:0]		ENLDO	CSFON	1000 0000	uuuu uu0u	*,*,*,*,*,*,*,*
02Fh	OSCCN0	OSCS[1:0]		DHS[1:0]		DMS[2:0]			CUPS	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
030h	OSCCN1	CCOPT	LCPS	DADC[1:0]		DTMB[1:0]		TMBS	-	0000 000.	uuuu uuu.	*,*,*,*,*,*,*,-
031h	OSCCN2	-	-	ENXT	XTS[1:0]		HAOM[1:0]		ENHAO	0000 0001	uuuu uuu1	*,*,*,*,*,*,*,*
032h	CSFCN0	SKRST	HAOTR[6:0]							.1.. ….	…. ….	-,-,-,- -,-,-,-
033h	CSFCN1	MCLR	-	ENINXCH	BOR_TH[2:0]			BORS	ENBOR2	0.00 0011	0.uu uuuu	*,-,*,*,*,*,*,*
034h	WDTCN	ENBZ	BZS	DBZ[1:0]		ENWDT	DWDT[2:0]			0000 0000	uuuu $000	-,*,*,* rw 1,*,*,*
035h	AD1H	ADC1 conversion high byte data register								0000 0000	uuuu uuuu	r,r,r,r r,r,r,r
036h	AD1M	ADC1 conversion middle byte data register								0000 0000	uuuu uuuu	r,r,r,r r,r,r,r
037h	AD1L	ADC1 conversion low byte data register								0000 0000	uuuu uuuu	r,r,r,r r,r,r,r

表 5-1 資料記憶體列表

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
038h	AD1CN0	ENAD1	-		OSR[3:0]				CMFR	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
039h	AD1CN1	-	-	VREGN	REFOS[1:0]		ADGN[2:0]			xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
03Ah	AD1CN2	-	-	-	SELVIN	DCSET[3:0]				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
03Bh	AD1CN3	INP[3:0]				INN[3:0]				xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
03Ch	AD1CN4	VRH[1:0]		VRL[1:0]		INX[1:0]		VRIS	INIS	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
03Dh	AD1CN5	ENACM	-	VCMS	LDOPL	ENREFO	-	ENTPS	TPSCH	0.00 0000	u.uu uuuu	*,*,*,*,*,*,*,*
03Eh	LVDCN	DAFM	ENCH	-	-	-	-	-	-	00..	uu..	*,*,*,*,*,*,*,*
03Fh	DACCN0	-	-	DANS[1:0]		-	DAPS[2:0]			..00 .000	..uu .uuu	*,*,*,*,*,*,*,*
040h	DACCN1	-	-	-	DADCS	DALH	-	DAOE[0]	ENDA	...0 0.00	...u u.uu	*,*,*,*,*,*,*,*
041h	DACBitH	-	-	-	-	DABIT[11:8]				 0000	.... uuuu	*,*,*,*,*,*,*,*
042h	DACBitL	DABIT[7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
043h	OP1CN0	OPINS	OPDR	OPCS	OPDFR	OPDEN	OP1OS[1:0]		ENOP1	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
044h	OP1CN1	-	OPC	OPGAINS[1:0]		OPDIEN[1:0]		OPOEG[1:0]		00 0000	uu uuuu	-,-,*,*,*,*,*,*
045h	OP1INP	VSS	AI13	DAOI	REFOI	AI10	AI3	AI2	AI0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
046h	OP1INN1	-	-	-	-	-	VSS	AI14	DAOI	.... .000	.... .uuu	-,-,-,- -,*,*,*
047h	OP1INN0	OPO	OPOS	OPOI	R1_fb	REFOI	AI9	AI4	AI1	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
048h	TMA1CN	ENTMA1	TMACL1	TMAS1	DTMA1[2:0]			-		0000 0000	u0uu uuuu	*,rw 1,*,*,*,*,*
049h	TMA1R	TMA1 counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
04Ah	TMA1C	TMA1C counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
04Bh	TB1Flag	-	PWM7A	PWM6A	PWM5A	PWM4A	PWM3A	PWM2A	PWM1A	..00 0000	..uu uuuu	-,-,r,r r,r,r,r
04Ch	TB1CN0	ENTB1	TB1M[1:0]		TB1RT[1:0]		TB1CL	PWMO1	PWMO0	0000 0000	uuuu u0uu	*,*,*,*,*,rw 1,*,*
04Dh	TB1CN1	PA1IV	PWMA1[2:0]			PA0IV	PWMA0[2:0]			0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
04Eh	TB1RH	TimerB1 counter Register [15:8]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
04Fh	TB1RL	TimerB1 counter Register [7:0]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
050h	TB1C0H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
051h	TB1C0L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
052h	TB1C1H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
053h	TB1C1L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
054h	TB1C2H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
055h	TB1C2L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
056h	TC1CN0	-	TC1S[1:0]		-	-	-	-	-	0000 0000	uuuu uuuu	uuuu uuuu
057h	PT1	-	PT1.6	PT1.5	PT1.4	PT1.3	PT1.2	PT1.1	PT1.0	.xxx xxxx	.xxx xxxx	-,*,*,*,*,*,*,*
058h	PT1IN	-	IN1.6	IN1.5	IN1.4	IN1.3	IN1.2	IN1.1	IN1.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
059h	TRISC1	-	TC1.6	TC1.5	TC1.4	TC1.3	TC1.2	TC1.1	TC1.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
05Ah	PT1DA	-	DA1.6	DA1.5	DA1.4	DA1.3	DA1.2	DA1.1	DA1.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
05Bh	PT1PU	-	PU1.6	PU1.5	PU1.4	PU1.3	PU1.2	PU1.1	PU1.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
05Ch	PT1M1	-	-	-	-	INTEG1[1:0]		INTEG0[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
05Dh	PT1M2	PM1.3[1:0]		-	PM1.2[0]	-	-	-	PM1.0[0]	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
05Eh	PT1M3	-	-	-	PM1.6[0]	PM1.5[1:0]		-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
05Fh	PT1INT	-	INTG1.6	INTG1.5	INTG1.4	INTG1.3	INTG1.2	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
060h	PT1INTE	-	INTE1.6	INTE1.5	INTE1.4	-	-	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
061h	PT1INTF	-	INTF1.6	INTF1.5	INTF1.4	-	-	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
062h	PT2	-	-	-	-	-	-	PT2.1	PT2.0	xx	.... ..uu	-,-,-,- -,-,*,*
063h	PT2IN	-	-	-	-	-	-	IN2.1	IN2.0	00	.... ..uu	-,-,-,- -,-,*,*
064h	TRISC2	-	-	-	-	-	-	TC2.1	TC2.0	00	.... ..uu	-,-,-,- -,-,*,*
065h	PT2PU	-	-	-	-	-	-	PU2.1	PU2.0	00	.... ..uu	-,-,-,- -,-,*,*
066h	PT2M1	-	-	-	-	PM2.1[1:0]		PM2.0[1:0]		 0000	.... uuuu	-,-,-,- *,*,*,*
067h	PT2INT	-	-	-	-	-	-	INTG2.1	INTG2.0	00	.... ..uu	-,-,-,- -,-,*,*
068h	PT2INTE	-	-	-	-	-	-	INTE2.1	INTE2.0	00	.... ..uu	-,-,-,- -,-,*,*
069h	PT2INTF	-	-	-	-	-	-	INTF2.1	INTF2.0	00	.... ..uu	-,-,-,- -,-,*,*
06Ah	PT3	PT3.7	PT3.6	PT3.5	PT3.4	PT3.3	PT3.2	PT3.1	PT3.0	xxxx xxxx	xxxx xxxx	*,*,*,*,*,*,*,*
06Bh	PT3IN	IN3.7	IN3.6	IN3.5	IN3.4	IN3.3	IN3.2	IN3.1	IN3.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
06Ch	TRISC3	TC3.7	TC3.6	TC3.5	TC3.4	TC3.3	TC3.2	TC3.1	TC3.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
06Dh	PT3DA	DA3.7	DA3.6	-	-	-	-	DA3.1	DA3.0	00.. ..00	uu.. ..uu	**,-,- -,-,*,*
06Eh	PT3PU	PU3.7	PU3.6	PU3.5	PU3.4	PU3.3	PU3.2	PU3.1	PU3.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
06Fh	PT3M1	-	PM3.3[0]	PM3.2[1:0]		-	-	PM3.0[1:0]		.000 ..00	uuuu uuuu	*,*,*,*,*,*,*,*
070h	PT3M2	-	-	PM3.6[1:0]		-	-	PM3.4[1:0]		..00 ..00	uuuu uuuu	*,*,*,*,*,*,*,*
071h	PT3INT	INTG3.7	INTG3.6	INTG3.5	INTG3.4	INTG3.3	INTG3.2	INTG3.1	INTG3.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
072h	PT3INTE	INTE3.7	INTE3.6	INTE3.5	INTE3.4	INTE3.3	INTE3.2	INTE3.1	INTE3.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
073h	PT3INTF	INTF3.7	INTF3.6	INTF3.5	INTF3.4	INTF3.3	INTF3.2	INTF3.1	INTF3.0	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*

表 5-2 資料記憶體列表

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
074h	UR0CN	ENSP	ENTX	TX9	TX9D	PARITY	-	-	WUE	0000 0..0	uuuu u..u	*,*,*,*,-,-,*
075h	UR0STA	-	RC9D	PERR	FERR	OERR	RCIDL	TRMT	ABDOVF	.000 0010	.uuu uuuu	-,r,r,r r,r,r,rw 0
076h	BA0CN	-	-	-	-	ENCR	RC9	ENADD	ENABD	 0000	.... uuuu	-,-,-,- *,*,*,*
077h	BG0RH	-	-	-	Baud Rate Generator Register High Byte					...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
078h	BG0RL	Baud Rate Generator Register Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
079h	TX0R	UART Transmit Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
07Ah	RC0REG	UART Receive Register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
07Bh	MCCN0	ENRCC[1:0]		CMPO	CPIS	CPOR	CPDF	CMPHS	ENCMP	0000 0000	uuuu uuuu	*,*,r,*,*,*,*,*
07Ch	MCCN1	CPRL	VRSEL	CPRH[1:0]		CPNS[1:0]		CPPS[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
07Dh	MCCN2				CPDA[4:0]					0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
07Eh	MCCN3				CPDM[4:0]					0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
07Fh	-	-		-	-	-	-		-	0000 .000	uuuu .uuu	*,*,*,-,*,*,*
180h	CFG0	-	-	-	-	-	GCRst	EN12CT	EN12C	.... .000	.... .uuu	-,-,-,- -,*,*,*
181h	ACT0	SLAVE	-	-	I2CER	START	STOP	I2CINT	ACK	0..0 0000	u..u uuuu	*,*,*,*,*,*,*,*
182h	STA0	MACTF	SACTF	RDBF	RWF	DFF	ACKF	GCF	ARBF	0001 0000	uuuu uuuu	*,*,*,*,*,*,*,*
183h	CRG0	CRG[7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
184h	TOC0	I2CTF	DI2C[2:0]			I2CTLT[3:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
185h	RDB0	RDB[7:1]							RDB[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
186h	TDB0	TDB0[7:1]							TDB0[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
187h	SID0	SID0[7:1],The corresponding address of the 7-bit mode							SID0V[0]	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
18Eh	BIE2ARH	ENBIE2	-	1	1	1	1	1	1	0.xx xxxx	u.uu uuuu	*,-,*,*,*,*,*,*
192h	EECR1	-	-	-	-	-	-	-	EEWR	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
193h	EECR2	Read Command : Write 0xA5, then reload datas to EERD0~ EERD31								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
197h	EERD0	EE Data0[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
198h	EERD1	EE Data1[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
199h	EERD2	EE Data2[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
19Ah	EERD3	EE Data3[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
19Bh	EERD4	EE Data4[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
19Ch	EERD5	EE Data5[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
19Dh	EERD6	EE Data6[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
19Eh	EERD7	EE Data7[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
19Fh	EERD8	EE Data8[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1A0h	EERD9	EE Data9[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1A1h	EERD10	EE Data10[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1A2h	EERD11	EE Data11[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1A3h	EERD12	EE Data12[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1A4h	EERD13	EE Data13[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1A5h	EERD14	EE Data14[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1A6h	EERD15	EE Data15[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1A7h	EERD16	EE Data16[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1A8h	EERD17	EE Data17[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1A9h	EERD18	EE Data18[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1AAh	EERD19	EE Data19[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1ABh	EERD20	EE Data20[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1ACh	EERD21	EE Data21[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1ADh	EERD22	EE Data22[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1AEh	EERD23	EE Data23[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1AFh	EERD24	EE Data24[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1B0h	EERD25	EE Data25[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1B1h	EERD26	EE Data26[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1B2h	EERD27	EE Data27[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1B3h	EERD28	EE Data28[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1B4h	EERD29	EE Data29[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1B5h	EERD30	EE Data30[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
1B6h	EERD31	EE Data31[7:0]								1111 1111	uuuu uuuu	*,*,*,*,*,*,*,*
080h ~ 0FFh		SRAM as 128Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*

表 5-3 資料記憶體列表

6. 電氣特性

Absolute Maximum Ratings :
Absolute maximum ratings over operating free-air temperature (unless otherwise noted)
Voltage applied at V_{DD} to V_{SS} . . . . −0.2 V to 6.0 V
Voltage applied to any pin . . . . −0.2 V to V_{DD} + 0.3 V
Diode current at any device terminal . . . . ±2 mA
Storage temperature, ... −55℃ to 125℃
(Operation Mode) . . . . −40℃ to 85℃
Total power dissipation. 0.5w
Maximum output current sink by any I/O pin. 20mA

6.1. Recommended operating conditions

T_A = -40℃ ~ 85℃,unless otherwise noted

Sym.	Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		All digital peripherals and CPU V_{DD} = 1.9V~5.5V, Frequency<=9.6MHz, V_{DD} = 3.6V~5.5V, Frequency<=16MHz,		1.9		5.5	V
V_{DDA}	Supply Voltage		Analog peripherals		2.4		5.5	
V_{SS}	Supply Voltage				0		0	
XT	External Oscillator Frequency	Watch crystal	V_{DD} = 2.2V~5.5V, ENXT[0]=1	XTS[1:0]=0x		32768		Hz
		Ceramic resonator, Crystal		XTS[1:0]=10	450K		4M	
				XTS[1:0]=11	1M		8M	
		Ceramic resonator, Crystal	V_{DD} = 3.6V~5.5V, ENXT[0]=1	XTS[1:0]=11	450K		16M	

6.2. Internal RC Oscillator

T_A = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
HAO	High Speed Oscillator Frequency (before trim)	ENHAO[0]=1, HAOM[1:0]=00b	VDD=2.2V~5.5V, TA = -40℃~ 85℃	-20%	1.843	+20%	MHz
		ENHAO[0]=1, HAOM[1:0]=01b,		-20%	4.147	+20%	MHz
		ENHAO[0]=1, HAOM[1:0]=10b		-20%	8.755	+20%	MHz
		ENHAO[0]=1, HAOM[1:0]=11b	VDD=3.6V~5.5V, TA = -40℃~ 85℃	-20%	17.51	+20%	MHz
	High Speed Oscillator Frequency (after trim *1)	ENHAO[0]=1, HAOM[1:0]=00b	VDD=3V/5V, TA = 25℃	-1%	1.843	+1%	MHz
			VDD=3V/5V, TA = -40℃~ 85℃	-3%	1.843	+3%	MHz
			VDD=2.2V~5.5V, TA = 25℃	-3%	1.843	+3%	MHz
			VDD=2.2V~5.5V, TA = -40℃~ 85℃	-6%	1.843	+6%	MHz
		ENHAO[0]=1, HAOM[1:0]=01b	VDD=3V/5V, TA = 25℃	-1%	4.147	+1%	MHz
			VDD=3V/5V, TA = -40℃~ 85℃	-3%	4.147	+3%	MHz
			VDD=2.2V~5.5V, TA = 25℃	-3%	4.147	+3%	MHz
			VDD=2.2V~5.5V, TA = -40℃~ 85℃	-6%	4.147	+6%	MHz
		ENHAO[0]=1, HAOM[1:0]=10b	VDD=3V/5V, TA = 25℃	-1%	8.755	+1%	MHz
			VDD=3V/5V, TA = -40℃~ 85℃	-3%	8.755	+3%	MHz
			VDD=2.2V~5.5V, TA = 25℃	-4%	8.755	+4%	MHz
			VDD=2.2V~5.5V, TA = -40℃~ 85℃	-8%	8.755	+8%	MHz
		ENHAO[0]=1, HAOM[1:0]=11b	VDD=3.6V/5V, TA = 25℃	-1%	17.51	+1%	MHz
			VDD=3.6V/5V, TA = -40℃~ 85℃	-3%	17.51	+3%	MHz
			VDD=3.6V~5.5V, TA = 25℃	-2%	17.51	+2%	MHz
			VDD=3.6V~5.5V, TA = -40℃~ 85℃	-5%	17.51	+5%	MHz

LPO	Low Power Oscillator Frequency	VDD supply voltage be enable LPO VDD=2.2V~5.5V, TA = -40℃~ 85℃	-20%	14.5	+20%	KHz

*1: “after trim” means that the frequency can be corrected more accurately through the programming of the chip, and although the HAO provides four frequencies, only one of the frequencies can be selected for the after trim during programming.

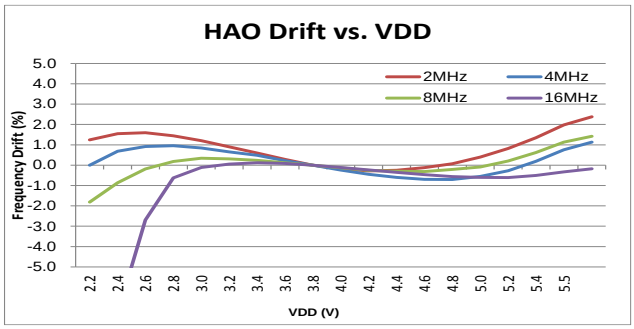


Figure 6.2-1 HAO vs. VDD

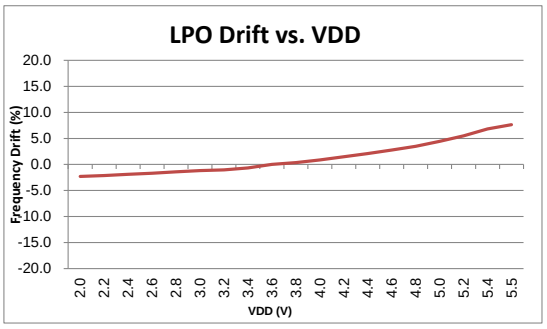


Figure 6.2-2 LPO vs. VDD

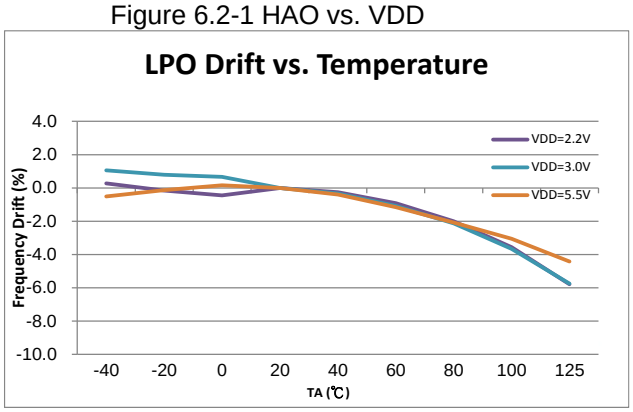


Figure 6.2-3 LPO vs. Temperature

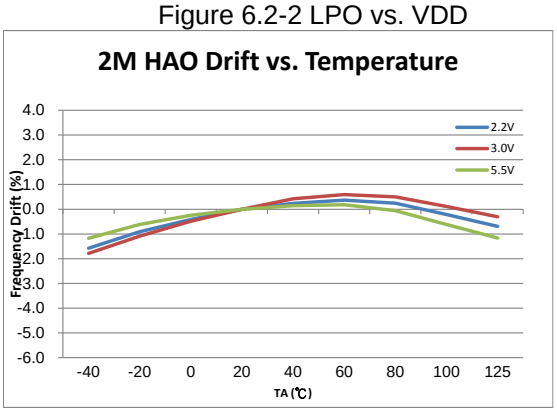


Figure 6.2-4 HAO(1.843MHz) vs. Temperature

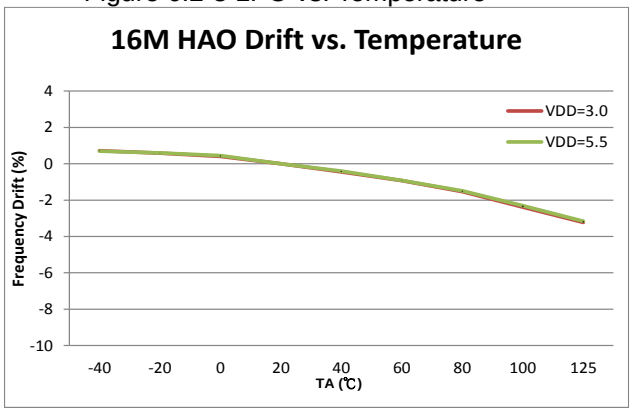


Figure 6.2-5 HAO(17.510MHz) vs. Temperature

6.3. Supply current into VDD excluding peripherals current

T_A = 25℃,V_{DD} = 3.0V,OSC_LPO = 14.5KHz, BOR2 OFF, OSC_CY = off, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{AM1}	Active mode 1	OSC_HAO = 17.510MHz, CPU_CK = 17.510MHz		1700	2500	uA
I_{AM3}	Active mode 3	OSC_HAO = 1.843MHz, CPU_CK = 1.843MHz		680	1000	uA
I_{AM4}	Active mode 4	OSC_HAO = 1.843MHz, CPU_CK = 1.843MHz/2		630	945	uA
I_{LP1}	Low Power 1	OSC_HAO=off, CPU_CK = LPO		490	735	uA
I_{LP2}	Low Power 2	OSC_HAO=off, CPU_CK = LPO, Idle state		0.5	2	uA
I_{LP3}	Low Power 3	OSC_HAO=off, CPU_CK = off, Sleep state		0.1	1	uA

OSC_CY：External Oscillator frequency.
OSC_HAO：Internal High Accuracy Oscillator frequency.
CPU_CK：CPU core work frequency.

T_A = 25℃,V_{DD} = 5.5V,OSC_LPO = 14.5KHz, BOR2 OFF, OSC_CY = off, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{AM1}	Active mode 1	OSC_HAO = 17.510MHz, CPU_CK = 17.510MHz		2850	4200	uA
I_{AM3}	Active mode 3	OSC_HAO = 1.843MHz, CPU_CK = 1.843MHz		900	1350	uA
I_{AM4}	Active mode 4	OSC_HAO = 1.843MHz, CPU_CK = 1.843MHz/2		770	1155	uA
I_{LP1}	Low Power 1	OSC_HAO=off, CPU_CK = LPO		510	765	uA
I_{LP2}	Low Power 2	OSC_HAO=off, CPU_CK = LPO, Idle state		1.3	4	uA
I_{LP3}	Low Power 3	OSC_HAO=off, CPU_CK = off, Sleep state		0.3	2	uA

OSC_CY：External Oscillator frequency.
OSC_HAO：Internal High Accuracy Oscillator frequency.
CPU_CK：CPU core work frequency.

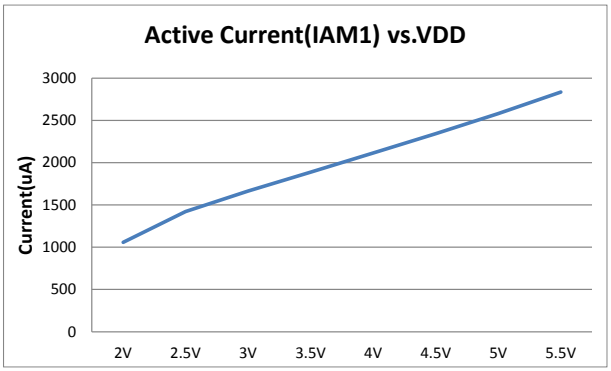


Figure 6.3-1 I_{AM1} vs. VDD

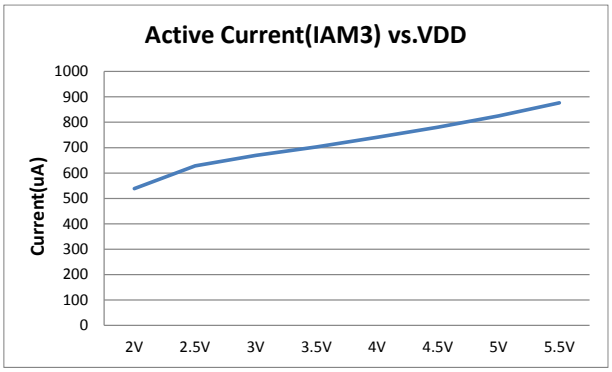


Figure 6.3-2 I_{AM3} vs. VDD

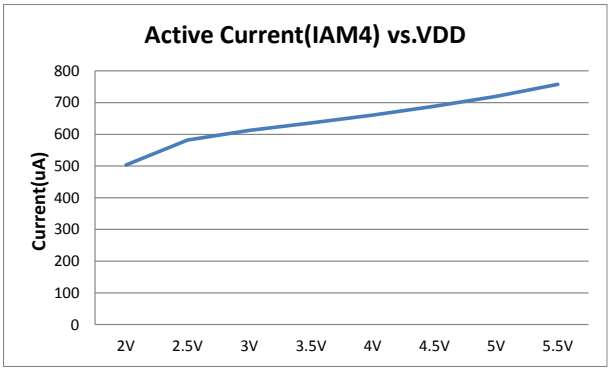


Figure 6.3-3 I_{AM4} vs. VDD

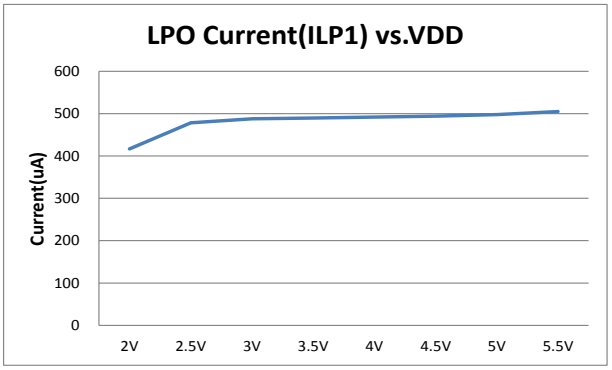


Figure 6.3-2 I_{LP1} vs. VDD

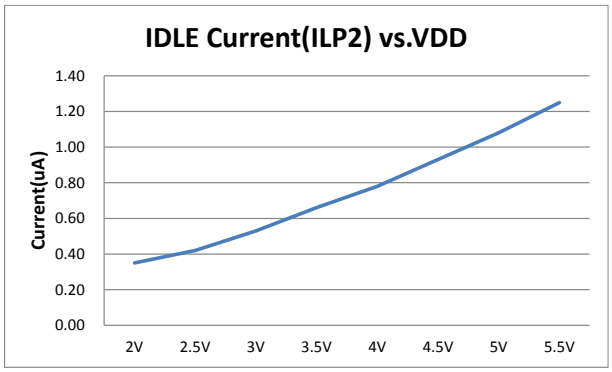


Figure 6.3-3 I_{LP2} vs. VDD

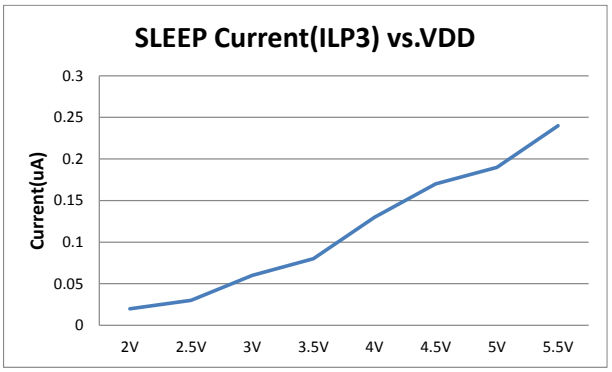


Figure 6.3-4 I_{LP3} vs. VDD

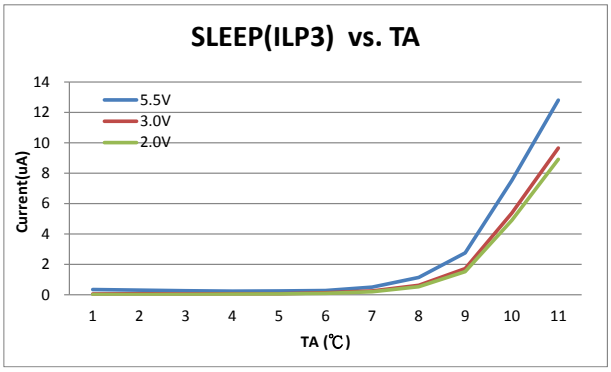


Figure 6.3-7 I_{LP3} vs. Temperature

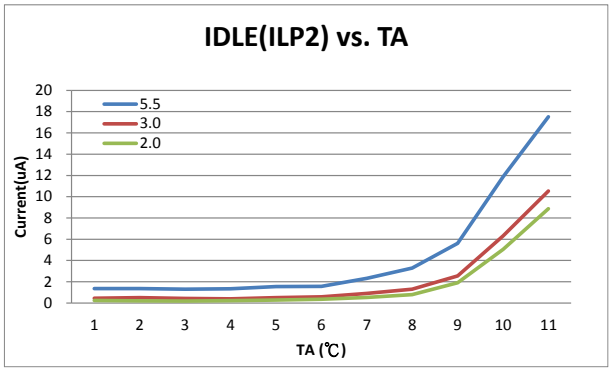


Figure 6.3-8 I_{LP2} vs. Temperature

6.4. Port 1~3

T_A = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				0.7*VDD	V
V_{IL}	Low-Level input voltage		0.3*VDD			
V_{hys}	Input Voltage hysteresis(V_{IH} - V_{IL})			0.3*VDD		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance		-25%	60	+25%	kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	VDD=3V, I_{OH}=-10mA,	V_{DD} -0.5			V
		VDD=5V, I_{OH}=-15mA,	V_{DD} -0.5			
V_{OL}	Low-level output voltage	VDD3V, I_{OL}=10mA			V_{SS} +0.4	
		VDD=5V, I_{OL}=15mA			V_{SS} +0.4	

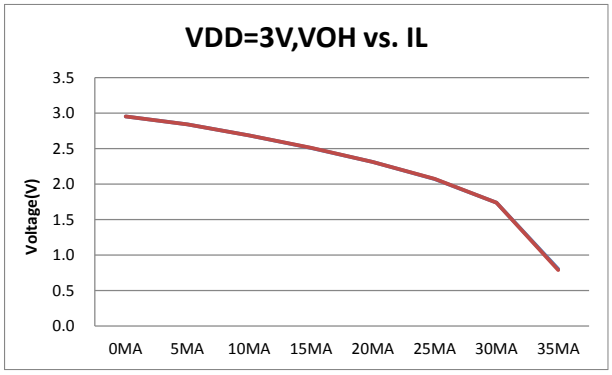


Figure 6.4-1 V_{OH} vs. I_{OH}

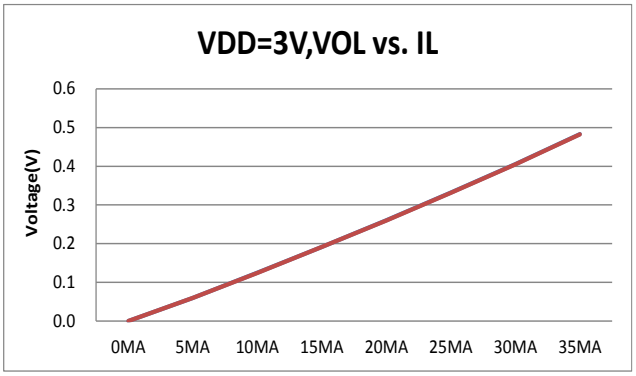


Figure 6.4-2 V_{OL} vs. I_{OL}

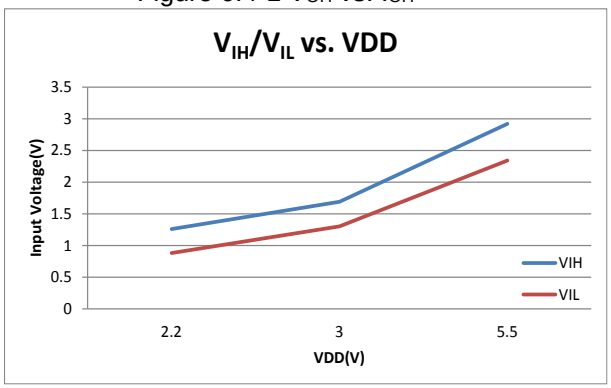


Figure 6.4-3 V_{IH}/V_{IL} vs. VDD

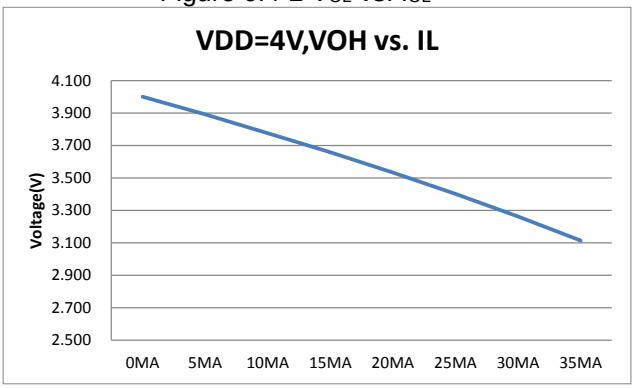


Figure 6.4-4 V_{IH}/V_{IL} vs. VDD

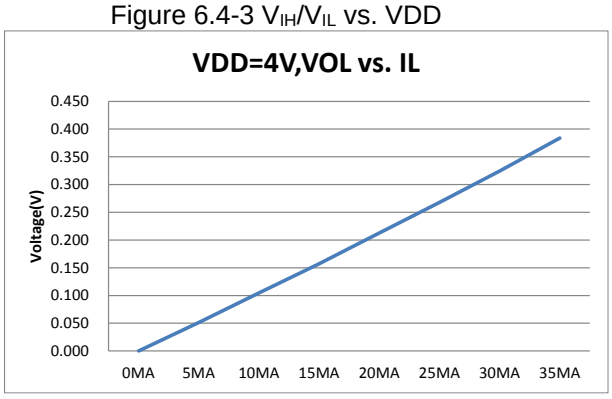


Figure 6.4-5 V_{IH}/V_{IL} vs. VDD

6.5. Reset(Brownout)

T_A = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BOR1	Pulse length needed to accepted reset internally, t_{d-LVR1}		2			uS
	V_{DD} Start Voltage to accepted reset internally (L➔H),V_{HYS1}		1.0	1.35	1.65	V
	BOR1 current, I_{BOR1}			0.1	0.5	uA
	Temperature Drift			15		%
BOR2	Pulse length needed to accepted reset internally, t_{d-LVR2}		2			uS
	V_{DD} Start Voltage to accepted reset internally (L➔H), V_{HYS2}	BOR_TH[2:0]=000b	-10%	1.73	+10%	V
		BOR_TH[2:0]=001b	-10%	2.0	+10%	
		BOR_TH[2:0]=010b	-10%	2.22	+10%	
		BOR_TH[2:0]=011b	-10%	2.5	+10%	
		BOR_TH[2:0]=100b	-10%	2.72	+10%	
		BOR_TH[2:0]=101b	-10%	3.0	+10%	
		BOR_TH[2:0]=110b	-10%	3.63	+10%	
		BOR_TH[2:0]=111b	-10%	4.0	+10%	
	V_{DD} Start Voltage to accepted reset internally (H➔L), V_{LVR2}	BOR_TH[2:0]=000b	-10%	1.67	+10%	
		BOR_TH[2:0]=001b	-10%	1.96	+10%	
		BOR_TH[2:0]=010b	-10%	2.17	+10%	
		BOR_TH[2:0]=011b	-10%	2.44	+10%	
		BOR_TH[2:0]=100b	-10%	2.69	+10%	
		BOR_TH[2:0]=101b	-10%	2.96	+10%	
		BOR_TH[2:0]=110b	-10%	3.58	+10%	
		BOR_TH[2:0]=111b	-10%	3.94	+10%	
	Hysteresis, $V_{HYS2-LVR2}$		25	60	90	mV
	BOR2 current, I_{BOR2}	VDD=3.3V		8	12	uA
		VDD=5.5V		10	15	uA
	Temperature Drift			3	5	%
RST	Pulse length needed as MCLR pin to accepted reset internally, t_{d-RST}		2			uS
	Input Voltage to accepted reset voltage			1.1		V
	Reset release voltage			2		V

BOR1/BOR2：Brownout Reset 1/2
LVR：Low Voltage Reset of BOR
MCLR：External Input Reset pin

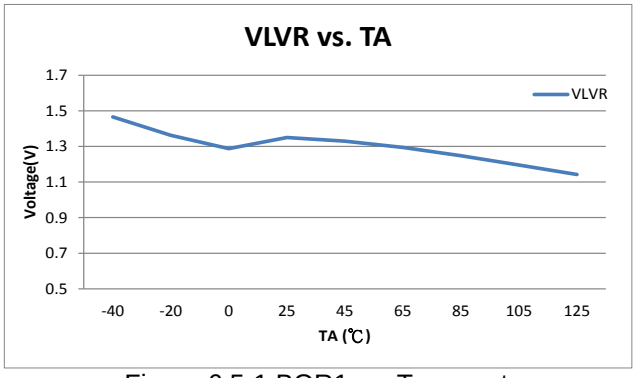


Figure 6.5-1 BOR1 vs. Temperature

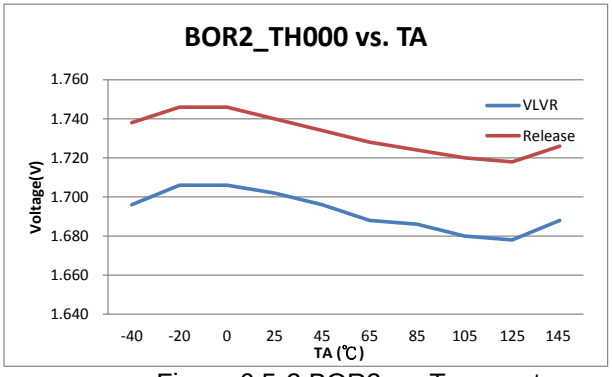


Figure 6.5-2 BOR2 vs. Temperature

6.6. Power System

T_A = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
VDDA	VDDA operation current, I_{VDDA}	I_L = 0mA	LDOC[2:0]=000b		20		uA
	Select VDDA output voltage	I_L = 0.1mA, VDD=5.5V	LDOC [2:0]=000b	-5%	2.4	+5%	V
			LDOC [2:0]=001b		2.6		
			LDOC [2:0]=010b		2.9		
			LDOC [2:0]=011b		3.3		
			LDOC [2:0]=100b		3.6		
			LDOC [2:0]=101b		4.0		
			LDOC [2:0]=110b		4.5		
			LDOC [2:0]=111b		5.0		
		I_L = 10mA, VDD=2.6V	LDOC [2:0]=000b	-6%	2.4	+5%	
	Dropout voltage	I_L = 10mA, VDD=2.9V	LDOC [2:0]=010b		200		mV
	Temperature drift	I_L = 0.1mA, T_A=-40℃~85℃	LDOC [2:0]=000b		50		PPM/℃
	V_{DD} Voltage drift	LDOC [2:0]=000b	V_{DD}=2.2V~5.5V		±0.2		%/V
REFO	operation current, I_{RERFO}	I_L = 10uA VDDA=2.4V, ENLDO[0]=1b,	ENREFO[0]=1b		50		uA
	output voltage, V_{REFO}		REFOS=00b	-5%	1.2	-5%	V
			REFOS=01b		2.0		
		VDDA=2.6V, ENLDO[0]=1b,	REFOS=10b		2.4		
			REFOS=11b		3.0		
	Output voltage with Load	VDDA=2.4V, I_L = ±200uA		0.95		1.05	V_{REFO}
	Temperature drift	T_A=-40℃~85℃			50		PPM/℃
	V_{DDA} Voltage drift				100		uV/V
ACM	operation current, I_{ACM}	ENVCM[0]=1b			50		uA
	Internal ADC common mdoe voltage, VACM	ENVCM[0]=1b	VCMS[0]=0b, SELVIN[0]=0b		VDDA/2		
			VCMS[0]=0b, SELVIN[0]=0b		1.2		V
			VCMS[0]=1b,		REFO		
V12	operation current, I_{V12}	ENVCM[0]=1b			50		uA
	Internal V12 buffer voltage, V_{V12}	ENBGR[0]=1b, ENAD1[0]=1b,			1.2		V

VDDA：Adjust Voltage Regulator
REFO：Analog common mode voltage
ACM：Internal ADC common mdoe voltage
V12：Internal V12 buffer voltage

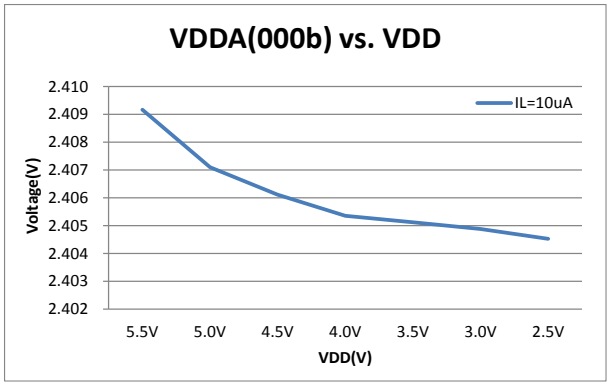


Figure 6.6-1 VDDA(000b) vs. VDD

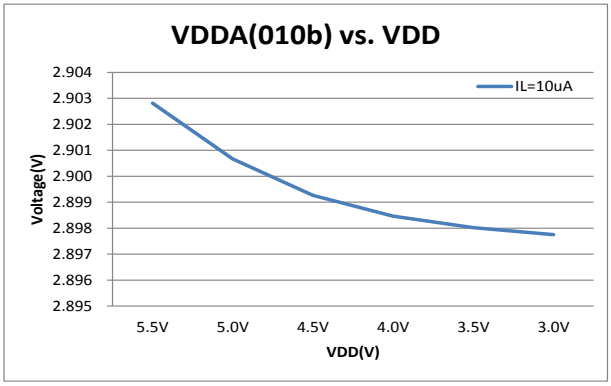


Figure 6.6-2 VDDA(010b) vs. VDD

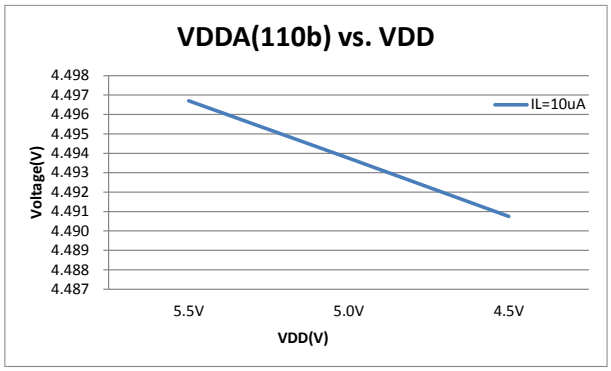


Figure 6.6-3 VDDA(110b) vs. VDD

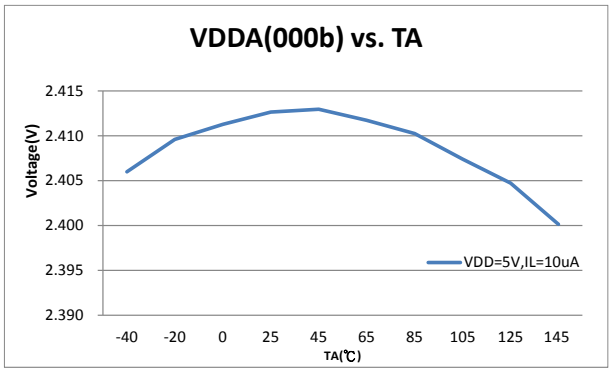


Figure 6.6-4 VDDA(000b) vs. Temperature

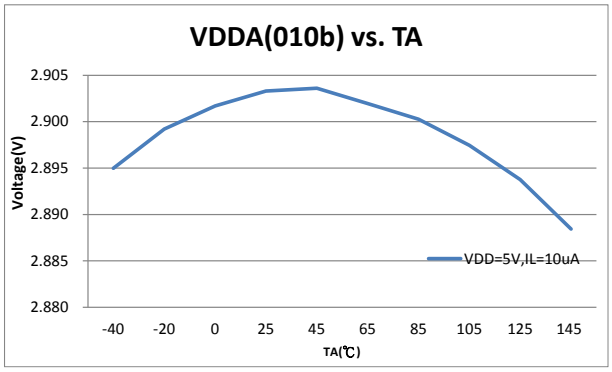


Figure 6.6-5 VDDA(010b) vs. Temperature

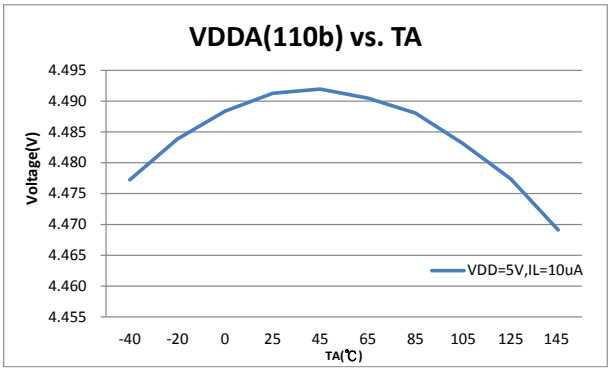


Figure 6.6-6 VDDA(110b) vs. Temperature

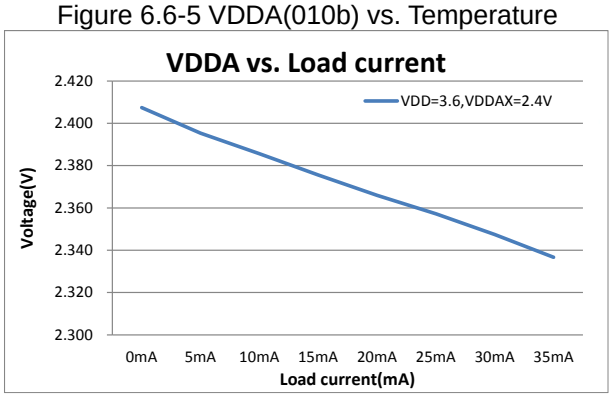


Figure 6.6-7 VDDA vs. Load current

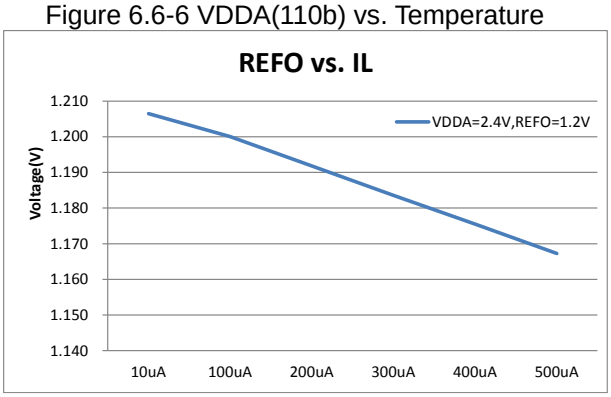


Figure 6.6-8 REFO vs. Load current

6.7. Multi-Comparator

T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{MC}	Operation supply current	ENCMP[0]=1, CMPHS[0]=1b		5		uA
	Low Power Mode	ENCMP[0]=1, CMPHS [0]=0b		1		
V_{IC}	Common-mode input voltage		0		V_{DD}-1	V
V_{OS}	Offset voltage		-5		5	mV
V_{hys}	Input hysteresis		0	0.7	1.5	mV
V_{ref}	Reference Voltage	CPPS[1:0]=11b, VRSEL[0]=0b,	1.1	1.2	1.3	V
	Temperature Drift			50		ppm/℃
	VDD Voltage drift			±2		%/V
V_{accy}	Reference Voltage	ENLDO[0]=1b,CPPS[1:0]=11b, VRSEL[0]=1b	1.15	1.2	1.25	V
	Temperature Drift			50		ppm/℃
	VDD Voltage drift			±0.2		%/V
I_R	Multi-node resistor current	CPRL[0]=0b		10		uA
		CPRL[0]=1b		30		

LVD	ENLDO[0]=1b,CPPS[1:0]=11b, CPRH[1:0]=01b,CPRL[0]=0b	CPDA[4:0]=00011b	-5%	3.89	+5%	V
		CPDA[4:0]=00100b		3.73		
		CPDA[4:0]=00101b		3.58		
		CPDA[4:0]=00110b		3.44		
		CPDA[4:0]=00111b		3.31		
		CPDA[4:0]=01000b		3.19		
		CPDA[4:0]=01001b		3.08		
		CPDA[4:0]=01010b		2.98		
		CPDA[4:0]=01011b		2.88		
		CPDA[4:0]=01100b		2.79		
		CPDA[4:0]=01101b		2.71		
		CPDA[4:0]=01110b		2.63		
		CPDA[4:0]=01111b		2.55		
		CPDA[4:0]=10000b		2.48		
		CPDA[4:0]=10001b		2.42		
		CPDA[4:0]=10010b		2.35		
		CPDA[4:0]=10011b		2.29		
		CPDA[4:0]=10100b		2.24		
		CPDA[4:0]=10101b		2.18		
		CPDA[4:0]=10110b		2.13		
		CPDA[4:0]=10111b		2.08		
		CPDA[4:0]=11000b		2.03		
		CPDA[4:0]=11001b		1.99		
		CPDA[4:0]=11010b		1.94		
		CPDA[4:0]=11011b		1.90		
		CPDA[4:0]=11100b		1.86		
		CPDA[4:0]=11101b		1.82		
	CPDA[4:0]=00000b~00010b, and 11110b~11111b (reserved)			-		

LVD：Low Voltage Detect.

6.8. Rail to Rail OPAMP

T_A = 25℃,V_{DD3V} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDDA	Power supply		2.4		5.5	V
V_{OUT}	Output range		0		VDDA	V
V_{IN}	Input common range		0		VDDA	V
I_{OPA}	OPAMP current			120		uA
I_{OPA_LOAD}	Output current loading (push or pull)	VDDA = 3.6V, 0.3V< Output voltage <VDDA-0.3V			1	mA
		VDDA = 2.4V, 0.3V< Output voltage <VDDA-0.3V			0.5	mA
C_{LOAD}	Max output capacitor load				1	nF
SR	Slew rate	Loading R=10K, C=100pF, 0.3V → VDDA-0.3V		0.6		V/us
UGB	Unit gain bandwidth	Loading C=100pF		1000		KHz
V_{OS}	Offset error	Vin = 1.2V	-5		+5	mV

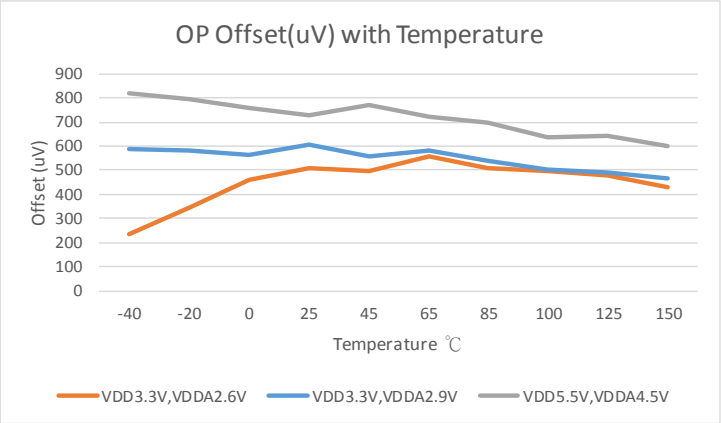


Figure 6.8-1 R2ROPAMP Offset Temperature

6.9. 12-Bit Resistance Ladders

Typical values are at T_A=25℃ and VDD = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Resolution		Monotonic		12		Bit
	Power Supply		2.4		VDDA	V
	Operation current			50		uA
V_{OUT}	Output range	Output is between Vrefp and Vrefn	0		VDDA	V
V_{REFP}	Positive reference voltage range	$V_{REFP} > V_{REFN}$	0		VDDA	V
V_{REFN}	Negative reference voltage range		0		VDDA	V
R_{ON}	12-Bit Resistance ladders. output switch	VDDA=2.4V, 0.5V < DACO < VDDA-0.5V			200	Ω
		VDDA=2.4V, DACO < 0.5V, DACO > VDDA-0.5V		10		Ω
R_{RSW}	Reference voltage switch	V_{REFP} = 2.2V, V_{REFN} = 0V, VDDA = 2.4V		15	30	Ω
R_{LADDER}	One LSB resistance ladder			200		Ω
INL	Integral linearity error	Vrefp = 2.4V, Vrefn = 0V			±3	LSB
DNL	Differential linearity error	Vrefp = 2.4V, Vrefn = 0V			±1	LSB
E_{OS}	Offset error	Vrefp = 2.4V, Vrefn = 0V			1	LSB
12-Bit Resistance Ladders.	(Vin Floating)	VDD=3.3V,VDDA=2.4V		0.1		uA

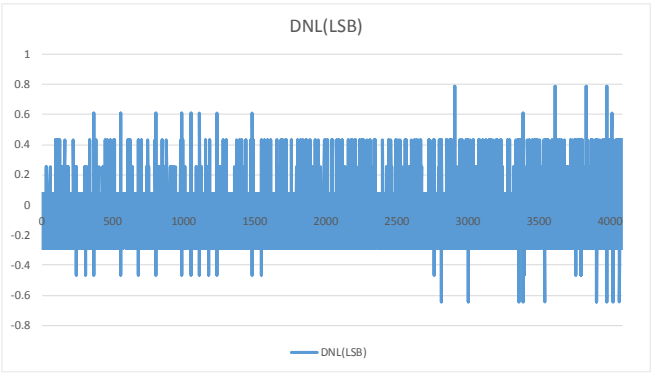


Figure 6.9-1 12-Bit Resistance DNL

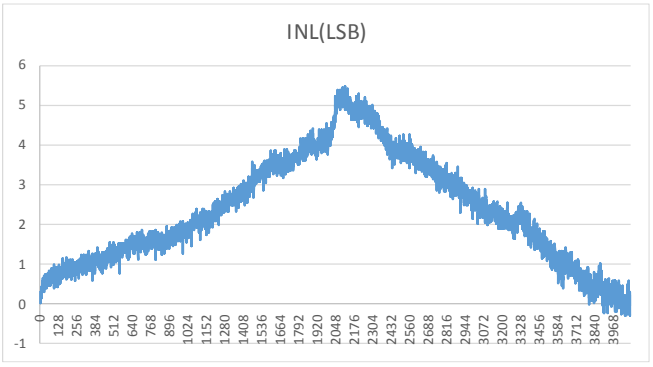


Figure 6.9-2 12-Bit Resistance INL

6.10. SD18, Power Supply and recommended operating conditions

TA = 25℃,VDD = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{SD18}	Supply Voltage at VDDA	ENLDO[0]=0		2.4		5.5	V
f_{SD18}	Modulator sample frequency, ADC_CK			125	1000	1200	KHz
	Over Sample Ratio, OSR			64		32768	
I_{SD18}	Operation supply current	ENAD1 [0]=1	GAIN =16, ADC_CK=500KHz		260		uA

6.11. SD18,performance

T_A = 25℃,V_{DD}=3.3V,VDDA=2.4V,V_{VR}=(VDDA-VSS)/2,GAIN=1,fSD18=1000KHz,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INL	Integral Nonlinearity(INL)	VDDA=2.4V,V_{VR}= VDDA/2, ΔSI=±450mV		±0.003	±0.01	%FSR
	No Missing Codes[3]	ADC_CK=1000KHz,OSR[3:0]=0000b	23			Bits
G_{SD18}	Temperature drift Gain x16	T_A = -40℃~ 85℃		10		ppm/℃

E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper	ΔAI=0V ΔVR=1.2V DCSET[3:0]=<0000> *ΔAI is external short Gain Normalized	Gain=2			1	%FSR
	Offset temperature drift with chopper		GAIN=1		0.021		uV/℃
			GAIN=2		0.026		
			GAIN=4		0.03		
			GAIN=16		0.45		
CM_{SD18}	Common-mode rejection	V_{CM}=0.7V to 1.7V, V_{VR}= 1.0V	V_{SI}=0V, GAIN=1		90		dB
			V_{SI}=0V, GAIN=16		75		dB
PSRR	DC power supply rejection	VDDA=3.0V,ΔVDDA =±100mV, V_{VR}=1.0V, V_{SI}=1.2V,V_{SI-}=1.2V,	GAIN=1	75			dB
			GAIN=16				dB

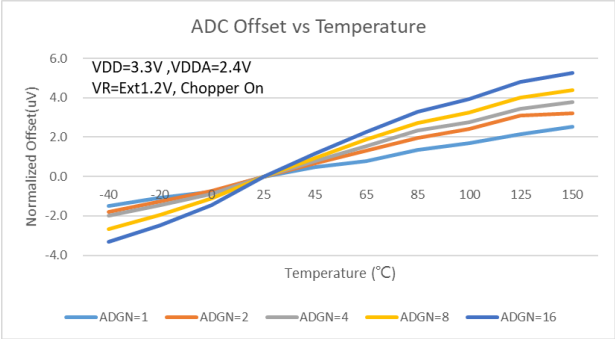


Figure 6.11-1 ADC Offset drift with Temperature

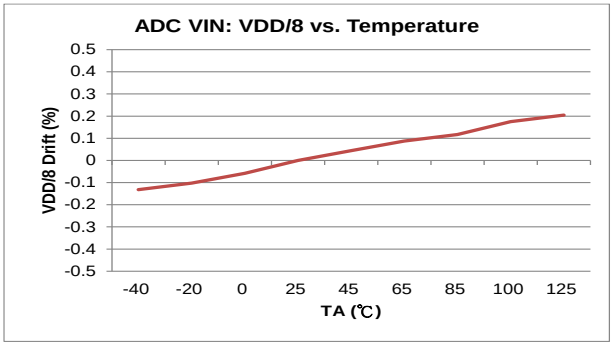


Figure 6.11-2 VDD/10 drift with Temperature

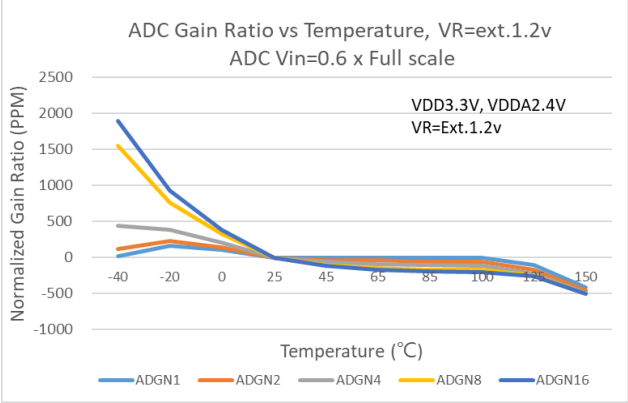


Figure 6.11-3 ADC Gain drift with Temperature

6.12. SD18 Noise Performance

HY17M24 針對 SD18 提供了重要的輸入雜訊規格。下表列出典型的雜訊規格表與 Gain, Output rate, 及差動最大輸入電壓等關係。測試條件設定在外部輸入訊號短路到 VDDA/2 電位下，取樣 1024 筆資料。

ENOB(RMS) with OSR/GAIN at A/D Clock=1MHz, VDD=3.6V, VDDA=2.4V, VREF=(VDDA-VSS)/2=1.2, Chopper Off														
Max. Vin(mV) =0.9*VREF(1)	OSR					64	128	256	512	1024	2048	4096	8192	16384	32768	65536
	Output rate(Hz)					15625	7813	3906	1953	977	488	244	122	61	31	15
	Gain	=	PGAGN	x	ADGN											
±2160	0.25	=	off	x	0.25	15.09	16.51	17.14	17.58	18.23	18.77	19.12	19.6	20	20.52	20.94
±2160	0.5	=	off	x	0.5	14.17	16.41	17.09	17.45	18.09	18.75	19.04	19.46	19.93	20.32	20.73
±1080	1	=	off	x	1	13.31	16.33	17.1	17.39	17.96	18.43	18.91	19.31	19.89	20.27	20.74
±540	2	=	off	x	2	13.88	16.14	16.91	17.19	17.71	18.11	18.57	19.03	19.61	19.99	20.53
±270	4	=	off	x	4	14.48	15.85	16.52	16.84	17.38	17.64	18.01	18.45	19.25	19.87	20.05
±135	8	=	off	x	8	10.75	15.56	16.11	16.16	16.55	16.8	17.18	17.69	18.63	19.34	19.75
±68	16	=	off	x	16	9.77	15.01	15.41	15.16	15.75	16.04	16.28	16.72	17.91	18.86	19.25

(1) Max. Vin(mV) is the max. input voltage of single end to ground(VSS).

RMS Noise(uV) with OSR/GAIN at A/D Clock=1MHz, VDD=3.6V, VDDA=2.4V, VREF=(VDDA-VSS)/2=1.2, Chopper Off														
Max. Vin(mV) =0.9*VREF(1)	OSR					64	128	256	512	1024	2048	4096	8192	16384	32768	65536
	Output rate(Hz)					15625	7813	3906	1953	977	488	244	122	61	31	15
	Gain	=	PGAGN	x	ADGN											
±2160	0.25	=	off	x	0.25	274.44	102.81	66.21	48.94	31.23	21.45	16.83	12.07	9.10	6.35	4.75
±2160	0.5	=	off	x	0.5	259.22	54.92	34.26	26.74	17.15	10.88	8.89	6.64	4.78	3.65	2.75
±1080	1	=	off	x	1	235.84	29.07	17.00	13.89	9.40	6.76	4.86	3.68	2.46	1.89	1.37
±540	2	=	off	x	2	79.17	16.58	9.72	7.97	5.57	4.22	3.08	2.23	1.49	1.15	0.79
±270	4	=	off	x	4	26.11	10.14	6.36	5.09	3.50	2.93	2.26	1.67	0.96	0.62	0.55
±135	8	=	off	x	8	173.09	6.19	4.23	4.10	3.12	2.62	2.01	1.41	0.74	0.45	0.34
±68	16	=	off	x	16	170.67	4.54	3.42	4.08	2.70	2.22	1.88	1.39	0.61	0.31	0.24

(1) Max. Vin(mV) is the max. input voltage of single end to ground(VSS).

Table 6.12-1(a) SD18 ENOB and RMS Noise Table

ENOB(RMS) with OSR/GAIN at A/D Clock=1MHz, VDD=3.6V, VDDA=2.4V, VREF=(VDDA-VSS)/2=1.2, Chopper On																
Max. Vin(mV) =0.9*VREF(1)	OSR					64	128	256	512	1024	2048	4096	8192	16384	32768	65536
	Output rate(Hz)					5208	2604	1302	651	326	163	122	61	31	15	8
	Gain	=	PGAGN	x	ADGN											
±2160	0.25	=	off	x	0.25	15.59	17.06	17.79	18.15	18.72	19.25	19.54	20.07	20.65	21.08	21.42
±2160	0.5	=	off	x	0.5	15.69	16.99	17.62	18.09	18.75	19.22	19.49	19.94	20.54	20.99	21.54
±1080	1	=	off	x	1	15.66	16.96	17.56	18.04	18.5	19.05	19.45	19.88	20.47	20.85	21.32
±540	2	=	off	x	2	15.56	16.74	17.31	17.79	18.35	18.73	18.99	19.66	20.24	20.56	21.14
±270	4	=	off	x	4	15.46	16.27	17.04	17.55	17.98	18.21	18.32	19.18	19.84	20.34	20.75
±135	8	=	off	x	8	15.14	15.54	16.6	16.9	17.3	17.38	17.57	18.51	19.45	19.95	20.41
±68	16	=	off	x	16	14.97	14.61	15.99	16.12	16.45	16.45	16.47	17.6	19.08	19.52	19.89

(1) Max. Vin(mV) is the max. input voltage of single end to ground(VSS).

RMS Noise(uV) with OSR/GAIN at A/D Clock=1MHz, VDD=3.6V, VDDA=2.4V, VREF=(VDDA-VSS)/2=1.2, Chopper On																
Max. Vin(mV) =0.9*VREF(1)	OSR					64	128	256	512	1024	2048	4096	8192	16384	32768	65536
	Output rate(Hz)					5208	2604	1302	651	326	163	122	61	31	15	8
	Gain	=	PGAGN	x	ADGN											
±2160	0.25	=	off	x	0.25	193.97	69.95	42.35	33.01	22.14	15.30	12.56	8.71	5.83	4.33	3.40
±2160	0.5	=	off	x	0.5	90.61	36.72	23.72	17.17	10.85	7.81	6.49	4.74	3.13	2.29	1.57
±1080	1	=	off	x	1	46.17	18.70	12.34	8.88	6.45	4.41	3.34	2.49	1.64	1.26	0.92
±540	2	=	off	x	2	24.74	10.93	7.34	5.28	3.59	2.75	2.29	1.44	0.97	0.77	0.52
±270	4	=	off	x	4	13.28	7.58	4.43	3.12	2.31	1.97	1.82	1.01	0.64	0.45	0.34
±135	8	=	off	x	8	8.31	6.27	3.00	2.44	1.85	1.75	1.54	0.80	0.42	0.30	0.21
±68	16	=	off	x	16	4.67	5.98	2.29	2.10	1.67	1.67	1.65	0.75	0.27	0.20	0.15

(1) Max. Vin(mV) is the max. input voltage of single end to ground(VSS).

Table 6.12-1(b) SD18 ENOB and RMS Noise Table

The RMS Noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$\text{ENOB(RMS)} = \ln\left(\frac{\text{FSR}}{\text{RMS Noise}}\right) \Big/ \ln(2)$$

$$\text{RMS Noise} = \left(2 \times \text{VREF} \times \sqrt{\sum_{k=1}^{1024}(\text{ADO}[k] - \text{Average})^2}\right) \Big/ 2^{23}$$

$$\text{Where FSR (Full - Scale Range)} = 2 \times \text{VREF/Gain.}$$

$$\text{Average} = \frac{\sum_{k=1}^{1024}(\text{ADO}[k])}{1024}$$

6.13. SD18 ,Temperature Sensor

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TC_S	Sensor temperature drift			173		uV/℃
KT	Absolute Temperature Scale 0°K			-277		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~85℃		±2		℃

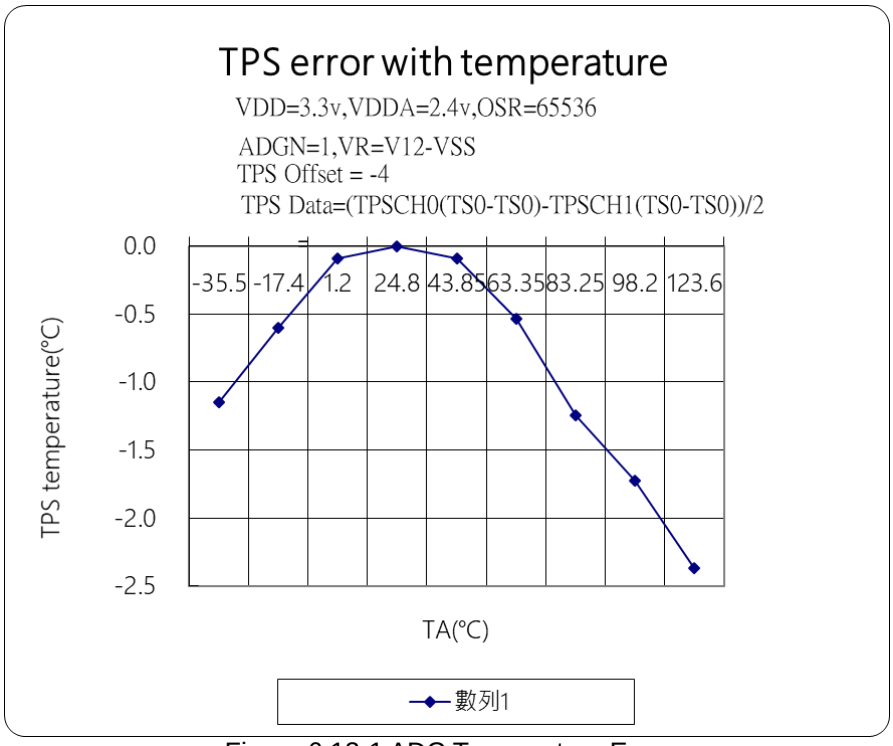


Figure 6.13-1 ADC Temperature Error

6.14. MTP Memory

TA = -40℃~85℃, VDD=3V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Main MTP Program Memory/ Build-In EEPROM Data Memory						
V_{DD}	Read/Write/Program/Erase Memory Operation supply Voltage		2.75		5.5	V
I_{BIEE}	Read/Write/Program/Erase Memory Operation supply current				22	mA
T_{DART}	Data retention time		10			Years
C_{MAIN}	Endurance cycles at main MTP block		100			Cycles
C_{EEPROM}	Endurance cycles at 32 bytes EEPROM block		3			k Cycles

7. 訂貨資訊

下單品名 1	封裝型式	引腳數	封裝型式		程式碼	出貨包裝	個裝	材料	MSL3
			描述方式		編號 2	形式	數量	組成	
HY17M24-ES28	SSOP	28	E	S28	000	Tube	50	Green[4]	MSL-3
HY17M24-ES28	SSOP	28	E	S28	000	Tape & Reel	3000	Green[4]	MSL-3
HY17M24-N024	QFN	24	N	024	000	Tape & Reel	3000	Green[4]	MSL-3
HY17M24-ES24	SSOP	24	E	S24	000	Tube	58	Green[4]	MSL-3
HY17M24-ES24	SSOP	24	E	S24	000	Tape & Reel	3000	Green[4]	MSL-3
HY17M24-S016	SOP	16	S	016	000	Tube	50	Green[4]	MSL-3
HY17M24-S016	SOP	16	S	016	000	Tape & Reel	2500	Green[4]	MSL-3

[1] **產品名稱 品名封裝型式描述方式 裝型程式碼編號（空白片 / 標準品 / 代客燒錄碼）**

例如：您的需求是 HY17M24 不帶程式碼的空白片且需要的產品是封裝片 SSOP24 出貨，則下單品名為 HY17M24-ES24，且需以 Tape & Reel 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tape & Reel

例如：您的 HY17M24 代客燒錄服務申請的程式碼編號為 009，而需求的產品是封裝片 SSOP24 出貨，則下單品名為 HY17M24-ES24-009，且需以 Tape & Reel 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tape & Reel

[2] 程式碼編號

“001” ~ “999” 為標準品或代客燒錄申請的程式碼編號，而空白晶片不帶此碼。

[3] MSL:

濕度敏感性等級係依據 IPC/JEDEC J-STD-020 的規範加以試驗分級，並參考 IPC/JEDEC J-STD-033 的標準處理、包裝、運輸與使用。

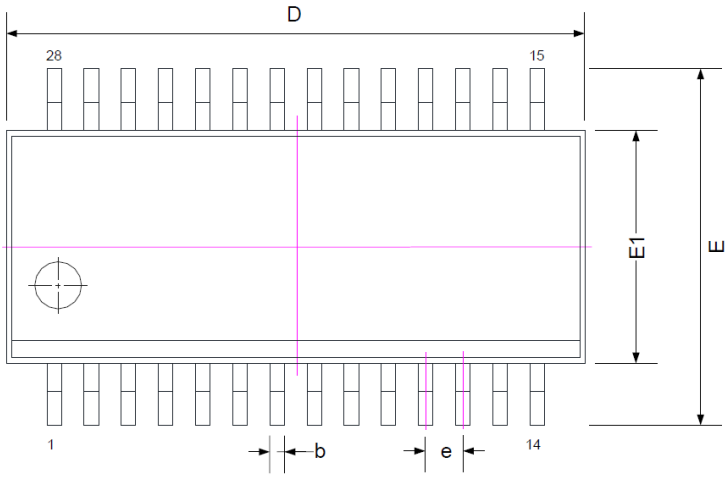
[4] Green (RoHS & no Cl/Br):

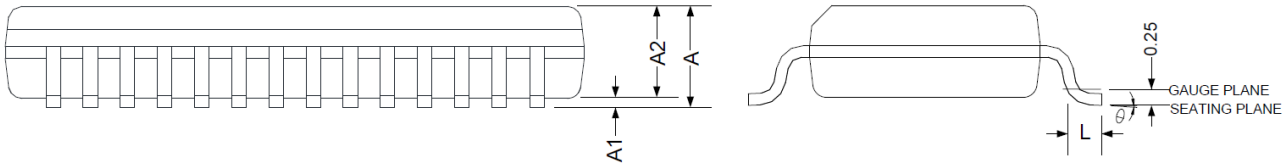
HYCON 產品皆為 Green Product，符合 RoHS 指令，REACH 高關注物質(SVHC)以及無鹵素規定 (Br<900ppm or Cl<900ppm or (Br+Cl)<1500ppm)。

8. 封裝型式資訊

8.1. SSOP28(ES28)

8.1.1. Package Dimensions SSOP28(150mil)



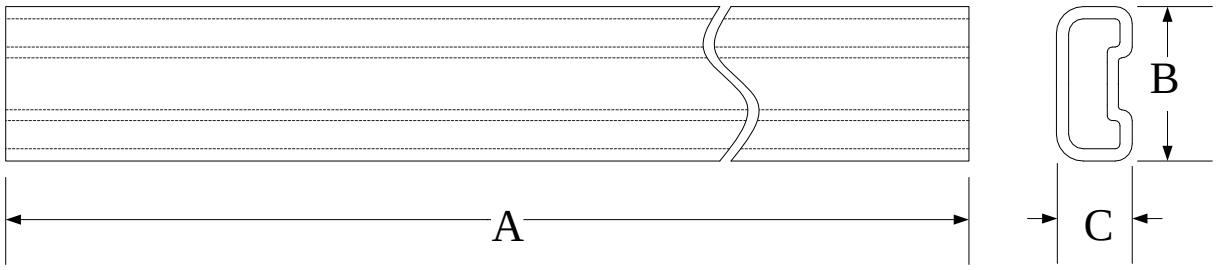


SYMBOLS	MIN	NOM	MAX
A	1.34	1.63	1.75
A1	0.10	0.15	0.25
A2	-	-	1.50
b	0.20	-	0.30
c	0.18	-	0.25
D	9.80	9.91	10.01
E1	3.81	3.91	3.99
E	5.79	5.99	6.20
L	0.41	0.64	1.27
e	0.635 BASIC		
θ°	0	-	8

Note:
1. All dimensions refer to JEDEC OUTLINE MO-137.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

8.1.2. Tube Dimensions SSOP28(150mil)

Unit : mm

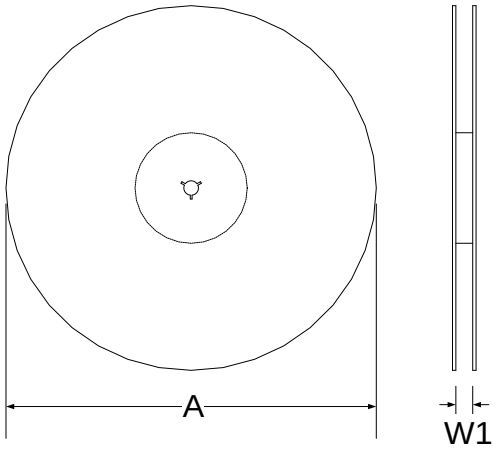


SYMBOLS	A	B	C
Spec.	529.6±1.0	8.001±0.127	3.937±0.127

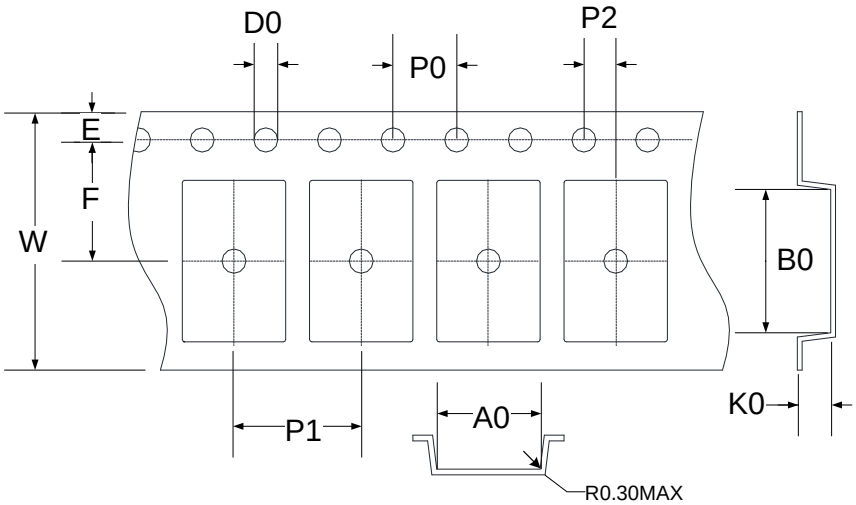
8.1.3. Tape & Reel Information

8.1.3.1. Reel Dimensions

Unit: mm



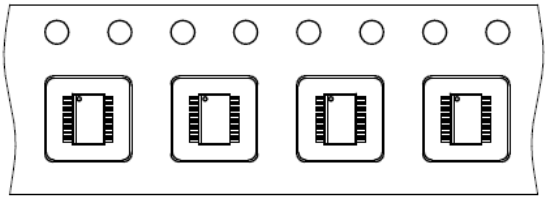
8.1.3.2. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	16.5	6.50	10.30	2.10	4.00	8.00	2.00	1.75	7.50	1.50	16.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.10	+0.1/-0	±0.30

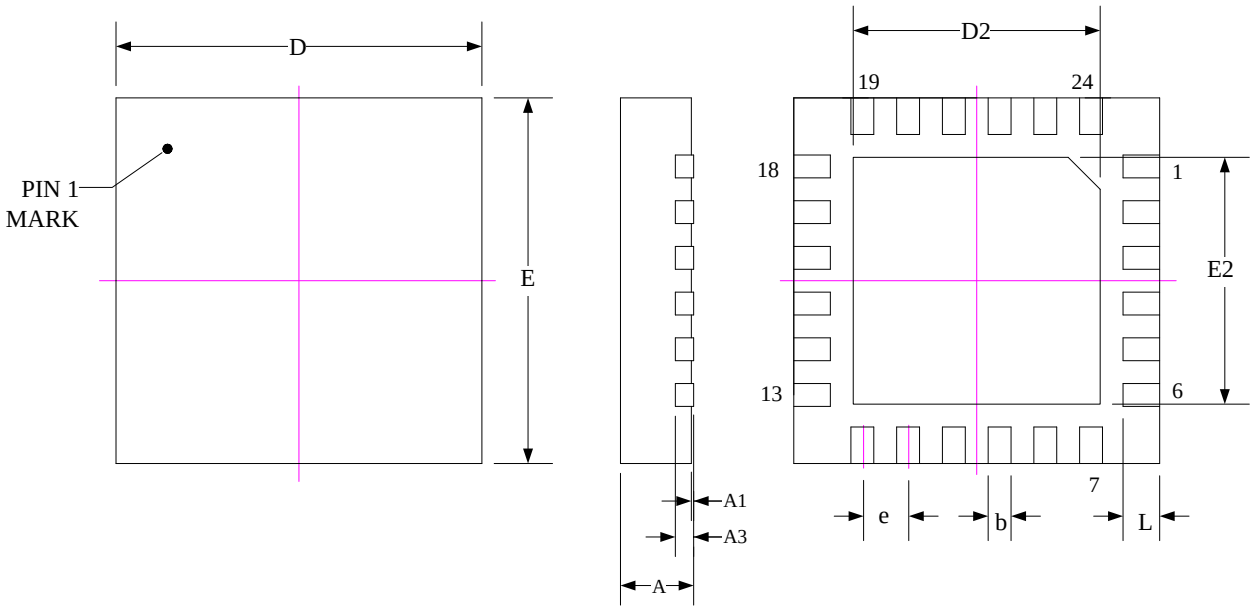
Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

8.1.3.3. Pin1 direction



8.2. QFN24(N024)

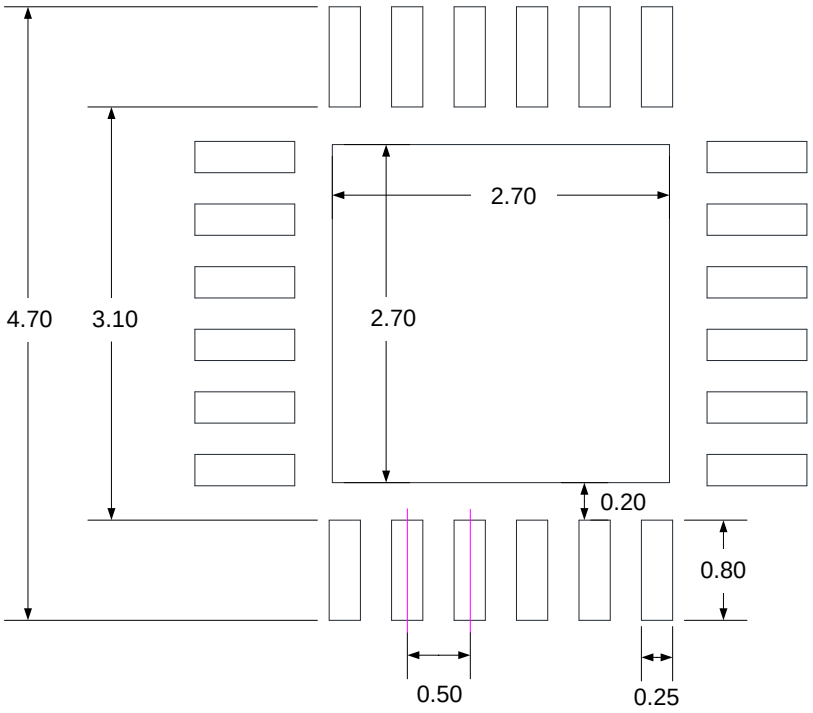
8.2.1. Package Dimensions QFN24(4x4x0.75)



SYMBOLS	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.18	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
L	0.35	0.40	0.45
e		0.50 BASIC	

Note:
1. All dimensions refer to JEDEC OUTLINE MO-220.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.
4. https://www.hycontek.com/hy_mcu/QFN_DFN_PCB.pdf

8.2.2. Land Pattern Design Recommendations

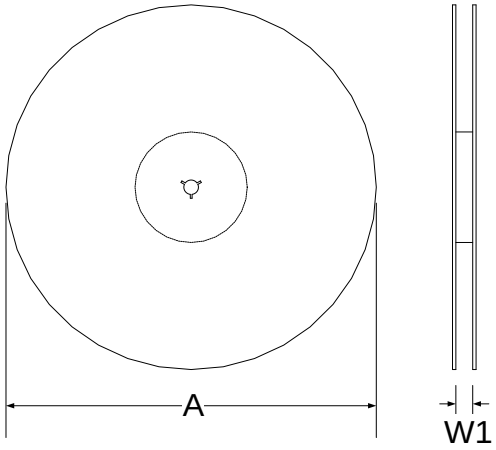


Note:
1. Publication IPC-7351 is recommended for alternate designs.
2. https://www.hycontek.com/hy_mcu/QFN_DFN_PCB.pdf
3. Unit: mm.

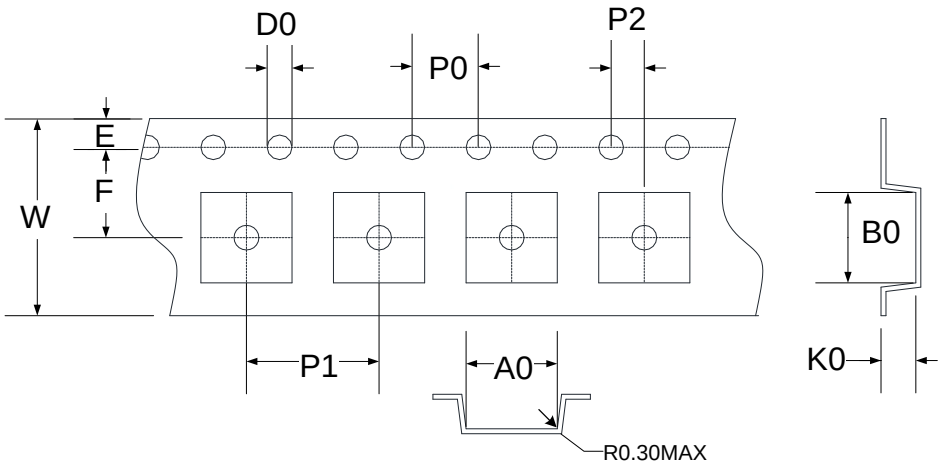
8.2.3. Tape & Reel Information

8.2.3.1. Reel Dimensions

Unit: mm



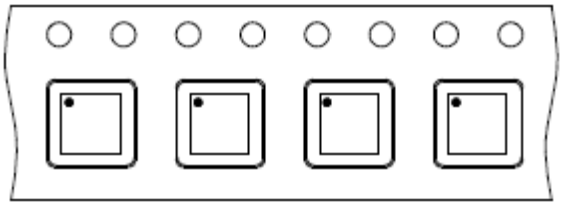
8.2.3.2. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	4.35	4.35	1.10	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

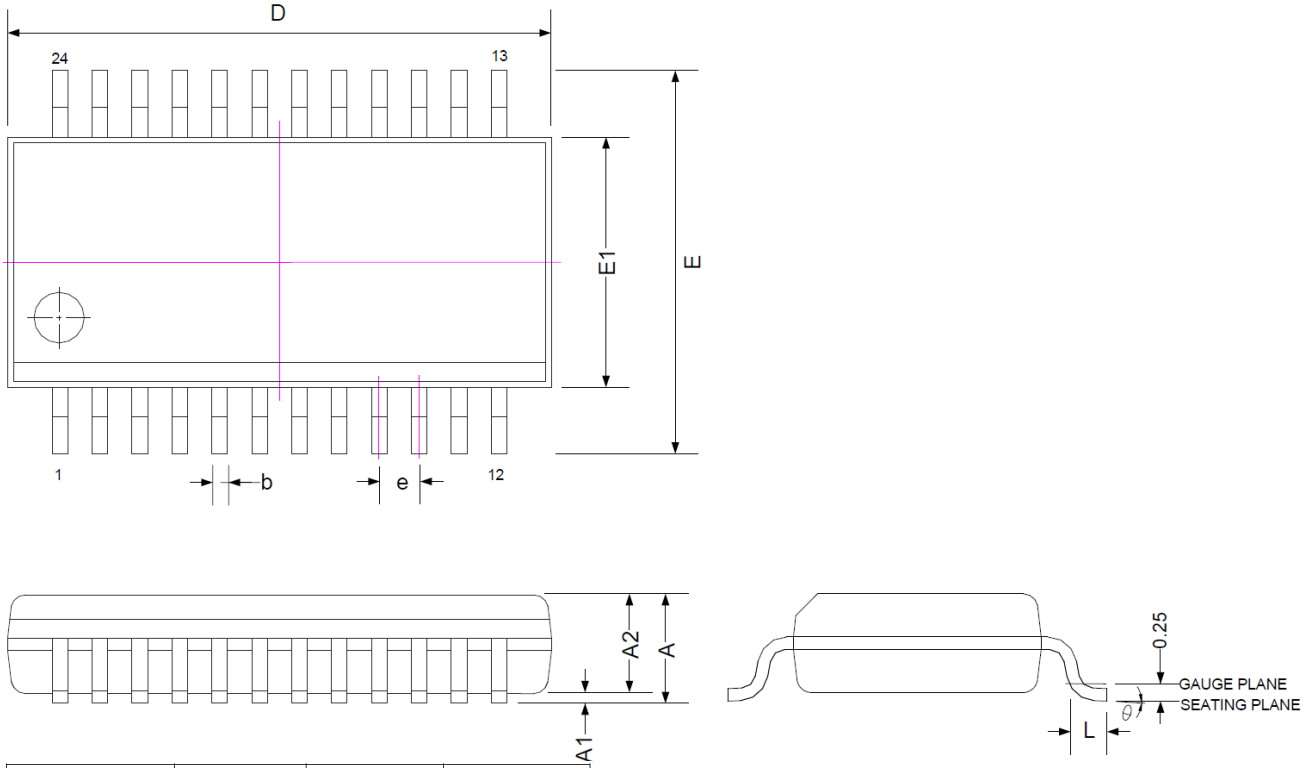
Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

8.2.3.3. Pin1 direction



8.3. SSOP24(ES24)

8.3.1. Package Dimensions SSOP24(150mil)

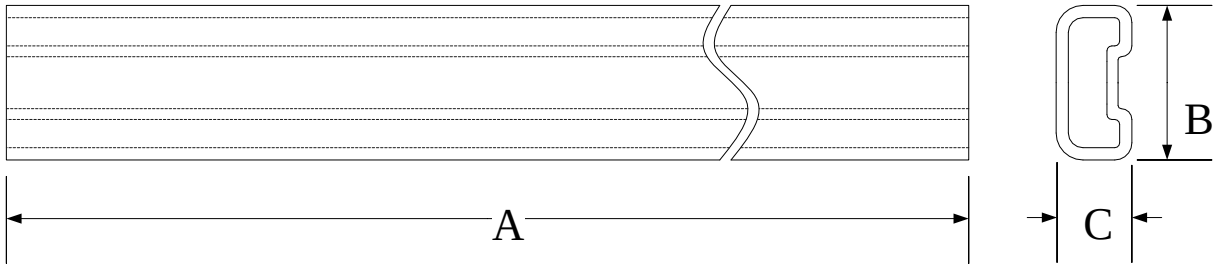


SYMBOLS	MIN	NOM	MAX
A	1.34	1.63	1.75
A1	0.10	0.15	0.25
A2	-	-	1.50
b	0.20	-	0.30
c	0.18	-	0.25
D	8.55	8.66	8.74
E1	3.81	3.91	3.99
E	5.79	5.99	6.20
L	0.41	0.64	1.27
e	0.635 BASIC		
θ°	0	-	8

Note:
1. All dimensions refer to JEDEC OUTLINE MS-137.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

8.3.2. Tube Dimensions SSOP24(150mil)

Unit : mm

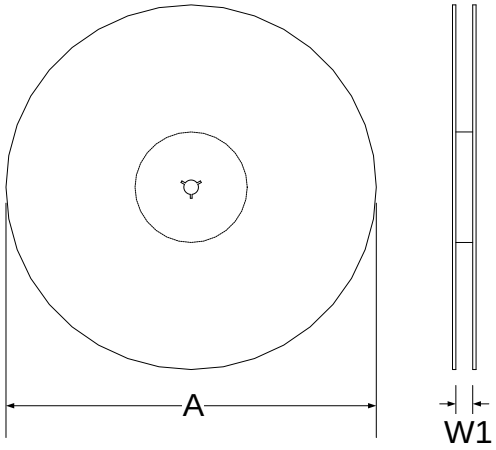


SYMBOLS	A	B	C
Spec.	529.6±1.0	8.001±0.127	3.937±0.127

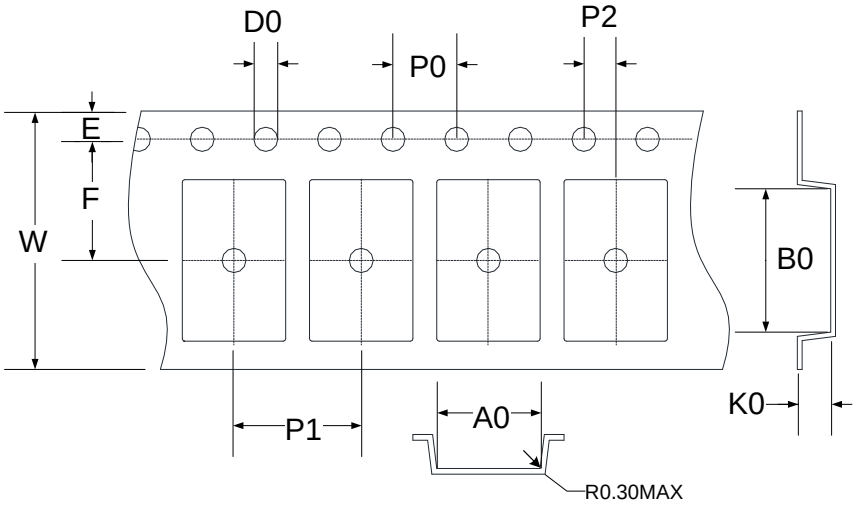
8.3.3. Tape & Reel Information

8.3.3.1. Reel Dimensions

Unit: mm



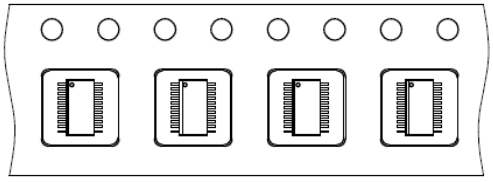
8.3.3.2. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	16.5	6.50	9.50	2.10	4.00	8.00	2.00	1.75	7.50	1.50	16.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.10	+0.1/-0	±0.30

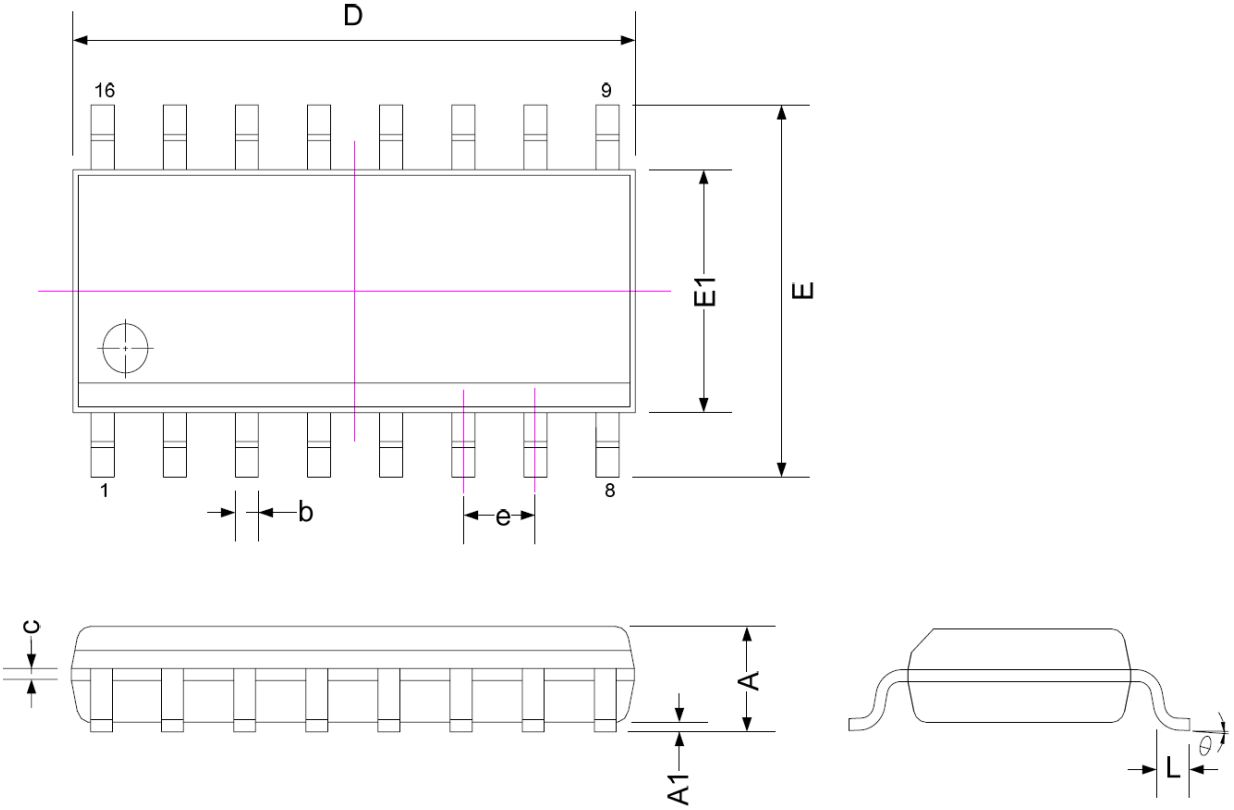
Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

8.3.3.3. Pin1 direction



8.4. SOP16(S016)

8.4.1. Package Dimensions SOP16(150mil)

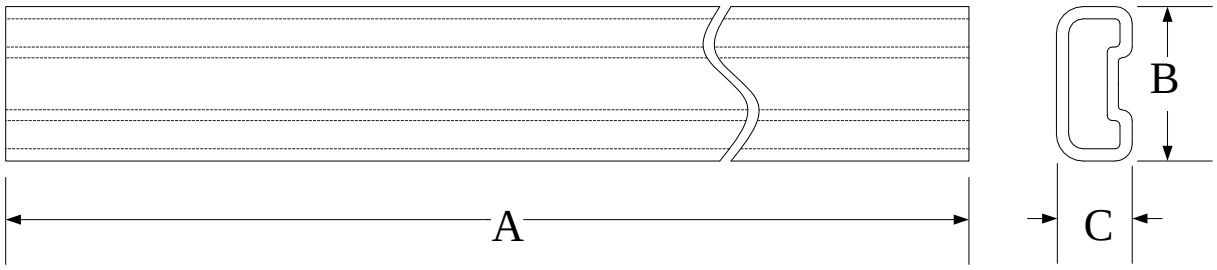


SYMBOLS	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	-	0.25
b	0.31	-	0.51
c	0.10	-	0.25
D	9.90 BASIC		
E1	3.90 BASIC		
E	6.00 BASIC		
L	0.40	-	1.27
e	1.27 BASIC		
θ	0	-	8

Note:
1. All dimensions refer to JEDEC OUTLINE MS-012.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

8.4.2. Tube Dimensions SOP16(150mil)

Unit : mm



Type 1:

SYMBOLS	A	B	C
Spec.	521.0±1.0	7.747±0.15	3.810±0.15

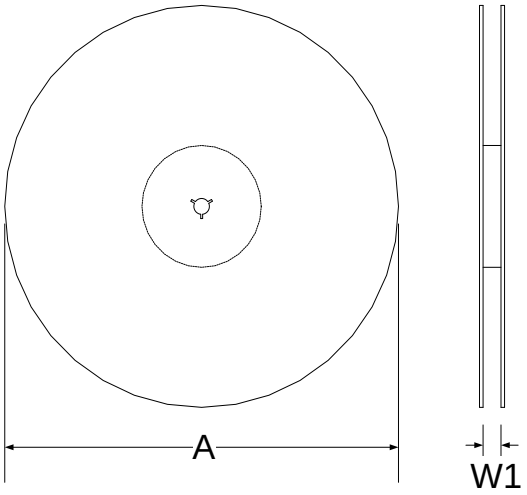
Type 2:

SYMBOLS	A	B	C
Spec.	521.0±1.0	7.874 REF.	3.810 REF.

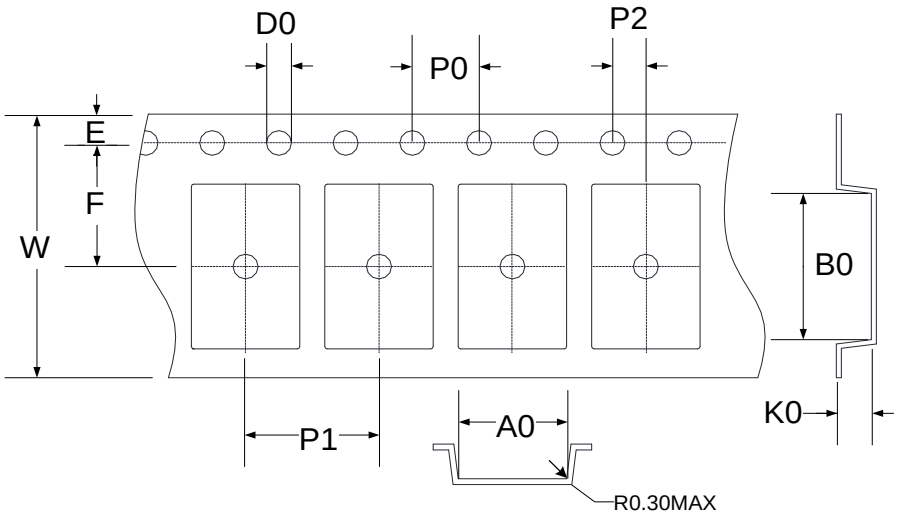
8.4.3. Tape & Reel Information

8.4.3.1. Reel Dimensions-Type1

Unit : mm



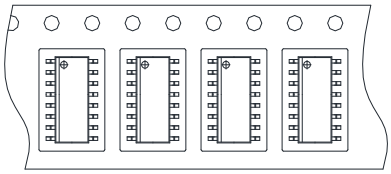
8.4.3.2. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	16.5	6.50	10.30	2.10	4.00	8.00	2.00	1.75	7.50	1.50	16.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.10	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

8.4.3.3. Pin1 direction



9. 修訂記錄

以下描述本文件差異較大的地方，而標點符號與字形的改變不在此描述範圍。

文件版次	頁次	日期	摘要
V01	All	2019/07/02	初版發行
V02	21 27-30	2020/05/08	修改 ADC 網路配置 修改暫存器列表
V03	6、30 20 42	2021/09/30	修改數位電路最低工作電壓 修改 4.6 圖片 修改 SD18 ENOB and RMS Noise Table
V04	All	2022/04/08	1. LPO 中心值規格從 15kHz 修正為 14.5kHz(+/-20%) 2. MCLR 的 Reset release voltage 從 1.6V 修正為 2V 3. BOR2 規格上下限範圍修正為+/-10% 4. 暫存器總列表修正. 5. POWER 的 REFO output with load 規格修正為 0.95~1.05V 6. 訂貨資訊章節, 修正 HY17M24-ES24 與 HY17M24-ES28 的描述方式, 移除 Die 出貨資訊.
V05	6 35 48	2022/09/16	1.新增選型功能列表 2.V_{OH} 最小值修改為 VDD-0.5V 3.修改 6.14 章節名稱與內容
V06	All	2023/01/31	1. 修改 MTP/EEPROM 的燒錄次數 修改前 MTP 燒錄次數 1K 次, 修改後 MTP 燒錄次數 100 次, 修改前 EEPROM 燒錄次數 30K 次, 修改後 EEPROM 燒錄次數 3K 次. 2. 修改 BOR1 的 current Typ.數值為 0.1uA. 3. 修改 BOR1 的 temperature drift Typ.數值為 15%