HYCON 紘康科技

HY16F3913
Datasheet

高精密混合信号处理控制器

4X44 ~ 8X40 LCD Driver

32-bit 低功耗微控制器

21-bit ENOB ΣΔADC

128KB Flash ROM

AC Impedance Converter AFE

目录

注意：

1、 本说明书中的内容，随着产品的改进，有可能不经过预告而更改。请客户及时到本公司网站下载更新 http://www.hycontek.com。

2、 本规格书中的图形、应用电路等，因第三方工业所有权引发的问题，本公司不承担其责任。

3、 本产品在单独应用的情况下，本公司保证它的性能、典型应用和功能符合说明书中的条件。当使用在客户的产品或设备中，以上条件我们不作保证，建议客户做充分的评估和测试。

4、 请注意输入电压、输出电压、负载电流的使用条件，使 IC 内的功耗不超过封装的容许功耗。对于客户在超出说明书中规定额定值使用产品，即使是瞬间的使用，由此所造成的损失，本公司不承担任何责任。

5、 本产品虽内置防静电保护电路，但请不要施加超过保护电路性能的过大静电。

6、 本规格书中的产品，未经书面许可，不可使用在要求高可靠性的电路中。例如健康医疗器械、防灾器械、车辆器械、车载器械及航空器械等对人体产生影响的器械或装置，不得作为其部件使用。

7、 本公司一直致力于提高产品的质量和可靠度，但所有的半导体产品都有一定的失效概率，这些失效概率可能会导致一些人身事故、火灾事故等。当设计产品时，请充分留意冗余设计并采用安全指标，这样可以避免事故的发生。

8、 本规格书中内容，未经本公司许可，严禁用于其他目的之转载或复制。

1. 特性

数字特性

- 32-bit 1T Andes Core E801 内核
- 支援 AndesSight C IDE 开发环境指令集
- 宽工作电压 VDD5V: 2.0V ~ 5.5V.
- 工作温度-40 to 85℃
- 低功耗(Typical@VDD5V=3.3V)：
  - 待机模式：4.5uA@LSRC=32KHz
  - 休眠模式：1.8uA
- 128KB Flash ROM
  - Write/Erase 的周期次数为：100,000 次
  - Write/Read/Erase 的操作电压 ≧2.0V
  - 内建硬件 ISP 功能，可在线更新 Flash
- 8KB SRAM
- 16-bit Timer A, Timer B(两组), Timer C, WDT
- 16-bit PWM 控制器及讯号捕抓功能
- 硬件实现 I^2C/32-bit SPI/UART(两通道) 通讯界面
- 硬件实现时钟 RTC 万年历功能
- 高达 72 个可编程复用型 I/O
  - 最多 24 个通用型数字输出入埠
  - 最多 48 个可选择 LCD 埠或数字输出入埠
- 4x44 ~ 8x40 LCD 液晶驱动器
  - 1/3、1/4、1/5、1/6、1/8Duty
  - 1/3 及 1/4 Bias 选择
  - 支援 R Type 驱动方式
  - 内建 Charge Pump 稳压线路，可提供 6 段 VLCD 偏压，分别为 2.8V, 3.0V, 3.3V, 3.9V, 4.5V 及 5.0V

模拟特性

- 模拟工作电压 VDDA: 2.4V ~ 3.6V
- 内建低噪声 24-bit Σ ADC
  - ADC 支援 x1~x4 讯号放大
  - 内建低噪声放大器 x8,x16,x32 讯号放大
  - 输入参考讯号可解析至 65nVrms (Gain=128)
  - 最高转换率高达 15K sps
  - 低温飘系数与内置绝对温度传感(TPS)
- 外部高速晶震频率高达 16MHz
- 外部低速晶震低至 32768Hz
- 内建 RC 高速震荡器频率
  - 频率可达 4.147MHz 及 31.795MHz
  - CPU 执行速度最高可达 16MHz
- 内建 RC 低速震荡器频率低至 32KHz
- 电源模块
  - 内建四段可调整稳压电源(VDDA)
  - 1.2V 带隙参考电压(REFO)
- 多功能比较器 Comparator
  - 支援外部电压输入比较
  - 支援 15 段 LVD 低电压检测(2.0V~4.0V)
- 交流阻抗量测模拟前端 AFE 硬件
  - 内建 24-bit Σ ADC、两组 12-bit DAC、3 组 Rail-to-rail OPAM 等硬件
  - 电化学分析(Electrochemical analysis)
  - 生物阻抗分析模块(**B**ioelectrical **I**mpedance **A**nalysis **Module**)，功能如下:
    -AC waveform frequency: 122Hz~250KHz
    -Impendence Range: 1K ~ 1MΩ
    -Phase detector: 0~90°

Part No.	24-b ΣΔADC	Flash (byte)	SRAM (byte)	TPS	RTC	I/O	Timer (bit x ch.)	PWM (bit x ch.)	Serial Interface	LCD (com x seg)	Impedance Converter AFE	ISP Mode	BIA Module	Package
HY16F3913-L100	9-CH	128K	8K	Y	Y	22+ 48 *	16bit x 3	8bit x 4 16bit x 2	UART x2 32bits SPI I^2C	4x44 6x42 8x40	Y	Y	Y	LQFP100
HY16F3913-N088	5-CH	128K	8K	Y	Y	24+ 38 *	16bit x 3	8bit x 4 16bit x 2	UART x2 32bits SPI I^2C	4x34 6x32 8x30	Y	Y	Y	QFN88

*: LCD pin shared I/O

2. 引脚名称定义

2.1. HY16F3913 LQFP100 引脚图

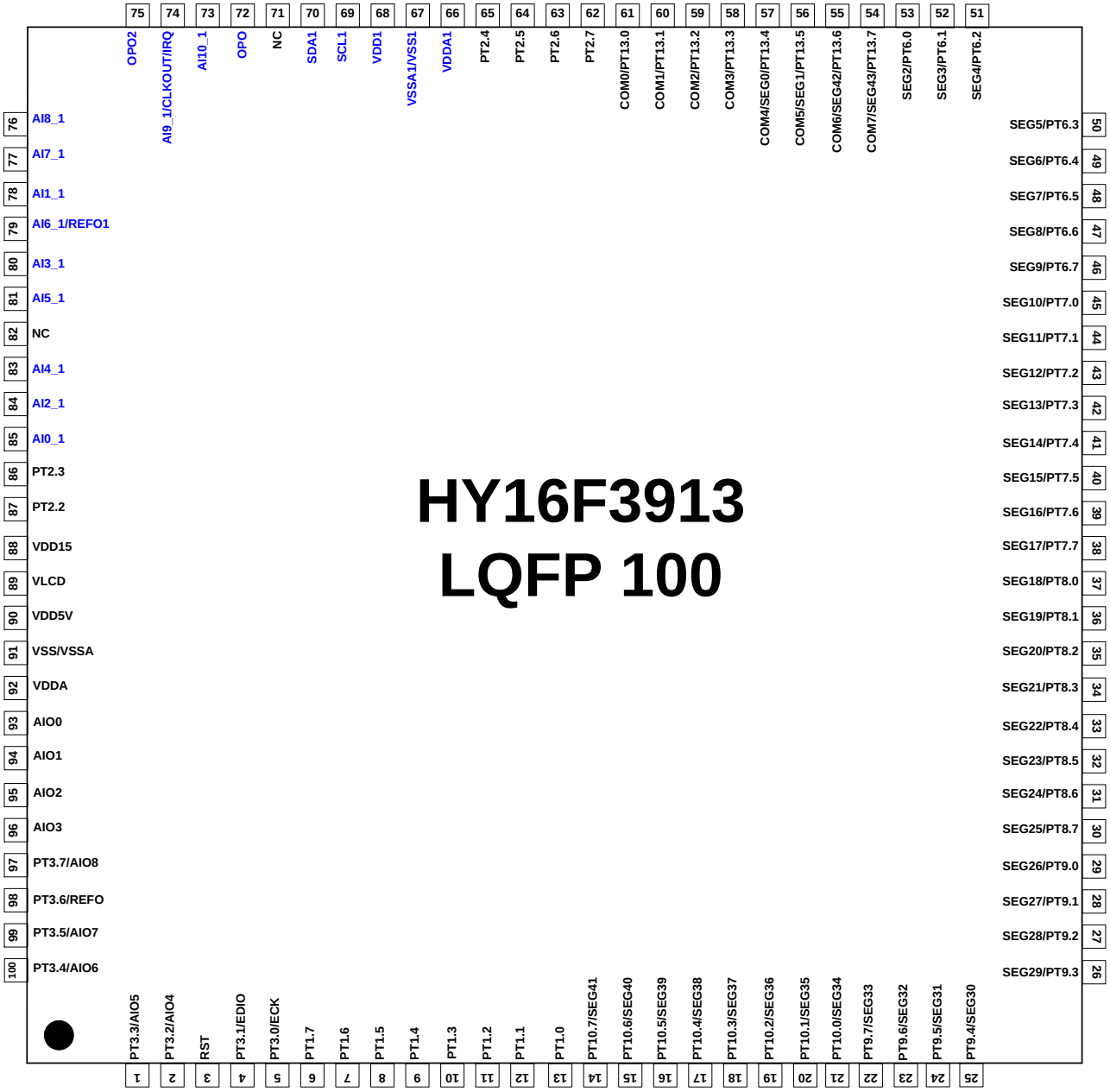


图 2-1 HY16F3913 LQFP100 引脚图

说明：脚位 66~85 属于**交流阻抗量测模拟前端**的相关引脚

2.2. HY16F3913 QFN88 引脚图

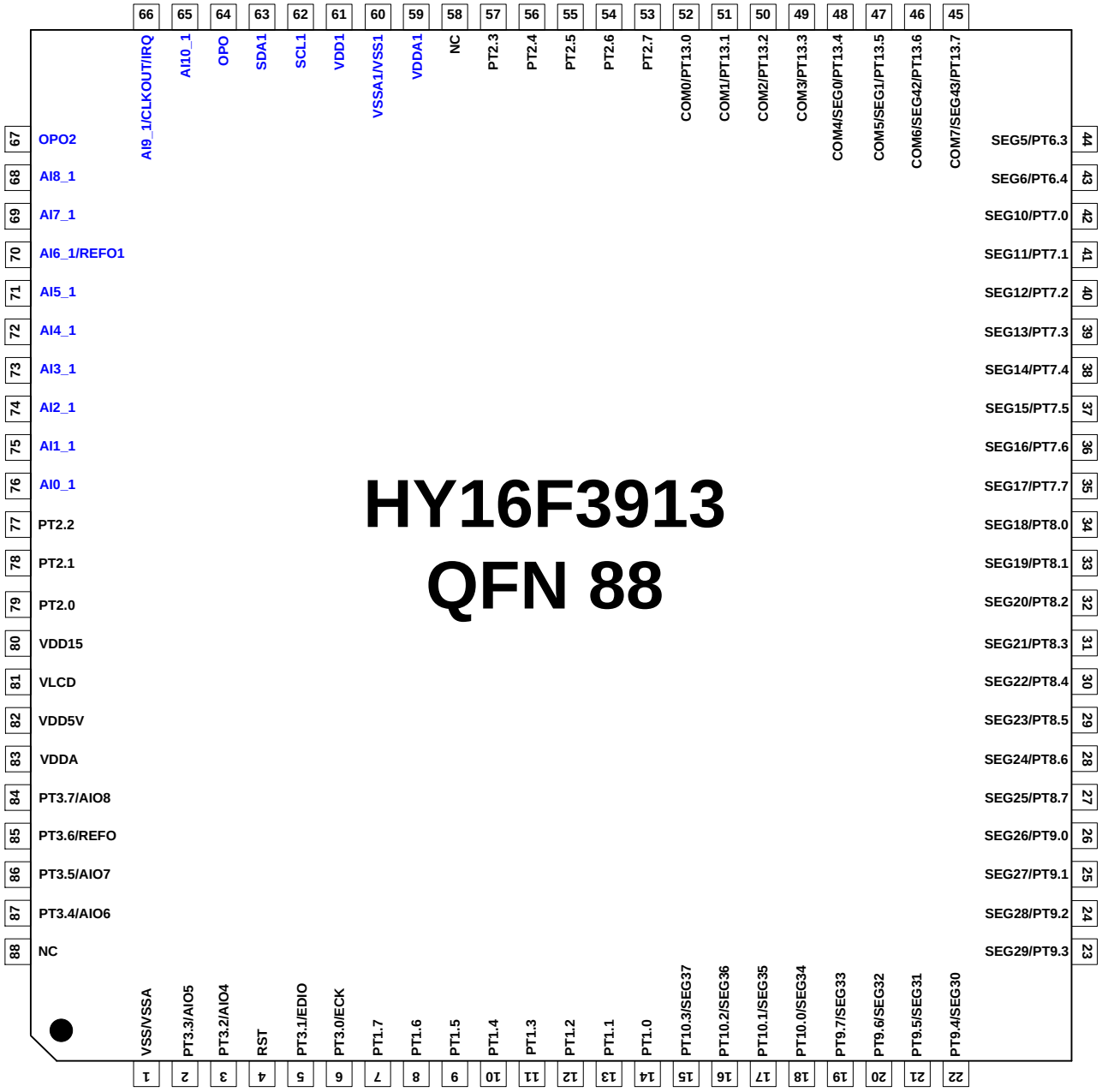


图 2-2 HY16F3913 QFN88 引脚图

说明：脚位 59~76 属于**交流阻抗量测模拟前端**的相关引脚

2.3. 引脚定义与功能描述

2.3.1. 引脚定义

"I"：Input ,"O"：Output, "A"：Analog, "S"： Smith triggers, "C"：CMOS I/O,"P"：Power Source,"/"：or ,"X"：Ignorable.

封装 / 引脚编号		引脚名称	特性		功能说明
LQFP100	QFN88		型态	缓冲	
1	2	PT3.3	I/O	S/C	通用数字输入/输出引脚
		INT3.3	I	S	外部中断源 INT3.3 输入引脚
		AIO5	I/O	A	ADC 模拟输入引脚 AIO5
2	3	PT3.2	I/O	S/C	通用数字输入/输出引脚
		INT3.2	I	S	外部中断源 INT3.2 输入引脚
		AIO4	I/O	A	ADC 模拟输入引脚 AIO4
3	4	RST	I	D	复位引脚(低电位有效) ，需外接 10nF 对地电容
4	5	PT3.1	I/O	S/C	通用数字输入/输出引脚
		INT3.1	I	S	外部中断源 INT3.1 输入引脚
		EDIO	I/O	D	开发调试通讯口(EDM)数据线输入/输出引脚，RST=L 时可动作
5	6	PT3.0	I/O	S/C	通用数字输入/输出引脚
		INT3.0	I	S	外部中断源 INT3.0 输入引脚
		ECK	I/O	D	开发调试通讯口(EDM)时钟线引脚，RST=L 时可动作
6	7	PT1.7	I/O	S/C	通用数字输入/输出引脚
		INT1.7	I	S	外部中断源 INT1.7 输入引脚
		PWM3_2	O	C	TimerB2, PWM3_2 输出引脚
		MOSI_2	O	C	SPI 通讯数据线引脚 MOSI_2(主机输出，从机输入)
		RX2_2	I	S	EUART2 通讯接收线引脚 RX2_2
		TCI2_4	I	S	捕捉比较器输入源引脚 TCI2_4
		SDA_4	I/O	S/C	I^2C 通讯数据线引脚 SDA_4
7	8	PT1.6	I/O	S/C	通用数字输入/输出引脚
		INT1.6	I	S	外部中断源 INT1.6 输入引脚
		PWM2_2	O	C	TimerB2, PWM2_2 输出引脚
		MISO_2	I	S	SPI 通讯数据线引脚 MISO_2(主机输入，从机输出)
		TX2_2	O	C	EUART2 通讯发送线引脚 TX2_2
		TCI1_4	I	S	捕捉比较器输入源引脚 TCI1_4
		SCL_4	I/O	S/C	I^2C 通讯时钟线引脚 SCL_4
8	9	PT1.5	I/O	S/C	通用数字输入/输出引脚
		INT1.5	I	S	外部中断源 INT1.5 输入引脚
		PWM1_2	O	C	TimerB, PWM1_2 输出引脚
		CK_2	O	C	SPI 通讯时钟线引脚 CK_2

封装 / 引脚编号		引脚名称	特性		功能说明
LQFP100	QFN88		型态	缓冲	
		RX_2	I	S	EUART 通讯接收线引脚 RX_2
		TCI2_3	I	S	捕捉比较器输入源引脚 TCI2_3
		SDA_3	I/O	S/C	I²C 通讯数据线引脚 SDA_3
		PT1.4	I/O	S/C	通用数字输入/输出引脚
		INT1.4	I	S	外部中断源 INT1.4 输入引脚
		PWM0_2	O	C	TimerB, PWM0_2 输出引脚
9	10	CS_2	I	S	SPI 通讯使能引脚 CS_2
		TX_2	O	C	EUART 通讯发送线引脚 TX_2
		TCI1_3	I	S	捕捉比较器输入源引脚 TCI1_3
		SCL_3	I/O	S/C	I²C 通讯时钟线引脚 SCL_3
		PT1.3	I/O	S/C	通用数字输入/输出引脚
		INT1.3	I	S	外部中断源 INT1.3 输入引脚
		PWM3_1	O	C	TimerB2, PWM3_1 输出引脚
10	11	MOSI_1	O	C	SPI 通讯数据线引脚 MOSI_1(主机输出，从机输入)
		RX2_1	I	S	EUART2 通讯接收线引脚 RX2_1
		TCI2_2	I	S	捕捉比较器输入源引脚 TCI2_2
		SDA_2	I/O	S/C	I²C 通讯数据线引脚 SDA_2
		PT1.2	I/O	S/C	通用数字输入/输出引脚
		INT1.2	I	S	外部中断源 INT1.2 输入引脚
		PWM2_1	O	C	TimerB2, PWM2_1 输出引脚
11	12	MISO_1	I	S	SPI 通讯数据线引脚 MISO_1(主机输入，从机输出)
		TX2_1	O	C	EUART2 通讯发送线引脚 TX2_1
		TCI1_2	I	S	捕捉比较器输入源引脚 TCI1_2
		SCL_2	I/O	S/C	I²C 通讯时钟线引脚 SCL_2
		PT1.1	I/O	S/C	通用数字输入/输出引脚
		INT1.1	I	S	外部中断源 INT1.1 输入引脚
		PWM1_1	O	C	TimerB, PWM1_1 输出引脚
12	13	CK_1	O	C	SPI 通讯时钟线引脚 CK_1
		RX_1	I	S	EUART 通讯接收线引脚 RX_1
		TCI2_1	I	S	捕捉比较器输入源引脚 TCI2_1
		SDA_1	I/O	S/C	I²C 通讯数据线引脚 SDA_1
		PT1.0	I/O	S/C	通用数字输入/输出引脚
		INT1.0	I	S	外部中断源 INT1.0 输入引脚
13	14	PWM0_1	O	C	TimerB, PWM0_1 输出引脚
		CS_1	I	S	SPI 通讯使能引脚 CS_1
		TX_1	O	C	EUART 通讯发送线引脚 TX_1

封装 / 引脚编号		引脚名称	特性		功能说明
LQFP100	QFN88		型态	缓冲	
		TCI1_1	I	S	捕捉比较器输入源引脚 TCI1_1
		SCL_1	I/O	S/C	I^2C 通讯时钟线引脚 SCL_1
14	-	PT10.7	I/O	S/C	通用数字输入/输出引脚
		SEG41	O	A	LCD Segment 41 输出
15	-	PT10.6	I/O	S/C	通用数字输入/输出引脚
		SEG40	O	A	LCD Segment 40 输出
		TCI3_8	I	S	TimerB2 输入源引脚 TCI3_8
16	-	PT10.5	I/O	S/C	通用数字输入/输出引脚
		SEG39	O	A	LCD Segment 39 输出
17	-	PT10.4	I/O	S/C	通用数字输入/输出引脚
		SEG38	O	A	LCD Segment 38 输出
		TCI3_7	I	S	TimerB2 输入源引脚 TCI3_7
18	15	PT10.3	I/O	S/C	通用数字输入/输出引脚
		SEG37	O	A	LCD Segment 37 输出
19	16	PT10.2	I/O	S/C	通用数字输入/输出引脚
		SEG36	O	A	LCD Segment 36 输出
20	17	PT10.1	I/O	S/C	通用数字输入/输出引脚
		SEG35	O	A	LCD Segment 35 输出
21	18	PT10.0	I/O	S/C	通用数字输入/输出引脚
		SEG34	O	A	LCD Segment 34 输出
22	19	PT9.7	I/O	S/C	通用数字输入/输出引脚
		SEG33	O	A	LCD Segment 33 输出
23	20	PT9.6	I/O	S/C	通用数字输入/输出引脚
		SEG32	O	A	LCD Segment 32 输出
24	21	PT9.5	I/O	S/C	通用数字输入/输出引脚
		SEG31	O	A	LCD Segment 31 输出
25	22	PT9.4	I/O	S/C	通用数字输入/输出引脚
		SEG30	O	A	LCD Segment 30 输出
26	23	PT9.3	I/O	S/C	通用数字输入/输出引脚
		SEG29	O	A	LCD Segment 29 输出
		PWM3_7	O	C	TimerB2, PWM3_7 输出引脚
		MOSI_7	O	C	SPI 通讯数据线引脚 MOSI_7(主机输出，从机输入)
		RX2_7	I	S	EUART2 通讯接收线引脚 RX2_7
27	24	PT9.2	I/O	S/C	通用数字输入/输出引脚
		SEG28	I	S	LCD Segment 28 输出
		PWM2_7	O	C	TimerB2, PWM2_7 输出引脚

封装 / 引脚编号		引脚名称	特性		功能说明
LQFP100	QFN88		型态	缓冲	
		MISO_7	I	S	SPI 通讯数据线引脚 MISO_7(主机输入，从机输出)
		TX2_7	O	C	EUART2 通讯发送线引脚 TX2_7
		TCI3_6	I	S	TimerB2 输入源引脚 TCI3_6
28	25	PT9.1	I/O	S/C	通用数字输入/输出引脚
		SEG27	I	S	LCD Segment 27 输出
		PWM1_7	O	C	TimerB, PWM1_7 输出引脚
		CK_7	O	C	SPI 通讯时钟线引脚 CK_7
		RX_7	I	S	EUART 通讯接收线引脚 RX_7
29	26	PT9.0	I/O	S/C	通用数字输入/输出引脚
		SEG26	I	S	LCD Segment 26 输出
		PWM0_7	O	C	TimerB, PWM0_1 输出引脚
		CS_7	I	S	SPI 通讯使能引脚 CS_1
		TX_7	O	C	EUART 通讯发送线引脚 TX_1
		TCI3_5	I	S	TimerB2 输入源引脚 TCI3_5
30	27	PT8.7	I/O	S/C	通用数字输入/输出引脚
		SEG25	O	A	LCD Segment 25 输出
31	28	PT8.6	I/O	S/C	通用数字输入/输出引脚
		SEG24	O	A	LCD Segment 24 输出
32	29	PT8.5	I/O	S/C	通用数字输入/输出引脚
		SEG23	O	A	LCD Segment 23 输出
33	30	PT8.4	I/O	S/C	通用数字输入/输出引脚
		SEG22	O	A	LCD Segment 22 输出
34	31	PT8.3	I/O	S/C	通用数字输入/输出引脚
		SEG21	O	A	LCD Segment 21 输出
		PWM3_8	O	C	TimerB2, PWM3_8 输出引脚
		MOSI_8	O	C	SPI 通讯数据线引脚 MOSI_8(主机输出，从机输入)
		RX2_8	I	S	EUART2 通讯接收线引脚 RX2_8
35	32	PT8.2	I/O	S/C	通用数字输入/输出引脚
		SEG20	I	S	LCD Segment 20 输出
		PWM2_8	O	C	TimerB2, PWM2_8 输出引脚
		MISO_8	I	S	SPI 通讯数据线引脚 MISO_8(主机输入，从机输出)
		TX2_8	O	C	EUART2 通讯发送线引脚 TX2_8
36	33	PT8.1	I/O	S/C	通用数字输入/输出引脚
		SEG19	I	S	LCD Segment 19 输出
		PWM1_8	O	C	TimerB, PWM1_8 输出引脚
		CK_8	O	C	SPI 通讯时钟线引脚 CK_8

封装 / 引脚编号		引脚名称	特性		功能说明
LQFP100	QFN88		型态	缓冲	
		RX_8	I	S	EUART 通讯接收线引脚 RX_8
37	34	PT8.0	I/O	S/C	通用数字输入/输出引脚
		SEG18	I	S	LCD Segment 18 输出
		PWM0_8	O	C	TimerB, PWM0_8 输出引脚
		CS_8	I	S	SPI 通讯使能引脚 CS_8
		TX_8	O	C	EUART 通讯发送线引脚 TX_8
38	35	PT7.7	I/O	S/C	通用数字输入/输出引脚
		SEG17	O	A	LCD Segment 17 输出
		PWM3_6	O	C	TimerB2, PWM3_6 输出引脚
		MOSI_6	O	C	SPI 通讯数据线引脚 MOSI_6(主机输出，从机输入)
		RX2_6	I	S	EUART2 通讯接收线引脚 RX2_6
39	36	PT7.6	I/O	S/C	通用数字输入/输出引脚
		SEG16	I	S	LCD Segment 16 输出
		PWM2_6	O	C	TimerB2, PWM2_6 输出引脚
		MISO_6	I	S	SPI 通讯数据线引脚 MISO_6(主机输入，从机输出)
		TX2_6	O	C	EUART2 通讯发送线引脚 TX2_6
		TCI3_4	I	S	TimerB2 输入源引脚 TCI3_4
40	37	PT7.5	I/O	S/C	通用数字输入/输出引脚
		SEG15	O	A	LCD Segment 15 输出
		PWM1_6	O	C	TimerB, PWM1_6 输出引脚
		CK_6	O	C	SPI 通讯时钟线引脚 CK_6
		RC_6	I	S	EUART 通讯接收线引脚 RX_6
41	38	PT7.4	I/O	S/C	通用数字输入/输出引脚
		SEG14	O	A	LCD Segment 14 输出
		PWM0_6	O	C	TimerB, PWM0_6 输出引脚
		CS_6	O	C	SPI 通讯时钟线引脚 CS_6
		TX_6	I	S	EUART 通讯发送线引脚 TX_6
		TCI3_3	I	S	TimerB2 输入源引脚 TCI3_3
42	39	PT7.3	I/O	S/C	通用数字输入/输出引脚
		SEG13	O	A	LCD Segment 13 输出
43	40	PT7.2	I/O	S/C	通用数字输入/输出引脚
		SEG12	O	A	LCD Segment 12 输出
44	41	PT7.1	I/O	S/C	通用数字输入/输出引脚
		SEG11	O	A	LCD Segment 11 输出
45	42	PT7.0	I/O	S/C	通用数字输入/输出引脚
		SEG10	O	A	LCD Segment 10 输出

封装 / 引脚编号		引脚名称	特性		功能说明
LQFP100	QFN88		型态	缓冲	
46	-	PT6.7	I/O	S/C	通用数字输入/输出引脚
		SEG9	O	A	LCD Segment 9 输出
47	-	PT6.6	I/O	S/C	通用数字输入/输出引脚
		SEG8	O	A	LCD Segment 8 输出
48	-	PT6.5	I/O	S/C	通用数字输入/输出引脚
		SEG7	O	A	LCD Segment 7 输出
49	43	PT6.4	I/O	S/C	通用数字输入/输出引脚
		SEG6	O	A	LCD Segment 6 输出
50	44	PT6.3	I/O	S/C	通用数字输入/输出引脚
		SEG5	O	A	LCD Segment 5 输出
		PWM3_5	O	C	TimerB2, PWM3_5 输出引脚
		MOSI_5	O	C	SPI 通讯数据线引脚 MOSI_5(主机输出，从机输入)
		RX2_5	I	S	EUART2 通讯接收线引脚 RX2_5
51	-	PT6.2	I/O	S/C	通用数字输入/输出引脚
		SEG4	O	A	LCD Segment 4 输出
		PWM2_5	O	C	TimerB2, PWM2_5 输出引脚
		MISO_5	I	S	SPI 通讯数据线引脚 MISO_5(主机输入，从机输出)
		TX2_5	O	C	EUART2 通讯发送线引脚 TX2_5
		TCI3_2	I	S	TimerB2 输入源引脚 TCI3_2
52	-	PT6.1	I/O	S/C	通用数字输入/输出引脚
		SEG3	O	A	LCD Segment 3 输出
		PWM1_5	O	C	TimerB, PWM1_5 输出引脚
		CK_5	O	C	SPI 通讯时钟线引脚 CK_5
		RX_5	I	S	EUART 通讯接收线引脚 RX_5
53	-	PT6.0	I/O	S/C	通用数字输入/输出引脚
		SEG2	O	A	LCD Segment 2 输出
		PWM0_5	O	C	TimerB, PWM0_5 输出引脚
		CS_5	I	S	SPI 通讯使能引脚 CS_5
		TX_5	O	C	EUART 通讯发送线引脚 TX_5
		TCI3_1	I	S	TimerB2 输入源引脚 TCI3_1
54	45	PT13.7	I/O	S/C	通用数字输入/输出引脚
		SEG43	O	A	LCD Segment 43 输出
		COM7	O	A	LCD Common 7 输出
55	46	PT13.6	I/O	S/C	通用数字输入/输出引脚
		SEG42	O	A	LCD Segment 42 输出
		COM6	O	A	LCD Common 6 输出

封装 / 引脚编号		引脚名称	特性		功能说明
LQFP100	QFN88		型态	缓冲	
56	47	PT13.5	I/O	S/C	通用数字输入/输出引脚
		SEG1	O	A	LCD Segment 1 输出
		COM5	O	A	LCD Common 5 输出
57	48	PT13.4	I/O	S/C	通用数字输入/输出引脚
		SEG0	O	A	LCD Segment 0 输出
		COM4	O	A	LCD Common 4 输出
58	49	PT13.3	I/O	S/C	通用数字输入/输出引脚
		COM3	O	A	LCD Common 3 输出
59	50	PT13.2	I/O	S/C	通用数字输入/输出引脚
		COM2	O	A	LCD Common 2 输出
60	51	PT13.1	I/O	S/C	通用数字输入/输出引脚
		COM1	O	A	LCD Common 1 输出
61	52	PT13.0	I/O	S/C	通用数字输入/输出引脚
		COM0	O	A	LCD Common 0 输出
62	53	PT2.7	I/O	S/C	通用数字输入/输出引脚
		HS_XOUT	A	A	外部高速晶震 2~16MHz 输出引脚
		INT2.7	I	S	外部中断源 INT2.7 输入引脚
		PWM3_4	O	C	TimerB2, PWM3_4 输出引脚
		MOSI_4	O	C	SPI 通讯数据线引脚 MOSI_4(主机输出，从机输入)
		RX2_4	I	S	EUART2 通讯接收线引脚 RX2_4
		TCI2_8	I	S	捕捉比较器输入源引脚 TCI2_8
		SDA_8	I/O	S/C	I^2C 通讯数据线引脚 SDA_8
63	54	PT2.6	I/O	S/C	通用数字输入/输出引脚
		HS_XIN	A	A	外部高速晶震 2~16MHz 输入引脚
		INT2.6	I	S	外部中断源 INT2.6 输入引脚
		PWM2_4	O	C	TimerB2, PWM2_4 输出引脚
		MISO_4	I	S	SPI 通讯数据线引脚 MISO_4(主机输入，从机输出)
		TX2_4	O	C	EUART2 通讯发送线引脚 TX2_4
		TCI1_8	I	S	捕捉比较器输入源引脚 TCI1_8
		SCL_8	I/O	S/C	I^2C 通讯时钟线引脚 SCL_8
64	55	PT2.5	I/O	S/C	通用数字输入/输出引脚
		LS_XIN	A	A	外部低速晶震 32768Hz 输出引脚
		INT2.5	I	S	外部中断源 INT2.5 输入引脚
		PWM1_4	O	C	TimerB, PWM1_4 输出引脚
		CK_4	O	C	SPI 通讯时钟线引脚 CK_4
		RX_4	I	S	EUART 通讯接收线引脚 RX_4

封装 / 引脚编号		引脚名称	特性		功能说明
LQFP100	QFN88		型态	缓冲	
		TCI2_7	I	S	捕捉比较器输入源引脚 TCI2_7
		SDA_7	I/O	S/C	I^2C 通讯数据线引脚 SDA_7
65	56	PT2.4	I/O	S/C	通用数字输入/输出引脚
		LS_XOUT	A	A	外部低速晶震 32768Hz 输入引脚
		INT2.4	I	S	外部中断源 INT2.4 输入引脚
		PWM0_4	O	C	TimerB2, PWM0_4 输出引脚
		CS_4	O	C	SPI 通讯使能引脚 CS_4
		TX_4	O	C	EUART 通讯发送线引脚 TX_4
		TCI1_8	I	S	捕捉比较器输入源引脚 TCI1_7
		SCL_7	I/O	S/C	I^2C 通讯时钟线引脚 SCL_7
66	59	VDDA1	I/O	P	AFE 模拟电压源输入/输出端，需外接 1~10uF 对地电容
67	60	VSS1	I	P	AFE 数字接地端引脚
		VSSA1	I	P	AFE 模拟比接地端引脚
68	61	VDD1	I	P	AFE 芯片工作电源电压输入引脚 ，需外接 10uF 对地电容
69	62	SCL1	I/O	S/C	AFE 的 I^2C 通讯时钟线引脚 SCL1
70	63	SDA1	I/O	S/C	AFE 的 I^2C 通讯数据线引脚 SDA1
		IRQ*	O	C	AFE 的 ADC 中断状态输出(复用选择)
72	64	OPO	A	P	AFE 的 OPAMP2 状态输出脚 OPO
73	65	AI10_1	I	A	AFE 的 ADC 模拟输入引脚 AI10_1
74	66	AI9_1	I	A	AFE 的 ADC 模拟输入引脚 AI9_1
		CLKOUT	O	C	AFE 的内部 RC 震荡除频输出脚
		IRQ	O	C	AFE 的 ADC 中断状态输出
75	67	OPO2	A	P	AFE 的 OPAMP3 状态输出脚 OPO2
76	68	AI8_1	I	A	AFE 的 ADC 模拟输入引脚 AI8_1
77	69	AI7_1	I	A	AFE 的 ADC 模拟输入引脚 AI7_1
78	75	AI1_1	I	A	AFE 的 ADC 模拟输入引脚 AI1_1
79	70	AI6_1	I	A	AFE 的 ADC 模拟输入引脚 AI6_1
		REFO1	I/O	P	AFE 模拟参考电压 1.2V 输出引脚，需外接 0.1uF 对地电容
80	73	AI3_1	I	A	AFE 的 ADC 模拟输入引脚 AI3_1
81	71	AI5_1	I	A	AFE 的 ADC 模拟输入引脚 AI5_1
83	72	AI4_1	I	A	AFE 的 ADC 模拟输入引脚 AI4_1
84	74	AI2_1	I	A	AFE 的 ADC 模拟输入引脚 AI2_1
85	76	AI0_1	I	A	AFE 的 ADC 模拟输入引脚 AI0_1
86	57	PT2.3	I/O	S/C	通用数字输入/输出引脚
		INT2.3	I	S	外部中断源 INT2.3 输入引脚

封装 / 引脚编号		引脚名称	特性		功能说明
LQFP100	QFN88		型态	缓冲	
		LVDOO	O	C	低电压比较器 LVDO 状态输出引脚
		PWM3_3	O	C	TimerB2, PWM3_3 输出引脚
		MOSI_3	O	C	SPI 通讯数据线引脚 MOSI_3(主机输出，从机输入)
		RX2_3	I	S	EUART2 通讯接收线引脚 RX2_3
		TCI2_6	I	S	捕捉比较器输入源引脚 TCI2_6
		SDA_6	I/O	S/C	I^2C 通讯数据线引脚 SDA_6
		PT2.2	I/O	S/C	通用数字输入/输出引脚
		INT2.2	I	S	外部中断源 INT2.2 输入引脚
		PWM2_3	O	C	TimerB2, PWM2_3 输出引脚
87	77	MISO_3	I	S	SPI 通讯数据线引脚 MISO_3(主机输入，从机输出)
		TX2_3	O	C	EUART2 通讯发送线引脚 TX2_3
		TCI1_6	I	S	捕捉比较器输入源引脚 TCI1_6
		SCL_6	I/O	S/C	I^2C 通讯时钟线引脚 SCL_6
		PT2.1	I/O	S/C	通用数字输入/输出引脚
		INT2.1	I	S	外部中断源 INT2.1 输入引脚
		PWM1_3	O	C	TimerB, PWM1_3 输出引脚
-	78	CK_3	O	C	SPI 通讯时钟线引脚 CK_3
		RX_3	I	S	EUART 通讯接收线引脚 RX_3
		TCI2_5	I	S	捕捉比较器输入源引脚 TCI2_5
		SDA_5	I/O	S/C	I^2C 通讯数据线引脚 SDA_5
		PT2.0	I/O	S/C	通用数字输入/输出引脚
		INT2.0	I	S	外部中断源 INT2.0 输入引脚
		PWM0_3	O	C	TimerB2, PWM0_3 输出引脚
-	79	CS_3	O	C	SPI 通讯使能引脚 CS_3
		TX_3	O	C	EUART 通讯发送线引脚 TX_3
		TCI1_5	I	S	捕捉比较器输入源引脚 TCI1_5
		SCL_5	I/O	S/C	I^2C 通讯时钟线引脚 SCL_5
88	80	VDD15	I	P	芯片数字电路电源电压引脚，需外接 0.1uF 对地电容
89	81	VLCD	I/O	P	LCD 稳压电源输出/LCD 电源输入，需外接 10uF 对地电容
90	82	VDD5V	I	P	芯片工作电源电压输入引脚，需外接 0.1uF 对地滤波电容
91	1	VSS	I	P	数字接地端引脚
		VSSA	I	P	模拟比接地端引脚
92	83	VDDA	I/O	P	模拟电压源输入/输出端，需外接 1~10uF 对地电容
93	-	AIO0	I	A	ADC 模拟输入引脚 AIO0
94	-	AIO1	I	A	ADC 模拟输入引脚 AIO1
95	-	AIO2	I	A	ADC 模拟输入引脚 AIO2

封装 / 引脚编号		引脚名称	特性		功能说明
LQFP100	QFN88		型态	缓冲	
96	-	AIO3	I	A	ADC 模拟输入引脚 AIO3
97	84	PT3.7	I/O	S/C	通用数字输入/输出引脚
		INT3.7	I	S	外部中断源 INT3.7 输入引脚
		LVDIN	I	A	低电压比较器外部输入引脚 LVDIN
		AIO8	I	A	ADC 模拟输入引脚 AIO8
98	85	PT3.6	I/O	S/C	通用数字输入/输出引脚
		INT3.6	I	S	外部中断源 INT3.6 输入引脚
		REFO	I/O	P	模拟参考电压 1.2V 输出引脚，需外接 0.1uF 对地电容
99	86	PT3.5	I/O	S/C	通用数字输入/输出引脚
		INT3.5	I	S	外部中断源 INT3.5 输入引脚
		AIO7	I/O	A	ADC 模拟输入引脚 AIO7
100	87	PT3.4	I/O	S/C	通用数字输入/输出引脚
		INT3.4	I	S	外部中断源 INT3.4 输入引脚
		AIO6	I/O	A	ADC 模拟输入引脚 AIO6
71 & 82	58 & 88	NC	-	-	空脚，应用时空接即可

表 2-1 引脚定义及引脚功能描述

2.4. 引脚复用功能及复用功能优先级

Function	INT	GPIO	Timer C Capture	Special Function	SPI	I²C	UART	Analog	Timer B/B2 PWM
Output Priority	I/P	I/P	I/P	0	1	2	3	4	5
PT1.0	INT1.0	DIO	TCI1_1		CS_1	SCL_1	Tx_1		PWM0_1
PT1.1	INT1.1	DIO	TCI2_1		CK_1	SDA_1	Rx_1		PWM1_1
PT1.2	INT1.2	DIO	TCI1_2		MISO_1	SCL_2	Tx2_1		PWM2_1
PT1.3	INT1.3	DIO	TCI2_2		MOSI_1	SDA_2	Rx2_1		PWM3_1
PT1.4	INT1.4	DIO	TCI1_3		CS_2	SCL_3	Tx_2		PWM0_2
PT1.5	INT1.5	DIO	TCI2_3		CK_2	SDA_3	Rx_2		PWM1_2
PT1.6	INT1.6	DIO	TCI1_4		MISO_2	SCL_4	Tx2_2		PWM2_2
PT1.7	INT1.7	DIO	TCI2_4		MOSI_2	SDA_4	Rx2_2		PWM3_2
PT2.0	INT2.0	DIO	TCI1_5		CS_3	SCL_5	Tx_3		PWM0_3
PT2.1	INT2.1	DIO	TCI2_5		CK_3	SDA_5	Rx_3		PWM1_3
PT2.2	INT2.2	DIO	TCI1_6		MISO_3	SCL_6	Tx2_3		PWM2_3
PT2.3	INT2.3	DIO	TCI2_6	LVDOO	MOSI_3	SDA_6	Rx2_3		PWM3_3
PT2.4	INT2.4	DIO	TCI1_7	LS_XOUT	CS_4	SCL_7	Tx_4		PWM0_4
PT2.5	INT2.5	DIO	TCI2_7	LS_XIN	CK_4	SDA_7	Rx_4		PWM1_4
PT2.6	INT2.6	DIO	TCI1_8	HS_XIN	MISO_4	SCL_8	Tx2_4		PWM2_4
PT2.7	INT2.7	DIO	TCI2_8	HS_XOUT	MOSI_4	SDA_8	Rx2_4		PWM3_4
PT3.0	INT3.0	DIO		**ECK**					
PT3.1	INT3.1	DIO		**EDIO**					
PT3.2	INT3.2	DIOAI						AIO4	
PT3.3	INT3.3	DIOAI						AIO5	
PT3.4	INT3.4	DIOAI						AIO6	
PT3.5	INT3.5	DIOAI						AIO7	
PT3.6	INT3.6	DIOAIO						REFO	
PT3.7	INT3.7	DIOAI						AIO8/LVDIN	
AIO0		AI						AIO0	
AIO1		AI						AIO1	
AIO2		AI						AIO2	
AIO3		AI						AIO3	
PT13.0		DIOAO		COM 0					
PT13.1		DIOAO		COM 1					
PT13.2		DIOAO		COM 2					
PT13.3		DIOAO		COM 3					

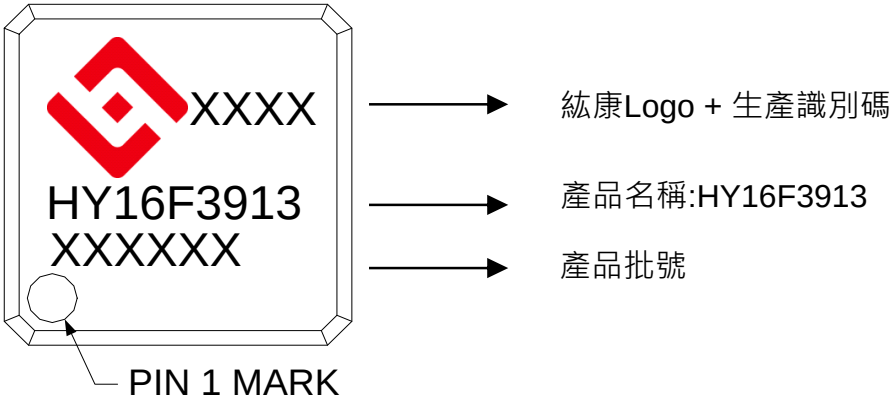
Function	INT	GPIO	Timer C Capture	Special Function	SPI	I²C	UART	Analog	Timer B/B2 PWM
Output Priority	I/P	I/P	I/P	0	1	2	3	4	5
PT13.4		DIOAO		COM 4/SEG 0					
PT13.5		DIOAO		COM 5/SEG 1					
PT13.6		DIOAO		COM 6/SEG 42					
PT13.7		DIOAO		COM 7/SEG 43					
PT6.0		DIOAO	TCI3_1	SEG 2	CS_5		Tx_5		PWM0_5
PT6.1		DIOAO		SEG 3	CK_5		Rx_5		PWM1_5
PT6.2		DIOAO	TCI3_2	SEG 4	MISO_5		Tx2_5		PWM2_5
PT6.3		DIOAO		SEG 5	MOSI_5		Rx2_5		PWM3_5
PT6.4		DIOAO		SEG 6					
PT6.5		DIOAO		SEG 7					
PT6.6		DIOAO		SEG 8					
PT6.7		DIOAO		SEG 9					
PT7.0		DIOAO		SEG 10					
PT7.1		DIOAO		SEG 11					
PT7.2		DIOAO		SEG 12					
PT7.3		DIOAO		SEG 13					
PT7.4		DIOAO	TCI3_3	SEG 14	CS_6		Tx_6		PWM0_6
PT7.5		DIOAO		SEG 15	CK_6		Rx_6		PWM1_6
PT7.6		DIOAO	TCI3_4	SEG 16	MISO_6		Tx2_6		PWM2_6
PT7.7		DIOAO		SEG 17	MOSI_6		Rx2_6		PWM3_6
PT8.0		DIOAO		SEG 18	CS_8		Tx_8		PWM0_8
PT8.1		DIOAO		SEG 19	CK_8		Rx_8		PWM1_8
PT8.2		DIOAO		SEG 20	MISO_8		Tx2_8		PWM2_8
PT8.3		DIOAO		SEG 21	MOSI_8		Rx2_8		PWM3_8
PT8.4		DIOAO		SEG 22					
PT8.5		DIOAO		SEG 23					
PT8.6		DIOAO		SEG 24					
PT8.7		DIOAO		SEG 25					
PT9.0		DIOAO	TCI3_5	SEG 26	CS_7		Tx_7		PWM0_7
PT9.1		DIOAO		SEG 27	CK_7		Rx_7		PWM1_7
PT9.2		DIOAO	TCI3_6	SEG 28	MISO_7		Tx2_7		PWM2_7
PT9.3		DIOAO		SEG 29	MOSI_7		Rx2_7		PWM3_7
PT9.4		DIOAO		SEG 30					
PT9.5		DIOAO		SEG 31					

Function	INT	GPIO	Timer C Capture	Special Function	SPI	I²C	UART	Analog	Timer B/B2 PWM
Output Priority	I/P	I/P	I/P	0	1	2	3	4	5
PT9.6		DIOAO		SEG 32					
PT9.7		DIOAO		SEG 33					
PT10.0		DIOAO		SEG 34					
PT10.1		DIOAO		SEG 35					
PT10.2		DIOAO		SEG 36					
PT10.3		DIOAO		SEG 37					
PT10.4		DIOAO	TCI3_7	SEG 38					
PT10.5		DIOAO		SEG 39					
PT10.6		DIOAO	TCI3_8	SEG 40					
PT10.7		DIOAO		SEG 41					

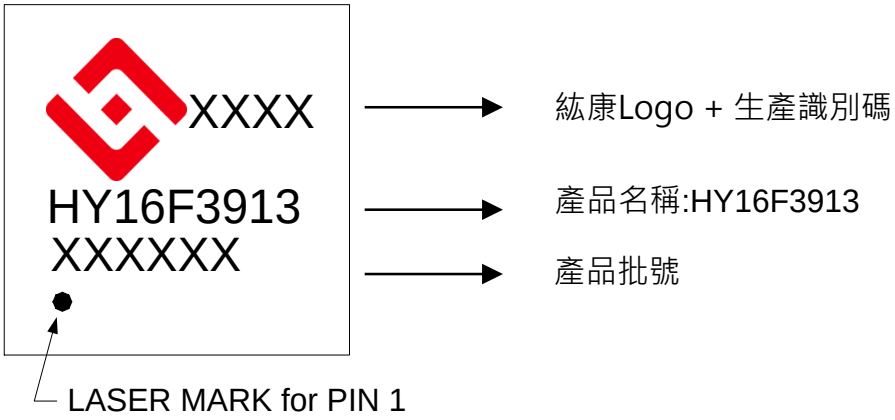
表 2-2 引脚复用功能及优先级描述

2.5. 封装片标记讯息

2.5.1. LQFP 封装片标记讯息



2.5.2. QFN 封装片标记讯息



3. 应用电路

3.1. HCT 血糖仪应用电路

※BIA Module 相关应用之详细资料请洽紘康科技联系窗口

4. 功能概述

4.1. 内部框图

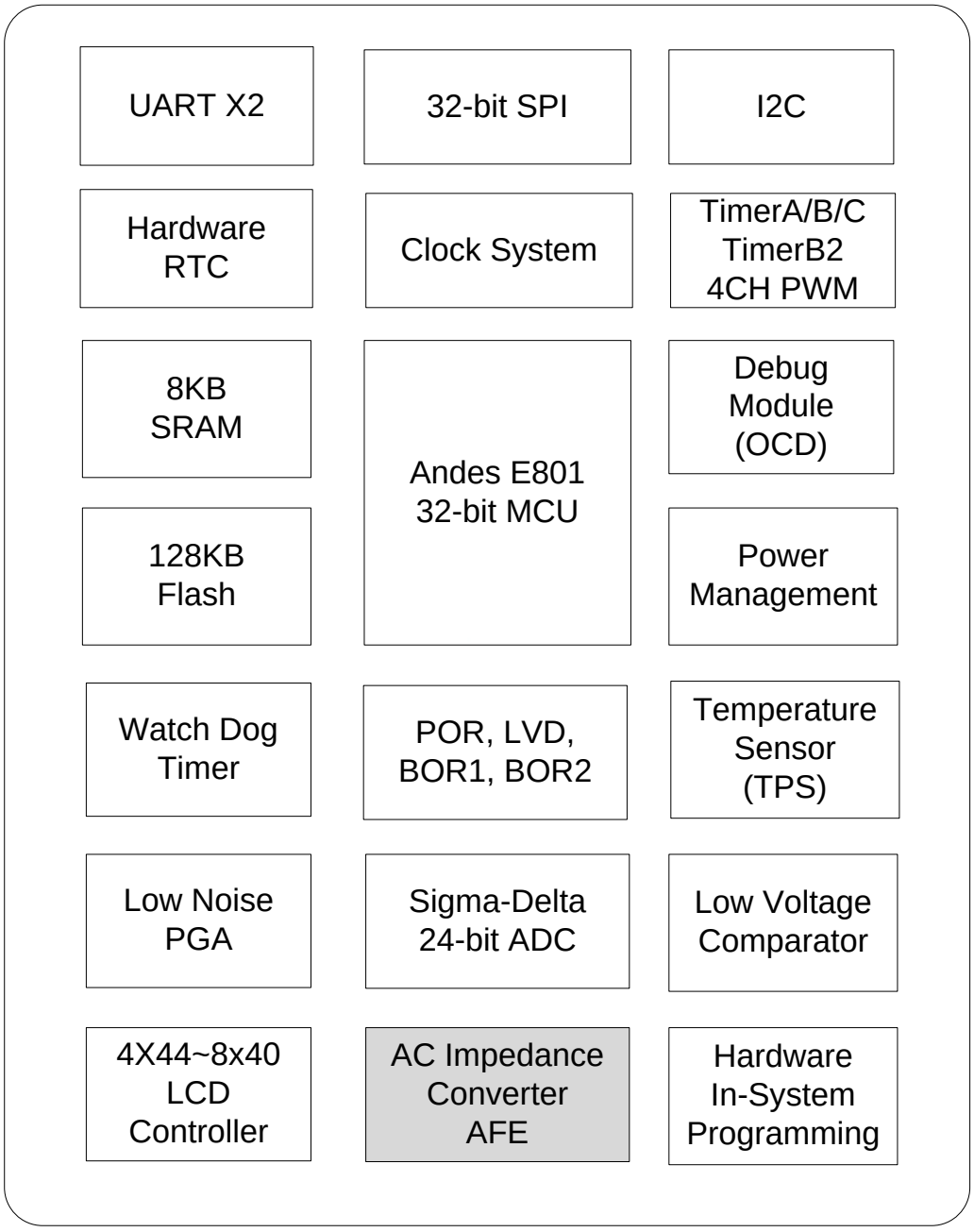


图4-1 HY16F3913 内部框图

4.2. 中央处理器核心方框图

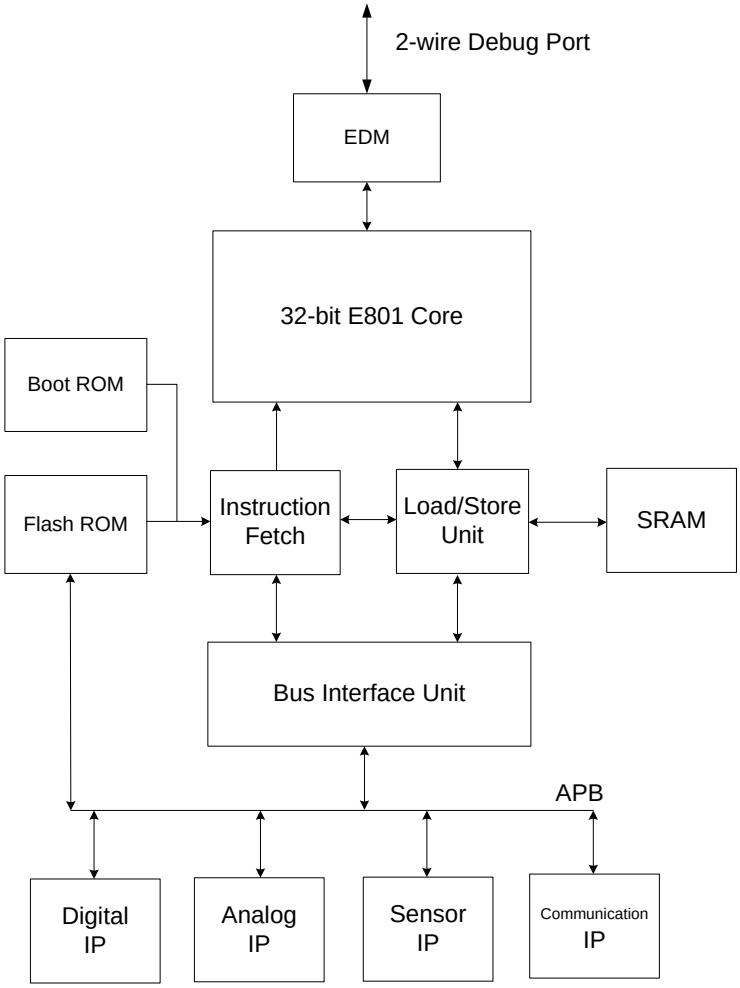


图4-2 中央处理器核心方框图

4.3. 相关的支援文档

文件名称	描述
DS-HY16F3913	HY16F3913 系列规格书
UG-HY16F3913	HY16F3913 系列用户手册
APD-HY16F39IDE0xx	HY16F3913 系列 C 函数库手册
APD-HY16F39IDE0xx	HY16F3913 系列各 IP 使用说明书
APD-HY16IDE030	AndeSight_RDS_V3xx IDE 软件使用说明书
APD-HY16F39IDE0xx	HY16F3913 系列开发工具硬件使用说明书
APD-HY16IDE006	HY16 系列烧录器软件使用说明书
APD-HYIDE020	HY10000-WK09 整合型烧录器硬件使用说明书

4.4. 时钟系统网络

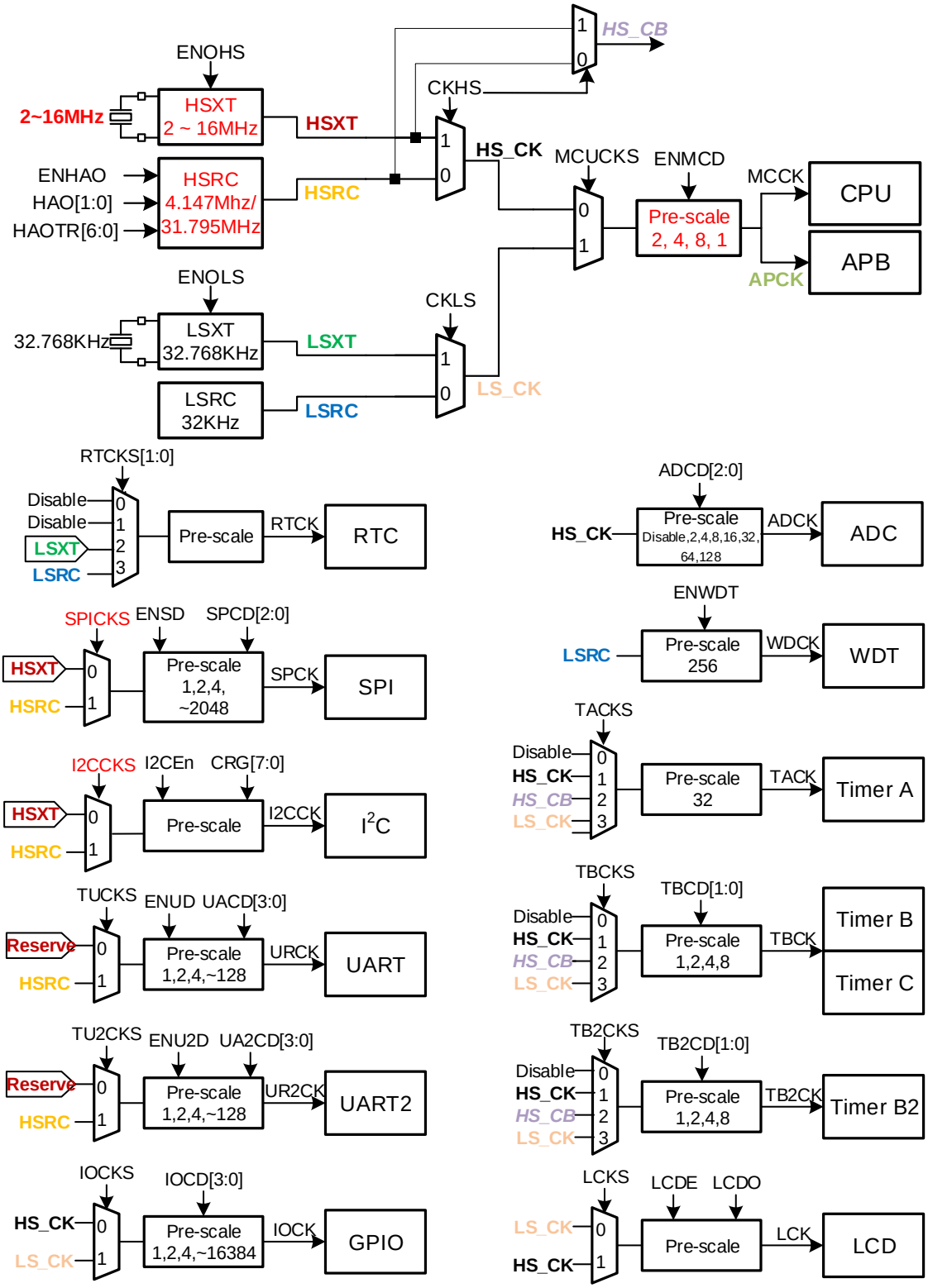


图 4-3 时钟系统网络方框图

4.5. 电源系统网络

4.5.1. MCU-电源系统网络

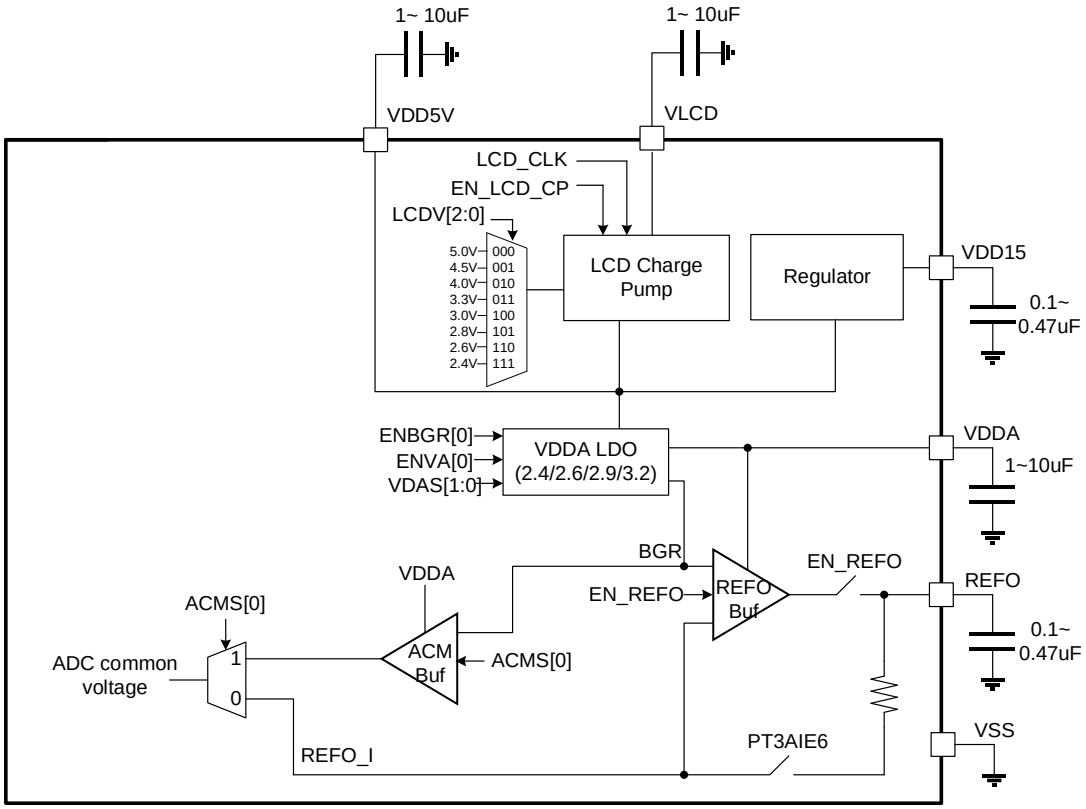


图4-4 MCU-电源系统网络方框图

4.5.2. 交流阻抗量测模拟前端-电源系统网络

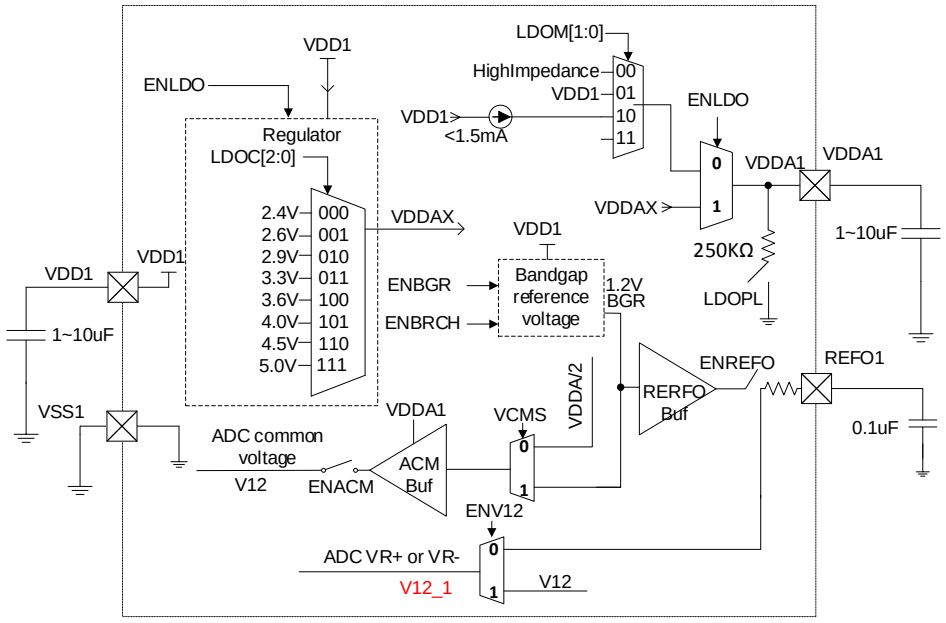


图4-5 AFE-电源系统网络方框图

4.6. 24-bit ΣΔADC 网络

4.6.1. MCU-24-bit ΣΔADC 网络

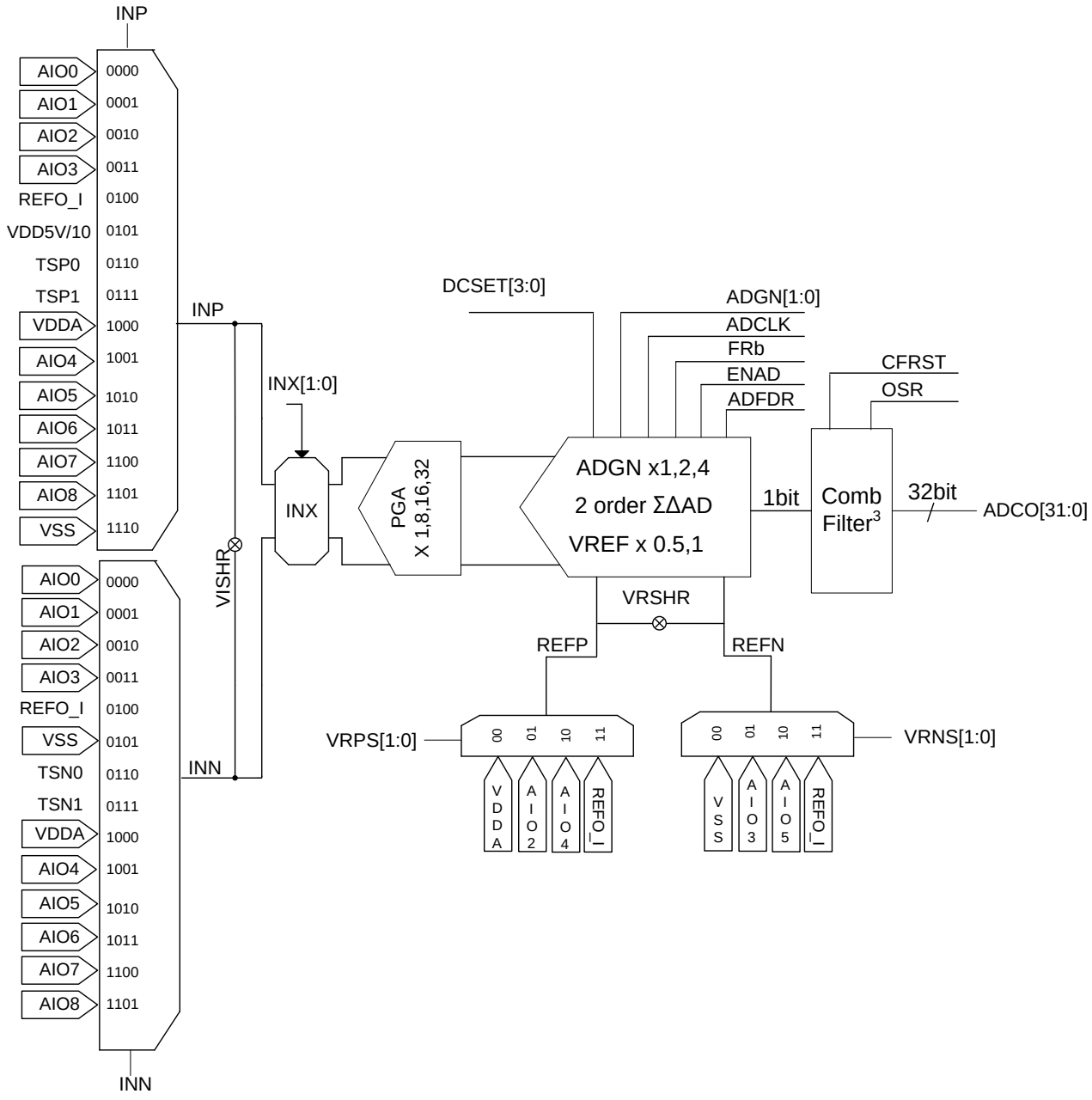


图4-6 MCU-24-bit ΣΔADC网络方框图

4.6.2. 交流阻抗量测模拟前端-24-bit ΣΔADC 网络

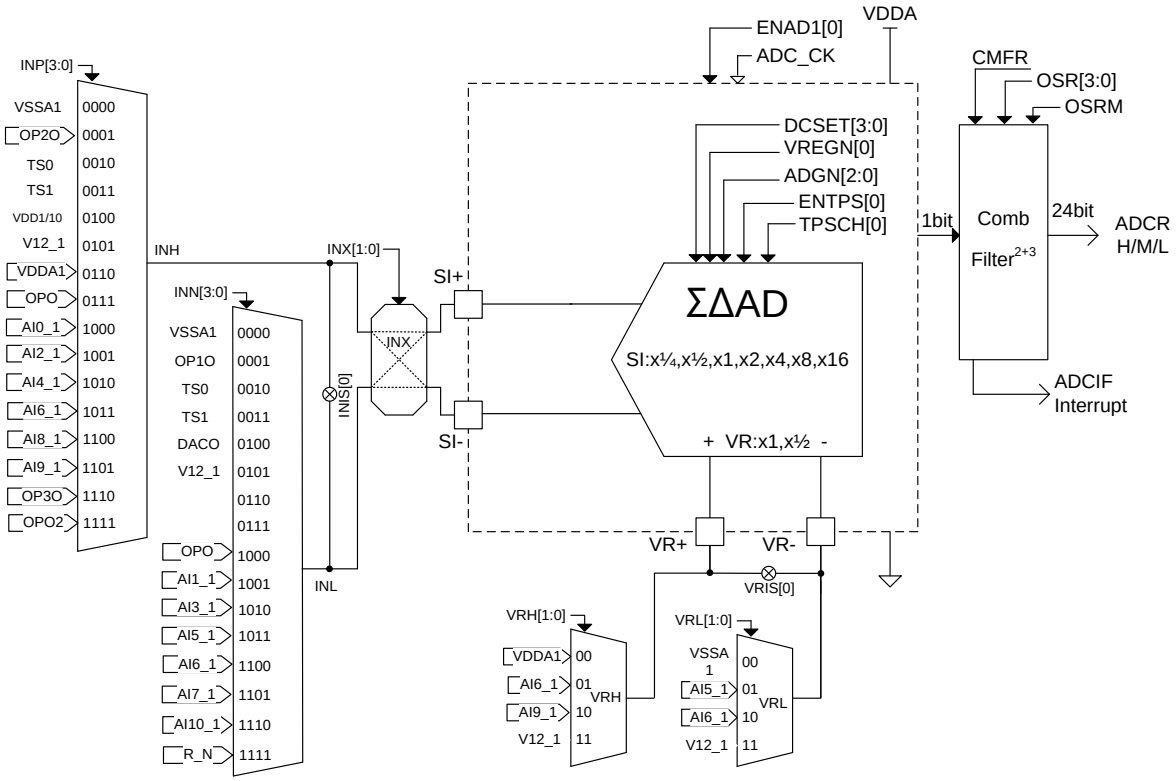


图4-7 AFE-24-bit ΣΔADC网络方框图

4.7. 低电压比较器网络

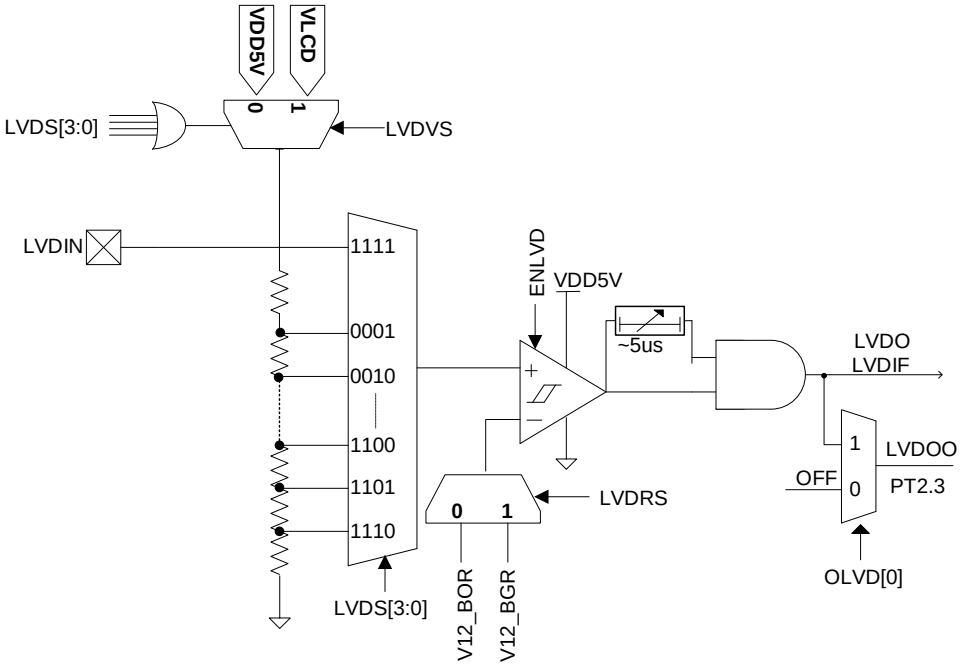
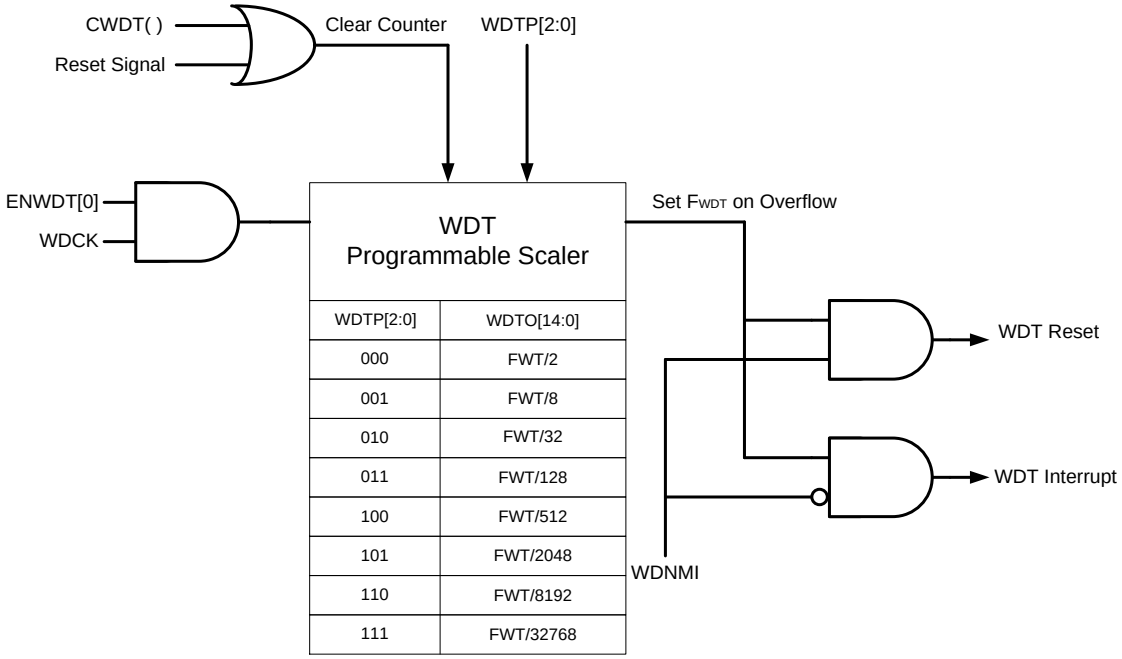


图4-8 低电压比较器网络方框图

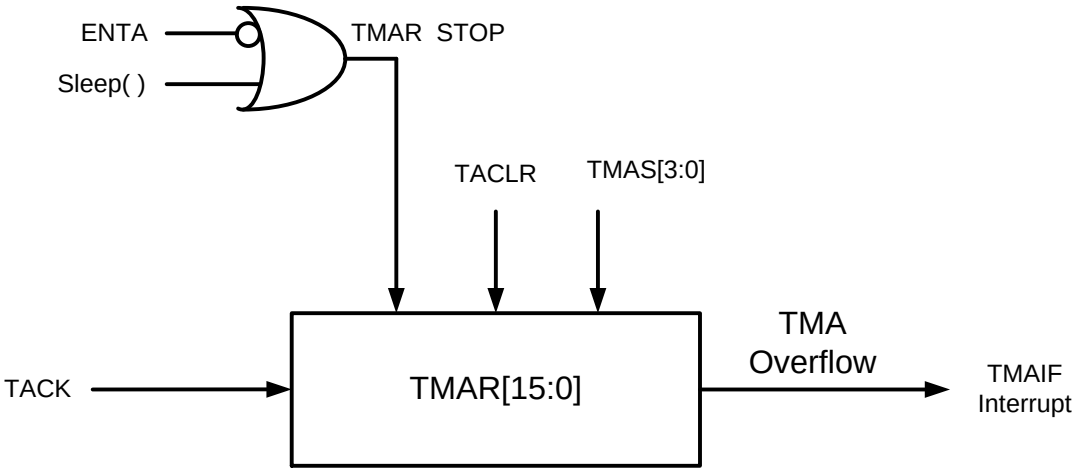
4.8. 看门狗(WDT)网络



WDTP[2:0]	WDTO[14:0]
000	FWT/2
001	FWT/8
010	FWT/32
011	FWT/128
100	FWT/512
101	FWT/2048
110	FWT/8192
111	FWT/32768

图4-9 看门狗(WDT)网络方框图

4.9. 定时计数器 A 网络



TMAS[3:0]	TMAR[15:0]	TMAS[3:0]	TMAR[15:0]
0000	TACK/2	1000	TACK/512
0001	TACK/4	1001	TACK/1024
0010	TACK/8	1010	TACK/2048
0011	TACK/16	1011	TACK/4096
0100	TACK/32	1100	TACK/8192
0101	TACK/64	1101	TACK/16384
0110	TACK/128	1110	TACK/32768
0111	TACK/256	1111	TACK/65536

图4-10 定时计数器A网络方框图

4.10. 定时计数器 B 网络

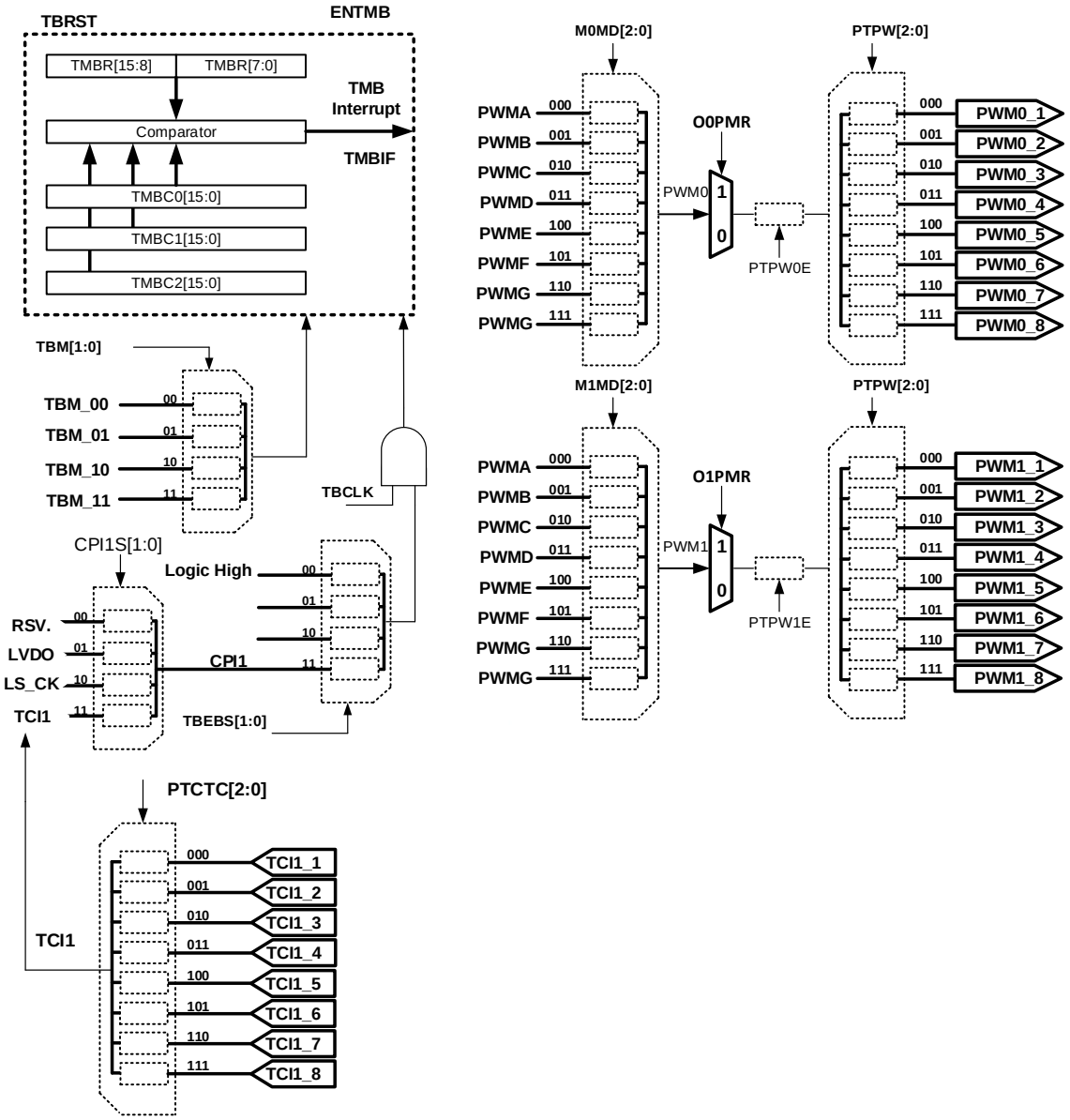
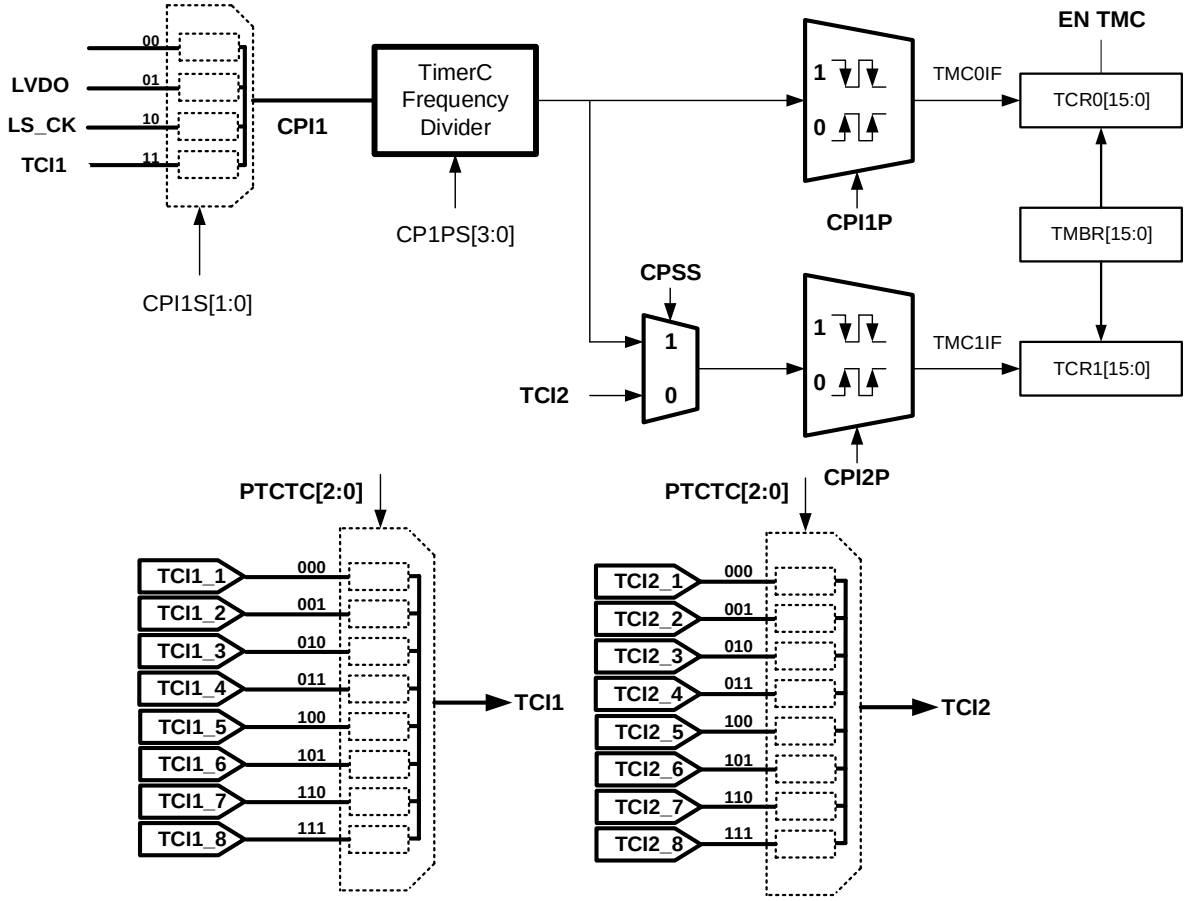


图4-11 定时计数器B网络方框图

4.11. 定时计数器 C 网络



CP1PS[3:0]	CPI1 Divider	CP1PS[3:0]	CPI1 Divider
0000	CPI1/1	1000	CPI1/256
0001	CPI1/2	1001	CPI1/512
0010	CPI1/4	1010	CPI1/1024
0011	CPI1/8	1011	CPI1/2048
0100	CPI1/16	1100	CPI1/4096
0101	CPI1/32	1101	CPI1/8192
0110	CPI1/64	1110	CPI1/16384
0111	CPI1/128	1111	CPI1/32768

图4-12 定时计数器C网络方框图

4.12. 定时计数器 B2 网络

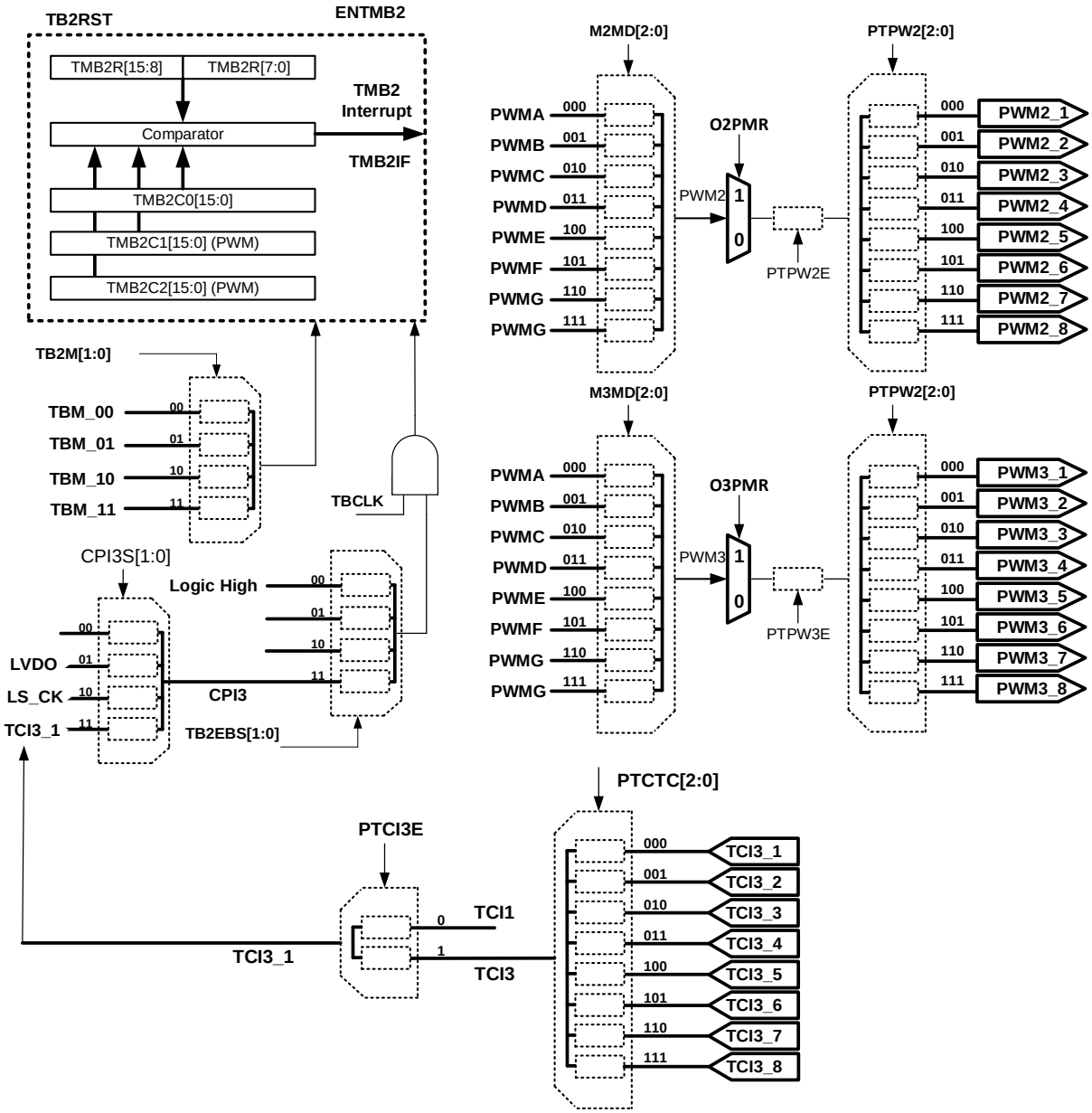


图4-13 定时计数器B2网络方框图

4.13. 32-bit SPI 网络

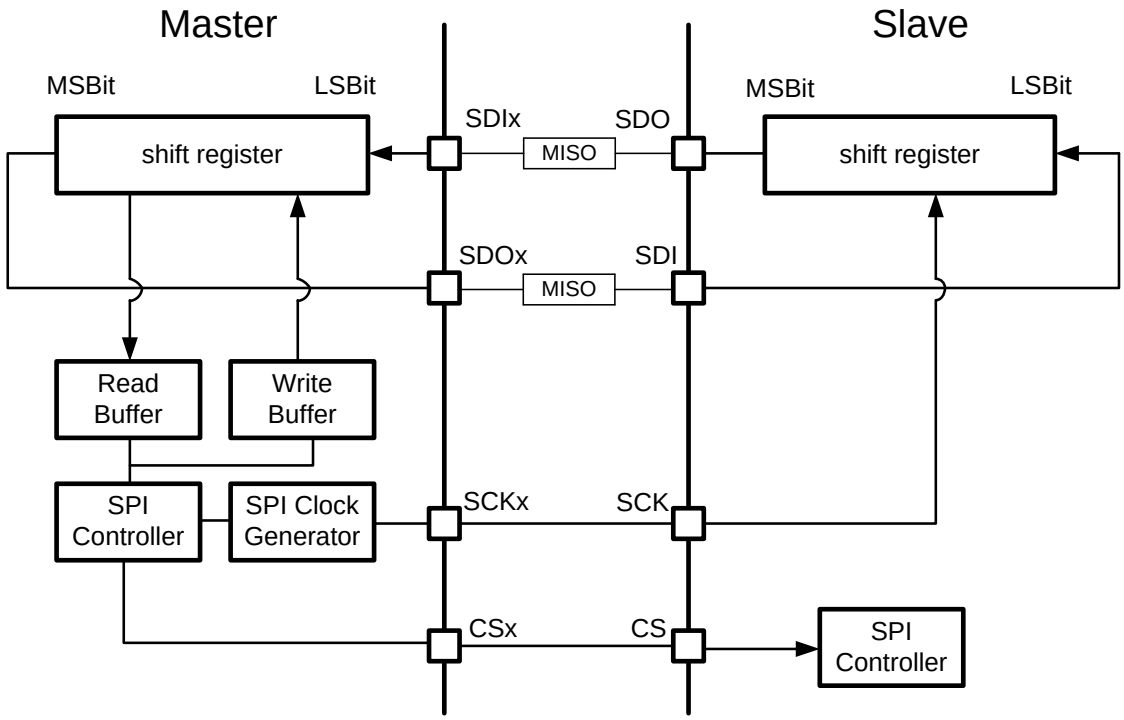


图4-13 32-bit SPI网络方框图

4.14. UART1/UART2 网络

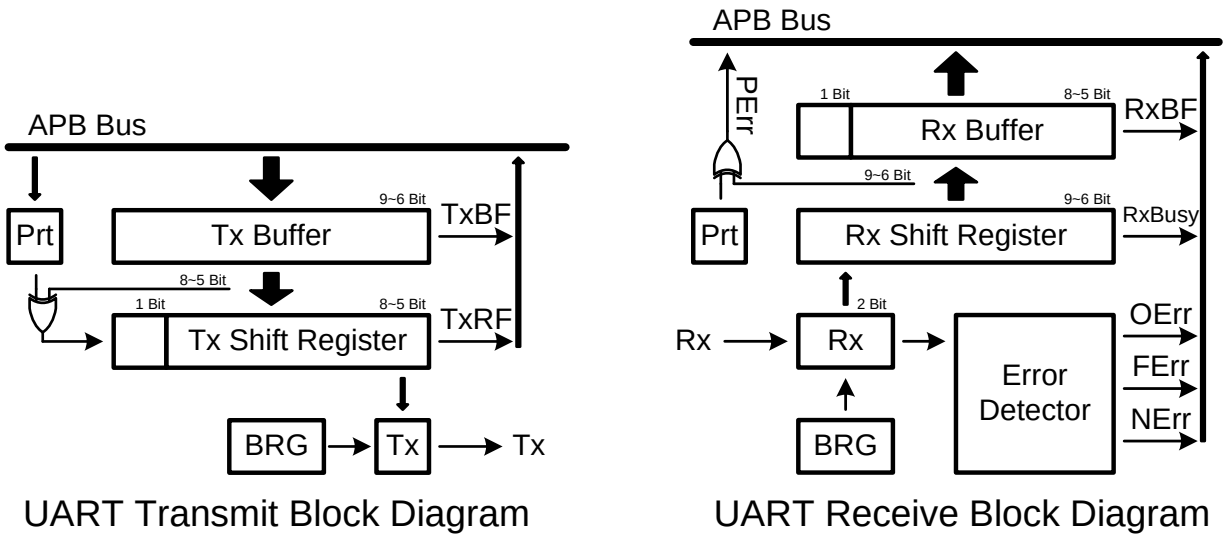


图4-14 UART1/UART2网络方框图

4.15. I²C 网络

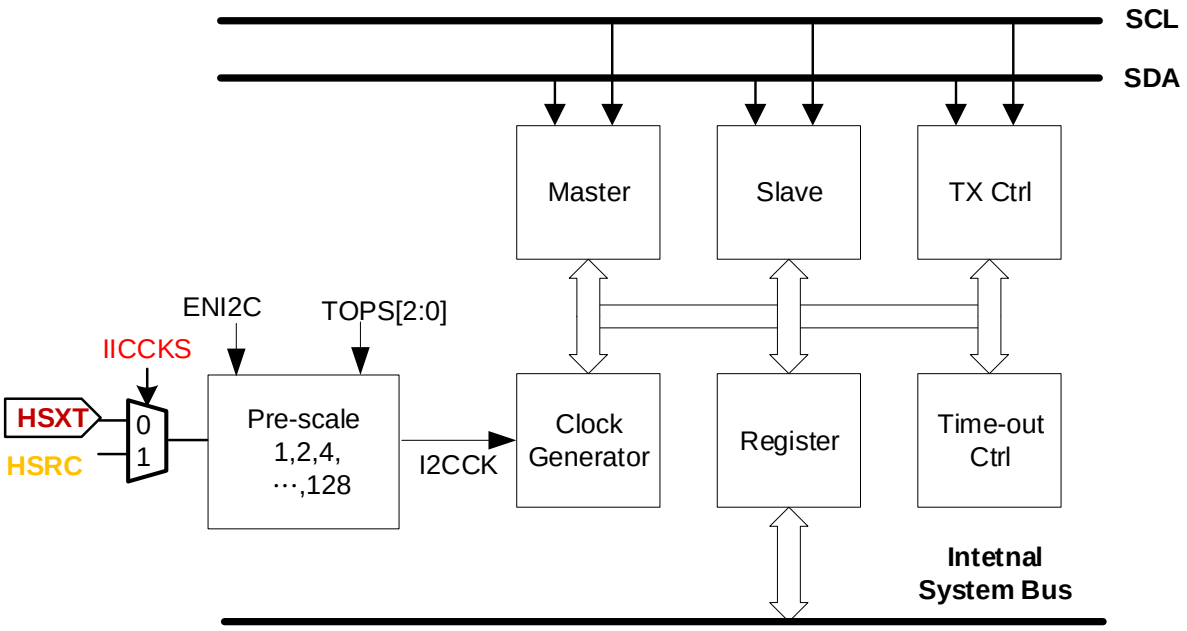


图4-15 I²C网络方框图

4.16. 硬件万年历 RTC 网络

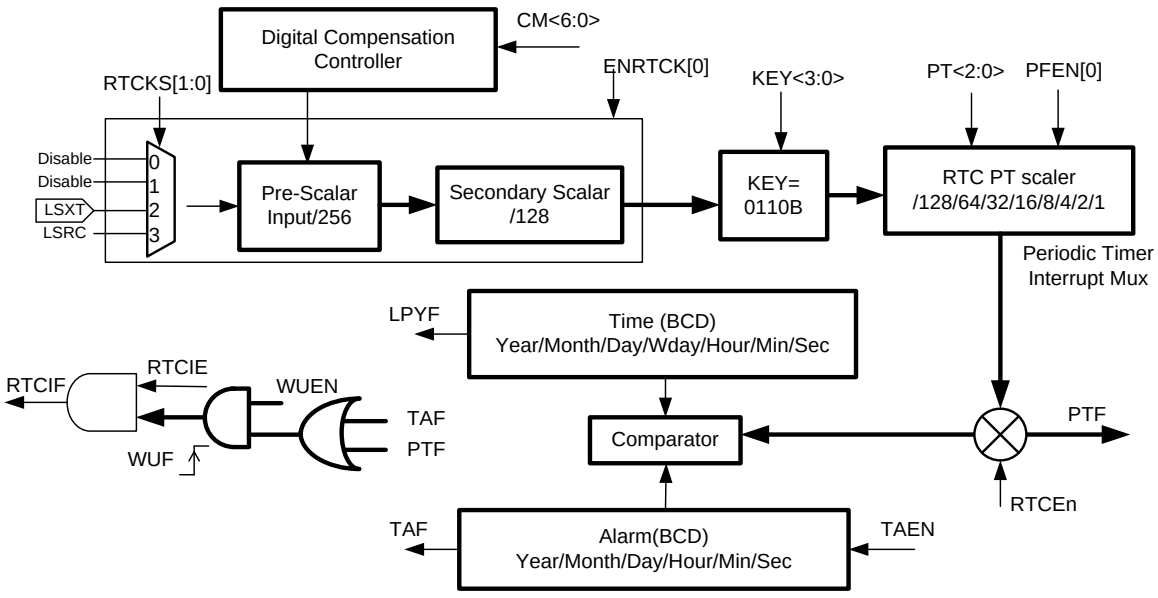


图4-16 硬件万年历RTC网络方框图

4.17. LCD 网络

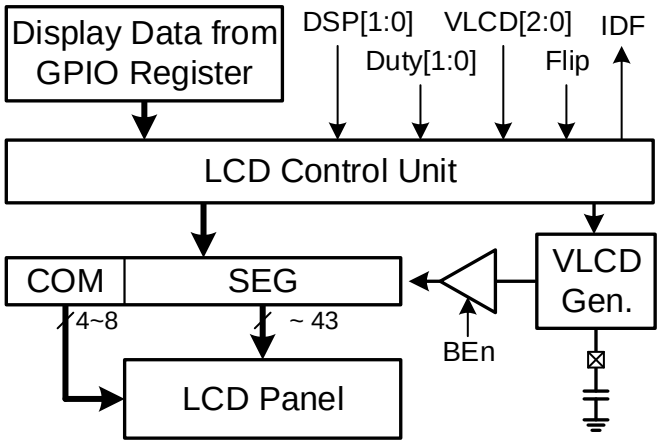


图4-17 LCD网络方框图

4.18. Reset/BOR1/BOR2 网络

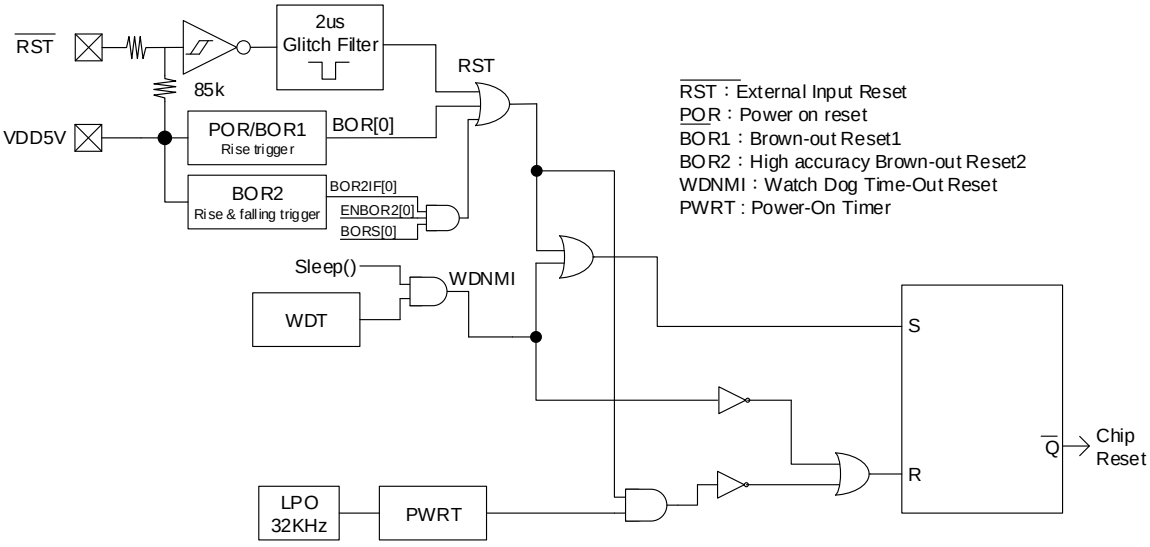


图4-18 Reset/BOR1/BOR2网络方框图

4.19. GPIO

4.19.1. MCU-Port 1~2 网络

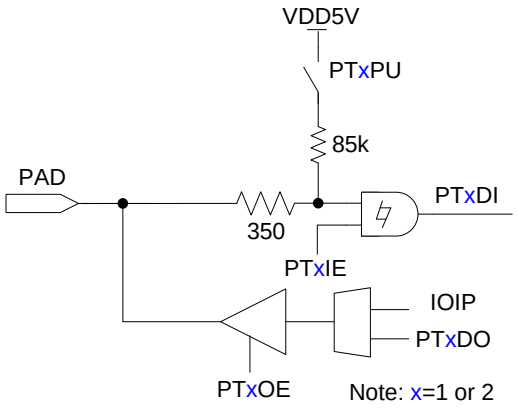


图4-19 MCU-Port 1~2网络方框图

4.19.2. MCU-Port3 网络

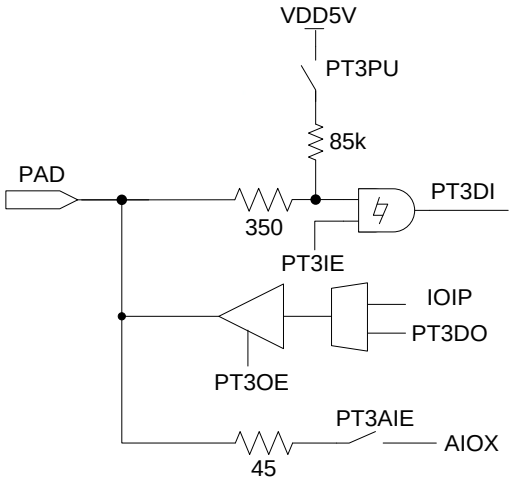


图4-20 MCU-Port3网络方框图

4.19.3. MCU-Port6~10、Port13 网络

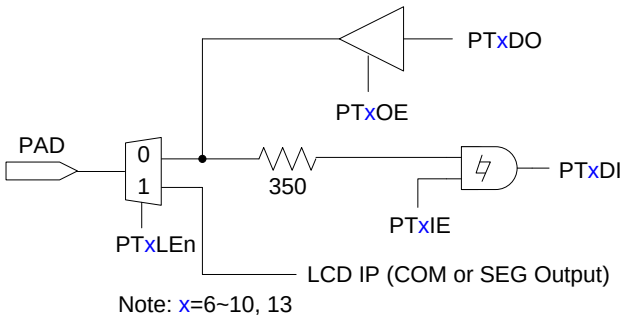


图4-21 MCU-Port 6~10、Port13网络方框图

4.19.4. 交流阻抗量测模拟前端-PORT CLKOUT/IRQ/AI9_1 网络

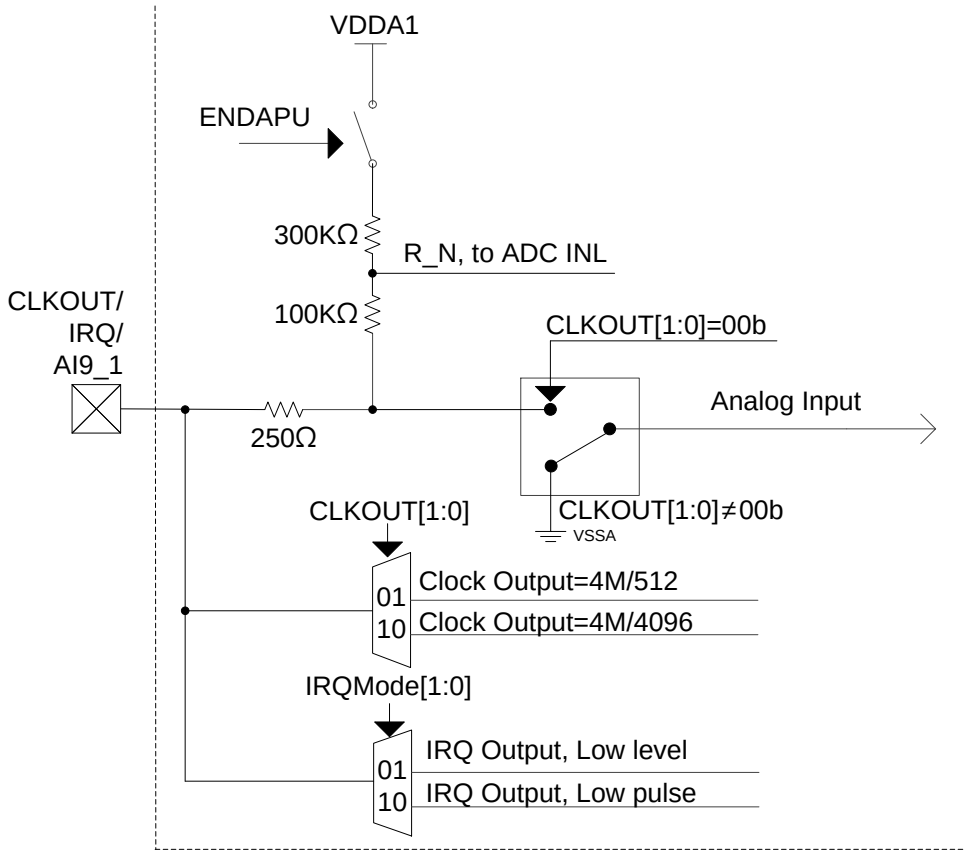


图4-22 AFE-PORT CLKOUT/IRQ/AI9_1网络方框图

4.20. 交流阻抗量测模拟前端-12-bit DAC I 网络

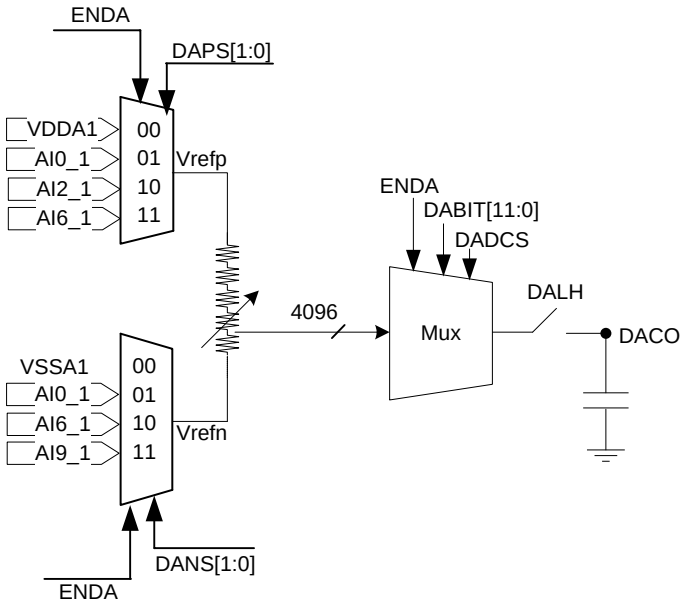


图4-23 AFE-12-bit DAC I网络方框图

4.21. 交流阻抗量测模拟前端-12-bit DAC II 网络

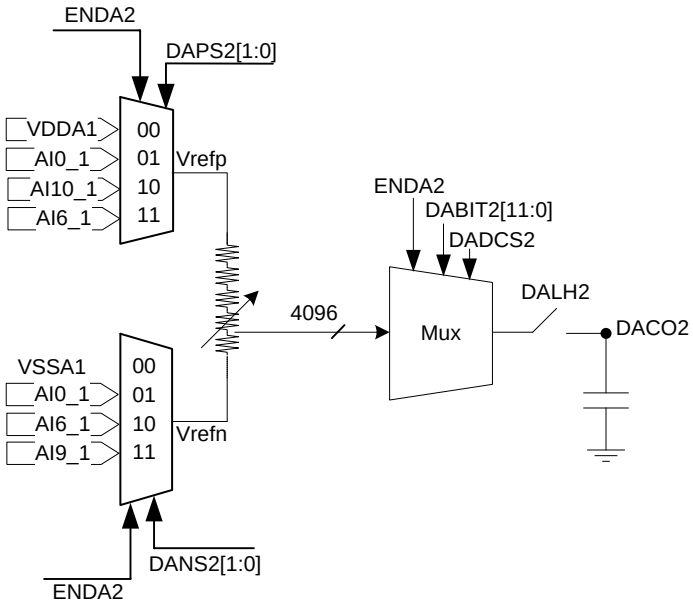


图4-24 AFE-12-bit DAC II网络方框图

4.22. 交流阻抗量测模拟前端-Rail to Rail OPAMP1 网络

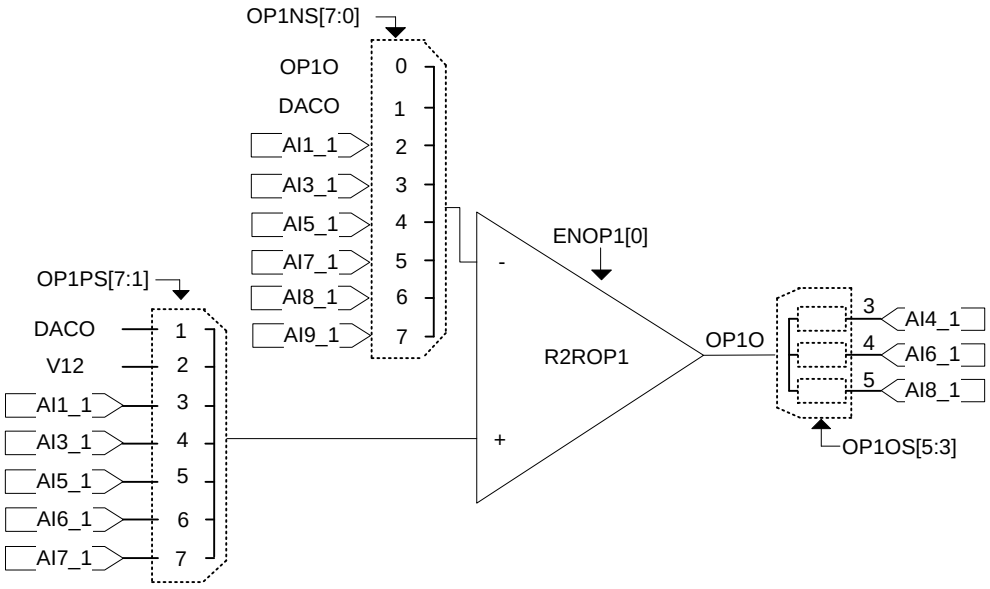


图4-25 AFE-Rail to Rail OPAMP1网络方框图

4.23. 交流阻抗量测模拟前端-Rail to Rail OPAMP2 网络

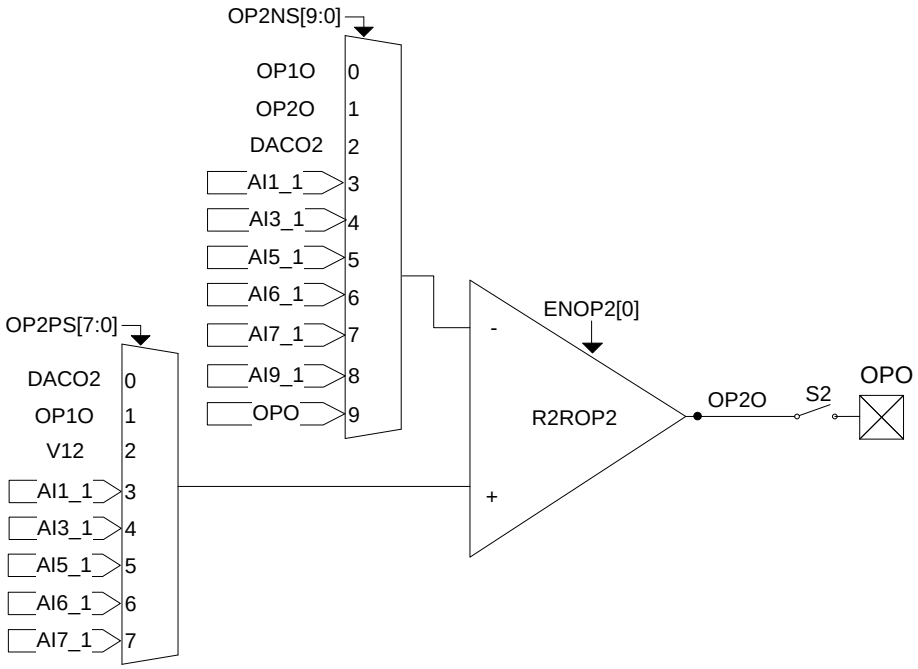


图4-26 AFE-Rail to Rail OPAMP2网络方框图

4.24. 交流阻抗量测模拟前端-Rail to Rail OPAMP3 网络

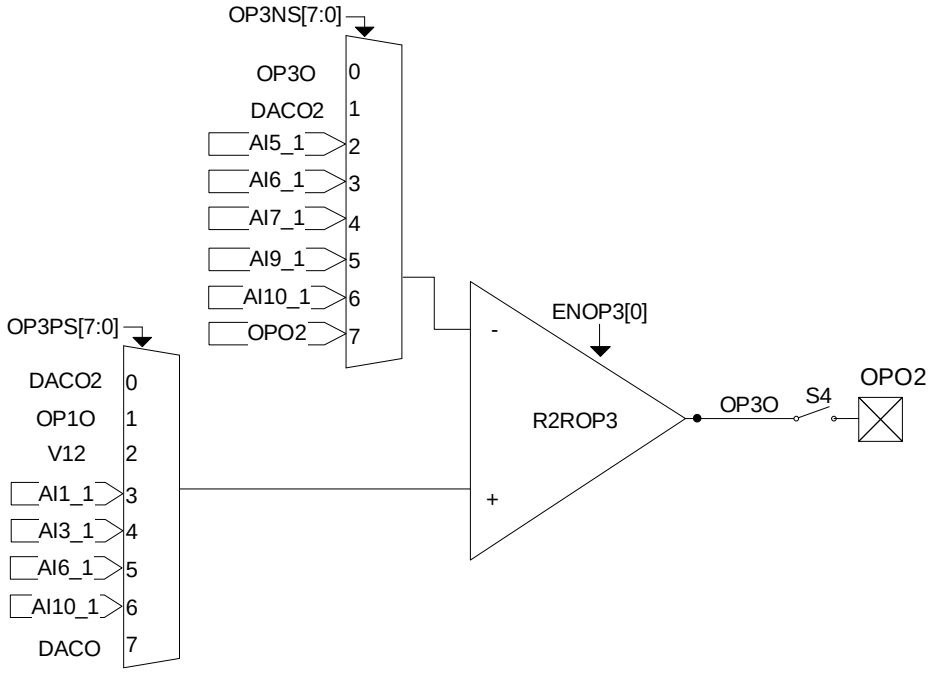


图4-27 AFE-Rail to Rail OPAMP3网络方框图

4.25. 交流阻抗量测模拟前端-BIA Module 网络

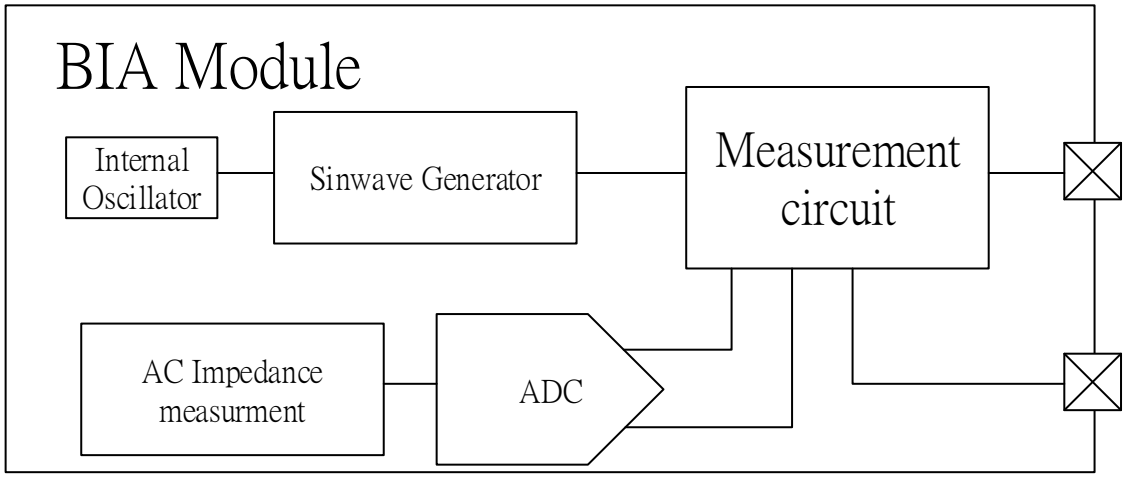


图4-27 AFE-BIA Module网络方框图

※BIA Module 详细资料请洽紘康科技联系窗口

5. 电气特性

5.1. MCU Electrical Characteristics

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)
Voltage applied at VDD5V to VSS ……−0.2 V to 6.0 V
Voltage applied to any pin …… −0.2 V to VDD5V + 0.3 V
Diode current at any device terminal…… ±2mA
Storage temperature, Tstg: (UN programmed device) ..... −55℃ to 150℃
(Programmed device) …….. −40℃ to 85℃
Soldering Temperature (10 Sec) …… +260°C
Maximum output current sink by any PORT1 to PORT13 I/O PIN ……20mA

5.1.1. Recommended Operating Conditions

VDD5V=3.0V.TA=25℃,Unless Otherwise Noted

Parameter	Sym.	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	VDD5V	Digital power	2.0		5.5	V
Supply Voltage	VDDA	Analog power	2.4		3.6	V
Supply Current	I_Sleep	Sleep Mode, @BOR2 OFF, VDD15 low power mode		1.8	4	uA
	I_Idle01	LSRC=32KHz, MCCK= LSRC/1, LSRC(LPO) IDLE Mode		4.5	8	uA
	I_Idle02	LSXT=32768Hz MCCK= LSRC/1, LSXT IDLE Mode		6	12	uA
	I_Idle03	HSRC=4.147MHz, MCCK= HSRC /1, HSRC IDLE Mode		80	120	uA
	I_Idle04	HSRC=31.795MHz, MCCK= HSRC /2, HSRC IDLE Mode		275	410	uA
	I_Free Run01	HSRC=4.147MHz, MCCK= HSRC/1		0.7		mA
	I_Free Run02	HSRC=31.795MHz, MCCK= HSRC /2,		2.5		mA
Power Up Delay	$t_{PU,DLY}$	Power on or wake up from sleep mode		4.1	7	ms

Note: HSRC=31.795MHz, MCCK= HSRC /2, CPU operate at VDD5V>=3V.

5.1.2. Clock System

Typical values are at T_A=25℃ and VDD5V = 3.0V.Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
External High Speed Oscillator						
VDD5V	Operation voltage		2.0		5.5	V
F_{XHS}	High speed oscillator frequency	OHS_HS = 0b			4	MHz
		OHS_HS = 1b			8	MHz
		OHS_HS = 1b			16	MHz
I_{XHS}	High speed oscillator current	F_{XHS} = 16MHz, OHS_HS = 1b		130		uA
D_{XHS}	Duty of high oscillator		40		60	%
External Low Speed Oscillator						
F_{XLS}	Low speed oscillator frequency	VDD5V = 2.0V ~ 5.5V		32.768		KHz
I_{XLS}	Low speed oscillator current			2		uA
D_{XLS}	Duty of low speed oscillator		40		60	%
Internal High Speed Oscillator						
F_{HAO}	Internal high speed oscillator frequency	F_{HAO} = 4.147MHz, F_{HAO} = 4.147MHz, after trim	-10% -2%	4.147	+10% +2%	MHz
		F_{HAO} = 31.795MHz, F_{HAO} = 31.795MHz, after trim	-10% -2%	31.795	+10% +2%	MHz
	Voltage coefficient	VDD5V = 2.0V ~ 5.5 V		1		%
T_{HAO}	Temperature coefficient	-40~85℃		5		%
I_{HAO}	Internal high speed oscillator current	F_{HAO} = 4.147MHz		50		uA
		F_{HAO} = 31.795MHz (VDD5V>= 3.0V)		180		uA
D_{HAO}	Duty of oscillator		40		60	%
WT_{HAO}	Wake up time	F_{HAO} = 4.147MHz		15		us
Internal Low Speed Oscillator						
F_{LPO}	Internal low speed oscillator frequency		-20%	32	+20%	KHz
	Voltage coefficient	VDD5V = 2.0V ~ 5.5V		1		%
T_{LPO}	Temperature coefficient	-40~85℃		5		%
I_{LPO}	Internal low speed oscillator current			2.5		uA
D_{LPO}	Duty of low speed oscillator		40		60	%

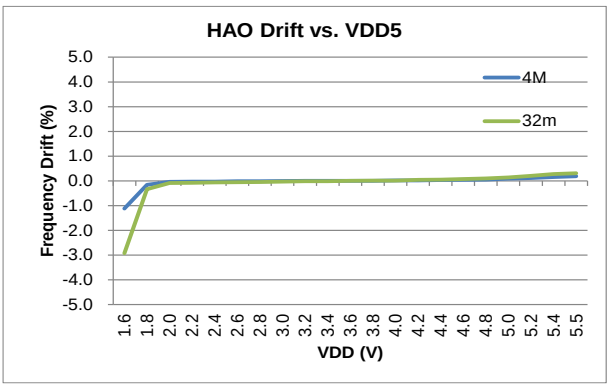


Figure5.1.2-1 HAO vs. VDD5

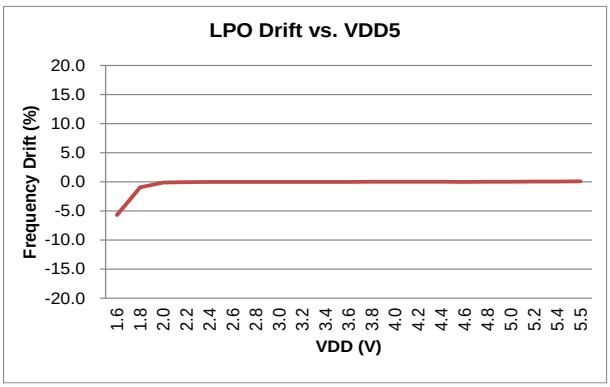


Figure5.1.2-2 LPO vs. VDD5

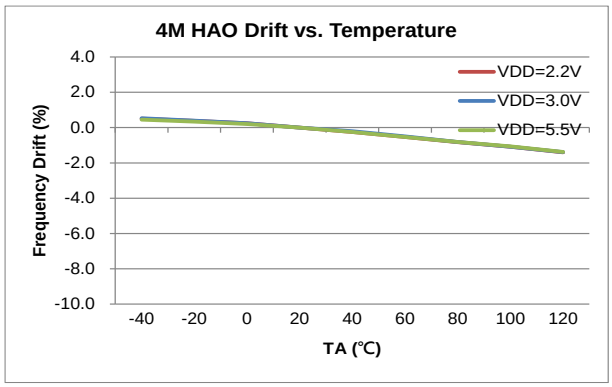


Figure5.1.2-3 HAO vs. Temperature

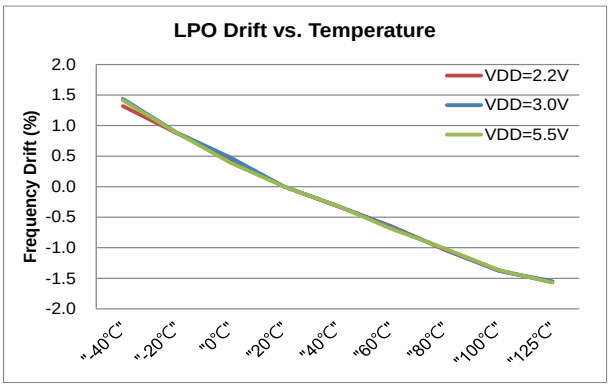


Figure5.1.2-4 LPO vs. Temperature

5.1.3. Power Management System

Typical values are at T_A=25℃ and VDD5V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDDA LDO (Analog power)						
	Output voltage error		-5		5	%
	Capacitor loading		0.1	1	10	uF
	Settling time	Capacitor loading = 0.1uF, 99% of VDDA		100		us
	Operation current	Bias + Band gap + VDDA LDO		35	50	uA
	Dropout voltage	VDD=2.9V, VDAS[1:0]=10b, I_L=10mA		0.4		V
	Select VDDA output voltage, VDD=5.5V, I_L=0.1mA	VDAS[1:0]=00b	-5%	2.4	+5%	V
		VDAS[1:0]=01b		2.6		
		VDAS[1:0]=10b		2.9		
		VDAS[1:0]=11b		3.2		
	Select VDDA output voltage, VDD=2.6V, I_L=10mA	VDAS[1:0]=00b	-6%	2.4	+5%	V
	Voltage coefficient	VDD5V = 2.5 ~ 3.6V		0.2		%/V
		VDD5V = 3.6 ~ 5.5V		0.2		%/V
	Temperature coefficient			100		ppm/°C
VDD15 LDO (Digital Core power)						
	Output voltage		1.35	1.5	1.65	V
	Capacitor loading		0.1	0.47	1	uF
	Dropout voltage	Load = 10mA		0.2		V
	Voltage coefficient	VDD5V= 2.0 ~ 3.6V		0.5		%/V
		VDD5V= 3.6 ~ 5.5V		1		%/V
	Temperature coefficient			200		ppm/°C
REFO Buffer (Bnadgap reference Buffer)						
	Output voltage		1.1	1.2	1.3	V
	Capacitor loading		0.022	0.1	1	uF
	Operation current			20		uA
	Output current		-1		1	mA
	Temperature coefficient	VDDA=2.9 V		80		ppm/°C
	Voltage coefficient	VDDA= 2.4V ~ 3.6V		0.2		%/V

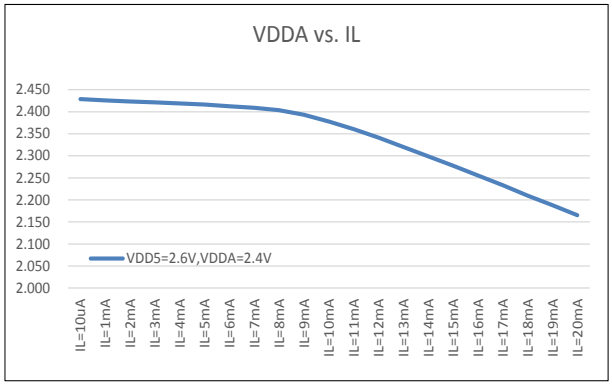


Figure5.1.3-1 VDDA vs. IL

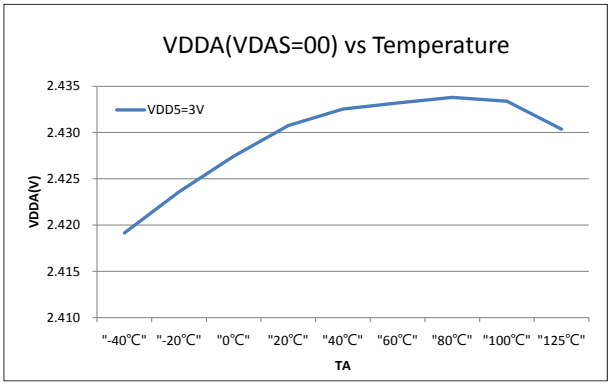


Figure5.1.3-2 VDDA vs. Temperature

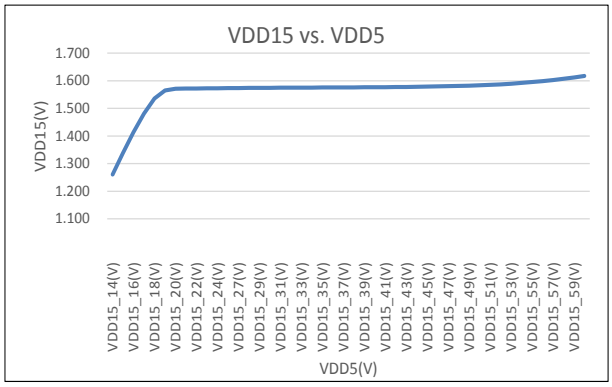


Figure5.1.3-3 VDD15 vs. VDD5

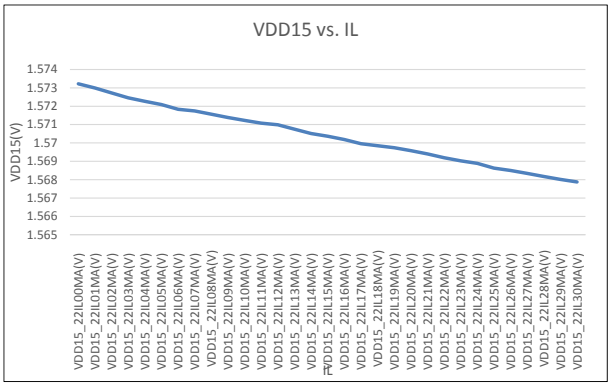


Figure5.1.3-4 VDD15 vs. IL

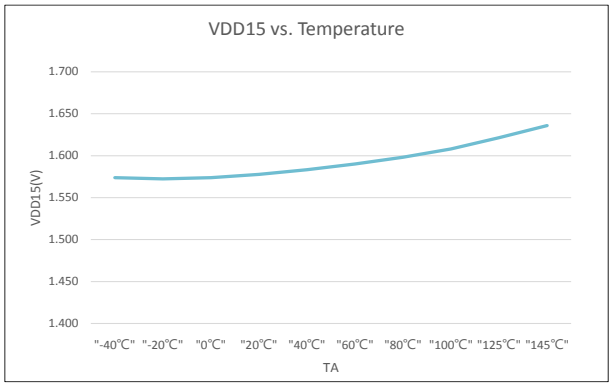


Figure5.1.3-5 VDD15 vs. Temperature

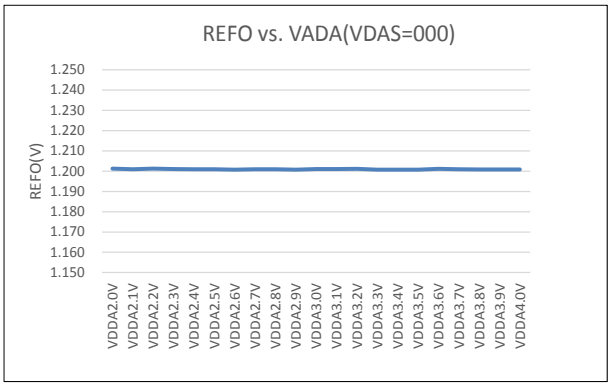


Figure5.1.3-6 REFO vs. VDDA

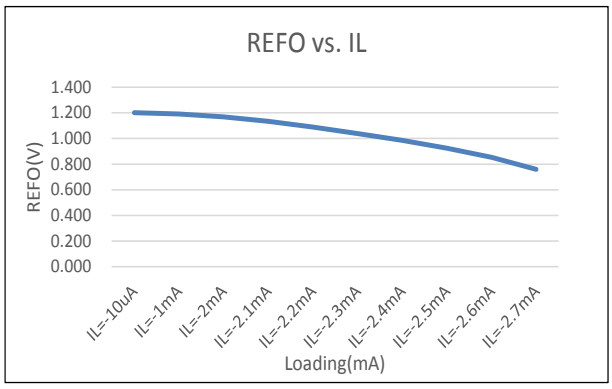


Figure5.1.3-7 REFO vs. IL

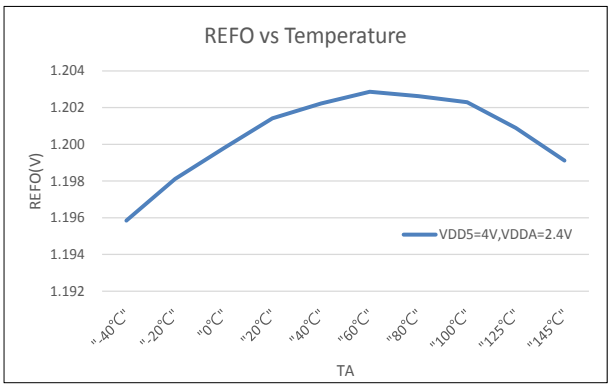


Figure5.1.3-8 REFO vs. Temperature

5.1.4. Reset Management System

Typical values are at T_A=25℃ and VDD5V = 3.0V. Unless otherwise noted.

Sym.	Parameter		Min.	Typ.	Max.	Unit
BOR1	Pulse length needed to accepted reset internally, t_{d-LVR}		2			us
	V_{DD5V} Start Voltage to accepted reset internally (H➔L),V_{LVR1}		1.2	1.4	1.6	V
	Temperature drift, T_A=-40℃~85℃			30		%
	BOR1 current, I_{BOR1}, (include BOR1 and VDD15 LDO)			2.5	5	uA
BOR2	Pulse length needed to accepted reset internally, t_{d-LVR2}		2			uS
	V_{DD5V} Start Voltage to accepted reset internally (L➔H),V_{HYS2}, and BORTH[2:0]:	000b		1.7		V
		001b		2.0		
		010b		2.2		
		011b		2.5		
		100b		2.7		
		101b		3.0		
		110b		3.6		
		111b		4.0		
	V_{DD} Start Voltage to accepted reset internally (H➔L),V_{LVR2}, and BORTH[2:0]:	000b~ 111b	13%	V_{HYS2}-0.06V	13%	V
	Hysteresis, $V_{HYS2-LVR2}$			60		mV
	BOR2 current, I_{BOR2}			10	15	uA
	Temperature Drift			5		%
RST	Pulse length needed as RST pin to accepted reset internally, t_{d-RST}		2			us
	Input Voltage to accepted reset voltage			1.1		V
	Reset release voltage			1.6		V
BOR1/BOR2：Brownout Reset 1/2 RST：External Reset pin						

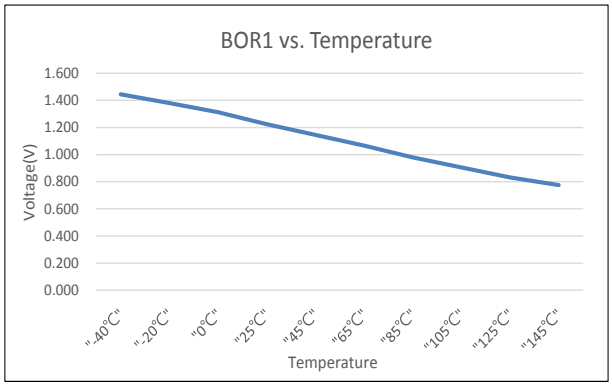


Figure5.1.4-1 BOR1 vs. Temperature

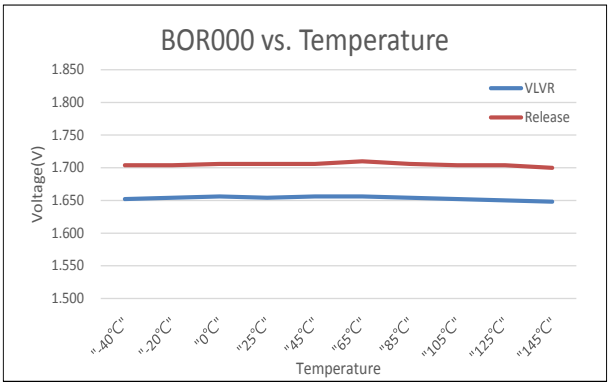


Figure5.1.4-2 BOR2 vs. Temperature

5.1.5. GPIO Port System

Typical values are at T_A=25℃ and VDD5V = 3.3V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PT 1 ~ 3 GPIO Port						
R_{PU}	Internal pull high resistor		65	85	105	kΩ
V_{IH}	Input high voltage		0.75*V_{DD5V}			V
V_{IL}	Input low voltage				0.3*V_{DD5V}	V
V_{hys}	Input Voltage hysteresis(V_{IH} - V_{IL})			0.3*V_{DD5V}		V
I_{LKG}	Leakage Current				0.1	uA
V_{OH}	High-level output voltage	V_{DD5V} =3.3V, I_{OH}=-10mA,	V_{DD5V} -0.4			
		V_{DD5V} 5V, I_{OH}=-15mA,	V_{DD5V} -0.4			
V_{OL}	Low-level output voltage	V_{DD5V} =3.3V, I_{OL}=10mA			V_{SS} +0.4	
		V_{DD5V} =5V, I_{OL}=15mA			V_{SS} +0.4	
PT 6 ~ 10、13 GPIO Port						
R_{PU}	Internal pull high resistor			NA		
V_{IH}	Input high voltage		0.75*V_{DD5V}			V
V_{IL}	Input low voltage				0.3*V_{DD5V}	V
V_{hys}	Input Voltage hysteresis(V_{IH} - V_{IL})			0.3*V_{DD5V}		V
V_{OH}	High-level output voltage	V_{DD5V} =3.3V, I_{OH}=10mA,	V_{DD5V} -0.5			
		V_{DD5V} =5V, I_{OH}=15mA,	V_{DD5V} -0.5			
V_{OL}	Low-level output voltage	V_{DD5V} =3.3V, I_{OL}=-10mA			V_{SS} +0.4	
		V_{DD5V} =5V, I_{OL}=-15mA			V_{SS} +0.4	

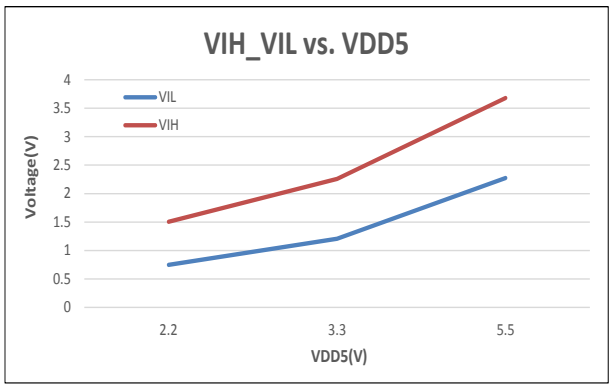


Figure5.1.4-1 VIH/VIL vs. VDD5

5.1.6. ADC Management System

All specifications at T_A=-40℃ to +85℃, VDDA=REFP=2.4V, REFN=VSS, Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Analog Inputs						
	Full-scale input voltage (VINP - AINN)	Considering ADC performance matches ADC ENOB table. REFP=VDDA, REFN=VSS VREF be set to 1/2 only	±0.5*VREF/Gain			V
		Considering ADC performance matches ADC ENOB table. REFP=REFO_I REFN=VSS VREF be set to 1 only	±VREF/Gain			
	Common-mode input range	Gain = 1, @25℃	VSS-0.2V		VDDA	V
System Performance						
	Resolution	No missing codes		24		Bits
	Data rate			ADC Clock /OSR		SPS
	Digital filter settling time	Full setting		3		Data
	Integral nonlinearity (INL)	Differential input End-point fit, OSR=65536		30		PPM
	ADC Gain drift			5	10	ppm/℃
	Normal-mode rejection	f_{IN}=60Hz ±1Hz, Output rate = 15 SPS		70		dB
	Common-mode rejection	ΔVDDA = 0.1V @ DC		80		dB
	Input-referred noise	Output rate= 31 SPS, ADC Gain=1		2.04		uV, rms
	Power-supply rejection	ΔVDDA = 0.1V @ DC		80		dB
Voltage Reference Input						
	Voltage reference input	VREF = REFP - REFN			VDDA	V
	Positive Reference Input	REFP, @25℃	VDDA/2		VDDA	V
	Negative Reference Input	REFN, @25℃	VSS		VDDA/2	V
ADC Modulator Current						
ADC	ADC Modulator	VDD5V=3.3V,VDDA=2.4V, ADC Clock=1Mhz		300		uA
PGA	ADC PGA	VDD5V=3.3V,VDDA=2.4V		700		uA

ENOB(RMS) with OSR/GAIN at CPUCK=4MHz, A/D Clock=4M/4=1MHz, VDDA=2.4V, VREF=AI2-AI3=VDDA-VSS, VRGN=0.5; Vin=AI0-AI1, ext.short with 1K load cell									
OSR					128	512	2048	8196	32768
Output rate(Hz)					7813	1953	488	122	31
Gain	=	PGAGN	x	ADGN					
1	=	off	x	1	16.48	17.5	18.47	19.15	20.18
2	=	off	x	2	16.38	17.61	18.19	19	20.25
3	=	off	x	3	16.22	17.22	18.17	19.06	20.19
4	=	off	x	4	15.84	16.92	17.97	19	20.34
4	=	8	x	1	16.5	17.52	18.43	19.07	19.7
8	=	16	x	1	16.13	17.11	18.18	19.09	19.7
16	=	32	x	1	16.15	16.81	17.63	18.83	19.71
4	=	8	x	4	15.3	15.94	17.23	18	19.05
8	=	16	x	4	14.55	15.77	16.67	17.53	18.44
16	=	32	x	4	14.18	15.14	16.2	17.37	18.15

RMS Noise(uV) with OSR/GAIN at CPUCK=4MHz, A/D Clock=4M/4=1MHz, VDDA=2.4V, VREF=AI2-AI3=VDDA-VSS, VRGN=0.5; Vin=AI0-AI1, ext.short with 1K load cell									
OSR					128	512	2048	8196	32768
Output rate(Hz)					7813	1953	488	122	31
Gain	=	PGAGN	x	ADGN					
1	=	off	x	1	26.376	13.049	6.672	4.146	2.038
2	=	off	x	2	14.145	6.043	4.043	2.311	0.966
3	=	off	x	3	10.559	5.275	2.739	1.472	0.674
4	=	off	x	4	10.337	4.881	2.356	1.151	0.454
8	=	8	x	1	3.257	1.603	0.858	0.547	0.369
16	=	16	x	1	2.112	1.065	0.508	0.272	0.184
32	=	32	x	1	1.041	0.657	0.371	0.162	0.088
32	=	8	x	4	1.874	1.204	0.490	0.288	0.139
64	=	16	x	4	1.570	0.676	0.363	0.200	0.139
128	=	32	x	4	1.016	0.522	0.252	0.111	0.065

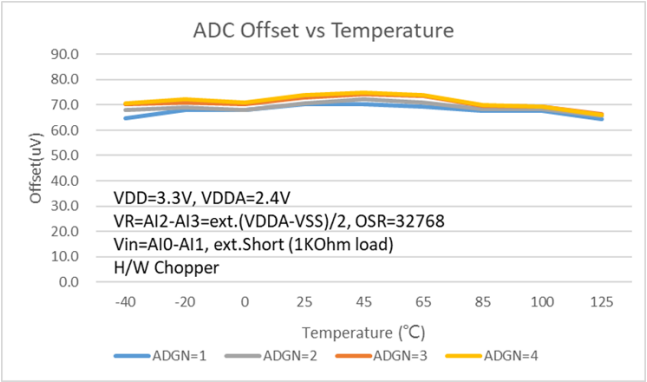


Figure5.1.6-1 ADC Offset vs. Temperature

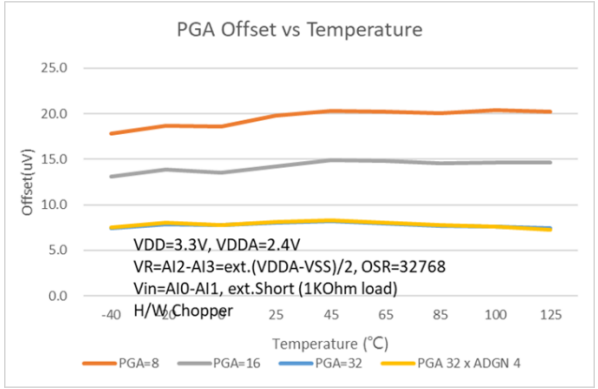


Figure5.1.6-2 PGA Offset vs. Temperature

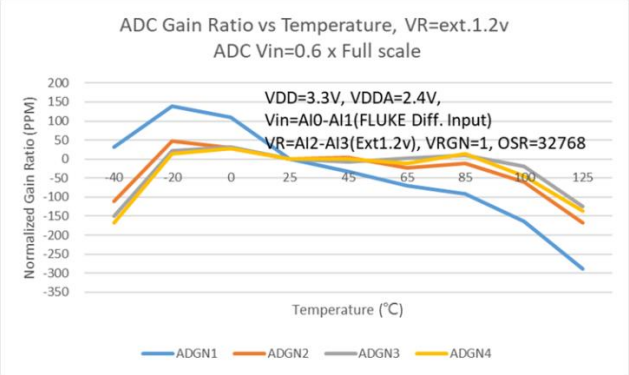


Figure5.1.6-3 ADC Gain Ratio vs. Temperature

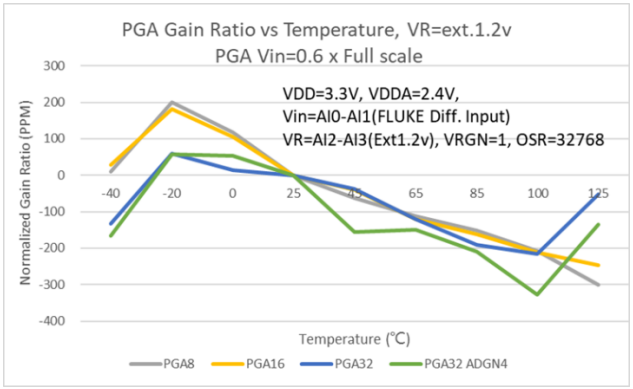


Figure5.1.6-4 PGA Gain Ratio vs. Temperature

5.1.7. Internal Temperature Sensor

Typical values are at T_A=25℃, VDD5V = 3.0V, and VDDA=2.4V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TC_S	Sensor temperature drift			172		uV/℃
KT	Absolute temperature scale 0K			-286		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~85℃		±2		℃

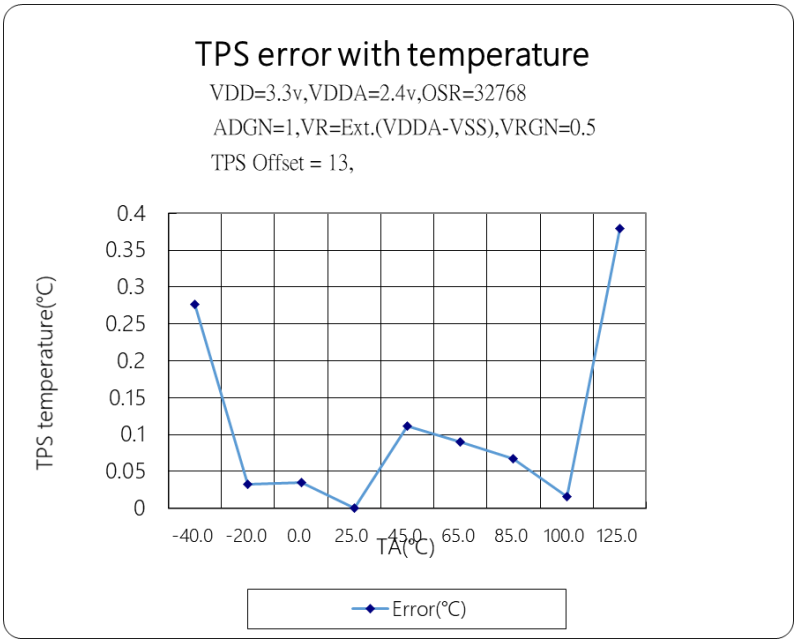


Figure5.1.7-1 ADC Temperature Sensor Error

5.1.8. LVD Comparator Management System

Typical values are at TA=25℃ and VDD5V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
LVD	Operation current, I_{V12_BOR}			2.5		uA
	Operation current, I_{V12_BGR}			10		uA
	V12_BOR Reference Voltage		1.1	1.2	1.3	V
	V12_BOR Reference Voltage Temperature drift			200		PPM/℃
	V12_BOR Reference Voltage to VDD5V Voltage drift			±2		%/V
	V12_BGR Reference Voltage		1.15	1.2	1.25	V
	V12_BGR Reference Voltage Temperature drift			50		PPM/℃
	V12_BGR Reference Voltage to VDD5V Voltage drift			±2		%/V
	Compare reference voltage temperature drift, T_A = -40℃ ~ 85 ℃			50		ppm/℃
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1111b			LVDIN		V
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1110b		5%	4.0	5%	
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1101b			3.6		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1100b			3.3		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1011b			3.0		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1010b			2.9		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1001b			2.8		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=1000b			2.7		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0111b			2.6		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0110b			2.5		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0101b			2.4		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0100b			2.3		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0011b			2.2		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0010b			2.1		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0001b			2.0		
	Detect V_{DD5V} voltage rang by user option, V_{SVS} LVDS [3:0]=0000b			Off		
LVD：Low Voltage Detect						

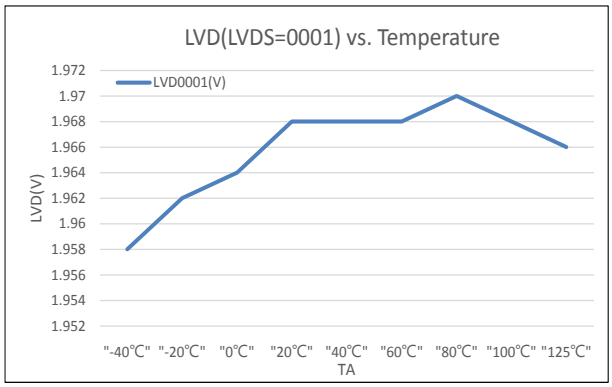


Figure5.1.8-1 LVD vs. Temperature

5.1.9. LCD System

Typical values are at T_A=25℃, VDD5V = 3.3V, and C_{VLCD}=4.7uF. Unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{LCD}	Operation Current Charge Pump Mode		W/O Panel		20		uA
V_{LCD}	Supply Voltage Range	VLCD	With Buffer, ENLCDP[0]=0b	2.5		5.5	V
		ENLCDP[0]=1b @VDD5V > 2.0V	VLCD=111b, @VDD5V>=2.75V		5.0		V
			VLCD=110b @VDD5V>=2.5V		4.5		
			VLCD=101b @VDD5V>=2.2V		3.94		
			VLCD=100b @VDD5V>=2V		3.3		
			VLCD=011b		3.0		
			VLCD=010b		2.8		
	VDD Voltage drift	ENLCDP[0]=1b			5		%
Z_{LCD}	Output Impedance With LCD Buffer	F_{LCD} = LS_CK/32/9, VLCD = 3 V			10		KΩ

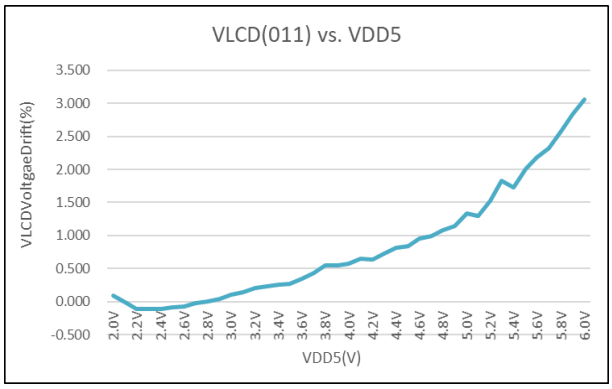


Figure5.1.9-1 VLCD vs. VDD5

5.1.10. Flash Memory

Typical values are at T_A=-40˚C~ 85˚C, VDD5V = 3.3V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	V_{DD5V} Supply voltage		2.0		5.5	V
	Program/Erase supply current				4	mA
	Data retention time		10			Years
	Number of program/Erase cycles(Endurance)		100			K Cycles
	Mass Erase time		10			ms
	Sector Erase time		2			ms
	Word Write time		20			us

5.2. AC Impedance Converter AFE Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at VDD1 to VSS1.....−0.2 V to 6.0 V

Voltage applied to any pin.....−0.2 V to VDD1 + 0.3 V

Diode current at any device terminal .....±2 mA

Storage temperature .....−55℃ to 150℃

Operation temperature.....−40℃ to 85℃

Total power dissipation.....0.5w

Maximum output current sink by CLKOUT pin..... 20mA

5.2.1. Recommended operating conditions

T_A = -40℃ ~ 85℃,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD1}	Supply Voltage	All digital peripherals	2.2		5.5	V
V_{DDA1}	Supply Voltage	Analog peripherals	2.4		4.5	
V_{SS1}	Supply Voltage		0		0	

5.2.2. Internal RC Oscillator

T_A = 25℃,V_{DD1} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
HAO	High Speed Oscillator frequency	2MHz Mode, HAOM[1:0]=00b	1.65	1.95	2.25	MHz
		4MHz Mode, HAOM[1:0]=01b	3.45	4.0	4.56	MHz
		8MHz Mode, HAOM[1:0]=10b	7.57	8.5	9.16	MHz
		HAO Trim Range[6:0]	-63		64	LSB
		2MHz HAO Trim LSB		0.345		%
		4MHz HAO Trim LSB		0.3		%
		8MHz HAO Trim LSB		0.21		%

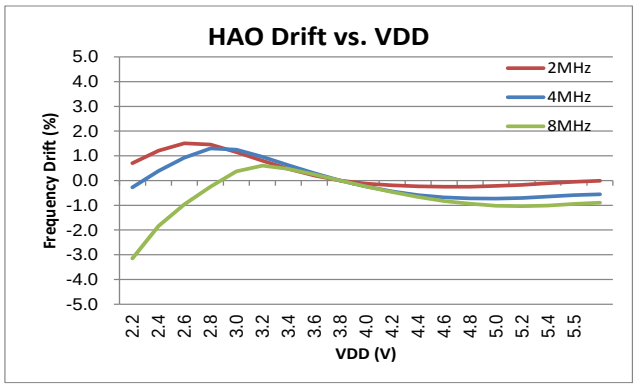


Figure 5.2.2-1 HAO vs. VDD1

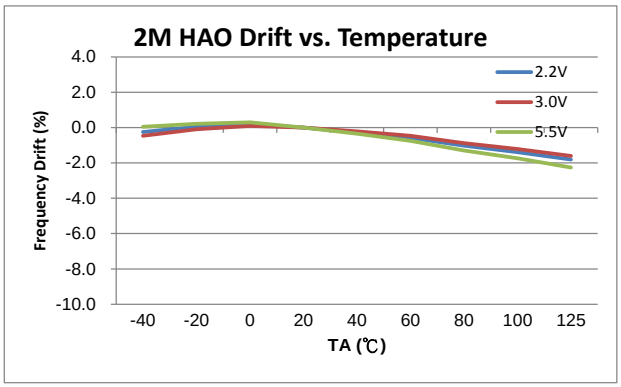


Figure 5.2.2-2 HAO(2.0MHz) vs. Temperature

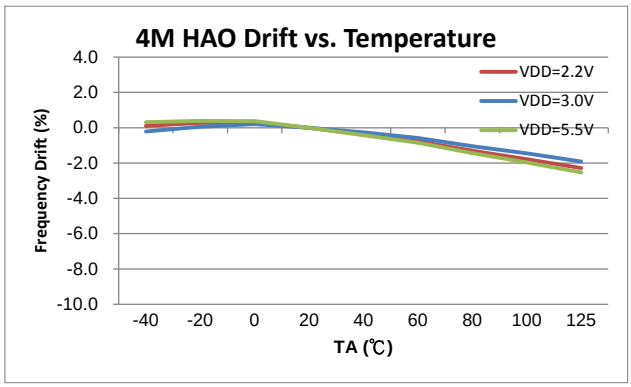


Figure 5.2.2-3 HAO(4.0MHz) vs. Temperature

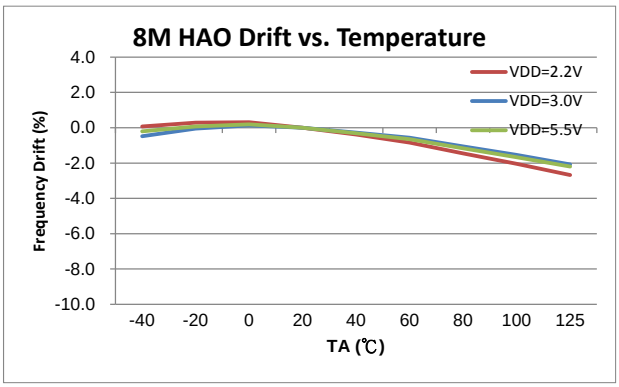


Figure 5.2.2-4 HAO(8.0MHz) vs. Temperature

5.2.3. Supply current into VDD1 excluding peripherals current

T_A = 25℃,V_{DD1} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{LP3}	Low Power 3	HAO = off, All IP Off, Sleep state		0.3	1.0	uA
HAO：Internal High Accuracy Oscillator frequency.						

T_A = 25℃,V_{DD1} = 5.5V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{LP3}	Low Power 3	HAO = off, All IP Off, Sleep state		0.5	2	uA

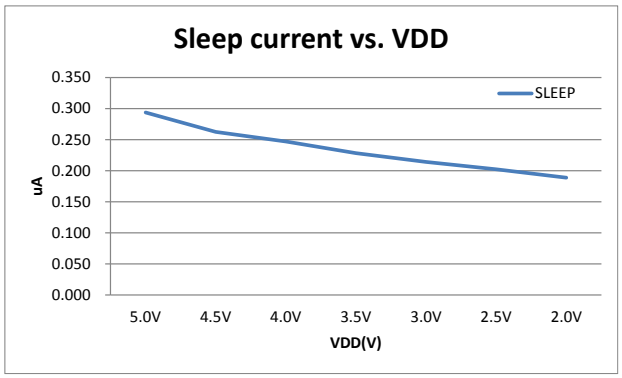


Figure 5.2.3-1 I_{LP3} vs. VDD1

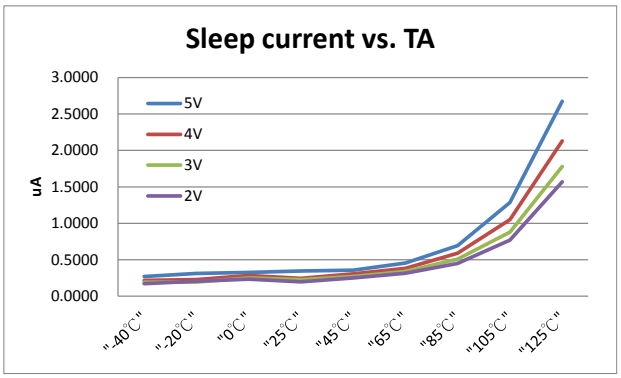


Figure 5.2.3-2 I_{LP3} vs. Temperature

5.2.4. GPIO PORT CLKOUT/IRQ/AI9

T_A = 25℃,V_{DD1} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Analog Input						
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance		351	390	429	kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	VDD1<4V, I_{OH}=10mA,	V_{DD1}-0.3			V
		VDD1>=4V, I_{OH}=15mA,	V_{DD1}-0.4			
V_{OL}	Low-level output voltage	VDD1<4V, I_{OL}=-10mA			V_{SS1}+0.3	
		VDD1>=4V, I_{OL}=-15mA			V_{SS1}+0.4	

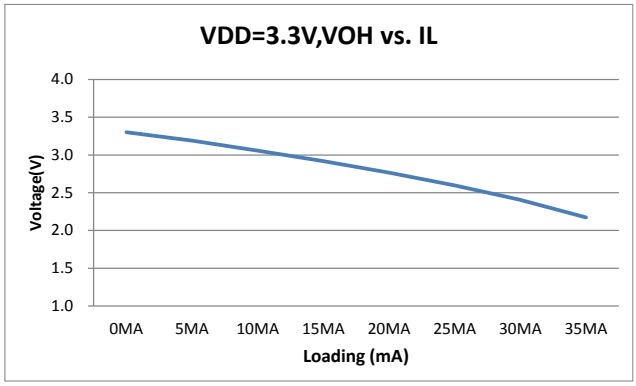


Figure 5.2.4-1 V_{OH} vs. I_{OH}

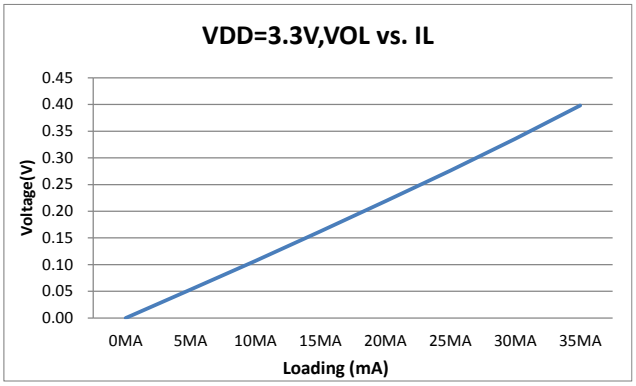


Figure 5.2.4-2 V_{OL} vs. I_{OL}

5.2.5. Brownout Reset (BOR)

T_A = 25℃,V_{DD1} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BOR	Pulse length needed to accepted reset internally, t_{d-LVR}		2			uS
	V_{DD1} Start Voltage to accepted reset internally (L➔H),V_{LVR}	T_A = 25℃	1.5	1.65	1.8	V
	V_{DD1} Start Voltage to accepted reset internally (L➔H),$V_{LVR,}$	T_A = -40℃ ~ 85 ℃	1.45		1.85	V
	Current consumption	VDD1=3.3V		0.3		uA
		VDD1=5.5V		0.5		uA

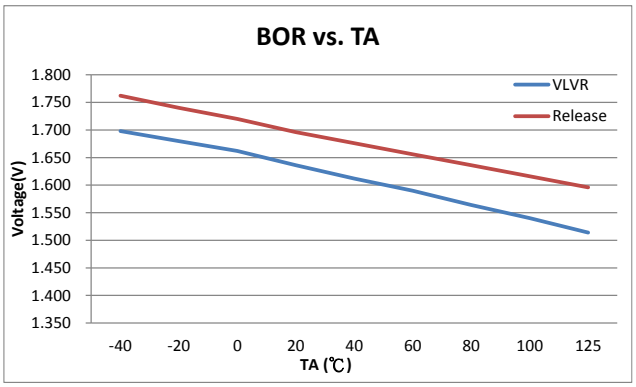


Figure5.2.5-1 BOR vs. Temperature

5.2.6. Power System

T_A = 25℃,VDD1 = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
VDDA1	VDDA1 operation current, I_{VDDA1}	I_L = 0mA	LDOC[2:0]=000b		20		uA
	Select VDDA1 output voltage	I_L = 0.1mA, VDD1 ≧VDDA1+0.25V	LDOC [2:0]=000b	2.28	2.4	2.52	V
			LDOC [2:0]=001b	2.47	2.6	2.73	V
			LDOC [2:0]=010b	2.755	2.9	3.045	V
			LDOC [2:0]=011b	3.135	3.3	3.465	V
			LDOC [2:0]=100b	3.42	3.6	3.78	V
			LDOC [2:0]=101b	3.8	4.0	4.2	V
			LDOC [2:0]=110b	4.275	4.5	4.725	V
			LDOC [2:0]=111b	4.75	5.0	5.25	V
	Dropout voltage	I_L = 10mA	LDOC [2:0]=000b		400		mV
	Temperature drift	LDOC [2:0]=000b I_L = 10uA	T_A=-40℃~85℃		50		ppm/℃
	V_{DD1} Voltage drift	LDOC [2:0]=000b	V_{DD1}=VDDA1+0.25V~5.5V		±0.2		%/V
REFO1	REFO1 operation current, I_{REFO1}	VDDA1=2.4V, ENV12=1b			50		uA
	output voltage, V_{REFO1}		I_L = 0mA,	1.14	1.2	1.26	V
			I_L = 0.2mA (include ESD resistance)	0.94		0.96	V_{REFO1}
	Temperature drift		T_A=-40℃~85℃		50		ppm/℃
	V_{DDA1} Voltage drift				100		uV/V
ACM1	ACM1 operation current, I_{ACM1}	VDDA1=2.4V, ENADC[0]=1b, ENACM=1b			50		uA
	Internal Analog Common Mode Voltage ,V_{ACM1}=1.2V or VDDA1/2		VCMS=0b, I_L = 0uA		VDDA1/2		V
			VCMS=1b, I_L = 0uA	1.14	1.2	1.26	V
	Temperature drift		T_A=-40℃~85℃, ENACM [0]=1b		50		ppm/℃
VDDA1：Adjust Voltage Regulator, ACM1：Internal Analog Common Mode Voltage VDDA1/2 (No voltage output) or 1.2V							

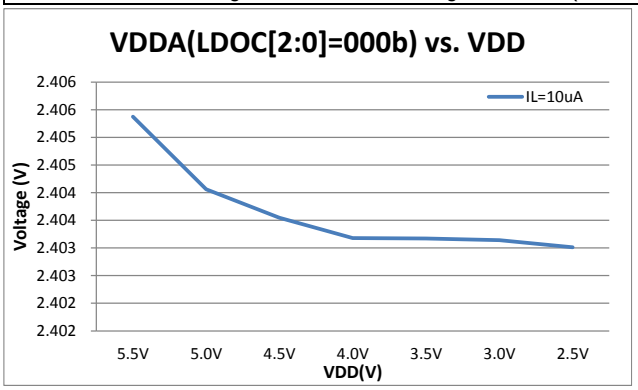


Figure 5.2.6-1 VDDA1(000b) vs. VDD1

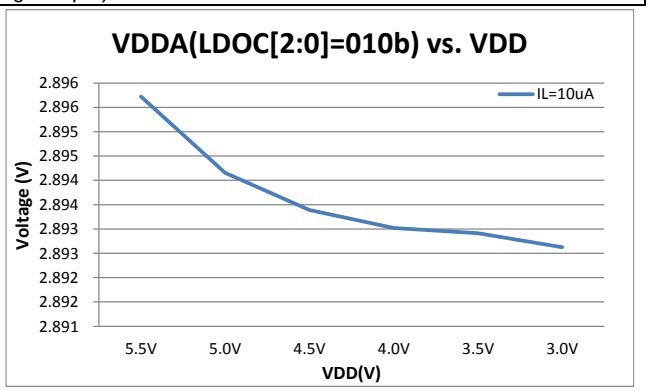


Figure 5.2.6-2 VDDA1(010b) vs. VDD1

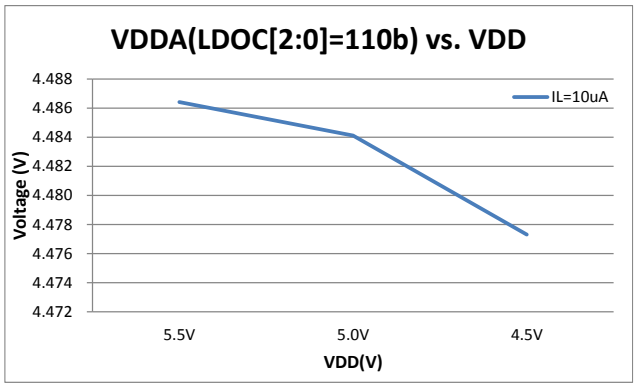


Figure 5.2.6-3 VDDA1(110b) vs. VDD1

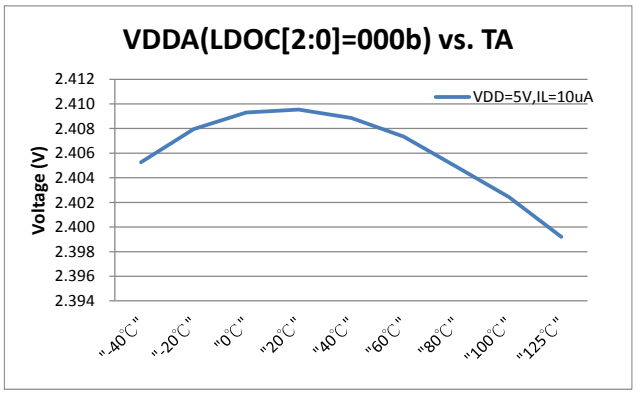


Figure 5.2.6-4 VDDA1(000b) vs. Temperature

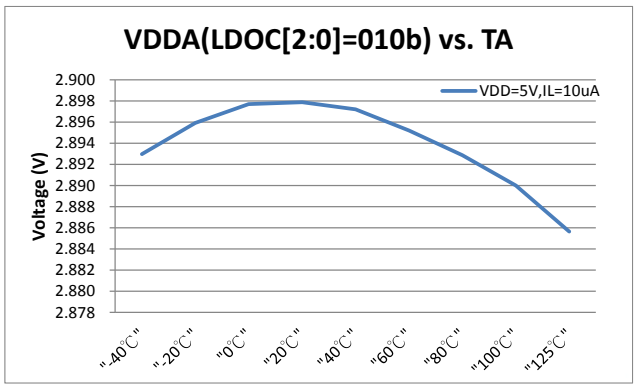


Figure 5.2.6-5 VDDA1(010b) vs. Temperature

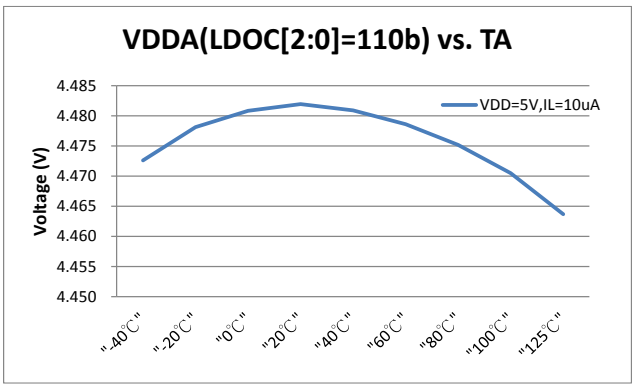


Figure 5.2.6-6 VDDA1(110b) vs. Temperature

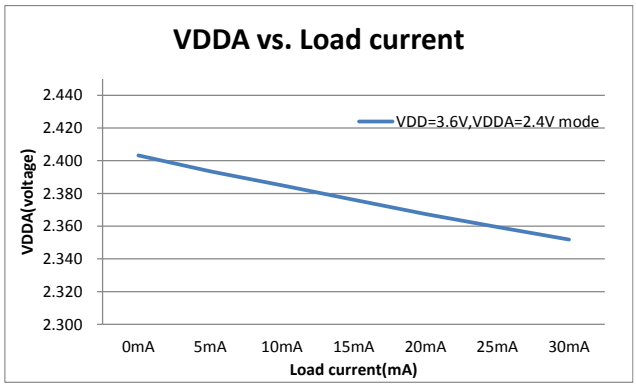


Figure 5.2.6-7 VDDA1 vs. Load current

5.2.7. ΣΔADC, Power Supply and recommended operating conditions

T_A = 25℃,V_{DD1} = 3.0V, VDDA1=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{SD18}	Supply Voltage at VDDA1	ENVDDA[0]=0		2.4		4.5	V
f_{SD18}	Modulator sample frequency, ADC_CK				1000		KHz
	Over Sample Ratio, OSR			64		65536	
I_{SD18}	Operation supply current without PGA	ENADC[0]=1	GAIN =16, ADC_CK=1MHz		260		uA

5.2.7.1. ΣΔADC, performance

T_A = 25℃,V_{DD1} = 3.0V, VDDA1=2.4V,V_{VR}=1.0V,GAIN=1 without PGA,fSD18=1MHz,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
INL	Integral Nonlinearity(INL)	VDDA1=2.4V,V_{VR}=1.0V,ΔSI=±200mV			±0.003	±0.01	%FSR
		VDDA1=2.4V,V_{VR}=1.0V,ΔSI=±450mV					
	No Missing Codes[3]	ADC_CK=1MHz,OSR=64000		23			Bits
G_{SD18}	Temperature drift Gain x16	T_A = -40℃~ 85℃,			10		ppm/℃
E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper	ΔAI=0V ΔVR=1.2V DCSET[3:0]=<0000> *ΔAI is external short	Gain=2			1	%FSR
	Offset error temperature drift with chopper		GAIN=1		0.004		uV/℃
			GAIN=2		0.003		
			GAIN=4		0.003		
			GAIN=16		0.002		
CM_{SD18}	Common-mode rejection	V_{CM}=0.7V to 1.7V, V_{VR}=1.0V	V_{SI}=0V, GAIN=1		90		dB
		V_{CM}=0.7V to 1.7V, V_{VR}=1.0V	V_{SI}=0V, GAIN=16		75		
PSRR	DC power supply rejection	VDDA1=3.0V, ΔVDDA1=±100mV, V_{VR}=1.0V, V_{SI}=1.2V,V_{SI-}=1.2V,	GAIN=1 PGA=off		75		dB

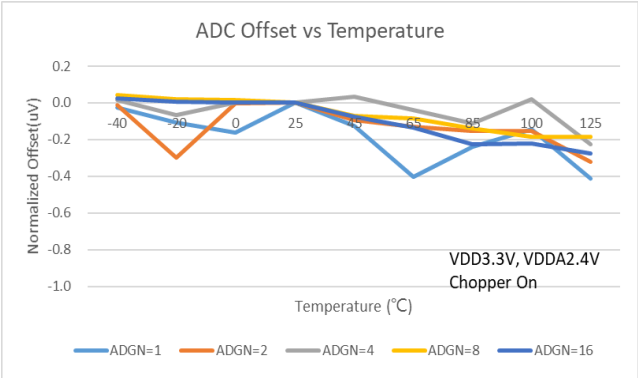


Figure 5.2.7-1 ADC Offset drift with Temperature

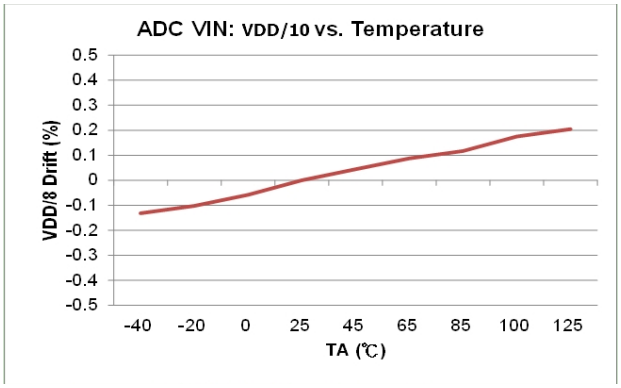


Figure 5.2.7-2 VDD1/10 drift with Temperature

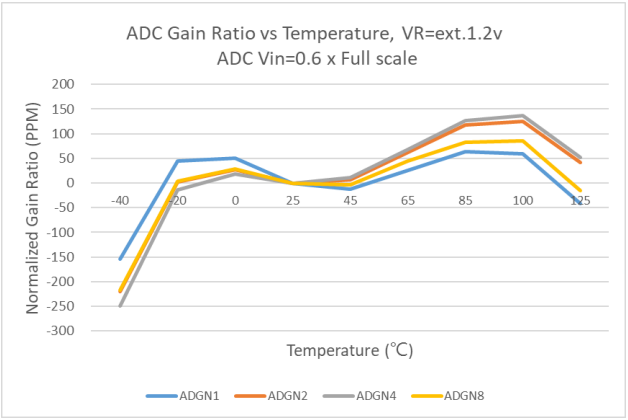


Figure 5.2.7-3 ADC Gain drift with Temperature

5.2.7.2. ΣΔADC Noise Performance

T_A = 25℃,V_{DD1} = 3.0V, VDDA1=2.4V,unless otherwise noted

针对 ΣΔADC 提供了重要的输入噪声规格。下表列出典型的噪声规格表与 Gain, Output rate，及单端最大输入电压等关系。测试条件设定在外部输入讯号短路，参考电压为 1.2V，取样 1024 笔资料。

ENOB(RMS) with OSR/GAIN at A/D Clock=1MHz, VDD1=3.3V, VDDA1=2.4V, Vin=VSSA1-VSSA1, VREF=(VDDA1-VSS1)/2=1.2V, 2nd conb filter

Max. Vin(mV) =0.9VREF(1)	OSR					32	64	125	250	500	1000	2000	4000	8000	16000	32000	64000
	Output rate(Hz)					31250	15625	8000	4000	2000	1000	500	250	125	63	31	16
	Gain	=	PGAGN	x	ADGN												
±2160	0.25	=	off	x	0.25	10.4	12.2	13.48	15.21	15.79	16.26	16.59	17.14	17.98	18.56	18.98	19.6
±2160	0.5	=	off	x	0.5	10.4	12.21	13.63	15.29	15.81	16.45	17.03	17.49	17.97	18.36	18.98	19.41
±1080	1	=	off	x	1	10.44	12.11	14.14	15.29	15.87	16.36	16.99	17.56	18.01	18.47	18.87	19.41
±540	2	=	off	x	2	10.39	12.18	13.57	15.21	15.9	16.46	16.98	17.47	17.93	18.41	18.86	19.41
±270	4	=	off	x	4	10.38	12.16	13.29	15.22	15.74	16.29	16.88	17.35	17.85	18.33	18.91	19.26
±135	8	=	off	x	8	10.42	12.09	13.49	15.1	15.63	16.19	16.81	17.28	17.86	18.28	18.72	19.09
±68	16	=	off	x	16	10.33	12	13.92	15.01	15.58	16.11	16.68	17.11	17.59	18.14	18.55	19

(1) Max. Vin(mV) is the max. input voltage single end to ground(VSS1)

ENOB(RMS) with OSR/GAIN at A/D Clock=1MHz, VDD1=3.3V, VDDA1=2.4V, Vin=VSSA1-VSSA1, VREF=(VDDA1-VSS1)/2=1.2V, 2nd conb filter, Chopper On

Max. Vin(mV) =0.9VREF(1)	OSR					32	64	125	250	500	1000	2000	4000	8000	16000	32000	64000
	Output rate(Hz)					15625	7813	4000	2000	1000	500	250	125	63	31	16	8
	Gain	=	PGAGN	x	ADGN												
±2160	0.25	=	off	x	0.25	10.89	12.7	14.2	15.88	16.39	16.74	16.83	17.63	18.5	19.07	19.5	20.04
±2160	0.5	=	off	x	0.5	10.8	12.65	14.21	15.66	16.25	16.93	17.38	17.92	18.47	19.01	19.48	20
±1080	1	=	off	x	1	10.85	12.69	14.07	15.66	16.43	16.95	17.49	17.88	18.48	19.04	19.35	20.01
±540	2	=	off	x	2	10.87	12.73	14.2	15.68	16.45	16.85	17.41	18.04	18.41	18.94	19.36	19.91
±270	4	=	off	x	4	10.92	12.72	14.11	15.69	16.2	16.93	17.41	17.95	18.37	18.86	19.46	19.87
±135	8	=	off	x	8	10.85	12.68	14.04	15.52	16.01	16.66	17.39	17.83	18.31	18.8	19.29	19.73
±68	16	=	off	x	16	10.81	12.53	13.88	15.48	16.1	16.63	17.1	17.68	18.06	18.52	19.14	19.48

(1) Max. Vin(mV) is the max. input voltage single end to ground(VSS1)

Table5.2.7-1 ΣΔADC ENOB Table

RMS(uV) with OSR/GAIN at A/D Clock=1MHz, VDD1=3.3V, VDDA1=2.4V, Vin=VSSA1-VSSA1, VREF=(VDDA1-VSS1)/2=1.2V, 2nd conb filter

Max. Vin(mV) =0.9VREF(1)	OSR					32	64	125	250	500	1000	2000	4000	8000	16000	32000	64000
	Output rate(Hz)					31250	15625	8000	4000	2000	1000	500	250	125	63	31	16
	Gain	=	PGAGN	x	ADGN												
±2160	0.25	=	off	x	0.25	7167.72	2052.62	846.32	255.25	170.77	122.81	97.90	66.85	37.35	25.06	18.76	12.19
±2160	0.5	=	off	x	0.5	3585.84	1019.28	380.01	120.90	84.36	53.83	36.00	26.22	18.85	14.33	9.37	6.94
±1080	1	=	off	x	1	1735.51	547.67	133.84	60.37	40.41	28.69	18.53	12.51	9.17	6.64	5.03	3.47
±540	2	=	off	x	2	900.82	259.54	99.46	31.89	19.82	13.37	9.36	6.67	4.85	3.47	2.53	1.73
±270	4	=	off	x	4	453.79	131.66	60.29	15.78	11.03	7.53	4.99	3.61	2.56	1.83	1.22	0.96
±135	8	=	off	x	8	219.94	69.37	26.29	8.58	5.94	4.03	2.64	1.90	1.27	0.95	0.70	0.54
±68	16	=	off	x	16	117.26	36.75	9.75	4.59	3.08	2.14	1.44	1.07	0.76	0.52	0.39	0.29

(1) Max. Vin(mV) is the max. input voltage single end to ground(VSS1)

RMS(uV) with OSR/GAIN at A/D Clock=1MHz, VDD1=3.3V, VDDA1=2.4V, Vin=VSSA1-VSSA1, VREF=(VDDA1-VSS1)/2=1.2V, 2nd conb filter, Chopper On

Max. Vin(mV) =0.9VREF(1)	OSR					32	64	125	250	500	1000	2000	4000	8000	16000	32000	64000
	Output rate(Hz)					15625	7813	4000	2000	1000	500	250	125	63	31	16	8
	Gain	=	PGAGN	x	ADGN												
±2160	0.25	=	off	x	0.25	5078.12	1456.73	515.21	159.79	112.25	88.58	83.03	47.74	25.99	17.59	12.99	8.96
±2160	0.5	=	off	x	0.5	2710.97	751.58	255.16	93.61	61.88	38.69	28.29	19.52	13.28	9.18	6.59	4.59
±1080	1	=	off	x	1	1306.67	365.13	140.05	46.81	27.27	19.14	13.14	9.99	6.62	4.48	3.62	2.30
±540	2	=	off	x	2	647.24	178.25	64.25	22.97	13.50	10.24	6.96	4.49	3.46	2.41	1.79	1.23
±270	4	=	off	x	4	312.62	89.41	34.05	11.41	8.04	4.85	3.46	2.38	1.79	1.27	0.84	0.63
±135	8	=	off	x	8	163.64	45.95	17.88	6.44	4.57	2.91	1.76	1.30	0.93	0.66	0.47	0.35
±68	16	=	off	x	16	83.87	25.55	10.02	3.31	2.14	1.49	1.07	0.72	0.55	0.40	0.26	0.21

Table5.2.7-2 ΣΔADC RMS Noise Table

The RMS noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$\text{ENOB(RMS)} = \ln\left(\frac{\text{FSR}}{\text{RMS Noise}}\right) \Big/ \ln(2)$$

$$\text{RMS Noise} = \left(2 \times \text{VREF} \times \sqrt{\sum_{k=1}^{1024}(\text{ADO}[k] - \text{Average})^2}\right) \Big/ 2^{23}$$

$$\text{Where FSR (Full - Scale Range)} = 2 \times \text{VREF/Gain.}$$

$$\text{Average} = \frac{\sum_{k=1}^{1024}(\text{ADO}[k])}{1024}$$

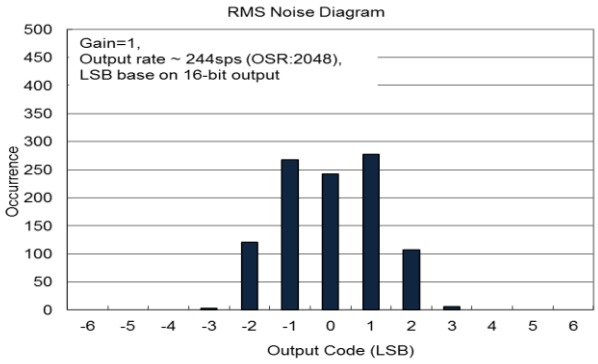


Figure 5.2.7-4 RMS Noise Diagram

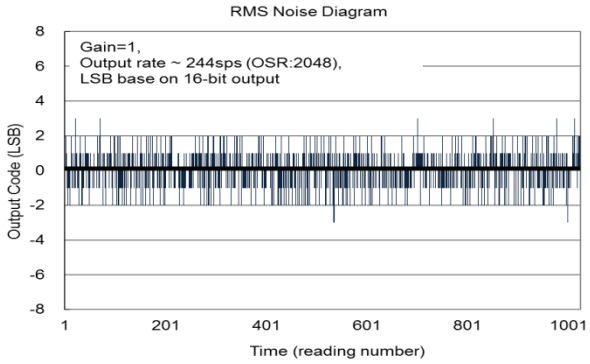


Figure 5.2.7-5 Outout code Diagram

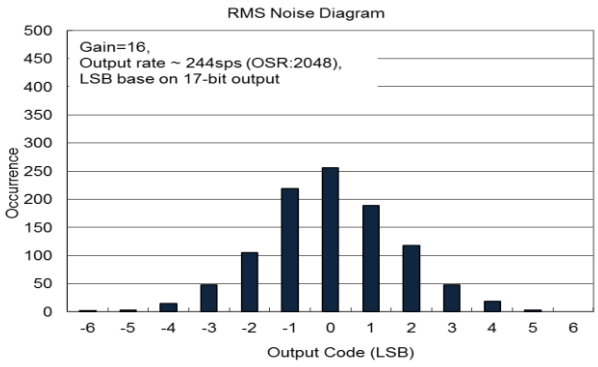


Figure 5.2.7-6 RMS Noise Diagram

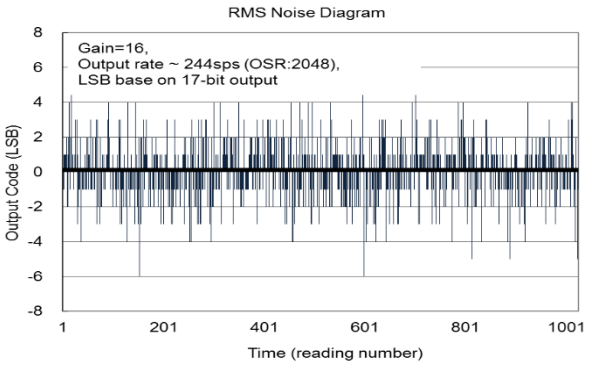


Figure 5.2.7-7 Output Code Diagram

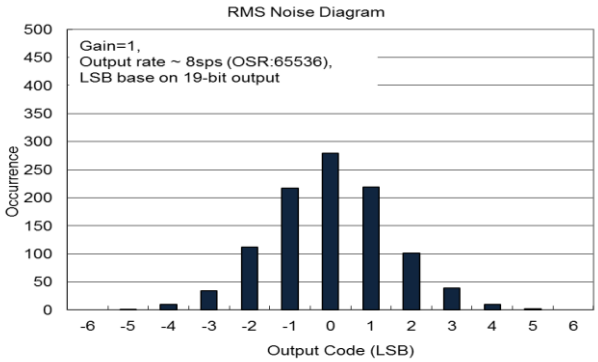


Figure 5.2.7-8 RMS Noise Diagram

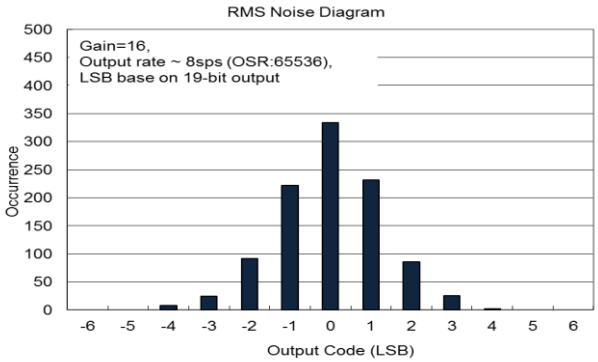


Figure 5.2.7-9 RMS Noise Diagram

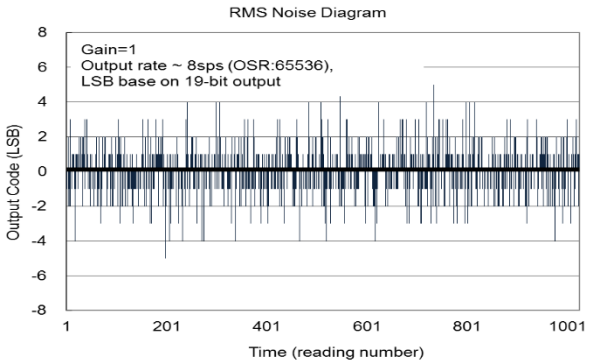


Figure 5.2.7-10 Output Code Diagram

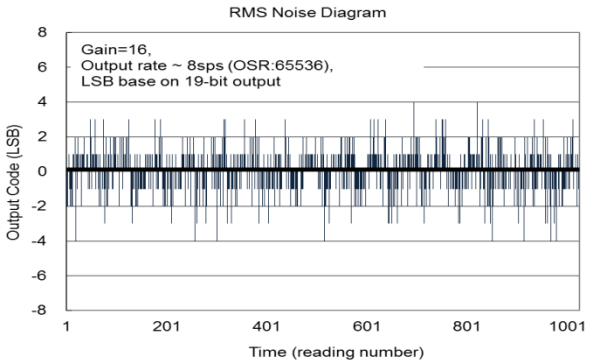


Figure 5.2.7-11 Output Code Diagram

5.2.7.3. ΣΔADC Temperature Sensor

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TC_S	Sensor temperature drift			173		uV/℃
KT	Absolute Temperature Scale 0°K			-272		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~85℃		±2		℃

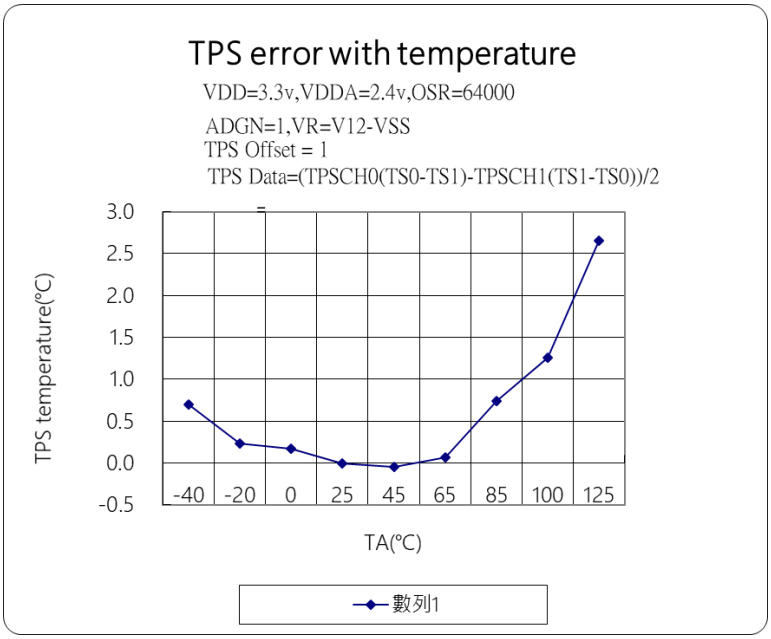


Figure 5.2.7-12 TPS Temperature Error

5.2.8. Rail to Rail OPAMP1、OPAMP2、OPAMP3

T_A = 25℃,V_{DD1}= 3.0V, VDDA1=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDDA1	Power supply		2.4		4.5	V
V_{OUT}	Output range		0		VDDA1	V
V_{IN}	Input common range		0		VDDA1	V
I_{OPA}	OPAMP current			360		uA
I_{OPA_LOAD}	Output current loading (push or pull)	VDDA1 = 3.0V, 0.3V< Output voltage <VDDA1-0.3V			1	mA
		VDDA1 = 2.4V, 0.3V< Output voltage <VDDA1-0.3V			0.5	mA
C_{LOAD}	Max output capacitor load				1	nF
SR	Slew rate	Loading R=10K, C=100pF, 0.3V → VDDA1-0.3V		0.6		V/uS
UGB	Unit gain bandwidth	Loading C=100pF		1000		KHz
V_{OS}	Offset error	Vin = 1.2V	-5		+5	mV
DFD	Digital filter delay	VDDA1 = 3.0V		2		uS
C_{SA}	Sample capacitor			10		pF

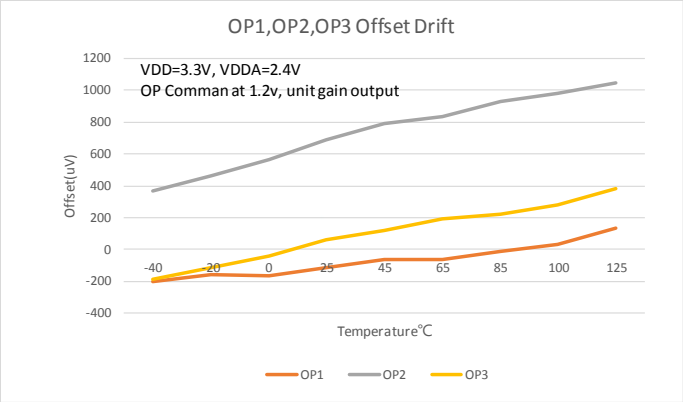


Figure5.2.8-1 Rail to Rail OPAMP 1~3 Offset Drift with Temperature

5.2.9. 12-Bit Resistance Ladders

Typical values are at T_A=25℃ and VDD1= 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Resolution		Monotonic		12		Bit
	Power Supply		2.4		VDDA1	V
	Operation current			50		uA
V_{OUT}	Output range	Output is between Vrefp and Vrefn	0		VDDA1	V
V_{REFP}	Positive reference voltage range	$V_{REFP} > V_{REFN}$	0		VDDA1	V
V_{REFN}	Negative reference voltage range		0		VDDA1	V
R_{LADDER}	One LSB resistance ladder			200		Ω
INL	Integral linearity error	Vrefp = 2.4V, Vrefn = 0V			±3	LSB
DNL	Differential linearity error	Vrefp = 2.4V, Vrefn = 0V			±1	LSB
E_{OS}	Offset error	Vrefp = 2.4V, Vrefn = 0V			1	LSB

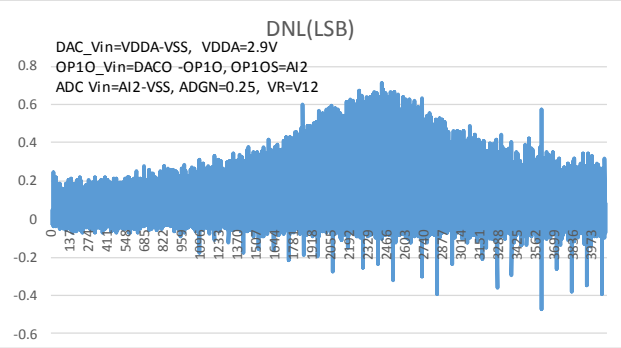


Figure 5.2.9-1 DNL(LSB)

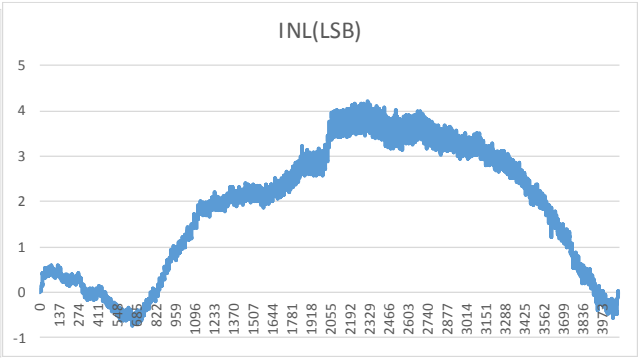


Figure 5.2.9-2 INL(LSB)

5.2.10. BIA Module

T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
IAM1	Active mode 1	HAO =8.5MHz, CPU_CK =8.5MHz VDDA=2.4V、ENADC、ENACM ADC_CK=8.5M/8 SinWave=50K Vpp=200mV		1840		uA
HAO：Internal High Accuracy Oscillator frequency.						

T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Err1	Avg/S.D	(10K//1nF)//10K SinWave=5K Vpp=200mV			0.1	CV
Err2		(10K//1nF)//10K SinWave=10K Vpp=200mV			0.1	CV
Err3		(100K//1nF)//100K SinWave=5K Vpp=200mV			0.1	CV
Err4		(100K//1nF)//100K SinWave=10K Vpp=200mV			0.1	CV
S.D：standard deviation						

6. 订货信息

下单品名 [1]	封装型式	引脚数	封装型式描述方式		程序码编号 [2]	出货包装形式	个装数量	材料组成	MSL[3]
HY16F3913-L100	LQFP	100	L	100	-	Tray	90	Green[4]	MSL-3
HY16F3913-N088	QFN	88	N	088	-	Tray	168	Green[4]	MSL-3

[1] 产品名称品名封装型式描述方式装型程序码编号（空白片 / 标准品 / 代客烧录码）:

例如 : 您的需求是 HY16F3913 不带程序码的空白片且需要的产品是封装片 LQFP100 出货 , 则下单品名为 HY16F3913-L100，且需以 Tray 出货，则除下单品名外，请特别注明出货包装形式为 Tray

例如：您的 HY16F3913 代客烧录服务申请的程序码编号为 009，而需求的产品是封装片 LQFP100 出货，则下单品名为 HY16F3913-L100-009，且需以 Tray 出货，则除下单品名外，请特别注明出货包装形式为 Tray

例如：您的需求是 HY16F3913 不带程序码的空白片且需要的产品是封装片 QFN88 出货，则下单品名为 HY16F3913-N088，且需以 Tray 出货，则除下单品名外，请特别注明出货包装形式为 Tray

例如：您的 HY16F3913 代客烧录服务申请的程序码编号为 001，而需求的产品是封装片 QFN88 出货，则下单品名为 HY16F3913-N088-001，且需以 Tray 出货，则除下单品名外，请特别注明出货包装形式为 Tray

[2] 程序码编号：

“式码编号装形式为外，请为标准品或代客烧录申请的程序码编号，而空白芯片不带此码。

[3] MSL:

湿度敏感性等级系依据 IPC/JEDEC J-STD-020 的规范加以试验分级，并参考 IPC/JEDEC J-STD-033 的标准处理、包装、运输与使用。

[4] Green (RoHS & no Cl/Br):

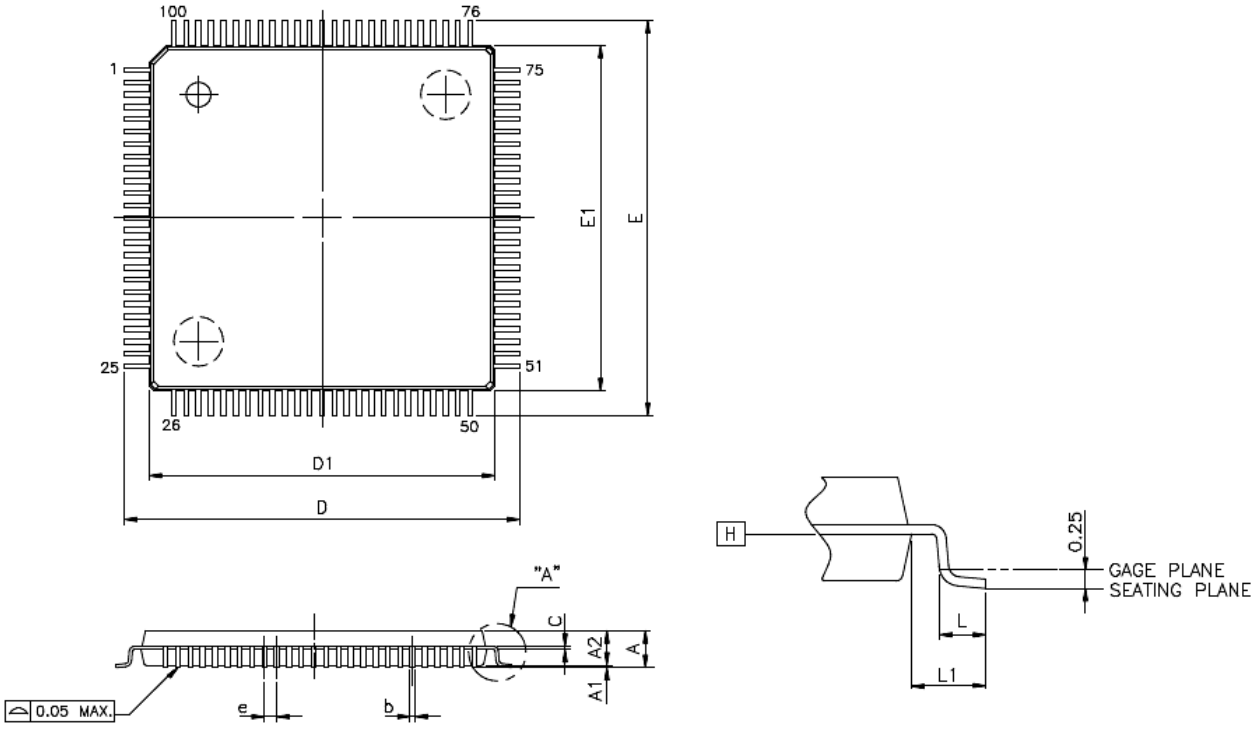
HYCON 产品皆为 Green Product，符合 RoHS 指令，REACH 高关注物质(SVHC)以及无卤素规定 (Br<900ppm or Cl<900ppm or (Br+Cl)<1500ppm)。

7. 封装尺寸信息

7.1. LQFP100(L100)

7.1.1. Package Dimensions LQFP100(14x14)

Unit: mm



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	0.127	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		

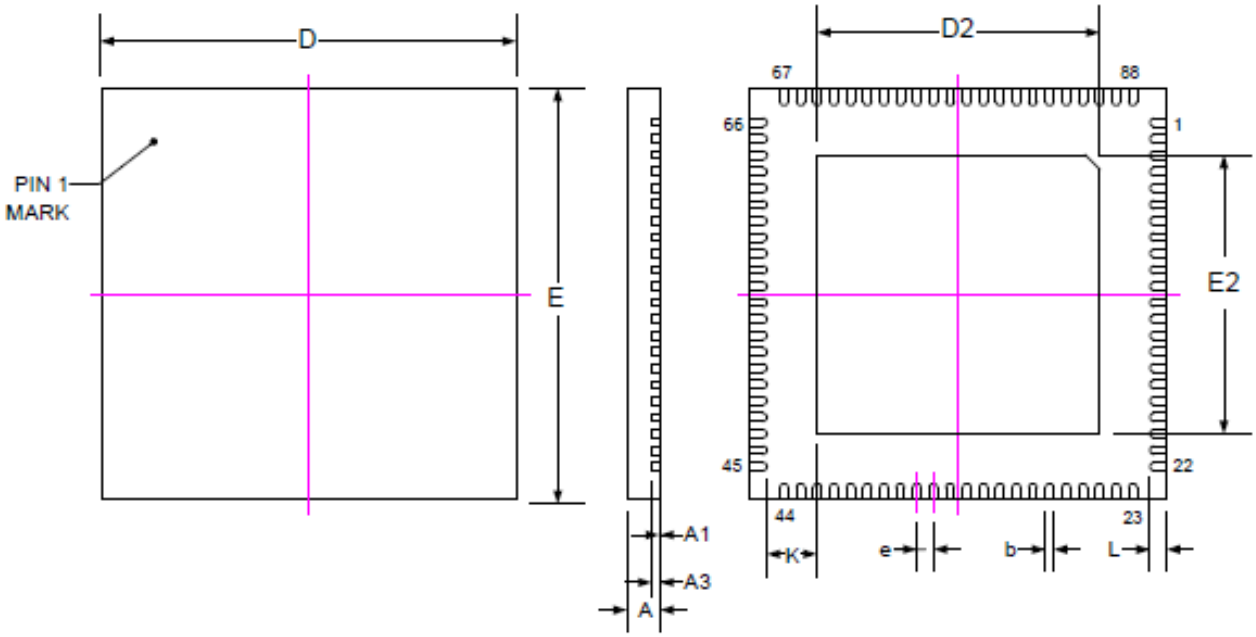
Note:

1. All dimensions refer to JEDEC OUTLINE MS-026.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

7.2. QFN88(N088)(TYPE1)

7.2.1. Package Dimensions QFN88(10x10)

Unit: mm

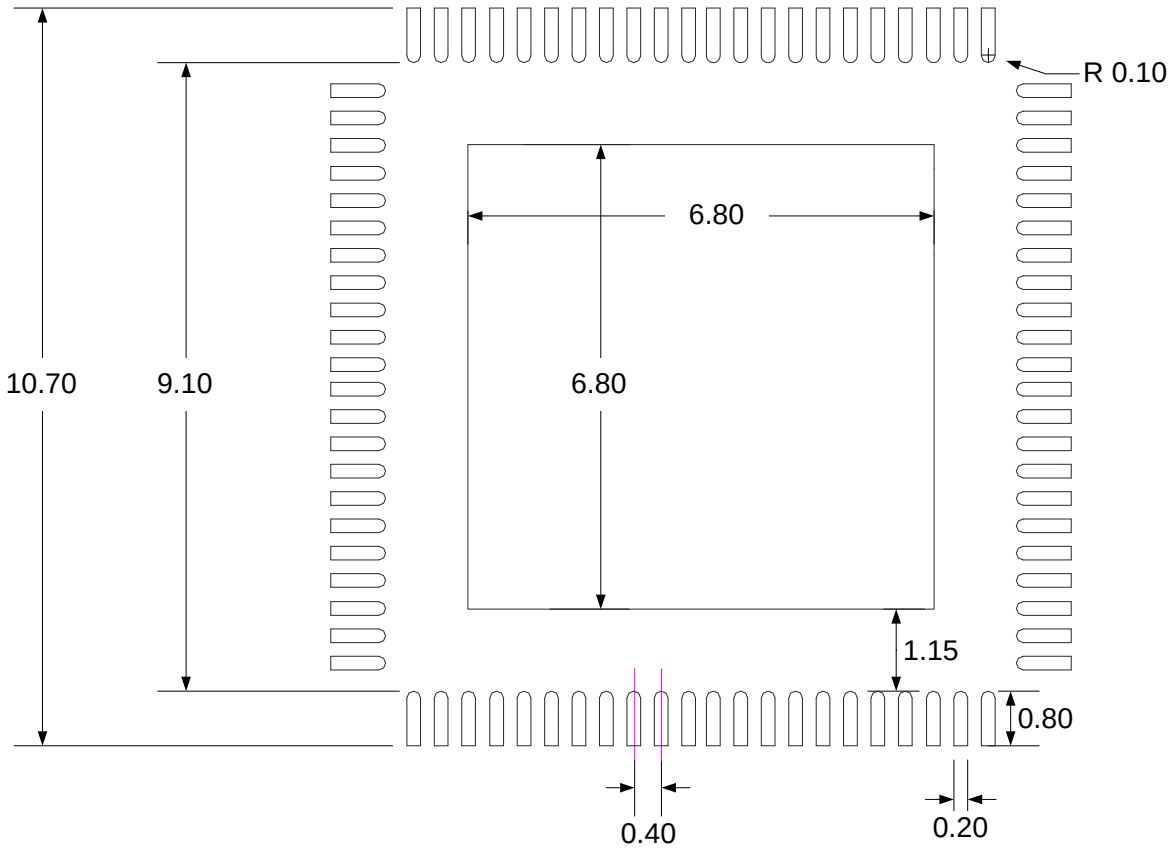


SYMBOLS	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.15	0.20	0.25
D		10.00 BSC	
E		10.00 BSC	
e		0.40 BSC	
D2	6.75	6.80	6.85
E2	6.75	6.80	6.85
L	0.30	0.40	0.50
K	1.08	1.20	1.33

Note:

1. All dimensions refer to JEDEC OUTLINE MO-220.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.
4. https://www.hycontek.com/wp-content/uploads/QFN_DFN_PCB.pdf

7.2.2. Land Pattern Design Recommendations



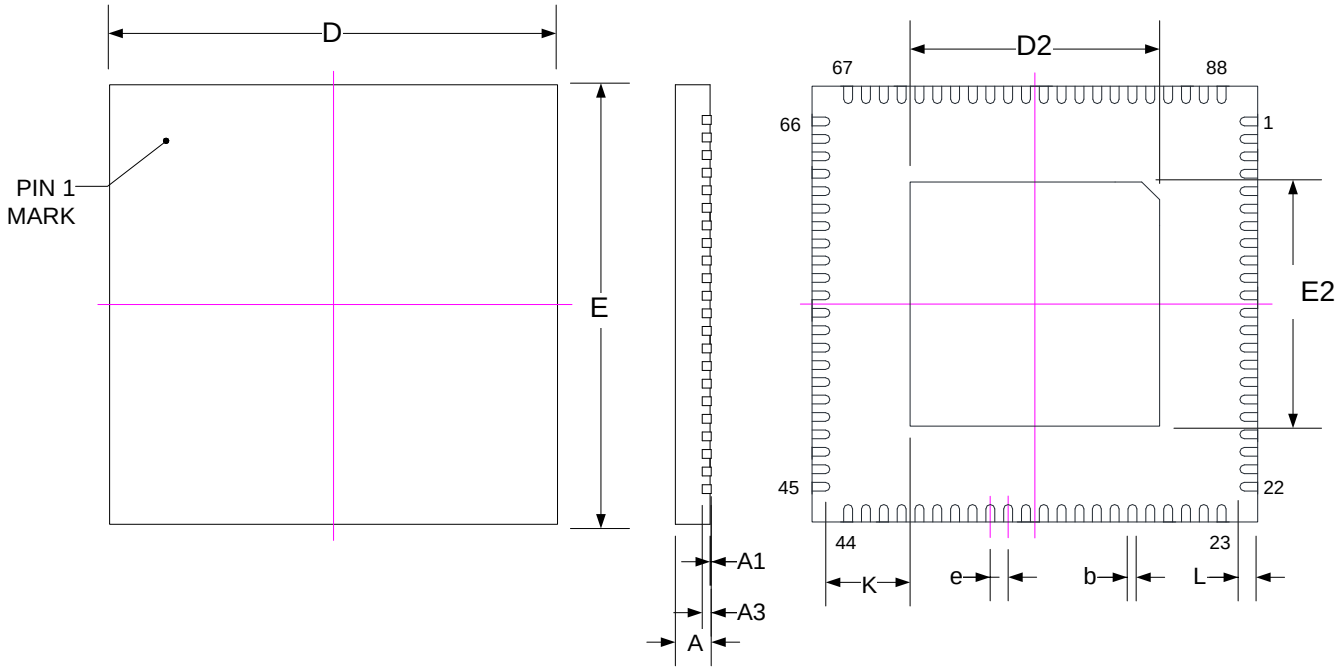
Note:

1. Publication IPC-7351 is recommended for alternate designs
2. Unit : mm

7.3. QFN88(N088)(TYPE2)

7.3.1. Package Dimensions QFN88(10x10)

Unit: mm

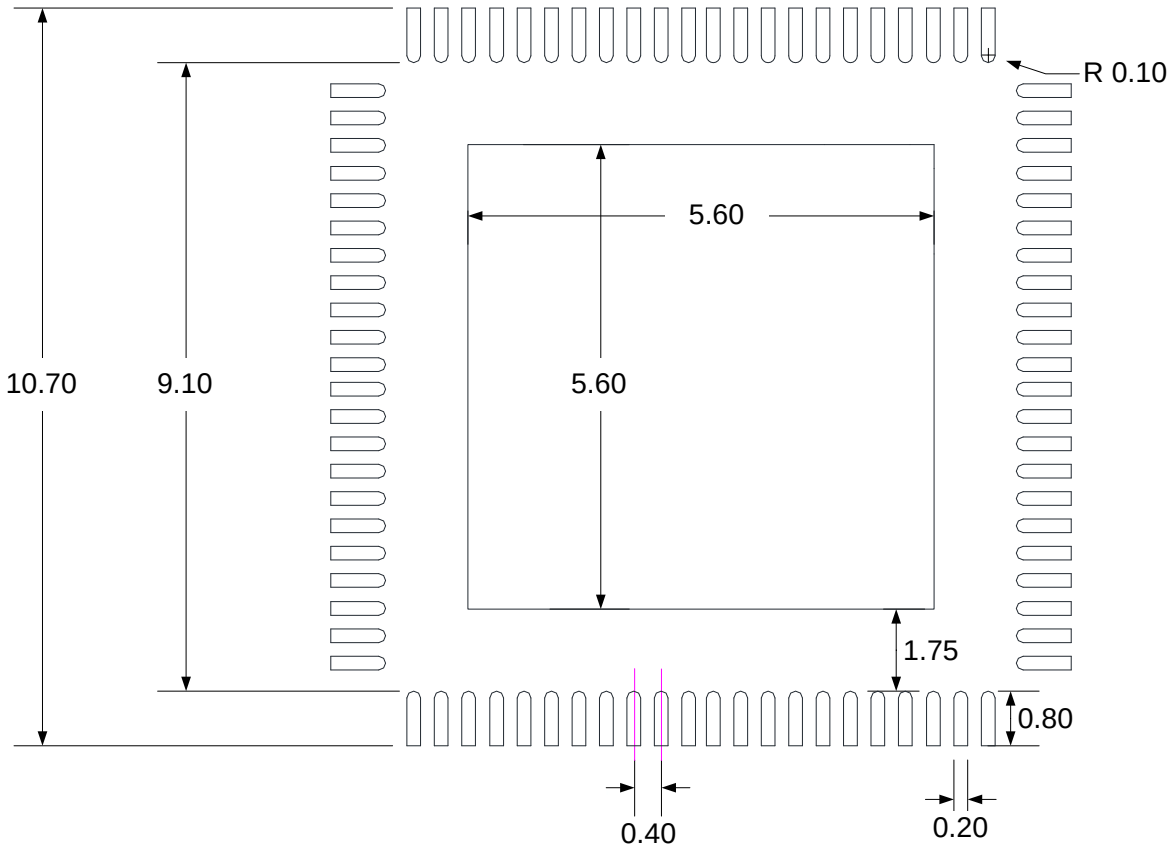


SYMBOLS	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.15	0.20	0.25
D		10.00 BSC	
E		10.00 BSC	
e		0.40 BSC	
D2	5.45	5.60	5.75
E2	5.45	5.60	5.75
L	0.30	0.40	0.50
K	1.62	1.80	1.98

Note:

1. All dimensions refer to JEDEC OUTLINE MO-220.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.
4. https://www.hycontek.com/wp-content/uploads/QFN_DFN_PCB.pdf

7.3.2. Land Pattern Design Recommendations



Note:

1. Publication IPC-7351 is recommended for alternate designs
2. Unit : mm

8. 修订记录

以下描述本文件差异较大的地方，而标点符号与字形的改变不在此描述范围。

文件版次	页次	日期	摘要
V01	ALL	2022/11/17	初版发行