



HY11P14
Datasheet
8-Bit RISC-Like Mixed Signal Microcontroller
Embedded 4x40 LCD Driver
Low Noise Amplifier
18-Bit $\Sigma\Delta$ ADC

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1. Features

- 8-bit RISC, 66 instructions included.
- Operating voltage range: 2.2V to 3.6V, operation temperature range: -40°C ~85°C.
- External Crystal Oscillator and Internal High Precision RC Oscillator, 6 CPU clock rates enable users to have the most power-saving plan.
 - Active Mode 300uA@2MHz
 - Standby Mode 3uA@32KHz
 - Sleep Mode 1uA
- 8K Word OTP (One Time Programmable) Type program memory, 512 Byte Data Memory.
- Brownout detector and Watch dog Timer, prevents CPU from Crash.
- 18-bit fully differential input Sigma-Delta Analog-to-Digital Converter (A/D)
 - Build-in PGA (Programmable Gain Amplifier) 1/4x · 1/2x · 1x. ...128x, 10 input signal gain selection.
 - Build-in Input zero point adjustment can increase measurement range according to different application.
 - Built-in high impedance input buffer (Not suitable for 4x or upwards input gain).
 - Built-in absolute temperature sensor
- Ultra-Low input noise (<1uVpp) OPAMP provides high output impedance small signal amplification and low current voltage transformation.
- 1.0V, 1.2V low temperatures drift parameter internal analog circuit common ground that equips with Push-Pull drive ability to provide sensor driving voltage.
- LVD low voltage detection function has 14 steps of voltage detect configuration and external input voltage detectable function.
- VDDA can select 4 different output voltage that equips with 10mA low dropout regulator function.
- 4x40 LCD driver
 - Static, 1/2, 1/3, 1/4 Duty and 1/3 Bias programmable option
 - Embedded Charge Pump Regulated Circuit with 4 LCD Bias Voltage.
- Enhanced comparator
 - Two sets power voltage generator
 - Equipped with 0.25x or 0.5x operating voltage comparison and auto-transformation function and 15 steps comparison voltage setup
 - Built-in temperature sensor
- 8-bit Timer A
- 16-bit Timer B Module has Capture/Compare function
- 8-bit Timer C Module generates PWM/PFD waveform
- Serial Communication SPI and EUART Module
- Support 8 stack level

2. Pin Definition

2.1 LQFP100 Pin Diagram

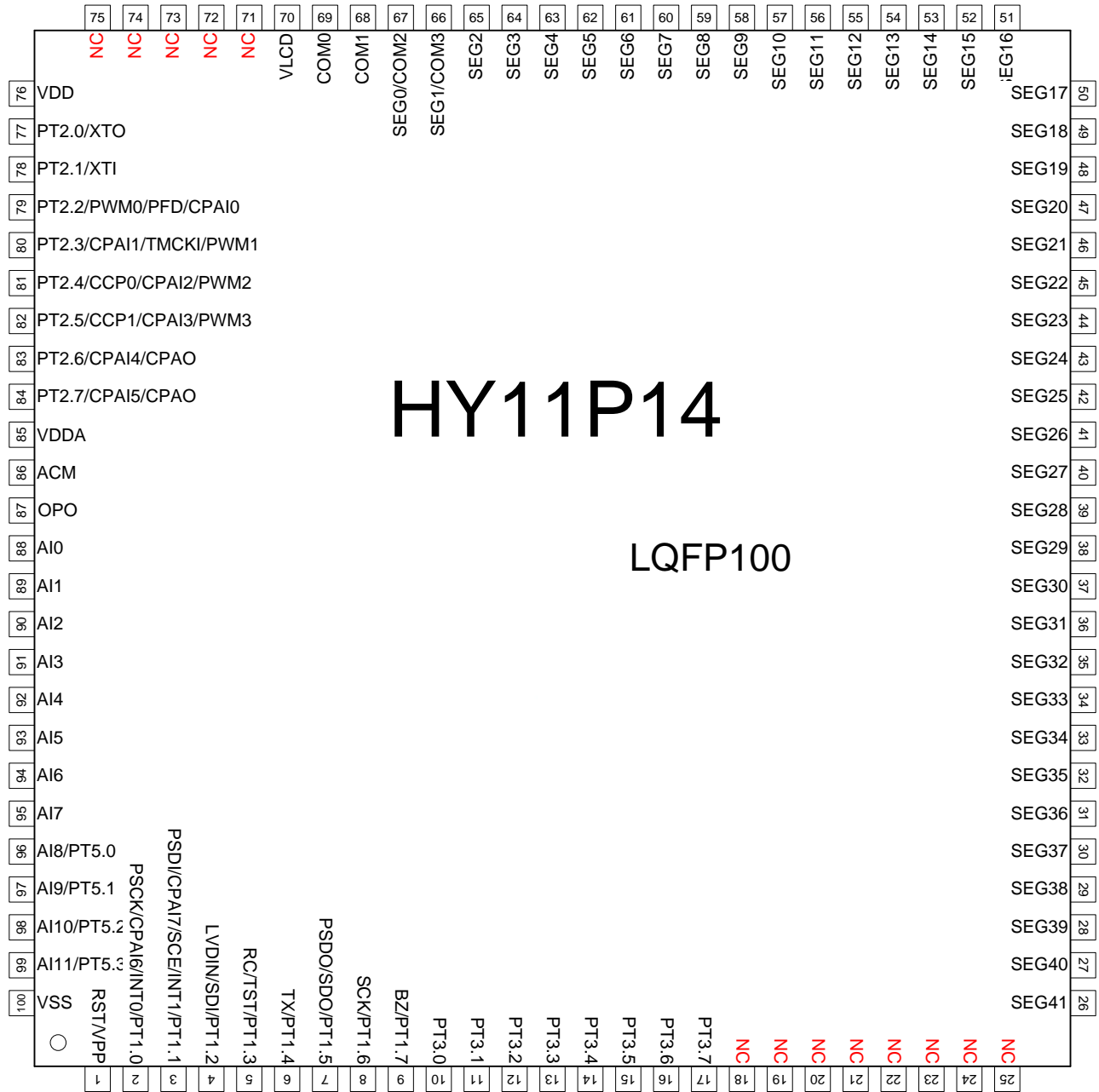


Figure 2-1 HY11P14 LQFP100 Pin Diagram

Note 1 : VPP and RST use the same pin. Input voltage cannot exceed 5.8V when not programming EPROM.

Note 2 : TST and PT1.3 use the same pin. Input voltage cannot exceed Vdd+0.3V while operating.

Note 3 : If PT1.3 is not configured as external button pin, it will enhance the anti-interference ability.

2.2 LQFP64 Pin Diagram

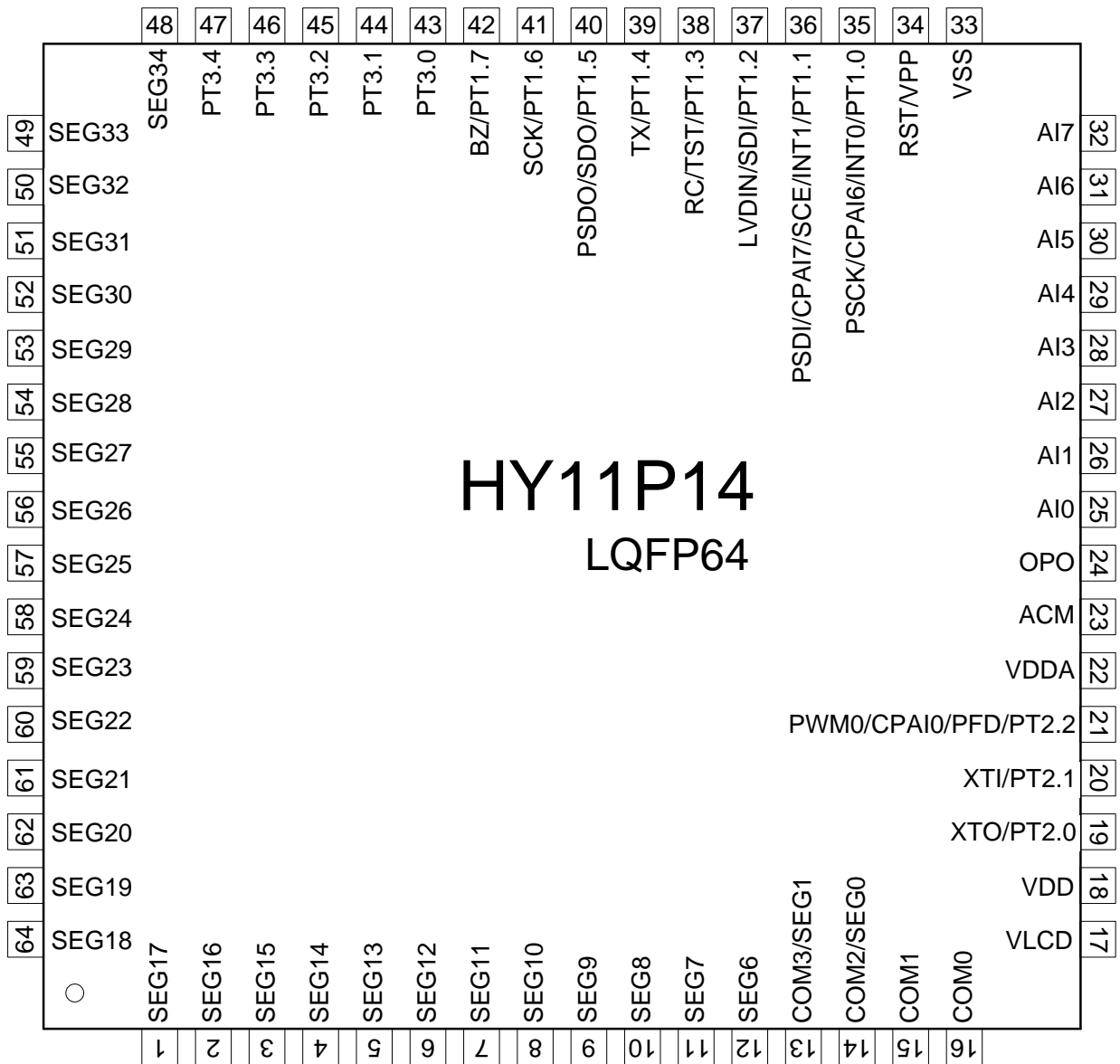


Figure 2-2 HY11P14 LQFP64 Pin Diagram

Note 1 : VPP and RST use the same pin. Input voltage cannot exceed 5.8V when not programming EPROM.

Note 2 : TST and PT1.3 use the same pin. Input voltage cannot exceed Vdd+0.3V while operating.

Note 3 : If PT1.3 is not configured as external button pin, it will enhance the anti-interference ability.

2.3 Pin Description

"I/O" input/output, "I" input, "O" output, "S" Smith Trigger, "C" CMOS features compatible input/output, "P" power supply, "A" analog channel

LQFP64 Pin No.	LQFP100 Pin No.	Pin Name	Pin Characteristic		Description
			Pin Type	Buffer Type	
34	1	RST	I	S	Reset IC
		VPP	P	P	EPROM Programming voltage input
35	2	PT1.0/INT0/PSCK/CPAI6			
		PT1.0	I	S	Digital input
		INT0	I	S	Interrupt input INT0
		PSCK	I	S	OTP programming interface SCK
		CPAI6	I	A	ECPA analog input channel
36	3	PT1.1/INT1/PSDI/SC E/CPAI7			
		PT1.1	I	S	Digital input
		INT1	I	S	Interrupt input INT1
		PSDI	I	S	OTP programming interface SDI
		SCE	I/O	S	SPI communication interface SCE
		CPAI7	I	A	ECPA analog input channel
37	4	PT1.2/SDI/LVDIN			
		PT1.2	I	S	Digital input
		SDI	I/O	S	SPI communication interface SDI
		LVDIN	A	A	LVD external signal input port
38	5	PT1.3/TST/RC			
		PT1.3	I	S	Digital input
		RC	I	S	EUART communication interface RC
		TST	I	S	Test Mode input pin (invalid)
39	6	PT1.4/TX			
		PT1.4	I/O	S	Digital I/O
		TX	I/O	S	EUART communication interface TX
40	7	PT1.5/PSDO/SDO			
		PT1.5	I/O	S	Digital I/O
		PSDO	O	C	OTP programming interface SDO
		SDO	I/O	S	SPI communication interface SDO
41	8	PT1.6/SCK			
		PT1.6	I/O	S	Digital I/O
		SCK	I/O	S	SPI communication interface SCK
42	9	PT1.7/BZ			

		PT1.7 BZ	I/O O	S C	Digital I/O Buzzer output
43	10	PT3.0	I/O	C	Digital I/O
44	11	PT3.1	I/O	C	Digital I/O
45	12	PT3.2	I/O	C	Digital I/O
46	13	PT3.3	I/O	C	Digital I/O
47	14	PT3.4	I/O	C	Digital I/O
-	15	PT3.5	I/O	C	Digital I/O
-	16	PT3.6	I/O	C	Digital I/O
-	17	PT3.7	I/O	C	Digital I/O
-	18	NC	-	-	Unused
-	19	NC	-	-	Unused
-	20	NC	-	-	Unused
-	21	NC	-	-	Unused
-	22	NC	-	-	Unused
-	23	NC	-	-	Unused
-	24	NC	-	-	Unused
-	25	NC	-	-	Unused
-	26	SEG41	O	A	Segment output for LCD
-	27	SEG40	O	A	Segment output for LCD
-	28	SEG39	O	A	Segment output for LCD
-	29	SEG38	O	A	Segment output for LCD
-	30	SEG37	O	A	Segment output for LCD
-	31	SEG36	O	A	Segment output for LCD
-	32	SEG35	O	A	Segment output for LCD
48	33	SEG34	O	A	Segment output for LCD
49	34	SEG33	O	A	Segment output for LCD
50	35	SEG32	O	A	Segment output for LCD
51	36	SEG31	O	A	Segment output for LCD
52	37	SEG30	O	A	Segment output for LCD
53	38	SEG29	O	A	Segment output for LCD
54	39	SEG28	O	A	Segment output for LCD
55	40	SEG27	O	A	Segment output for LCD
56	41	SEG26	O	A	Segment output for LCD
57	42	SEG25	O	A	Segment output for LCD
58	43	SEG24	O	A	Segment output for LCD
59	44	SEG23	O	A	Segment output for LCD

60	45	SEG22	O	A	Segment output for LCD
61	46	SEG21	O	A	Segment output for LCD
62	47	SEG20	O	A	Segment output for LCD
63	48	SEG19	O	A	Segment output for LCD
64	49	SEG18	O	A	Segment output for LCD
1	50	SEG17	O	A	Segment output for LCD
2	51	SEG16	O	A	Segment output for LCD
3	52	SEG15	O	A	Segment output for LCD
4	53	SEG14	O	A	Segment output for LCD
5	54	SEG13	O	A	Segment output for LCD
6	55	SEG12	O	A	Segment output for LCD
7	56	SEG11	O	A	Segment output for LCD
8	57	SEG10	O	A	Segment output for LCD
9	58	SEG9	O	A	Segment output for LCD
10	59	SEG8	O	A	Segment output for LCD
11	60	SEG7	O	A	Segment output for LCD
-	61	SEG6	O	A	Segment output for LCD
-	62	SEG5	O	A	Segment output for LCD
-	63	SEG4	O	A	Segment output for LCD
-	64	SEG3	O	A	Segment output for LCD
-	65	SEG2	O	A	Segment output for LCD
13	66	COM3/SEG1	O	A	COM/segment output for LDO
14	67	COM2/SEG0	O	A	COM/segment output for LDO
15	68	COM1	O	A	COM output for LDO
16	69	COM0	O	A	COM output for LDO
17	70	VLCD	P	P	Power supply for LCD
-	71	NC	-	-	Unused
-	72	NC	-	-	Unused
-	73	NC	-	-	Unused
-	74	NC	-	-	Unused
-	75	NC	-	-	Unused
18	76	VDD	P	P	Power supply for IC operation
19	77	PT2.0/XTO	I/O A	S A	Digital I/O External oscillator output
20	78	PT2.1/XTI	I/O	S	Digital I/O

		XTI	A	A	External oscillator input
21	79	PT2.2/PWM0/PFD/CPAI0			
		PT2.2	I/O	C	Digital I/O
		PWM0	O	C	PWM output
		PFD	O	C	PFD output
		CPAI0	I	A	ECPA analog channel pin
-	80	PT2.3/TMCKI/CPAI1/PWM1			
		PT2.3	I/O	S	Digital I/O
		TMCKI	I	S	TIMERC clock source input
		CPAI1	I	A	ECPA analog channel pin
		PWM1	O	C	PWM input
-	81	PT2.4/CCP0/CPAI2/PWM2			
		PT2.4	I/O	S	Digital I/O
		CCP0	I	S	Capture/compare mode signal interface
		CPAI2	I	A	ECPA analog channel pin
		PWM2	O	C	PWM output
-	82	PT2.5/CCP1/CPAI3/PWM3			
		PT2.5	I/O	S	Digital I/O
		CCP1	I	S	Capture/compare mode signal interface
		CPAI3	I	A	ECPA analog channel pin
		PWM3	O	C	PWM output
-	83	PT2.6/CPAI4/CPAO			
		PT2.6	I/O	C	Digital I/O
		CPAI4	I	A	ECPA analog input channel
		CPAO	I	A	ECPA comparator output interface
-	84	PT2.7/CPAI5/CPAO			
		PT2.7	I/O	C	Digital I/O
		CPAI5	I	A	ECPA analog input channel
		CPAO	I	A	ECPA comparator output interface
22	85	VDDA	P	P	Regulator output, analog circuit power source
23	86	ACM	P	P	Internal analog circuit command ground pin
24	87	OPO	A	A	OP output
25	88	AI0	A	A	Analog channel pin
26	89	AI1	A	A	Analog channel pin
27	90	AI2	A	A	Analog channel pin

28	91	AI3		A	A	Analog channel pin
29	92	AI4		A	A	Analog channel pin
30	93	AI5		A	A	Analog channel pin
31	94	AI6		A	A	Analog channel pin
32	95	AI7		A	A	Analog channel pin
-	96	PT5.0/AI8	PT5.0 AI8	I A	C A	Digital input Analog channel pin
-	97	PT5.1/AI9	PT5.1 AI9	I A	C A	Digital input Analog channel pin
-	98	PT5.2/AI10	PT5.2 AI10	I A	C A	Digital input Analog channel pin
-	99	PT5.3/AI11	PT5.3 AI11	I A	C A	Digital input Analog channel pin
33	100	VSS		P	P	Grounding pin for IC operation voltage

Table 2-1 Pin Definition and Function Description

3. Application Circuit

3.1 Bridge Sensor

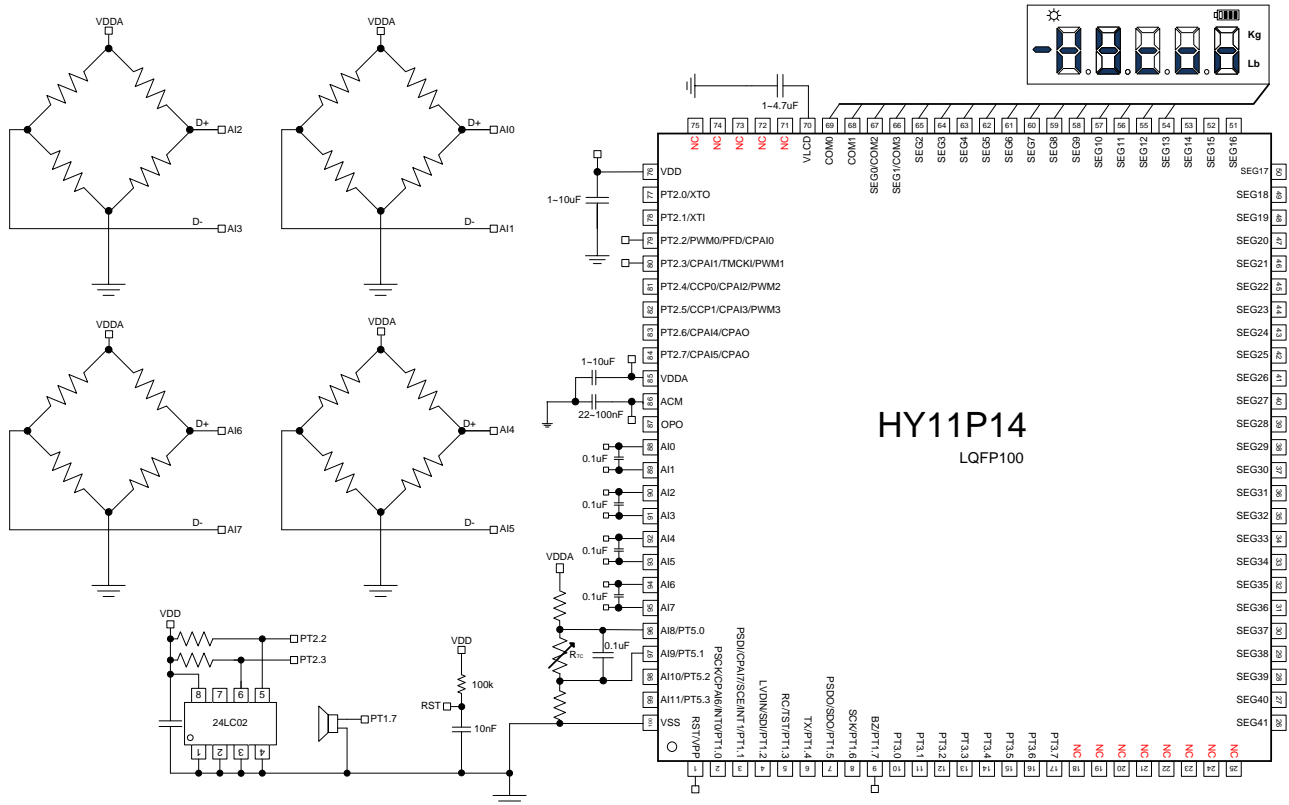


Figure 3-1 Application Circuit of Temperature Compensation Bridge Sensor

Note 1 : Using temperature compensation resistor NTC basic circuit

Note 2 : DCSET[2:0] can conduct bias adjustment of Load Cell zero point voltage address

4. Function Outline

4.1 Internal Block Diagram

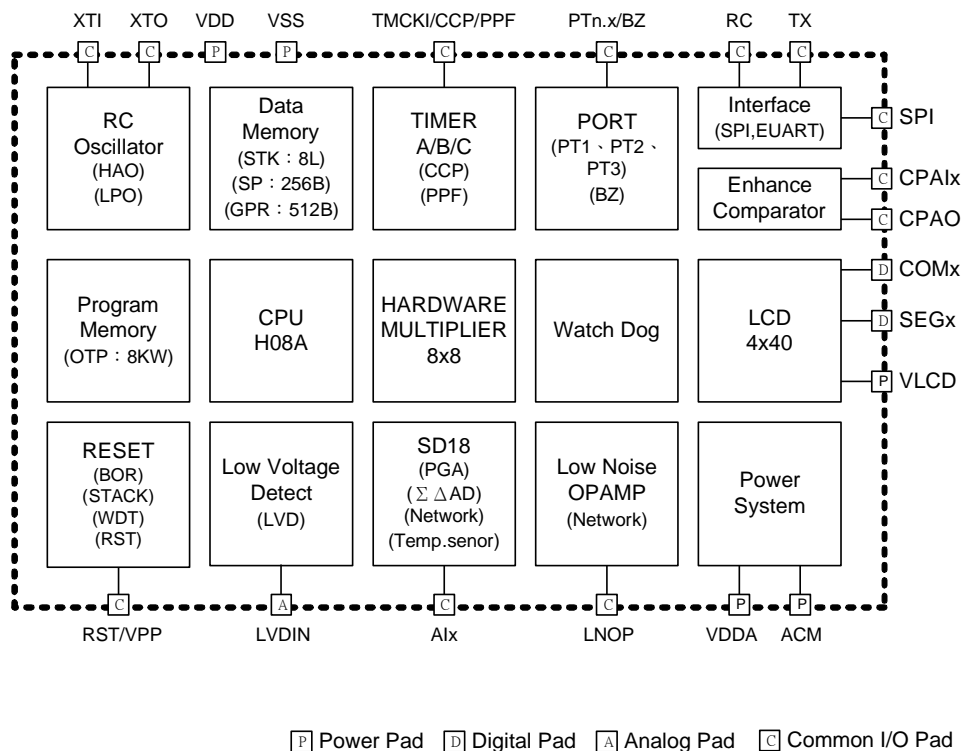


Figure 4-1 HY11P14 Internal Block Diagram

4.2 Related Description and Supporting Documents

IC Function Related Operating Instruction

- DS-HY11P14-Vxx HY11P14 Data Sheet
- UG-HY11S14-Vxx HY11Pxx Series Users' Manual
- APD-CORE002-Vxx H08A Instruction Description

Development Tool Related Operating Instruction

- APD-HYIDE006-Vxx HY11xxx Series Development Tool Software
Instruction Manual
- APD-HYIDE005-Vxx HY11xxx Series Development Tool Hardware
Instruction Manual
- APD-OTP001-Vxx OTP Products Programming Pin Manual

Product Production Related Operating Instruction

- APD-HYIDE004-Vxx HY1xxxx Series Production Line Specialized
Programmer Manual
- BDI-HY11P14-Vxx HY11P14 Individual Product Die Bonding Information

4.3 SD18 Network

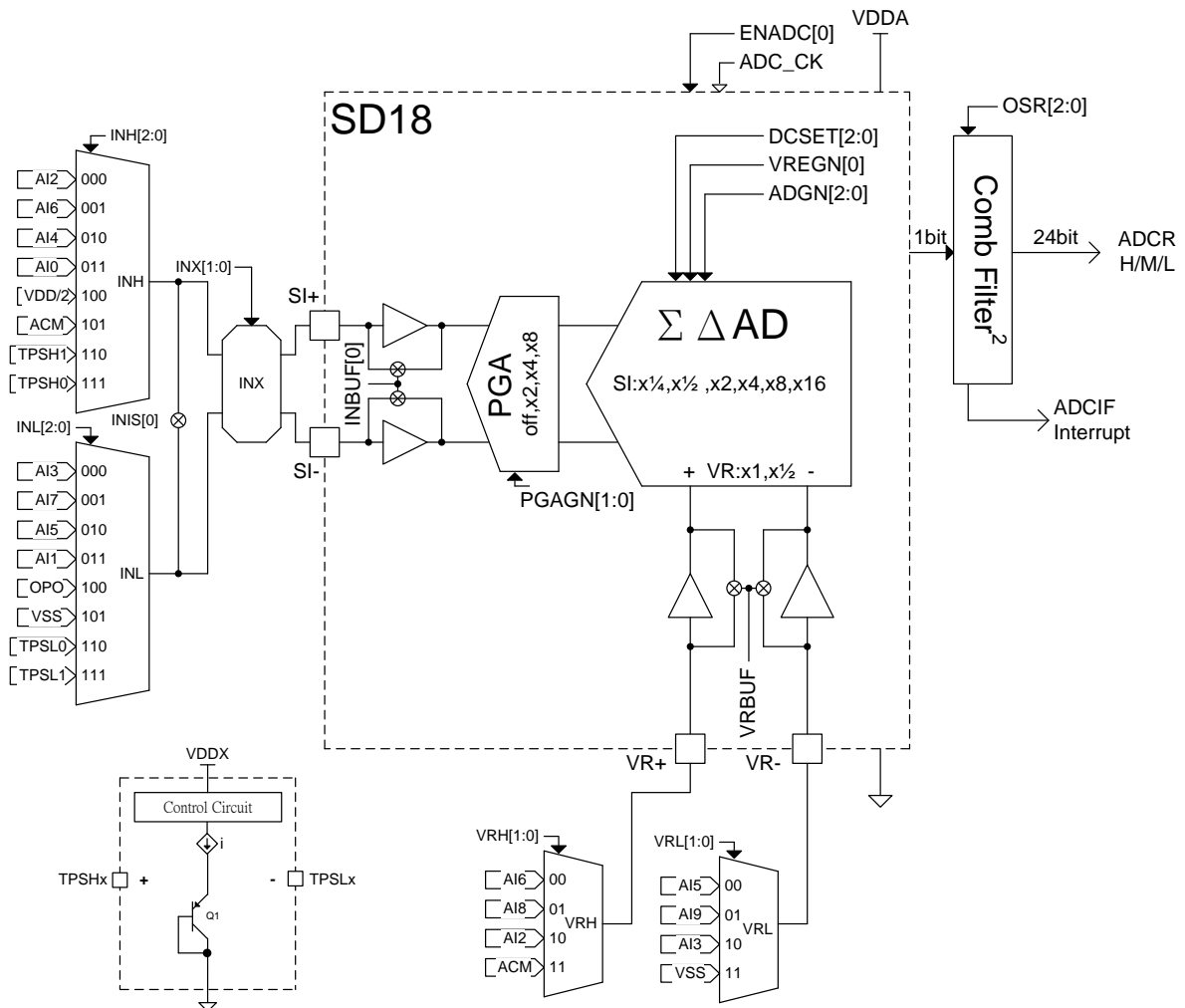


Figure 4-2 SD18 Network

4.4 Low Noise OPAMP Network

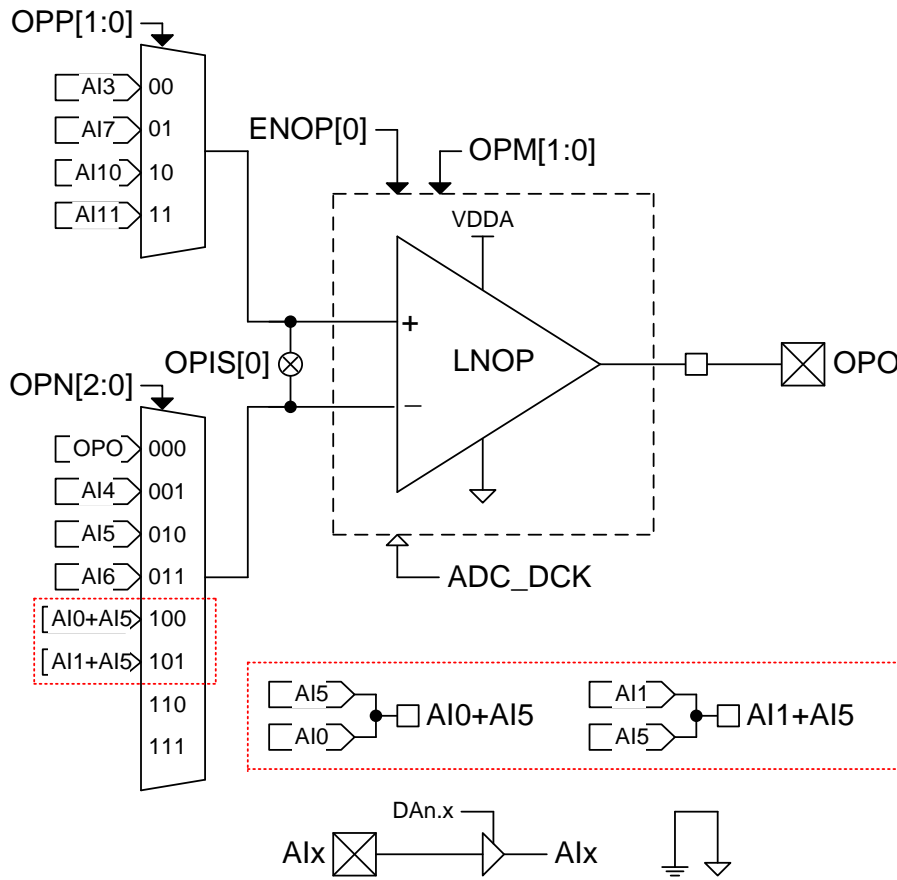


Figure 4-3 Low Noise OPAMP Network

4.5 Enhance Comparator Network

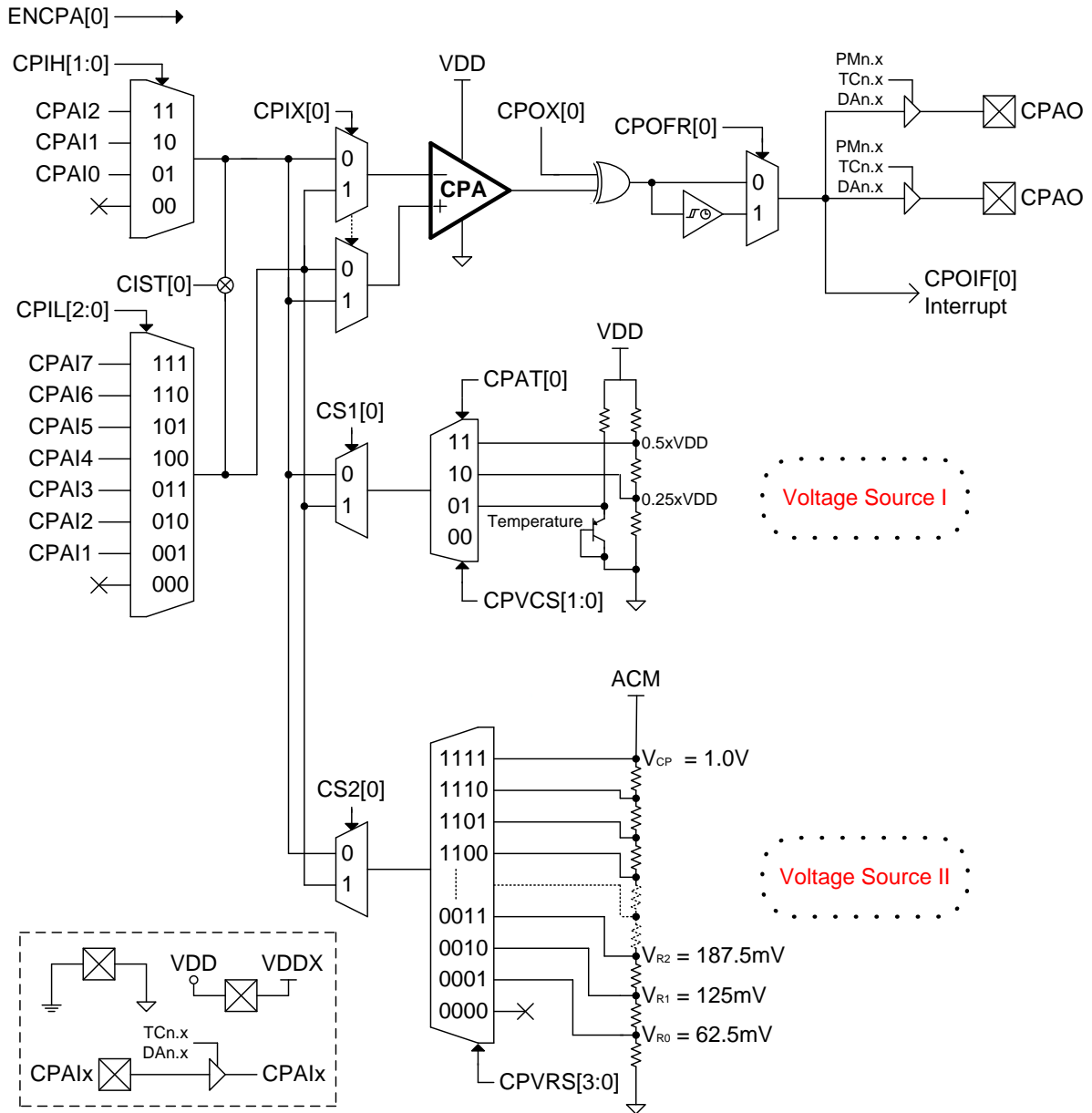


Figure 4-4 Enhance Comparator Network

5. Register List

"-"no use,"**"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1 "u"unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition															
Address	File Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A-RESET	i-RESET	R/W			
00H	INDF0	Contents of FSR0 to address data memory value of FSR0 not changed								N/A	N/A	*****			
01H	POINC0	Contents of FSR0 to address data memory value of FSR0 post-incremented								N/A	N/A	*****			
02H	PODEC0	Contents of FSR0 to address data memory value of FSR0 post-decremented								N/A	N/A	*****			
03H	PRINC0	Contents of FSR0 to address data memory value of FSR0 pre-incremented								N/A	N/A	*****			
04H	PLUSW0	Contents of FSR0 to address data memory value of FSR0 offset by W								N/A	N/A	*****			
05H	INDF1	Contents of FSR1 to address data memory value of FSR0 not changed								N/A	N/A	*****			
06H	POINC1	Contents of FSR1 to address data memory value of FSR0 post-incremented								N/A	N/A	*****			
07H	PODEC1	Contents of FSR1 to address data memory value of FSR0 post-decremented								N/A	N/A	*****			
08H	PRINC1	Contents of FSR1 to address data memory value of FSR0 pre-incremented								N/A	N/A	*****			
09H	PLUSW1	Contents of FSR1 to address data memory value of FSR0 offset by W								N/A	N/A	*****			
0FH	FSR0H									FSR0[9]	FSR0[8]xx ..uu	r,r,r,r,r,r,r,r		
10H	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*****			
11H	FSR1H									FSR1[9]	FSR1[8]xx ..uu	r,r,r,r,r,r,r,r		
12H	FSR1L	Indirect Data Memory Address Pointer 1 Low Byte,FSR1[7:0]								xxxx xxxx	uuuu uuuu	*****			
16H	TOSH					TOS[12]	TOS[11]	TOS[10]	TOS[9]	TOS[8]	...0 0000	...0 0000	*****		
17H	TOSL	Top-of-Stack Low Byte (TOS<7:0>)											0000 0000	0000 0000	*****
18H	STKPTR	STKFL	STKUN	STKOV	STKPTR[3:0]								000. 0000	000. 0000	r,rw0,rw0-,r,r,r,r
1AH	PCLATH					PC[12]	PC[11]	PC[10]	PC[9]	PC[8]	...0 0000	...0 0000	*****		
1BH	PCLATL	PC Low Byte for PC<7:0>											0000 0000	0000 0000	*****
1DH	TBLPTRH					TBLPTR[12]	TBLPTR[11]	TBLPTR[10]	TBLPTR[9]	TBLPTR[8]	...0 0000	...0 0000	*****		
1EH	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)											0000 0000	0000 0000	*****
1FH	TBLDH	Program Memory Table Latch High Byte											0000 0000	0000 0000	*****
20H	TBLDL	Program Memory Table Latch Low Byte											0000 0000	0000 0000	*****
21H	PRODH	Product Register of Multiply High Byte											xxxx xxxx	uuuu uuuu	r,r,r,r,r,r,r,r
22H	PRODL	Product Register of Multiply Low Byte											xxxx xxxx	uuuu uuuu	r,r,r,r,r,r,r,r
23H	INTE1	GIE	ADCIE	TMCIIE	TMBIE	TMAIE	WDTIE	E1IE	E0IE	0000 0000	0000 0000	*****			
24H	INTE2	TXIE	RCIE			CPOIE	SSPIE	CCP1IE	CCP0IE	00.. 0000	00.. 0000	*****			
26H	INTF1		ADCIF	TMCIF	TMBIF	TMAIF	WDTIF	E1IF	E0IF	.000 0000	.000 0000	*****			
27H	INTF2	TXIF	RCIF			CPOIF	SSPIF	CCP1IF	CCP0IF	00.. 0000	00.. 0000	*****			
29H	WREG	Working Register											xxxx xxxx	uuuu uuuu	*****
2AH	BSRCN									BSR[1]	BSR[0]0000	*****	
2BH	STATUS					C	DC	N	OV	Z	...x xxxx	...u uuuu	*****		
2CH	PSTATUS	PD	TO	IDLEB	BOR		SKERR					000d ..	u0uu ..d	rw0,rw0,rw0,rw0-,rw0,-,r	
2DH	LVDCN		LVDFG	LVD	LVDON	VLDX[3:0]						.000 0000	.000 uuuu	r,r,r,r,r,r,r,r	
30H	PWRCN	ENVDDA	VDDAX[1:0]		ENACM							0000	0000	*****	
31H	MCKCN1	ADCS[2:0]			ADCK	XTHSP	XTSP	ENXT	ENHAO	0000 0001	0000 0001	*****			
32H	MCKCN2		LSCK	HSCK	HSS[1:0]			CPUCK[1:0]			..00 0000	..00 0000	*****		
33H	MCKCN3	LCDS[2:0]					PERCK	BZS[2:0]					000. 0000	000. 0000	*****
34H	CPACN1	ENCPA	CPIST	CPIX	CPIH[1:0]			CPIL[2:0]				0000 0000	0000 0000	*****	
35H	CPACN2	CPOX		CPOFR	CS1	CPAT	CPVCS[1:0]					.000 0000	.000 0000	*****	
36H	CPACN3					CS2	CPVRX[3:0]						...0 0000	...0 0000	*****
37H	OPCN1	ENOP	OPM[1:0]			OPP[1:0]		OPN[2:0]				0000 0000	0000 0000	*****	
39H	ADCRH	ADC conversion memory HighByte											xxxx xxxx	uuuu uuuu	r,r,r,r,r,r,r,r
3AH	ADCRM	ADC conversion memory Middle Byte											xxxx xxxx	uuuu uuuu	r,r,r,r,r,r,r,r
3BH	ADCRL	ADC conversion memory Low Byte											xxxx xxxx	uuuu uuuu	r,r,r,r,r,r,r,r
3CH	ADCCN1	ENADC	ENHIGN	ENCHP	PGAGN[1:0]			ADGN[2:0]				0000 0000	0000 0000	*****	
3DH	ADCCN2		INBUF	VRBUF	VREGN		DCSET[2:0]					..00 0000	..00 0000	*****	
3EH	ADCCN3	OSR[2:0]											000.	000.	*****
3FH	AINET1	INH[2:0]				INL[2:0]			INIS		OPIS		0000 0000	0000 0000	*****
40H	AINET2	VRH[1:0]			INX[1:0]			VRL[1:0]				.000 000.	.000 000.	*****	
41H	TMACN	ENTMA	TMACK	TMAS[1:0]		ENWDT	WDT[2:0]					0000 0000	0000 0000	***** w1,***	
42H	TMAR	TimerA data register											xxxx xxxx	uuuu uuuu	r,r,r,r,r,r,r,r
43H	TMBCN	ENTMB	TMBCK	TMBS[1:0]			TMBSYC	TMBR2R				0000 00..	0000 00..	*****	
44H	TMBRH	TimerB High Byte data register											xxxx xxxx	uuuu uuuu	*****
45H	TMBRL	TimerB Low Byte data register											xxxx xxxx	uuuu uuuu	*****
46H	TMCCN	ENTMC	TMCCK[1:0]		TMCS[2:0]			TMCS0[1:0]				0000 0000	0000 0000	*****	
47H	PRC	TimerC programmable register											1111 1111	1111 1111	*****
48H	TMCR	TimerC register											0000 0000	0000 0000	r,r,r,r,r,r,r,r
49H	CCPCN	CCP1M[3:0]						CCP0M[3:0]					0000 0000	0000 0000	*****
4AH	CCP0RH	CCP0 High Byte data register											xxxx xxxx	uuuu uuuu	*****
4BH	CCP0RL	CCP0 Low Byte data register											xxxx xxxx	uuuu uuuu	*****
4CH	CCP1RH	CCP1 High Byte data register											xxxx xxxx	uuuu uuuu	*****
4DH	CCP1RL	CCP1 Low Byte data register											xxxx xxxx	uuuu uuuu	*****
4EH	PASC	PASF	PASC[1:0]			PSSCN0[1:0]			PSSCN1[1:0]			0.00 0000	0.00 0000	*****	
4FH	PWMCN	ENPWM	ENPFD	PWMRL[1:0]			PWMCG[1:0]		PWMM[1:0]			0000 0000	0000 0000	*****	
50H	PDBD	ENPRS											0000 0000	0000 0000	*****
51H	PWMR	PWM MSB Byte register											xxxx xxxx	uuuu uuuu	*****

Table 5-1(a) HY11P14 Register List

HY11P14
Embedded 18-Bit Σ ADC
8-Bit RISC-Like Mixed Signal Microcontroller



"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1 "u"unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition														
Address	File Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A-RESET	i-RESET	R/W		
52H	LCDCN1	ENLCD	LCDPR	VLCDX[1:0]		LCDBF	LCDB[1:0]			0000 000.	0000 000.	*****		
53H	LCDCN2	LcdbL	LcdmX[1:0]							000.	000.	*****		
54H	LCD0	Segment SEG2@[3:0] and SEG3@[7:4] data register of LCD0										xxxx xxxx	uuuu uuuu	*****
55H	LCD1	Segment SEG4@[3:0] and SEG5@[7:4] data register of LCD1										xxxx xxxx	uuuu uuuu	*****
56H	LCD2	Segment SEG6@[3:0] and SEG7@[7:4] data register of LCD2										xxxx xxxx	uuuu uuuu	*****
57H	LCD3	Segment SEG8@[3:0] and SEG9@[7:4] data register of LCD3										xxxx xxxx	uuuu uuuu	*****
58H	LCD4	Segment SEG10@[3:0] and SEG11@[7:4] data register of LCD4										xxxx xxxx	uuuu uuuu	*****
59H	LCD5	Segment SEG12@[3:0] and SEG13@[7:4] data register of LCD5										xxxx xxxx	uuuu uuuu	*****
5AH	LCD6	Segment SEG14@[3:0] and SEG15@[7:4] data register of LCD6										xxxx xxxx	uuuu uuuu	*****
5BH	LCD7	Segment SEG16@[3:0] and SEG17@[7:4] data register of LCD7										xxxx xxxx	uuuu uuuu	*****
5CH	LCD8	Segment SEG18@[3:0] and SEG19@[7:4] data register of LCD8										xxxx xxxx	uuuu uuuu	*****
5DH	LCD9	Segment SEG20@[3:0] and SEG21@[7:4] data register of LCD9										xxxx xxxx	uuuu uuuu	*****
5EH	SSPCON1	SSPEN	CKP	CKE	SMP	-	-	SSPM<1:0>		0000 ..00	uuuu ..uu	*****		
60H	SSPSTA	SSPBUY	SSPOV	Reserve for IIC						BF	00... ..0	00... ..0	r,r,r,r,r,r,r	
61H	SSPBUF	SSP Receive Buffer/Transmit Register										xxxx xxxx	uuuu uuuu	*****
63H	URCON	ENSP	ENTX	TX9	TX9D	PARITY			WUE	0000 0..0	0000 0..0	*****		
64H	URSTA		RC9D	PERR	FERR	OERR	RCIDL	TRMT	ABDOVF	.000 0110	.000 0110	r,r,r,r,r,r,rw0		
65H	BAUDCON					ENCR	RC9	ENADD	ENABD 0000 0000	*****		
66H	BRGRH	Baud Rate Generator Register High Byte										...x xxxx	...u uuuu	*****
67H	BRGRL	Baud Rate Generator Register Low Byte										xxxx xxxx	uuuu uuuu	*****
68H	TXREG	UART Transmit Register										xxxx xxxx	uuuu uuuu	*****
69H	RCREG	UART Receive Register										xxxx xxxx	uuuu uuuu	r,r,r,r,r,r,r
6DH	PT1	PT1.7	PT1.6	PT1.5	PT1.4	PT1.3	PT1.2	PT1.1	PT1.0	xxxx xxxx	uuuu uuuu	r,r,r,r,r,r,r		
6EH	TRISC1	TC1.7	TC1.6	TC1.5	TC1.4					0000	0000	*****		
6FH	PT1DA						DA1.2	DA1.1	DA1.0000000	*****		
70H	PT1PU	PU1.7	PU1.6	PU1.5	PU1.4	PU1.3	PU1.2	PU1.1	PU1.0	0000 0000	0000 0000	*****		
71H	PT1M1					INTEG1[1:0]		INTEG0[1:0]	 0000 0000	*****		
72H	PT1M2		PM1.7[0]		PM1.6[0]		PM1.5[0]		PM1.4[0]	.0.0 0.0	.0.0 0.0	*****		
74H	PT2	PT2.7	PT2.6	PT2.5	PT2.4	PT2.3	PT2.2	PT2.1	PT2.0	xxxx xxxx	uuuu uuuu	*****		
75H	TRISC2	TC2.7	TC2.6	TC2.5	TC2.4	TC2.3	TC2.2	TC2.1	TC2.0	0000 0000	0000 0000	*****		
76H	PT2DA	DA2.7	DA2.6	DA2.5	DA2.4	DA2.3	DA2.2			0000 00..	0000 00..	*****		
77H	PT2PU	PU2.7	PU2.6	PU2.5	PU2.4	PU2.3	PU2.2	PU2.1	PU2.0	0000 0000	0000 0000	*****		
78H	PT2M1		PM2.3[0]	PM2.2[1]	PM2.2[0]					.000000	*****		
79H	PT2M2	PWMTR[1:0]		PM2.6[0]	PM2.5[1]	PM2.5[0]	PM2.4[1]	PM2.4[0]		00.0 0000	00.0 0000	*****		
7AH	PT3	PT3.7	PT3.6	PT3.5	PT3.4	PT3.3	PT3.2	PT3.1	PT3.0	xxxx xxxx	uuuu uuuu	*****		
7BH	TRISC3	TC3.7	TC3.6	TC3.5	TC3.4	TC3.3	TC3.2	TC3.1	TC3.0	0000 0000	0000 0000	*****		
7DH	PT3PU	PU3.7	PU3.6	PU3.5	PU3.4	PU3.3	PU3.2	PU3.1	PU3.0	0000 0000	0000 0000	*****		
80H ~ FFH		GENERAL PURPOSE REGISTER @ 128Byte										xxxx xxxx	uuuu uuuu	*****
100H~17FH		GENERAL PURPOSE REGISTER @ 128Byte										xxxx xxxx	uuuu uuuu	*****
180H	LCD10	Segment SEG22@[3:0] and SEG23@[7:4] data register of LCD10										xxxx xxxx	uuuu uuuu	*****
181H	LCD11	Segment SEG24@[3:0] and SEG25@[7:4] data register of LCD11										xxxx xxxx	uuuu uuuu	*****
182H	LCD12	Segment SEG26@[3:0] and SEG27@[7:4] data register of LCD12										xxxx xxxx	uuuu uuuu	*****
183H	LCD13	Segment SEG28@[3:0] and SEG29@[7:4] data register of LCD13										xxxx xxxx	uuuu uuuu	*****
184H	LCD14	Segment SEG30@[3:0] and SEG31@[7:4] data register of LCD14										xxxx xxxx	uuuu uuuu	*****
185H	LCD15	Segment SEG32@[3:0] and SEG33@[7:4] data register of LCD15										xxxx xxxx	uuuu uuuu	*****
186H	LCD16	Segment SEG34@[3:0] and SEG35@[7:4] data register of LCD16										xxxx xxxx	uuuu uuuu	*****
187H	LCD17	Segment SEG36@[3:0] and SEG37@[7:4] data register of LCD17										xxxx xxxx	uuuu uuuu	*****
188H	LCD18	Segment SEG38@[3:0] and SEG39@[7:4] data register of LCD18										xxxx xxxx	uuuu uuuu	*****
189H	LCD19	Segment SEG40@[3:0] and SEG41@[7:4] data register of LCD19										xxxx xxxx	uuuu uuuu	*****
192H	PT5					PT5.3	PT5.2	PT5.1	PT5.0 xxxx uuuu	r,r,r,r,r,r,r		
193H	PT5DA					DA5.3	DA5.2	DA5.1	DA5.0 1111 1111	*****		
194H	PT5PU					PU5.3	PU5.2	PU5.1	PU5.0 0000 0000	r,r,r,r,r,r,r		
200H ~ 2FFH		GENERAL PURPOSE REGISTER @ 256Byte										xxxx xxxx	uuuu uuuu	*****

Table 5-1(b) HY11P14 Register List (continued)

6. Electrical Characteristics

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at V_{DD} to V_{SS}	-0.2 V to 4.0 V
Voltage applied to any pin (see Note 1)	-0.2 V to $V_{DD} + 0.3$ V
Voltage applied to RST/VPP pin	-0.2 V to 6.9 V
Voltage applied to TST/PT1.3 pin (see Note 1)	-0.2 V to $V_{DD} + 1$ V
Diode current at any device terminal	± 2 mA
Storage temperature, Tstg: (unprogrammed device)	-55°C to 150°C
(programmed device)	-40°C to 85°C
Total power dissipation	0.5w
Maximum output current sink by any PORT1 to PORT3 I/O pin25mA

6.1 Recommended Operating Conditions

$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$, unless otherwise noted

Sym.	Parameter		Test Conditions	Min.	Typ.	Max.	unit	
V_{DD}	Supply Voltage		All digital peripherals and CPU	2.2		3.6	V	
			Analog peripherals	2.4		3.6		
V_{SS}	Supply Voltage			0		0		
XT	External	Watch crystal	$V_{DD} = 2.2\text{V}$, ENXT[0]=1	XTSP[0]=0, XTHSP[0]=0		32.768K	Hz	
	Oscillator	Ceramic resonator		XTSP[0]=1, XTHSP[0]=0		450K		8M
	Frequency	Crystal		XTSP[0]=1, XTHSP[0]=0		1M		8M

6.2 Internal RC Oscillator

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1	1.8	2.0	2.2	MHz
LPO	Low Power Oscillator frequency	V_{DD} supply voltage be enable LPO	22	28	35	KHz

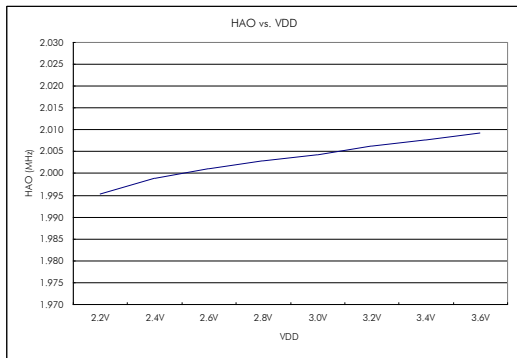


Figure 6.2-1 HAO vs. VDD

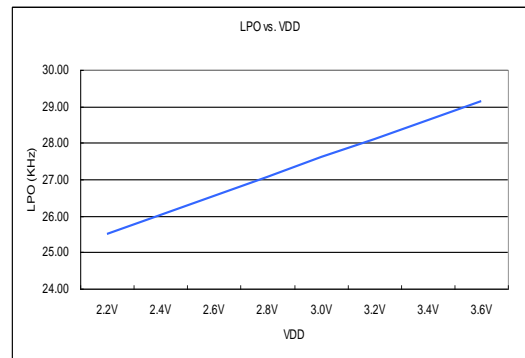


Figure 6.2-2 LPO vs. VDD

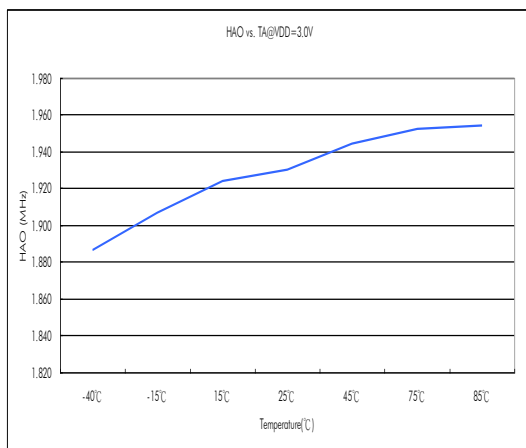


Figure 6.2-3 HAO vs. Temperature

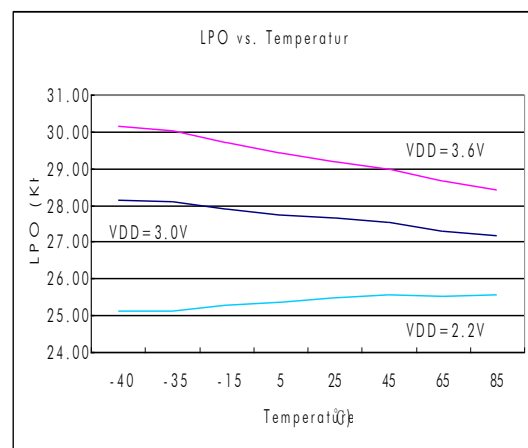


Figure 6.2-4 LPO vs. Temperature

6.3 Supply Current into VDD Excluding Peripherals Current

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{V}$, $\text{OSC_LPO} = 28\text{KHz}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM1}	Active mode 1	OSC_CY = 8MHz, OSC_HAO = off, CPU_CK = 8MHz		1.34	2	mA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 2MHz		0.36	0.55	mA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 1MHz		0.2	0.3	mA
I_{LP1}	Low Power 1	OSC_CY = 32768Hz, OSC_HAO = off, CPU_CK = 16384Hz		7	12	μA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		1.65	3	μA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.65	1.2	μA

OSC_CY : External Oscillator frequency.

OSC_HAO : Internal High Accuracy Oscillator frequency.

CPU_CK : CPU core work frequency.

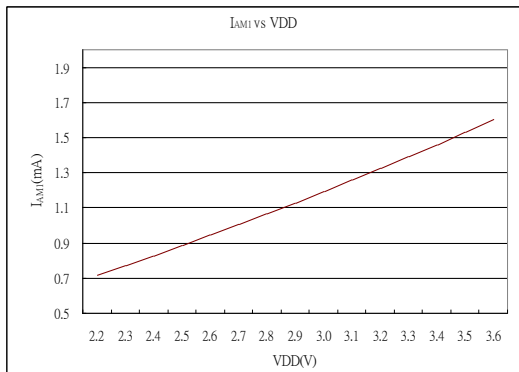


Figure 6.3-1 I_{AM1} vs. VDD

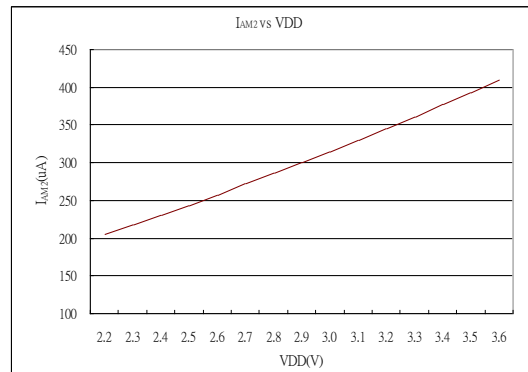


Figure 6.3-2 I_{AM2} vs. VDD

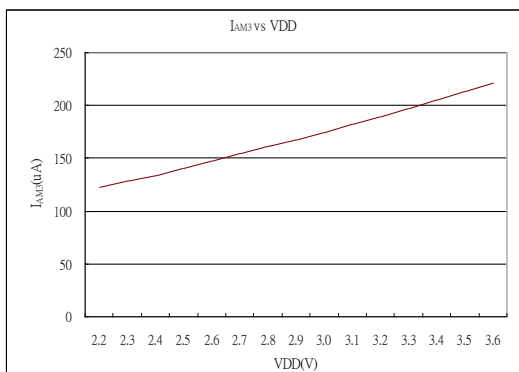


Figure 6.3-3 I_{AM3} vs. VDD

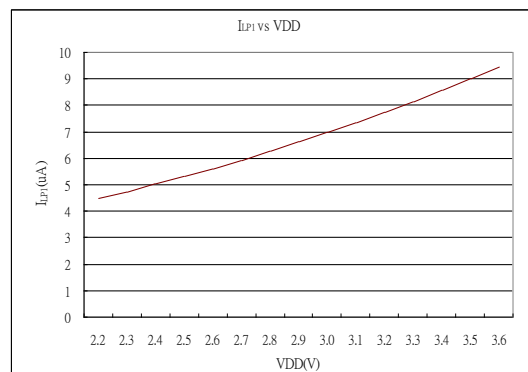


Figure 6.3-4 I_{LP1} vs. VDD

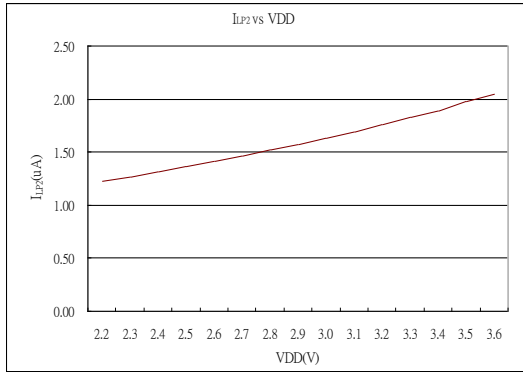


Figure 6.3-5 I_{LP2} vs. VDD

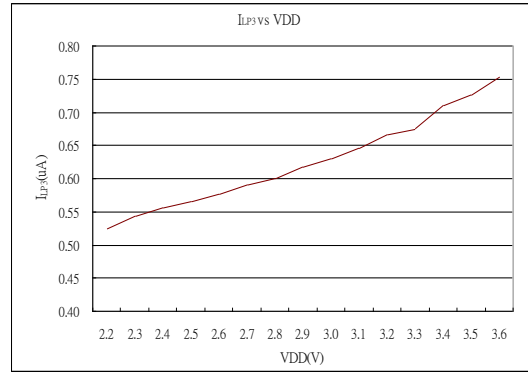


Figure 6.3-6 I_{LP3} vs. VDD

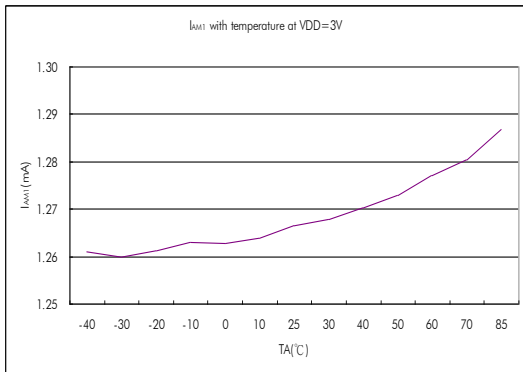


Figure 6.3-7 I_{AM1} vs. Temperature

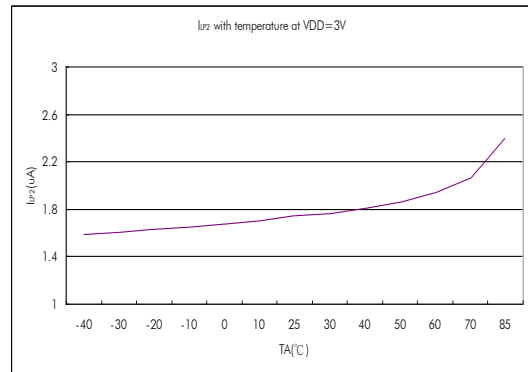


Figure 6.3-8 I_{LP2} vs. Temperature

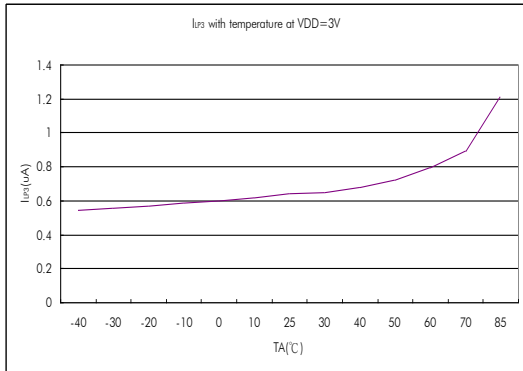


Figure 6.3-9 I_{LP3} vs. Temperature

6.4 Port1~5

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				2.1	V
V_{IL}	Low-Level input voltage		0.9			
V_{hys}	Input Voltage hysteresis($V_{IH} - V_{IL}$)			0.8		V
I_{LKG}	Leakage Current				0.1	μA
R_{PU}	Port pull high resistance			180		$\text{k}\Omega$
Output voltage and current and frequency						
V_{OH}	High-level output voltage	$I_{OH}=10\text{mA}$	$V_{DD} - 0.3$			V
V_{OL}	Low-level output voltage	$I_{OL}=-10\text{mA}$	$V_{SS} + 0.3$			

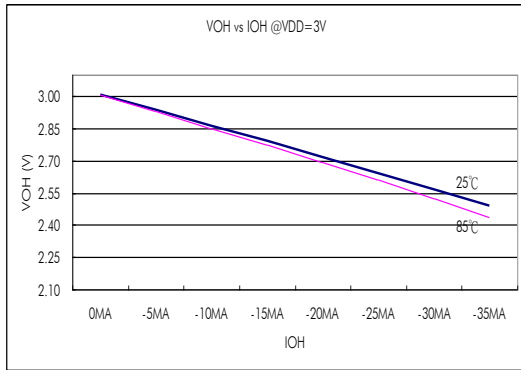


Figure 6.4-1 V_{OH} vs. I_{OH} @ $V_{DD}=3.0\text{V}$

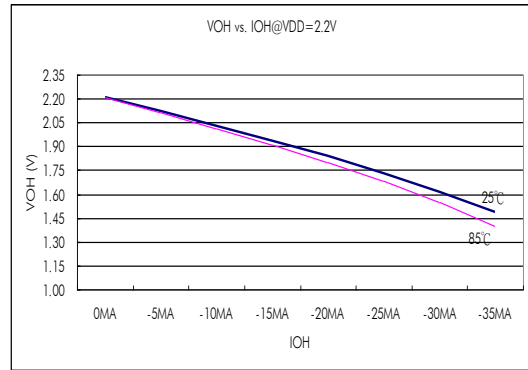


Figure 6.4-2 V_{OH} vs. I_{OH} @ $V_{DD}=2.2\text{V}$

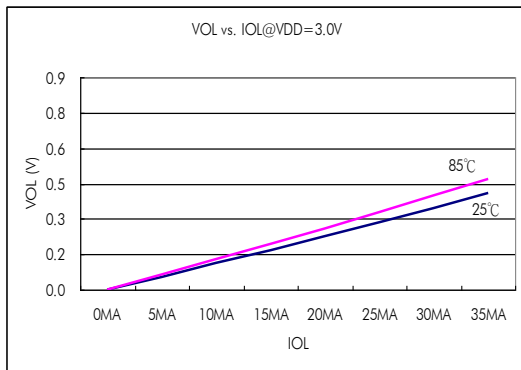


Figure 6.4-3 V_{OL} vs. I_{OL} @ $V_{DD}=3.0\text{V}$

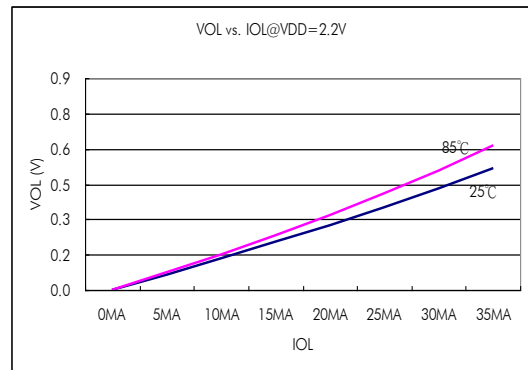


Figure 6.4-4 V_{OL} vs. I_{OL} @ $V_{DD}=2.2\text{V}$

6.5 Reset (Brownout, External RST Pin, Low Voltage Detect)

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit	
BOR	Pulse length needed to accepted reset internally, t_{d-LVR}		2			us	
	V_{DD} Start Voltage to accepted reset internally (L→H), V_{LVR}		1.6	1.85	2.1	V	
	Hysteresis, $V_{HYS-LVR}$			70		mV	
RST	Pulse length needed as RST/VPP pin to accepted reset internally, t_{d-RST}		2			us	
	Input Voltage to accepted reset internally		0.9			V	
	Hysteresis, $V_{HYS-RST}$			0.8		V	
LVD	Operation current, I_{LVD}			10	15	uA	
	External input voltage to compare reference voltage			1.2		V	
	Compare reference voltage temperature drift	$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$		100		ppm/ $^\circ\text{C}$	
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=1110b$			3.3		V	
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=1101b$			3.2			
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=1100b$			3.1			
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=1011b$			3.0			
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=1010b$			2.9			
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=1001b$			2.8			
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=1000b$			2.7			
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=0111b$			2.6			
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=0110b$			2.5			
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=0101b$			2.4			
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=0100b$			2.3			
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=0011b$			2.2			
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=0010b$			2.1			
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=0001b$			2.0			
BOR : Brownout Reset LVR : Low Voltage Reset of BOR LVD : Low Voltage Detect RST : External Reset pin							

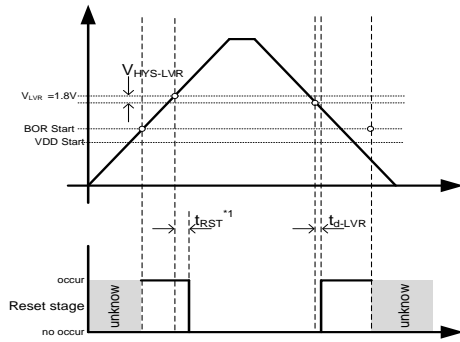


Figure 6.5-1 BOR Reset Diagram

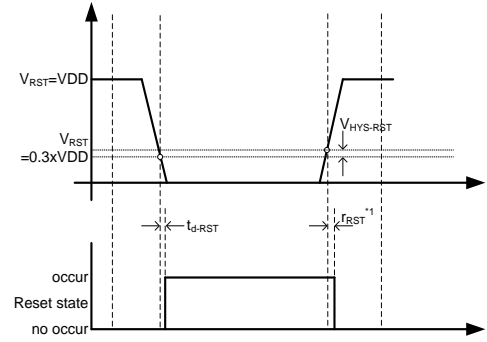


Figure 6.5-2 RST Reset Diagram

*1 t_{RST} : Please see BOR Introduce of HY11Pxx series User's Guide (UG-HY11S14-Vxx).

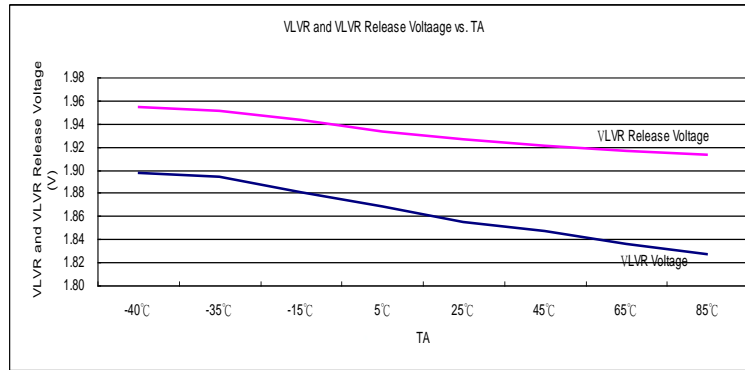


Figure 6.5-3 LVR vs. Temperature

6.6 Power System

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit	
VDDA	VDDA operation current, I_{VDDA}	$I_L = 0\text{mA}$	VDDAX[1:0]=00b		22		μA	
	Select VDDA output voltage	$I_L = 0.1\text{mA}$, $V_{DD} \geq V_{VDDA} + 0.2\text{V}$	VDDAX[1:0]=00b		3.3		V	
			VDDAX[1:0]=01b		2.9		V	
			VDDAX[1:0]=10b		2.6		V	
			VDDAX[1:0]=11b		2.4		V	
	Dropout voltage	$I_L = 10\text{mA}$	VDDAX[1:0]=00b			135		mV
			VDDAX[1:0]=01b			150		mV
VDDAX[1:0]=10b					165		mV	
VDDAX[1:0]=11b					180		mV	
Temperature drift	VDDAX[1:0]=11b	$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$		50		ppm/ $^\circ\text{C}$		
V_{DD} Voltage drift	$I_L = 0.1\text{mA}$	$V_{DD} = 2.5\text{V} \sim 3.6\text{V}$		± 0.2		%/V		
ACM	ACM operation current, I_{ACM}	$I_L = 0\text{mA}$			20		μA	
	Output voltage, V_{ACM}	ENACM[0]=1, *1	$I_L = 0\mu\text{A}$		1.0		V	
	Output voltage with Load		$I_L = \pm 200\mu\text{A}$	0.98		1.02	V_{ACM}	
	Output voltage, V_{ACM}	ENACM[0]=1, *2	$I_L = 0\mu\text{A}$		1.2		V	
	Output voltage with Load		$I_L = \pm 200\mu\text{A}$	0.98		1.02	V_{ACM}	
	Temperature drift	ENACM[0]=1,	$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$		50		ppm/ $^\circ\text{C}$	
	VDDA Voltage drift	$I_L = 10\mu\text{A}$			100		$\mu\text{V}/\text{V}$	

VDDA : Adjust Voltage Regulator
 ACM : Analog Common Mode Voltage

*1: $V_{ACM} = 1.0\text{V}$ is just for VDDAX[1:0]=1xb mode. (at A/D differential voltage reference < 1.4V)
 *2: $V_{ACM} = 1.2\text{V}$ is just for VDDAX[1:0]=0xb mode. (at A/D differential voltage reference > 1.4V)

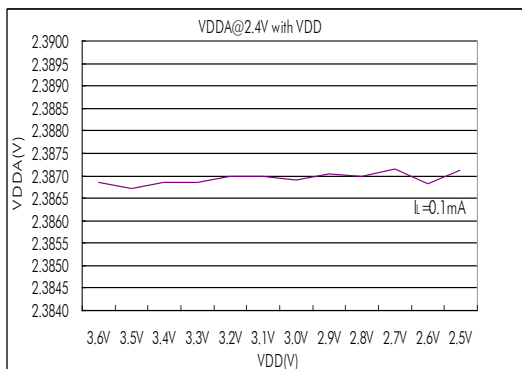


Figure 6.6-1 VDDA $I_L=0.1\text{mA}$ vs. VDD

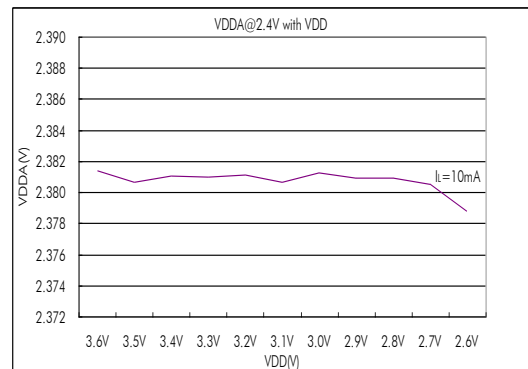


Figure 6.6-2 VDDA $I_L=10\text{mA}$ vs. VDD

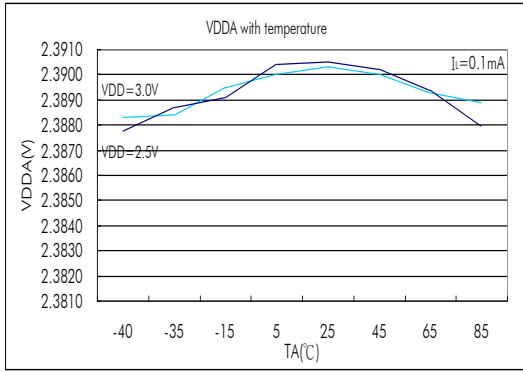


Figure 6.6-3 VDDA $I_L=0.1\text{mA}$ vs. Temperature

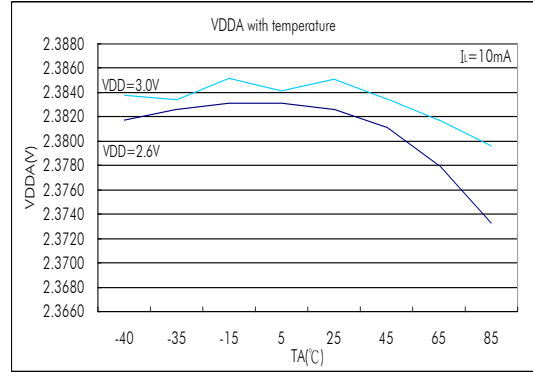


Figure 6.6-4 VDDA $I_L=10\text{mA}$ vs. Temperature

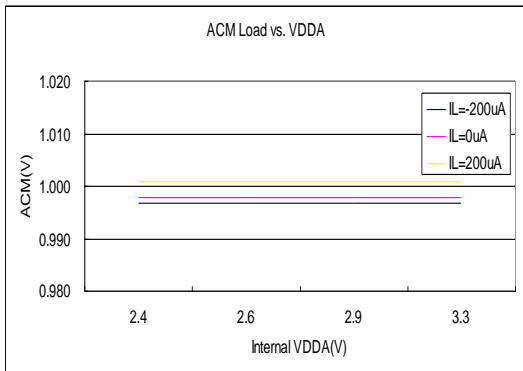


Figure 6.6-5 ACM Load vs. VDDA (a)

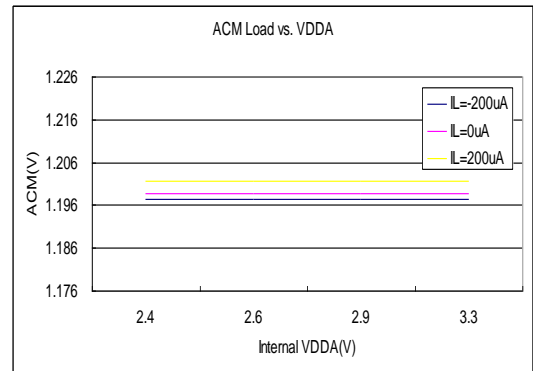


Figure 6.6-5 ACM Load vs. VDDA (b)

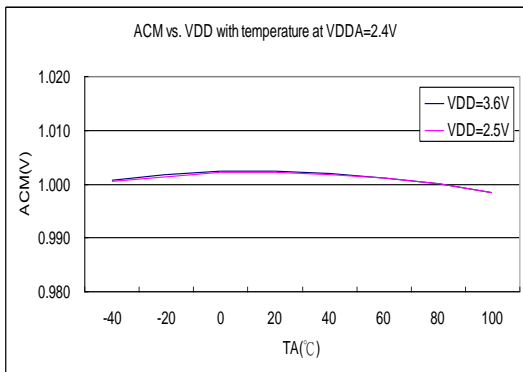


Figure 6.6-6 ACM vs. Temperature (a)

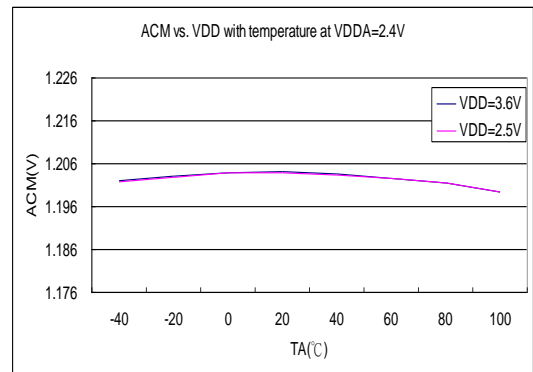


Figure 6.6-6 ACM vs. Temperature (b)

6.7 LCD

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, C_{VLCD} = 4.7\mu\text{F}$, unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
I_{LCD}	Operation supply current without output buffer.(all segment turn on)	LCDPR[0]=1	$V_{DD} = 2.2\text{V}$	10			uA
		LCDS_CK=122hz	$V_{DD} = 3.0\text{V}$				
VLCD	Supply Voltage at VLCD pin	LCDPR[0]=0		2.2		3.6	V
	Embedded Charge Pump output voltage at VLCD pin	LCDPR[0]=1, $C_{VLCD} = 4.7\mu\text{F}$	VLCDX[1:0]=11b	2.295	2.55	2.805	V
			VLCDX[1:0]=10b	2.52	2.8	3.08	
			VLCDX[1:0]=01b	2.745	3.05	3.355	
VLCDX[1:0]=00b	2.97	3.3	3.63				
Z_{LCD}	Output impedance with LCD buffer	$f_{LCD} = 128\text{Hz}, VLCD = 3.05\text{V}$		10			k Ω

Curve Chart :

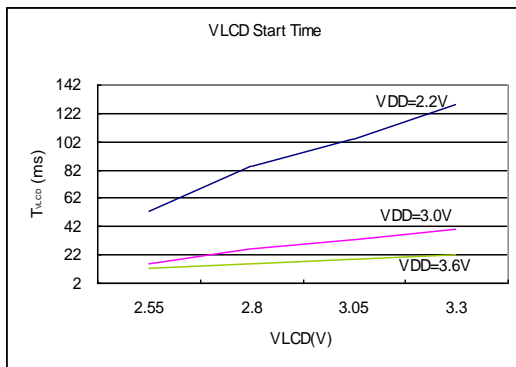


Figure 6.7-1 LCD start time

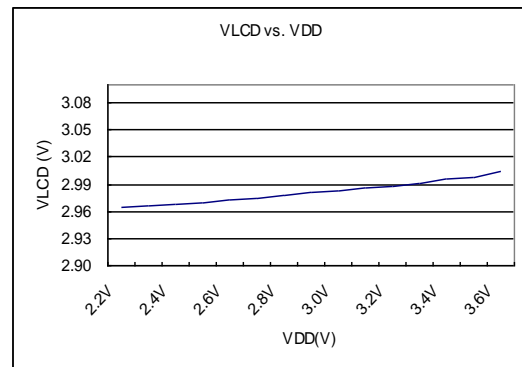


Figure 6.7-2 VLCD vs. VDD

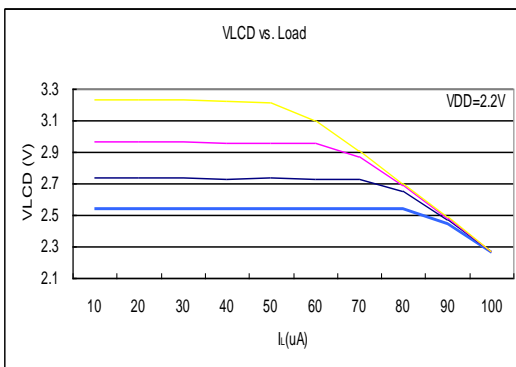


Figure 6.7-3 VLCD vs. I_L @ VDD=2.2V

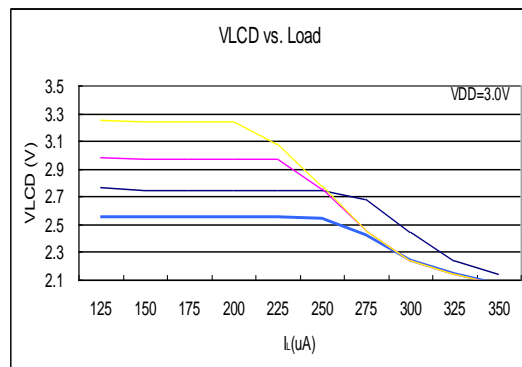


Figure 6.7-4 VLCD vs. I_L @ VDD=3.0V

6.8 Low Noise OPAMP

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{V}$, $V_{DDA}=2.4\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{LNO}	Supply voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
I_{LNO}	Operation supply current		OPM[1:0]=xxb		200		μA
V_{OS-OP}	Input offset voltage without chopper.		OPM[1:0]=1xb	-2		2	mV
	Input offset voltage with chopper		OPM[1:0]=0xb		20		μV
	Input offset voltage temperature drift.	OPM[1:0]=00b OPM[1:0]=10	$T_A=-40^\circ\text{C} \sim 85^\circ\text{C}$		0.1 2		$\mu\text{V}/^\circ\text{C}$
V_{OLR}	Unit gain load regulation	$V_O=1.2\text{V}$, $V_{DDA}=2.4\text{V}$	$I_L=+1\text{mA}$ $I_L=-1\text{mA}$		0.1		$\%V_O$
CMVR	Common-mode voltage input range		OPM[1:0]=xxb	0.1		$V_{DDA}-1.1$	V
CMRR	Common-mode rejection ratio		OPM[1:0]=xxb		90		dB

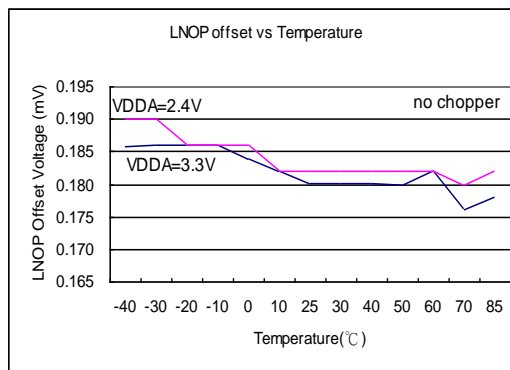


Figure 6.8-1 LNOP Offset Temperature

6.9 SD18, Power Supply and Recommended Operating Conditions

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA}=2.4\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{SD18}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
f_{SD18}	Modulator sample frequency, ADC_CK			25	250	300	KHz
	Over Sample Ratio, OSR			256		32768	
I_{SD18}	Operation supply current without PGA	ENADC[0]=1 INBUF[0]=1,VRBUF[0]=0	GAIN =4, ADC_CK=250KHz	168		uA	
		ENADC[0]=1 INBUF[0]=0,VRBUF[0]=1		150			
		ENADC[0]=1 INBUF[0]=0,VRBUF[0]=0		120			

6.10 PGA, Power Supply and Recommended Operating Conditions

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA}=2.4\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{PGA}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
I_{PGA}	Operation supply current	PGAGN[1:0]=<01>or<1x>			320		uA
G_{PGA}	Gain temperature drift	$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$	GAIN=128		5		ppm/ $^\circ\text{C}$

6.11 SD18, Performance II (fSD18=250KHz)

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA}=2.9\text{V}, V_{VR}=1.0\text{V}, \text{GAIN}=1$ without PGA, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
INL	Integral Nonlinearity(INL)	$V_{DDA}=2.4\text{V}, V_{VR}=1.0\text{V}, \Delta\text{SI}=\pm 200\text{mV}$			± 0.003	± 0.01	%FSR
		$V_{DDA}=2.4\text{V}, V_{VR}=1.0\text{V}, \Delta\text{SI}=\pm 450\text{mV}$					
	No Missing Codes ³	ADC_CK=250KHz, OSR[2:0]=010b		23			Bits
G_{SD18}	Temperature drift	INBUF[0]=0b,VRBUF[0]=0b	$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$	2		ppm/ $^\circ\text{C}$	
	Gain 1~x16 (INBUF[0]=0b)	INBUF[0]=1b,VRBUF[0]=0b					
		INBUF[0]=0b,VRBUF[0]=1b					
		INBUF[0]=1b,VRBUF[0]=1b					
E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper and Buffer(INBUF,VRBUF) without PGA	$\Delta\text{AI}=0\text{V}$ $\Delta\text{VR}=0.9\text{V}$	Gain=2	1		%FSR	
	Offset error of Full Scale Rang input voltage range with Chopper without PGA and Buffer(INBUF,VRBUF)	DCSET[2:0]=<000> * ΔAI is external short	Gain=2	1			
	Offset temperature drift with		GAIN=1	2		uV/ $^\circ\text{C}$	

	chopper without PGA and Buffer (INBUF,VRBUF).		GAIN=2	1	
			GAIN=4	0.5	
			GAIN=16	0.15	
	Offset temperature drift with chopper and Buffer (INBUF,VRBUF) without PGA.	GAIN=1	2		
		GAIN=2	1		
		GAIN=4	0.5		
Offset temperature drift with chopper without Buffer (INBUF,VRBUF).			GAIN=128	0.02	
CM _{SD18}	Common-mode rejection	V _{CM} =0.7V to 1.7V, V _{VR} =1.0V, without PGA	V _{SI} =0V, GAIN=1	90	dB
		V _{CM} =0.7V to 1.7V, V _{VR} =1.0V, without PGA	V _{SI} =0V, GAIN=16	75	
PSRR	DC power supply rejection	V _D =3.0V, Δ V _D = \pm 100m V _I , V _{VR} =1.0V, V _{SI} =1.2V, V _{SI} =1.2V,	GAIN=1 PGA=off	75	dB
			GAIN=16 PGA=8		

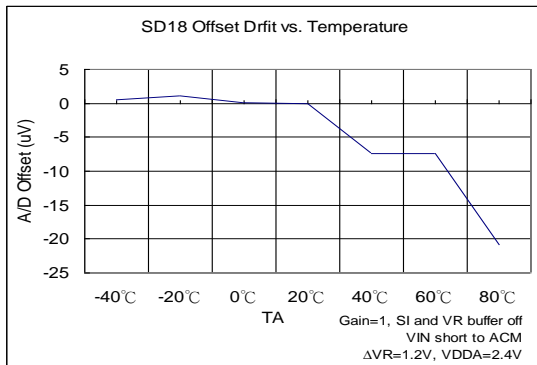


Figure 6.9-1(a) SD18 Offset Temperature Drift

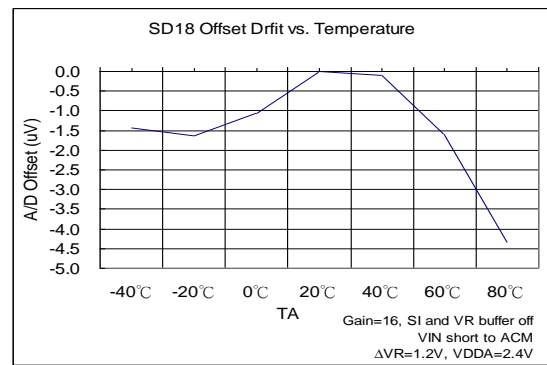


Figure 6.9-1(b) SD18 Offset Temperature Drift

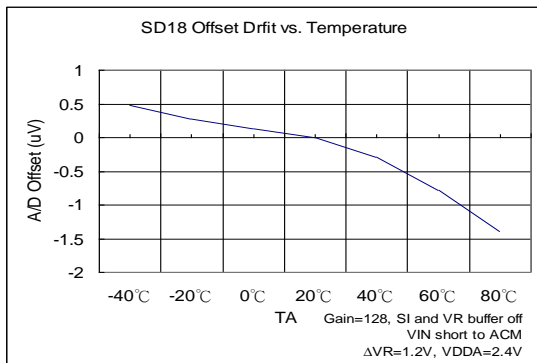


Figure 6.9-1(c) SD18 Offset Temperature Drift

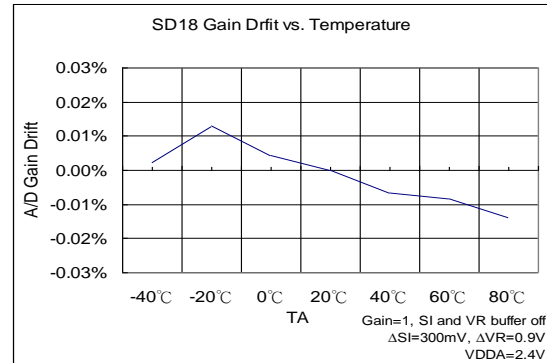


Figure 6.9-2(a) SD18 Gain Drift with Temperature

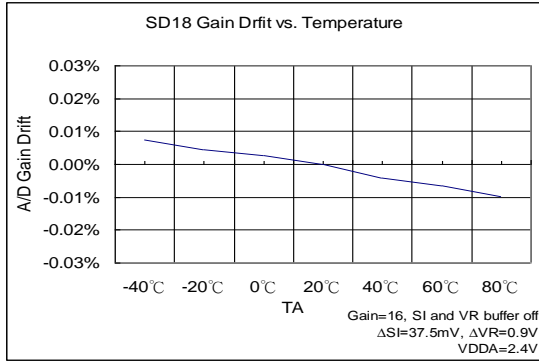


Figure 6.9-2(b) SD18 Gain Drift with Temperature

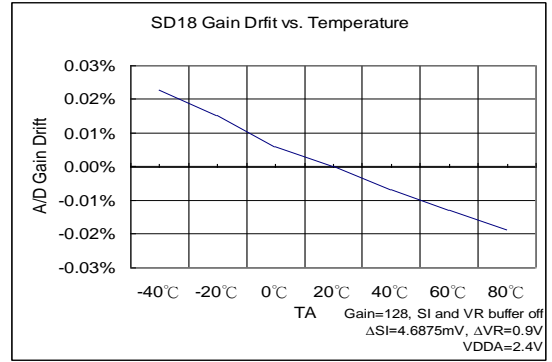


Figure 6.9-2(c) SD18 Gain Drift with Temperature

6.12 SD18, Temperature Sensor

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{V}$, $V_{DDA} = 3.3\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
TC_S	Sensor temperature drift			178		$\mu\text{V}/^\circ\text{C}$
KT	Absolute Temperature Scale 0°K	INBUF[0]=1		-289		$^\circ\text{C}$
TC_{ERR}	One point calibrate error temperature	Calibration at 25°C of $-40^\circ\text{C} \sim 85^\circ\text{C}$		± 2		$^\circ\text{C}$

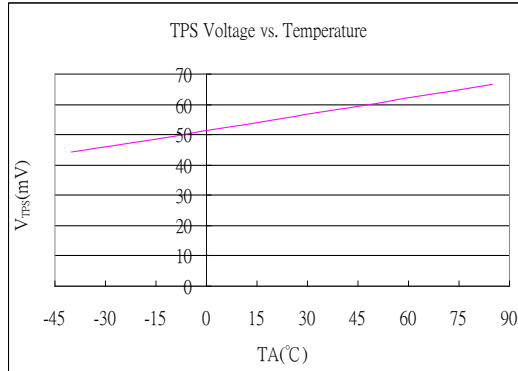


Figure 6.9-3 TPS output voltage vs. Temperature Drift

6.13 SD18 Noise Performance

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA} = 2.4\text{V}$, unless otherwise noted

HY11P14 provides important input noise specification that aims at SD18. Table 6.9-4(a) and Table 6.9-4(b) lists out the relations of typical noise specification, gain, output rate and maximum input voltage of single end. Test conditions are external input signal short, voltage reference: 1.2V and 1024 records were sampled.

ENOB(RMS) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V													
Max. Vin(mV) =0.9*VREF ⁽¹⁾	OSR					256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					977	488	244	122	61	31	15	8
	Gain	=	PGA	x	ADGN								
± 2400	0.25	=	1	x	0.25	16.3	17.4	17.9	18.5	19.0	19.5	20.0	20.4
± 2160	0.5	=	1	x	0.5	16.3	17.3	17.9	18.4	18.9	19.4	19.8	20.2
± 1080	1	=	1	x	1	16.2	17.2	17.8	18.3	18.8	19.3	19.7	20.1
± 540	2	=	1	x	2	16.1	17.1	17.6	18.2	18.7	19.2	19.6	20.0
± 270	4	=	1	x	4	16.0	16.9	17.5	18.0	18.5	18.9	19.4	19.8
± 135	8	=	1	x	8	15.9	16.6	17.2	17.7	18.2	18.7	19.2	19.6
± 68	16	=	1	x	16	15.6	16.3	16.8	17.3	17.7	18.3	18.8	19.3
± 34	32	=	2	x	16	14.8	15.3	15.9	16.4	16.9	17.4	17.8	18.3
± 17	64	=	4	x	16	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0
± 8	128	=	8	x	16	14.0	14.6	15.1	15.6	16.0	16.6	17.0	17.5

(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).

Table 6.9-4(a) SD18 ENOB Table

RMS Noise(uV) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V													
Max. Vin(mV) =0.9*VREF	OSR					256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					977	488	244	122	61	31	15	8
	Gain	=	PGA	x	ADGN								
± 2400	0.25	=	1	x	0.25	121.08	57.40	38.74	26.66	18.39	13.21	9.49	6.98
± 2160	0.5	=	1	x	0.5	61.63	29.23	19.21	13.51	9.78	7.02	5.12	3.91
± 1080	1	=	1	x	1	32.21	15.70	10.25	7.31	5.19	3.77	2.80	2.13
± 540	2	=	1	x	2	16.59	8.54	5.91	4.06	2.86	2.06	1.48	1.12
± 270	4	=	1	x	4	9.00	4.84	3.33	2.37	1.67	1.19	0.87	0.65
± 135	8	=	1	x	8	5.04	2.97	2.02	1.44	1.01	0.73	0.51	0.39
± 68	16	=	1	x	16	3.03	1.84	1.29	0.92	0.70	0.46	0.33	0.24
± 34	32	=	2	x	16	2.61	1.81	1.27	0.89	0.62	0.45	0.32	0.23
± 17	64	=	4	x	16	1.66	1.13	0.80	0.56	0.41	0.29	0.20	0.14
± 8	128	=	8	x	16	1.13	0.77	0.55	0.38	0.28	0.19	0.14	0.10

Table 6.9-4(b) SD18 RMS Noise Table

The RMS noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$\text{ENOB(RMS)} = \frac{\ln\left(\frac{\text{FSR}}{\text{RMS Noise}}\right)}{\ln(2)}$$

$$\text{RMS Noise} = \frac{\left(2 \times \text{VREF} \times \sqrt{\sum_{k=1}^{1024} (\text{ADO}[k] - \text{Average})^2}\right)}{2^{23}}$$

Where FSR (Full - Scale Range) = $2 \times \text{VREF}/\text{Gain}$.

$$\text{Average} = \frac{\sum_{k=1}^{1024} (\text{ADO}[k])}{1024}$$

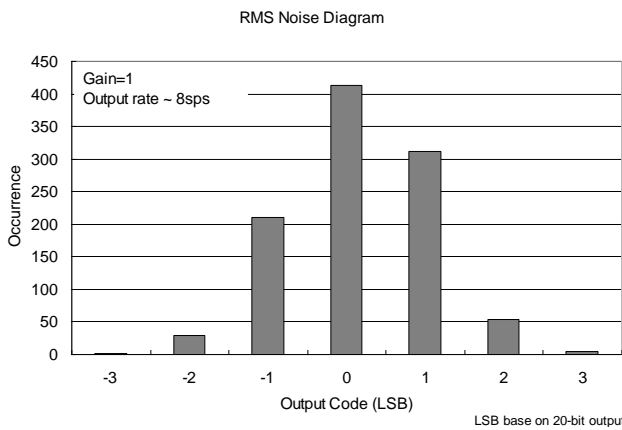


Figure 6.9-4(a) RMS Noise Diagram

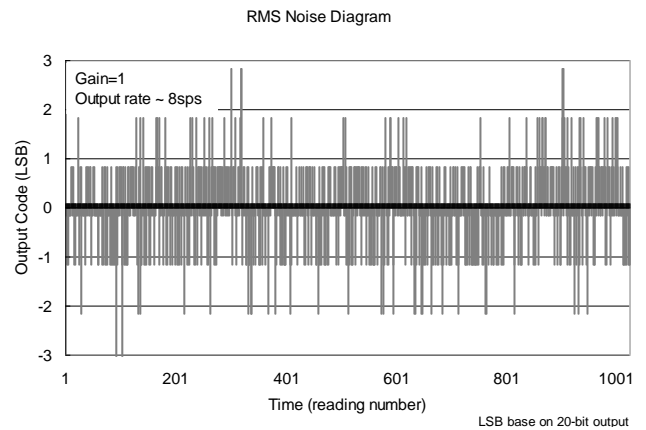


Figure 6.9-4(b) Output Code Diagram

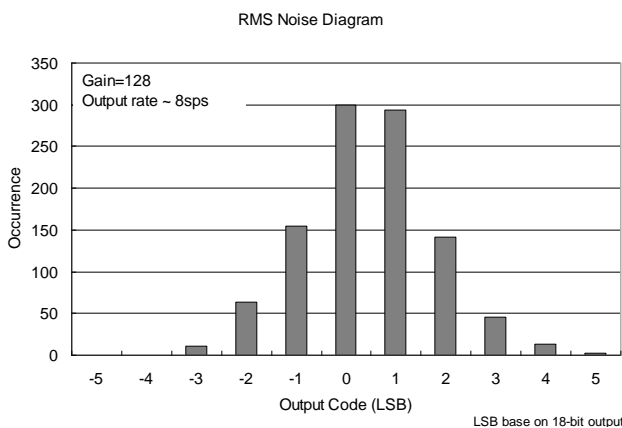


Figure 6.9-4(c) RMS Noise Diagram

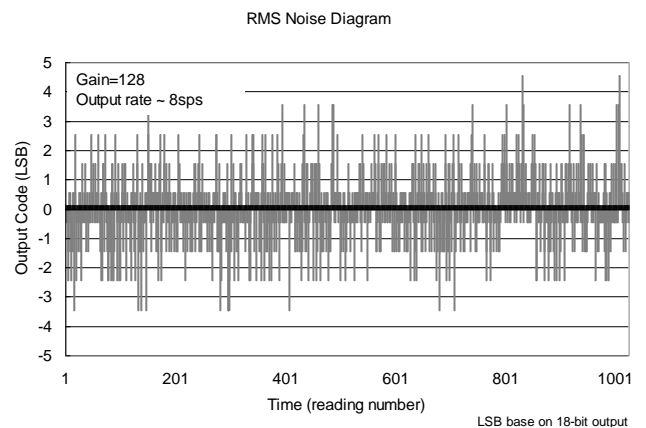


Figure 6.9-4(d) Output Code Diagram

7. Ordering Information

Device No. ¹	Package Type	Pins	Package Drawing		Code ²	Shipment Packing Type	Unit Q'ty	Material Composition	MSL ³
			D	000					
HY11P14-D000	Die	-	D	000	000	-	100	Green ⁴	-
HY11P14-L100	LQFP	100	L	100	000	Tray	90	Green ⁴	MSL-3
HY11P14-L064	LQFP	64	L	064	000	Tray	250	Green ⁴	MSL-3

¹ **Device No.:** Model No. – Package Type Description – Code (Blank Code/ Standard/ Customized Programming Code)

Ex: Your customized programming code is 008 and you require die shipment.

The device No. will be HY11P14-D000-008

Ex: You request blank code in die package.

The device No. will be HY11P14-D000.

Ex: You request blank code in LQFP 100 package.

The device No. will be HY11P14-L100.

And please clearly indicate the shipment packing type when placing orders.

Ex: Your customized programming code is 009 and you require products in LQFP 100 package.

The device No. will be HY11P14-L100-009.

And please clearly indicate the shipment packing type when placing orders.

² **Code:**

“001”~ “999” is standard or customized programming code. Blank code does not have these numbers.

³ **MSL:**

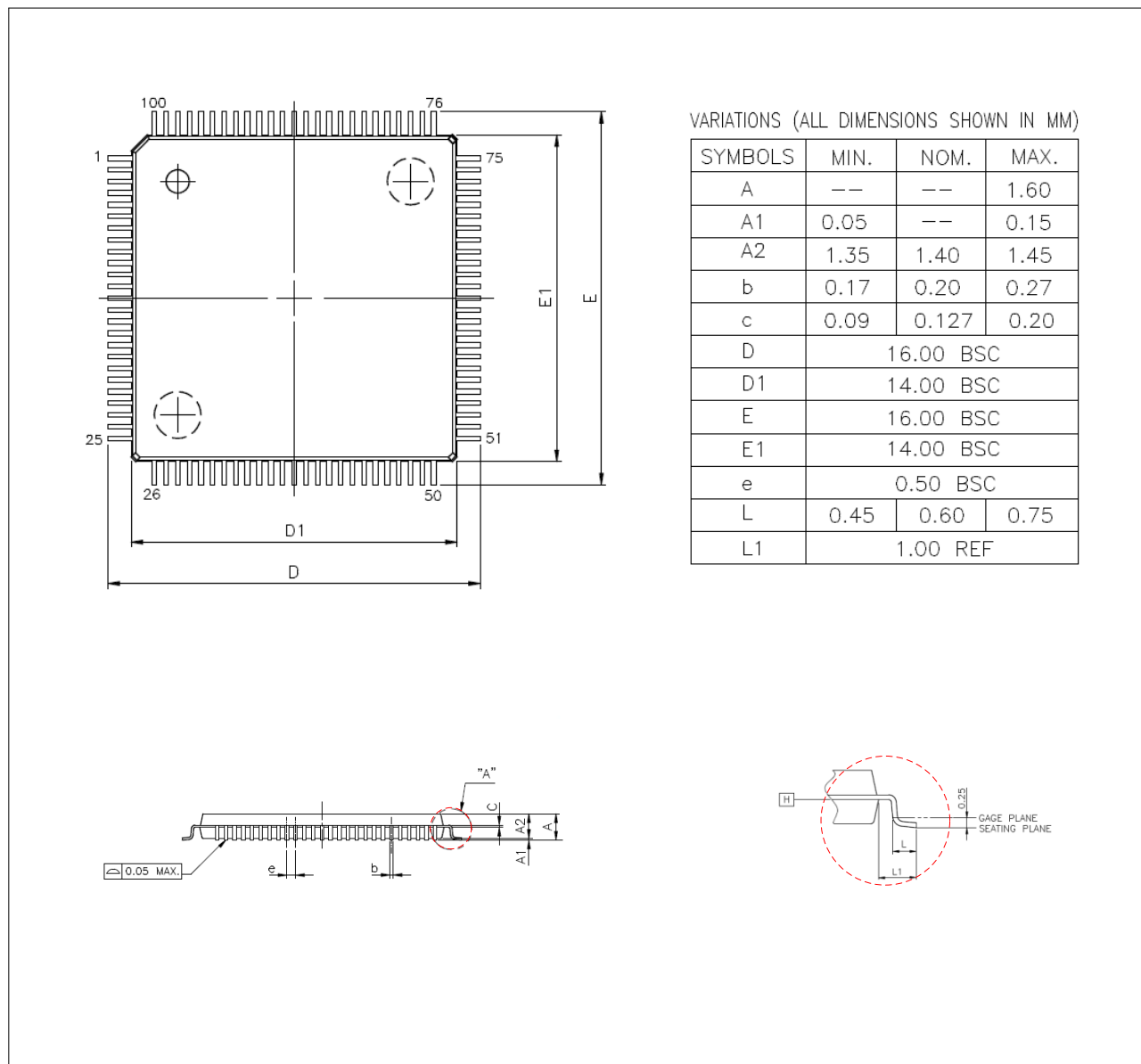
The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

⁴ **Green (RoHS & no Cl/Br):**

HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br<900ppm or Cl<900ppm or (Br+Cl)<1500ppm).

8. Package Information

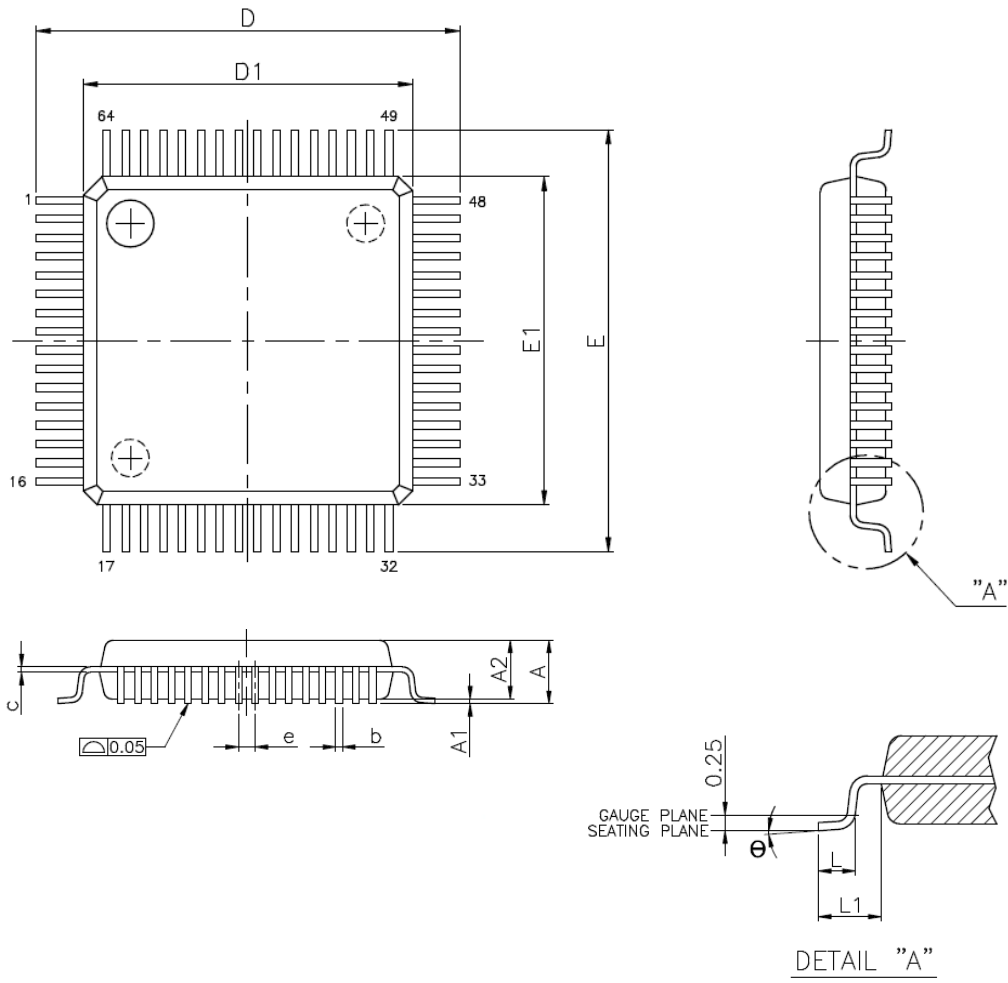
8.1 LQFP100(L100 10x10)



Note:

1. All dimensions refer to JEDEC OUTLINE MS-026.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

8.2 LQFP64(L064 7x7)



SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Note:

1. All dimensions refer to JEDEC OUTLINE MS-026.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

9. Revision History

Major differences are stated thereafter:

Version	Page	Revision Summary
V03	ALL	First edition
V05		With reference to documentation: DS-HY11P14-V05_TC
	4	Features revision
	6~9	Table 2-1 Pin Definition and Function Description revision
	11	Chapter 3 Application Circuit revision
	13	Chapter 4 Register List revision
	22~23	Chapter 6.6 Power System revision
	25	Chapter 6.8 Low Noise OPAMP revision
	26~28	Chapter 6.9 SD18, Power Supply and recommended operating conditions revision
V06	13	Chapter 5 Register List revision
V08	4	Features revision
	6	Table 2-1 Pin Definition and Function Description revision
	22~23	Chapter 6.6 Power System revision
V09	1	Cover revision
	4	Features revision, delete description of 1/2bias
	5	Add in Note 3
	11	Revised application circuit, add in RC circuit of RST
	12	Revised Internal Block Diagram
	20	Deleted Detect VDD voltage error description
V12	5	Revise Chapter 1
	12	Revise Figure 3-1
	13	Revise Figure 4-1 and Chapter 4.2
	14	Add in SD19 network chapter
	17	Revise Chapter 6 electrical characteristics
	24	Revise Power system temp. drift spec
	25	Revise the background color of Figure 6.6-5 and Figure 6.6-6
	32~33	Add in SD18 Noise Performance chapter
	34	Chapter 7 Ordering information revision
V14	15	Add in 4.4 Low Noise OPAMP Network
	16	Add in 4.5 Enhance Comparator Network
	28	Chapter 6.7 LCD, update the test conditions and typical value of I_{LCD}
V15	ALL	Add in LQFP64 package information
V16	7~11	Revise the pin name and definition of the 21st pin of LQFP64 package

37 Revise the Green (RoHS & no Cl/Br) descriptions