HY16F Series
Development Precautions Note

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1. Brief Introduction

In this article, the product application notes are applicable to the following HY16F series products :

- HY16F18x Series : HY16F184, HY16F187, HY16F188.
- HY16F19xB Series : HY16F196B, HY16F197B, HY16F198B.
- HY16F39 Series : HY16F3981.

2. Precautions for the use of HY16F series IP

In this chapter, especially for the HY16F series in the use of specific IP, it explains the precautions for use. If you use this IP for applications, but do not pay attention to the restrictions on the use of IP, unpredictable results may occur. Before using the IP , It should take time to study it, and then design and use it, which can reduce many unexpected error in development.

2.1. WDT

The watch dog timer (WDT) is, as the name implies, the watcher of the chip, and its main function is to generate the wake-up event or execute basic reset function after the chip crashes accidentally. Here is a special emphasis on the precautions for using the WDT Reset function.

2.1.1. WDT Reset- Precautions for use

When the WDT Reset Mode function is enabled, it cannot be switched back to WDT Timer Mode, that is, after setting WDNMI 0x40108[6]=1b, it cannot be set back to WDNMI 0x40108[6]=0b. Before setting and using this function, users need to know that WDT Reset Mode has this application limitation. In addition, programmers should also note that after the WDT function is turned on, WDT Count, WDTO 0x40108[30:16] will start to count, which cannot be turned off, that is, set ENWDT 0x40108[4]=1b, it cannot be set back. ENWDT 0x40108[4]=0b. So if you enable WDNMI 0x40108[6]=1b and ENWDT 0x40108[4]=1b, remember to reset the WDT counter within the expected planning time, that is, set 0x40108[5]=1b to avoid forgetting during the program development process Clear the WDT counter, causing the WDT Reset event to take action.
Note : When the WDT Reset occurs, the status of the IP registers will remain the same, that is, the status of the IP registers before the WDT Reset is the same as that after the WDT Reset. After the WDT Reset occurs, the program will only jump back to the Reset vector position, and then execute the Startup code and CPU initialization and other related actions, but the IP register state will not be re-initialized. The result is different from the actual reset of the HY16F hardwar reset pin.

2.1.2. WDT Reset- Example program

```
DrvWDT_Open(E_IRQ , E_PRE_SCALER_D32);    //Set WDT to IRQ mode and CLK / 32
DrvWDT_ResetEnable();    // WDT interrupt working mode is selected as Reset Mode
```

2.2. GPIO

GPIO ports have multiple multiplexing functions, but only one function can be set to be valid at the same time, so when the multiplexing function is not needed, please remember to turn off the multiplexing function. The two multiplexed GPIOs PT3.6/PT3.7 should be used with special attention. If the analog and digital functions are turned on at the same time, the VDDA power supply may be backflowed and the ADC measurement abnormality may occur.

2.2.1. GPIO multiplexing pins PT3.6/PT3.7- Precautions for use

PT3.7/OPO multiplexing pin:

- Designed as OPO output ; control register OPOE 0x41900[1]=1b, PT3PU7 =PT3OE7=PT3IE7=0b
- Designed as PT3.7 GPIO input ; control register ENRFO 0x40400[1]=0b, PT3IE7=1b
- Designed as PT3.7 GPIO output ; control register ENRFO 0x40400[1]=0b, PT3IE7=1b**(Mandatory setting even if not used as input)**, PT3OE7=1b

PT3.6/REFO multiplexing pin :

- Designed as REFO output ; control register ENRFO 0x40400[1]=1b, PT3PU6=PT3OE6=PT3IE6=0b
- Designed as REFO input ; control register ENRFO 0x40400[1]=0b, PT3PU6=PT3OE6=PT3IE6=0b
- Designed as PT3.6 GPIO input ; control register ENRFO 0x40400[1]=0b, PT3IE6=1b
- Designed as PT3.6 GPIO output ; control register ENRFO 0x40400[1]=0b, PT3IE6=1b**(Mandatory setting even if not used as input)**, PT3OE6=1b

2.2.2. GPIO multiplexing pins PT3.6/PT3.7- Example program

When users design PT3.6 and PT3.7 as GPIO Output functions, the setup and initialization process of PT3.6 and PT3.7 programs is as follows :

```
DrvPMU_REFO_Disable();    //setting ENRFO 0x40400[1]=0b
DrvGPIO_Open(E_PT3,0xC0,E_IO_INPUT);    // setting PT3IE6=1b, PT3IE7=1b
DrvGPIO_Open(E_PT3,0xC0,E_IO_OUTPUT);    // setting PT3OE6=1b, PT3OE7=1b
```

2.3. Analog power VDDA, VDD18, VPP

When designing the schematic of HY16F series, users should pay special attention to the connection of the three pins of VDDA, VDD18, and VPP.

2.3.1. VDDA- Precautions for use

VDDA's capacitor can be connected in the range of 1uF~10uF, and it should be noted that VDDA needs to wait for stabilization time when it is turned on. The larger the capacitance, the longer the stabilization time for VDDA to wait, and the external capacitance of VDDA is also related to the load and current drive capability.

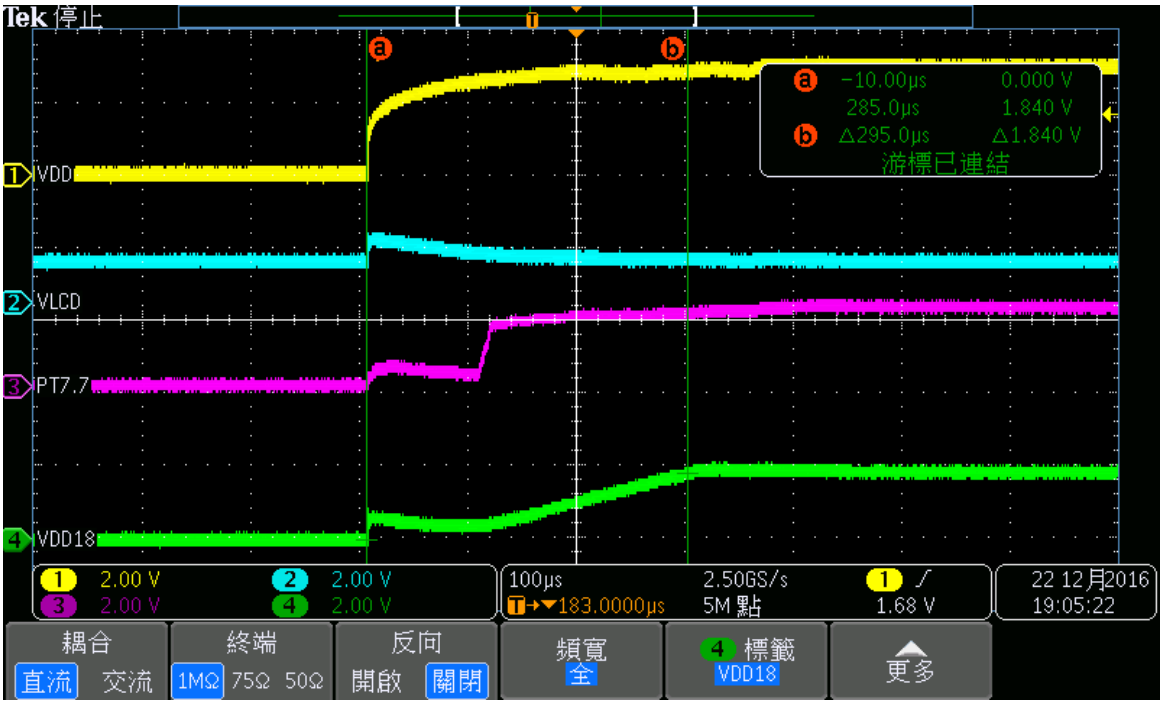
When VDDA is connected to a 1uF capacitor to ground, the stabilization time of VDDA needs to be at least greater than 0.5ms, and when VDDA is connected to a 10uF capacitor to ground, the stabilization time of VDDA needs to be at least greater than 1ms. If the ADC function is enabled when VDDA is not stable, it will result in incorrect ADC data capture.

The VDDA external capacitor is mainly related to the capability of driving current, according to the design requirements of HY16F series chips as follows :
When the VDDA drive capability is required to be 1mA: The external capacitor to ground should be 1uF.
When the VDDA drive capability is required to be 10mA: The external capacitor to ground should be 10uF.
It is recommended that users set the VDDA-to-ground capacitance to 10uF to enhance the driving capability and voltage stability.
Note : Since the capacitor of the VDDA is related to the driving capability and voltage stability, it is recommended that the capacitor should be selected as 10uF-Y5R or 10uF-X5R, and the error specification of capacitor temperature and capacitance change within 15%

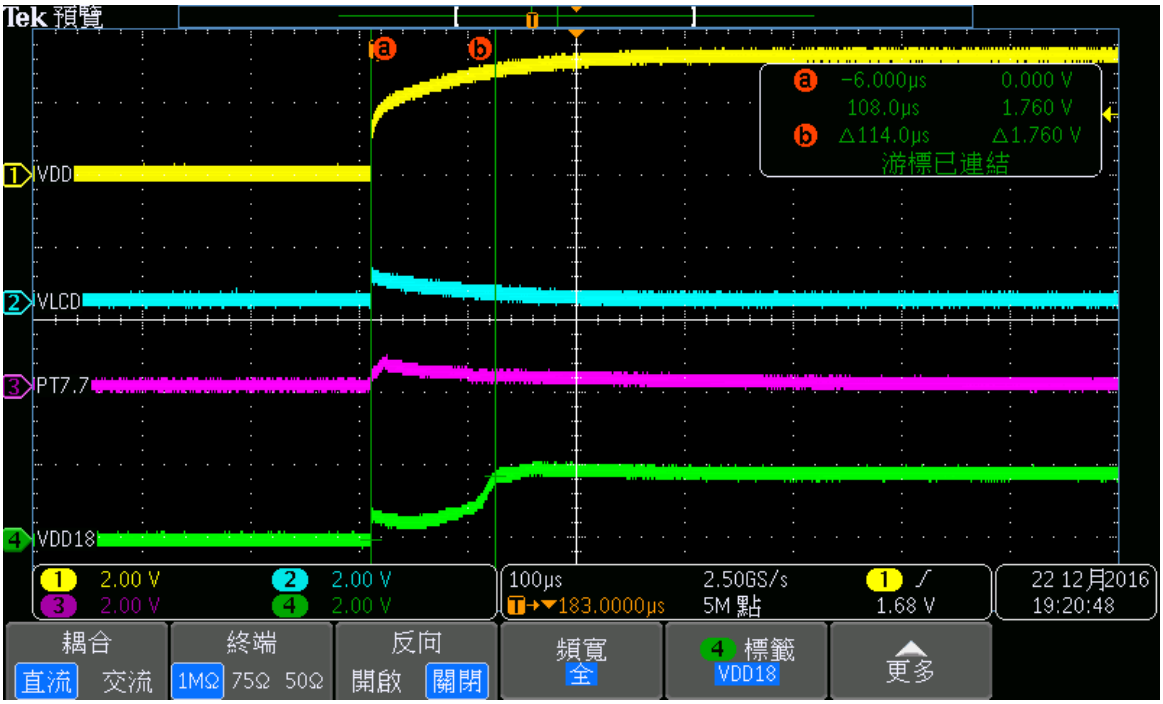
2.3.2. VDD18- Precautions for use

The capacitor of VDD18 can only be connected to 1uF. If the capacitor of VDD18 is connected too large, it may cause LCD afterimage problem during power-on.

Take the following figure as an example: VDD18 uses a 10uF capacitor pattern, because VDD18 takes a long time from power on to stable, about 295us, observe the SEG pin PT7.7, because the control logic has not yet stabilized, PT7.7 has been pulled up abnormally, resulting in LCD afterimage phenomenon occurs.



Take the following figure as an example: VDD18 uses a 1uF capacitor pattern, because the time from power on to stabilization of VDD18 is about 114us, observe the SEG pin PT7.7, because the control logic has been stabilized, PT7.7 is not pulled up abnormally, and there will be no LCD Afterimage phenomenon occurs.



2.3.3. VPP- Precautions for use

When the VPP pin is connected to 0.1uF, the programming failure(error) message will be displayed when doing online programming in Andesight IDE or using the HY16F WRITER tooling. Therefore, **the VPP pin cannot be connected to any capacitors, nor can it be used for any load voltage output application. The VPP pin should remain in the NC state (keep an empty connection).**

2.4. ADC

When the ADC is doing channel switching (EX: switching from AIO0-AIO1 to AIO2-AIO3), it should be noted that the ADC Combfilter (comb filter) setting needs to be done, Otherwise, the ADC Offset may stop in a different state and effect the measurement result.

2.4.1. ADC Channel Switching- Precautions for use

When the user switches the ADC channel, the first two ADC signals are invalid.
The user can use the reset (CFRST=1b) control to automatically discard the first two data, and the third data will generate an ADC interrupt to read the ADC signal. If in practical application, there is no need to switch the ADC input channel, and the measurement channels are the same, there is no need to reset CFRST=1b.

2.4.2. ADC Channel Switching- Example Instructions

Change ADINP,ADINN to A (EX : AIO0-AIO1)
comb filter reset,
sample A0, The hardware discards itself
sample A1, The hardware discards itself
sample A2, The first interrupt output value of the hardware

Change ADINP,ADINN to B (EX : AIO2-AIO3)
comb filter reset,
sample B0, The hardware discards itself
sample B1, The hardware discards itself
sample B2, The first interrupt output value of the hardware

Change ADINP,ADINN to A (EX : AIO0-AIO1)
comb filter reset,
sample A3, The hardware discards itself
sample A4, The hardware discards itself
sample A5, The first interrupt output value of the hardware

Change ADINP,ADINN to B (EX : AIO2-AIO3)
comb filter reset,
sample B3, The hardware discards itself
sample B4, The hardware discards itself
sample B5, The first interrupt output value of the hardware

Change ADINP,ADINN to A (EX : AIO0-AIO1)
comb filter reset,
sample A6, The hardware discards itself
sample A7, The hardware discards itself
sample A8, The first interrupt output value of the hardware

Change ADINP,ADINN to B (EX : AIO2-AIO3)
comb filter reset,
sample B6, The hardware discards itself
sample B7, The hardware discards itself
sample B8, The first interrupt output value of the hardware

When ADC OSR=32768, ADC Clock=327Khz, then ADC Output rate is about 10sps=0.1sec
Because of the ADC 3nd comb filter architecture, the first two values need to be discarded at the beginning, and the third value is the stable state. That is to say, the output time of the first ADC stable value after each channel switching is 3/10=0.3sec. However, if the ADC channel is not switched, because there is no need to do CFRST=1b, the ADC stable output time of the second, third and N data is 0.1sec.

2.4.3. ADC Startup time stabilization Issues

Every time VDDA does on/off switching, it needs to wait for stabilization time. When VDDA does not have any load, and when ADC is external input short, there will be no problem of ADC startup stabilization time. When the VDDA has a load and the ADC has an input impedance, it will be observed that the data before the ADC is unstable. Therefore, in practical applications, if VDDA on/off switching is performed, when VDDA is on, it is necessary to wait for a stabilization time of 100ms, and then perform the acquisition of ADC data, which can avoid the instability of the previous few data of the ADC.

2.4.4. ADC Linearity Issues

In the HY16F series, the best measurable voltage range of the ADC is related to the setting of the reference voltage. Users should pay attention to avoid the occurrence of ADC linearity error.

The following are the precautions for use:

When REFP-REFN(VREF) = 1*VDDA,

Then the differential input signal of VINP-VINN cannot be greater than 1/2*VDDA, otherwise there will be linearity problems

When REFP-REFN(VREF) = 1/2*VDDA,

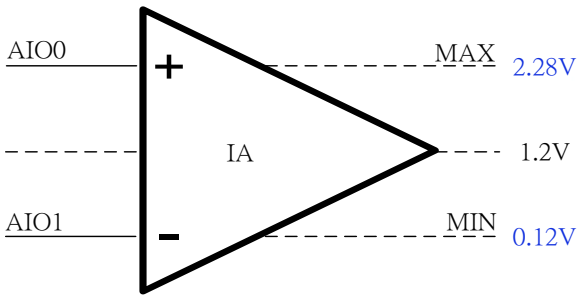
Then the differential input signal of VINP-VINN cannot be greater than 0.9*VREF, otherwise there will be linearity problems

Example: Set REFP-REFN=VDDA-VSSA, and VDDA=2.4V, then set FRb=0b, full-scale reference voltage input, ie VREF*1 At this time, the maximum measurable voltage Vin range of ADC is 1/2* VDDA=1.2V, not 0.9*VREF=2.16V. Therefore, under this setting condition, if the measurement voltage Vin exceeds 1.2V, the ADC linearity error will occur.

2.4.5. ADC-IA Instructions for use

In the HY16F series, only the HY16F3981 has IA (Instrumentation Amplifier function) at the front end of the ADC. When using an instrumentation amplifier, it should be noted that the measurement input signal of the IA is limited by the IA Input range. The input range is BIAS=1.2V, input signal=+/-1.08V. In actual use, it can be designed and used in this way, the ADC measurement channel is set to AIO0-AIO1, and there needs to be a BIAS reference voltage at the input negative end (AIO1) of the ADC. (EX: 1.2V of HY16F3981's REFO output can be used as BIAS reference voltage), if there is no BIAS reference voltage connected to the IA input, problems will occur in measurement, and users should pay special attention to this IA application limitation.

HY16F3981 IA Input Range : BIAS=1.2V, input signal=+ /-1.08V



Although the IA of HY16F3981 has high input impedance characteristics, when connecting a sensor with high input impedance characteristics, if the program is set to IA Chopper On mode (ie 0x41600[5:4]=11b), When the input impedance of the Sensor is greater than 10k ohms, the overall ADC accuracy will be attenuated. As the input impedance increases, the ADC accuracy will be more attenuated. It is recommended that the user set the program to IA Chopper Off (ie 0x41600[5:4]=00b) when connecting the high input impedance Sensor signal, and use the software SW Chopper to deduct the ADC offset noise. This method does not The accuracy of the ADC will be affected by the high input impedance.

2.5. Power

HY16F can reach 5uA in Idle Mode and 3.5uA in Sleep Mode, when VDD18 LDO is turned OFF before entering Sleep Mode, it can reach 2.5uA. Before entering the Idle or Sleep Mode, the user must ensure that the related analog power supply and the internal high-frequency crystal oscillator are both turned off, in order to achieve the same power saving as the specification. In addition, the user also needs to pay attention to the need to re-initialize and open the relevant application IP after waking up from the power saving mode. To avoid the problem that the IP works normally before entering the power saving mode, but the IP works abnormally after waking up. This application problem often occurs in the program development stage, and programmers should pay special attention.

2.5.1. Active Mode --> Idle Mode/Sleep Mode- Precautions for use

Before entering the power saving mode, the following settings can be made in order :

1. Switch the working frequency of CPU to LPO low frequency first, and then turn off HAO high frequency.
2. If the related analog power output is turned on, the corresponding analog power off action is also required.
3. The Pull High or Pull Low design of GPIO is set according to the external circuit design to avoid leakage or voltage inversion when entering Sleep/Idle.
4. At the same time, ensure that the corresponding wake-up interrupt function is enabled before entering the power saving mode, so as to achieve the same power saving specification as the datasheet.

2.5.2. Active Mode --> Idle Mode/Sleep Mode- Example program

The following example, the program design is applied to ADC and LCD IP, before entering Sleep Mode, do the corresponding shutdown action :

```
//Sleep Mode setting, Closed VLCD+Clock
DrvLCD_VLCDMode(0);    //LCD VLCD
while((inw(0x41B00)&(1<<IDF))==0);    //Wait LCD Idle, IDF=20
DrvCLOCK_SelectMCUClock(E_LS_CK,0);    //SET CPUCKL=LPO/1
DrvCLOCK_CloseIHOSC();    //Close HAO

// Sleep Mode setting, Closed VDDA+ADC
DrvPMU_VDDA_LDO_Ctrl(E_PullDown);    //Closed VDDA
DrvPMU_BandgapDisable();    //Closed Bandgap
DrvADC_Disable();    //Closed ADC
```

```
//Enter sleep Mode
DrvPMU_LDO_LowPower(1);    //Closed VDD18 LDO
SYS_LowPower(0);    //Enter Sleep Mode
```

Description: In this sample program, before entering Sleep Mode, first close VLCD and Clock, and then close VDDA and ADC. After confirming that the related IPs are completely closed, do the last VDD18 LDO close before entering Sleep Mode. After entering Sleep Mode, the power consumption of 2.5uA can be measured.

2.5.3. Idle Mode/Sleep Mode --> Active mode- Precautions for use

To wake up from Idle or Sleep Mode, do the following settings in sequence:

1. First, you can turn on the HAO high-frequency oscillation. After the HAO high-frequency oscillation is turned on, you also need to wait for a stable period of time.
2. After HAO is stable, do other analog power restarts and IP settings.

An application example is given: the PWM frequency source is selected as HAO. After entering Sleep Mode, the HAO high-frequency oscillation will be turned off. When the chip wakes up from Sleep Mode, restart PWM for output, and find that PWM has no action. This is because HAO did not restart first, and the PWM frequency source HAO did not oscillate. For applications like this, users need to pay special attention when developing programs.

2.5.4. Idle Mode/Sleep Mode --> Active mode- Example program

The following sample program is to re-initialize the corresponding ADC and LCD IP after waking up from Sleep Mode.

```
//VDD18 LDO On
DrvPMU_LDO_LowPower(0);    //Enable VDD18 LDO

//Clock start to work
DrvCLOCK_EnableHighOSC(E_INTERNAL,10);    //Enable HAO
DrvCLOCK_SelectMCUClock(E_HS_CK,0);    //SET CPUCKL=LPO/1
Delay(5000);    //Delay time for HAO stable

// LCD start to work
DisplayInit();    // re-initial LCD

//ADC start to work
DrvPMU_VDDA_LDO_Ctrl(E_LDO);    //Enable VDDA
DrvADC_ClearIntFlag();
```

```
DrvADC_Enable();    //Enable ADC
DrvADC_CombFilter(ENABLE);      //Enable comb filter
DrvADC_EnableInt();
```

Description: This sample program, after waking up from Sleep Mode, firstly restarts the Clock action, and then performs the LCD, VDDA, ADC and other related IP initialization actions.

2.5.5. Idle Mode/Sleep Mode --> Active mode- GPIO Wake-up use precautions

The GPIO of HY16F is often used as a wake-up button design for Sleep or Idle Mode. In the program settings, special attention should be paid to adding the IDF interrupt condition flag judgment of each GPIO, so as to avoid the situation that the GPIO wakes up from the Sleep/Idle Mode crash.

Example: If PT1.7 is set as the wake-up button for Idle or Sleep Mode, before the chip enters Idle or Sleep Mode, it must first determine whether the PT17IDF interrupt condition flag is 1, and the interrupt condition flag is 1 before entering Idle or Sleep Mode.

GPIO Base Address + 0X0C (0X4080C)						
Symbol	PT1CR3 (PT1 Control Register 3)					
Bit	[31:24]	[23:21]	[21:18]	[17:16]		
Name	PT17IDF~ PT10IDF	PT17ITT	PT16ITT	PT15ITT		
RW	R-0	RW-0				
Bit	[15]	[14:12]	[11:9]	[8:6]	[5:3]	[2:0]
Name	PT15ITT	PT14ITT	PT13ITT	PT12ITT	PT11ITT	PT10ITT
RW	RW-0					

Bit	Name	Description
		PT1.7 Interrupt condition flag For example: check this flag before entering the Sleep Mode: When Bit = 1b, can be PT1.7 pin wake up MCU. When Bit = 0b, PT1.7 pin cannot be awakened MCU.

2.6. Internal high speed HAO & Internal low speed LPO

When the CPU power on and switches the internal high-frequency oscillation for use, you should pay attention to waiting for the stabilization time. You shouldn't rush to do other things when the oscillator has not stabilized. In addition, users often have problems such as UART transmission data errors in some chips during mass production, and this problem is also closely related to HAO related settings.

2.6.1. Internal high speed DrvCLOCK_CalibrateHAO- Precautions for use

For the HY16F19x series, the HAO of each frequency band provides correction(HAO trim)values for users to use. After filling the correction(HAO trim) value into the HATOR register, the HAO frequency error can be reduced within 2%. When users use the UART function, if they use HAO as the main frequency of the UART, they must use the DrvCLOCK_CalibrateHAO function, which can reduce the HAO frequency error within 2%. It can solve the problem of UART transmission data error in some chips during mass production.

2.6.2. Internal high speed DrvCLOCK_CalibrateHAO- Example program

The sample program is as follows:

```
DrvCLOCK_EnableHighOSC(E_INTERNAL,10);     //Select HSRC
DrvCLOCK_SelectIHOSC(1);    //Select internal 4MHZ
DrvCLOCK_SelectMCUClock(0,0);    //CPU CLOCK IS 'hs_ck/1'
DrvCLOCK_CalibrateHAO(1);    //Calibration HAO_4MHz=4.147MHz
DrvUART_ClkEnable(1,0);    //choose the internal HAO as UART clock source
DrvUART_Open(4147,B9600,DRVUART_PARITY_NONE,DRVUART_DATABITS_8,DRVUART_STOPBITS
_1,2);
```

Description:

In this sample program, HAO=4MHz is preset, and the frequency error of HAO is 4MHz +/- 10%. When the function DrvCLOCK_CalibrateHAO(1) is executed, After filling the correction(HAO trim) value into the HATOR register, it can make the frequency of HAO to be 4.147MHz +/- 2% error. After the HAO frequency setting is completed, the UART frequency source setting option also needs to enter the correct value. This can effectively solve the problem of UART transmission data errors in some chips during mass production. And it should be noted that the HAO frequencies of different frequency bands have different HAO Trim values, so when HAO=4MHz is set, only DrvCLOCK_CalibrateHAO(1) can be selected. When HAO=2MHz is set, only DrvCLOCK_CalibrateHAO(0) can be selected. So on and so forth.

2.6.3. Internal high speed HAO & low speed LPO- Precautions for use

Notes on using the internal crystal oscillator :

- When using HAO 16MHz crystal oscillator, the operating voltage of the chip must be limited to high voltage operation.
- Set the value of register HAOTR 0x40304[7:0] to adjust the HAO output frequency value.
- Example: When HAO is set to work at 2MHz, if the actual output is only 1.99MHz, then the frequency output can be adjusted by adjusting the control bits HAOTR[7:0]. The default value of HAOTR is 0x80, and the HAO actual operating frequency can be increased by adjusting it upwards.
- The chip's default startup oscillator is the internal HAO 2MHz, and the user can set the register 0x40300[4:3] to configure other HAO output frequency values.
- Settling time for HAO configured to 4MHz onset is about 0.5ms.
- After executing the sleep (SLEEP) command, all HAO oscillators will stop oscillating and enter the sleep state
- The time from Sleep Mode to wake-up is about 1024*HAO+2048*LPO=< 64ms.

Note: If you want to meet the wake-up time described above, you should select HAO as the CPU frequency source before entering Sleep Mode.

- Executing the IDLE instruction will not stop the HAO oscillator, but the CPU will enter the standby state.
- It takes about 500 instruction cycles from Idle Mode to wake-up. When the CPU Clock uses the default HAO=2MHz, the wake-up time is about 250us.

The LPO is a low-speed RC oscillator inside the chip, with an operating frequency of 35KHz, with low power consumption and current characteristics. It starts to vibrate after the chip is powered on or wakes up, and the LPO cannot be turned off. The LPO is running throughout the working process of the chip.

- The LPO start-up stabilization time is about 510us and is the only working clock source for the watchdog (WDT).
- After executing the sleep command (SLEEP), the LPO oscillator will stop oscillating.
- After executing the standby instruction (IDLE), the LPO will not stop oscillating, but the CPU will enter the standby state.
- It takes about 500 instruction cycles from Idle Mode to wake-up. When the CPU Clock uses the preset LPO=35kHz, the wake-up time is about 14ms.

2.6.4. Internal high speed HAO =16MHz- Precautions for use

When the HY16F chip is at HAO=16MHz, and the operating voltage of the chip is lower than 2.2V~1.8V, there will be a chance that the PC counter will jump, causing the program to malfunction. Therefore, in the case of setting HAO=16MHz, it is recommended to set the main operating frequency of the CPU to HAO=16MHz/2 instead of using HAO=16MHz/1. This can reduce the problem of PC counter jumping. If the application must work at HAO=16MHz/1, a Reset IC can be added externally. When the working voltage of the HY16F chip VDD3V is lower than 2.2V, immediately pull the voltage to 0V, Avoid the occurrence of chip operating voltage in the range of 1.8V~2.2V..

2.7. Flash

HY16F series are Flash products, you can plan and specify the location of the Flash block for the Data Flash to use as the storage effect parameter. Before using Flash for data (Write/Read) access, some usage restrictions should also be noted.

2.7.1. Flash Read/Write- Precautions for use

1. Before executing the flash write and read commands, you must execute SYS_DisableGIE(); disable the global enable interrupt, which can avoid the abnormal behavior of the program running.
2. Flash has a limit on the number of writes, and Flash has a guaranteed write life of at least 20,000 times. Before performing Flash Write, there must be an Erase action, so that the writing will be normal. The flash life is calculated according to the number of erases, not The number of writes. Erase all+ N* Page Write, only counts the lifetime of 1 use. The same Page uses N*page Erase, it means that N times of life have been used.
3. Flash Write and Read have write time. Users can directly use the Flash-related control functions of the HY16F C library to do Write and Read. It takes about 30ms to use ROM_BurnWord or ROM_BurnPage, and about 25ms to use PageErase or SectorErase. The above function already contains the Erase function.
4. When executing the Flash (write)programming command, make sure that the chip operating voltage VDD3V is higher than 2.7V. If the chip voltage VDD3V is lower than 2.7V, (write)programming errors may occur.

The following describes the execution time of Flash Read/Write library instructions :
1. DrvFlash_Burn_Word(unsigned int addr,unsigned int DelayTime,unsigned int data): The execution time is about 30ms, and the delay time is filled with 0x2000 (when HAO=2M, fill in 0x2000, when HAO=4M, fill in 0x4000 and so on)
2. ROM_BurnPage(unsigned int addr,unsigned int DelayTime,int* data); The execution time is about 30ms, and the Delay time is filled with 0x2000 (when HAO=2M, fill in 0x2000, when HAO=4M, fill in 0x4000, and so on)
3. PageErase(unsigned int addr,unsigned int DelayTime); The execution time is about 25ms, and the Delay time is filled in with 0x2000 (When HAO=2M, fill in 0x2000, when HAO=4M, fill in 0x4000 and so on)
4. SectorErase(unsigned int addr,unsigned int DelayTime); The execution time is about 25ms, and the Delay time is filled in with 0x2000 (When HAO=2M, fill in 0x2000, when HAO=4M, fill in 0x4000 and so on)

2.8. LCD

HY16F19xB series products have LCD IP function. When using LCD, you need to pay attention to the VLCD operating voltage, and also need to pay attention to the LCD operating frequency LCK setting. If the voltage setting does not match the voltage of the LCD panel, it will cause the LCD display to appear insufficiently bright or the areas of the LCD that are not lit up to appear to be lit display problems (obvious from an oblique viewing angle). If the LCD operating frequency is set too slow, there will be an abnormal display of flickering frequency from the LCD display. Therefore, special attention should be paid to the LCD operating voltage VLCD and LCD operating frequency LCK settings.

2.8.1. DrvLCD_VLCDTrim- Precautions for use

The VLCD voltage has a (VLCD Trim)correction value that can be used. When using the function DrvLCD_VLCDTrim, the VLCD correction value can be brought in, so that the VLCD voltage can be controlled within a 5% error range. If the function DrvLCD_VLCDTrim is not used, the VLCD voltage error is within 10%. Users often find that the LCD display of some chips is too bright or too dark during mass production. This is due to the 10% error of VLCD voltage mass production. If the function DrvLCD_VLCDTrim is used, the VLCD voltage problem caused by mass production can be effectively solved, and the VLCD voltage error range of mass production can be controlled within 5%.

2.8.2. DrvLCD_VLCDTrim- Example program

```
//Case5, VLCD=2.55V, +/- 5% :
DrvLCD_VLCDMode(E_VLCD24);
DrvLCD_VLCDTrim(5);

//Case4, VLCD=2.73V, +/- 5%
DrvLCD_VLCDMode(E_VLCD27);
DrvLCD_VLCDTrim(4);

//Case3, VLCD=2.93V, +/- 5%:
DrvLCD_VLCDMode(E_VLCD30);
DrvLCD_VLCDTrim(3);

//Case2, VLCD=3.16V, +/- 5%:
DrvLCD_VLCDMode(E_VLCD30);
DrvLCD_VLCDTrim(2);
```

```
//Case1, VLCD=3.43V, +/- 5%: :
DrvLCD_VLCDMode(E_VLCD33);
DrvLCD_VLCDTrim(1);
```

Explanation: This sample program shows how to set the valid value in the VLCD voltage, using the DrvLCD_VLCDMode and DrvLCD_VLCDTrim functions together. It should be noted that because different VLCD voltages have their own VLCD Trim values, So set the correct use just follow the Case1~Case5 methods in the sample program to use

2.8.3. LCD Frequency LCK- Precautions for use

LCD frequency (LCK) setting problem, when the LCD is set to 1/4duty, the external voltage is R-TYPE, and the scanning frequency of LS_CK/8/32=136HZ=LCK is selected, the LCD display will flicker. According to 4com, if you want to see the LCD without flickering, the LCD frame Freq should be close to 60Hz. Therefore, the LCD scan frequency should be at least 4com x 60 = 240Hz. The time of LCK is calculated in half cycle (1/2T), so LCK should be set to 240Hz x 2= 480Hz, so it should be changed to LS_CK/8/ 8=544Hz, to avoid the problem of display flicker when connected to 4com LCD frame Freq will be written on the LCD specification (usually 50~60Hz).

2.9. RTC

For HY16F series products, RTC is a commonly used IP function. Here, we will introduce the precautions for the IP function of RTC.

2.9.1. RTC- Precautions for use

1. For programmers, if they want to enter the power saving mode (Sleep/Idle), they still continue to let the RTC do the counting work. It should be noted that the RTC can work in the Idle Mode, but the RTC cannot work normally in the Sleep Mode. The following is the RTC +Idle Mode reference operating current:
(1)RTC + idle without LCD, 8uA
(2)RTC + Idle + LCD pump, 18uA
(3)RTC + Idle + LCD pump + HYCON LCD panel, 25uA

2. The frequency source selection of the RTC can be the internal low frequency LPO or the external low frequency LSXT (32768Hz). If the external low frequency LSXT is selected, the 32768 start-up stability problem needs to be considered. The start-up stability problem involves the PCB Layout trace. It will be related to the brand specifications of the crystal oscillator. When connecting the external pins of the 32768 crystal oscillator, the HY16F series can choose to adjust the capacitance value (0~20pF) and the parallel connection resistance (10M ohm) to achieve the stable start-up of the 32768.

3. The register 0x41A04[22:16] of the RTC IP can provide RTC compensation. When the oscillation frequency of the external oscillator LSXT deviates from 32768Hz, the RTC counting frequency can be approached to 32768Hz by means of compensation, which can be compensated. The range is: the maximum input frequency is 32772Hz, and the minimum input frequency is 32763Hz. For example: the oscillating frequency of the external oscillator LSXT is 32764Hz, at this time, if the 0x41A04[22:16] register is filled with 0111111b, the compensation value is +126PPM, allowing the RTC counting frequency to reach 32768Hz.

4. In the actual circuit, the oscillator can be observed by the oscilloscope to determine whether the oscillator is working in the best state. When the oscilloscope observes the oscillator waveform, the OSCO pin (Oscillator output) should be observed, and an oscilloscope probe with a bandwidth of more than 100MHz should be selected. The input impedance of this probe is high, the capacitive reactance is small, and the impact on the oscillation waveform is relatively small. Since there is generally a capacitance of 10-20pF on the probe, when observing, appropriately reducing the capacitance on the OSCO pin can get closer to the actual oscillation. Waveform. A good oscillation waveform should be a beautiful sine wave, and the peak-to-peak value should be greater than 70% of the power supply voltage. If the peak-to-peak value is less than 70%, the external load capacitance on the OSCI and OSCO pins can be appropriately reduced. On the contrary, if When the

peak-to-peak value is close to the power supply voltage and the oscillation waveform is distorted, the load capacitance can be appropriately increased.

5. In the oscillation circuit, a very important characteristic is the load capacitance (Load Capacitance; CL) on the entire circuit, which is determined by the frequency adjustment capacitor CG of the gate terminal (OSCI), the frequency adjustment capacitor CD of the drain terminal OSCO and the miscellaneous It is composed of three parameters such as the stray capacitance CS. The load capacitance and the two frequency adjustment capacitors are known, and the stray capacitance value can be obtained by the following formula:
CL = (CG // CD) + CS --->> CL = [(CGxCD)/(CG+CD)] + CS
Usually, the external load capacitance (CL) of 32768Hz recommended by manufacturers is 7pF, 9pF, and 12.5pF (usually 12.5pF is the most common specification),
The general stray capacitance (CS) = PCB stray capacitance + chip circuit junction capacitance, generally about 3~5pF, if CS is not considered for the time being,
Then CL = (CG // CD, 12.5pF= (CG // CD, get CG, CD use 25pF each.

2.10. Timer

For HY16F series products, Timer is a commonly used IP function. Here, we will introduce the precautions for the IP function of Timer.

2.10.1. TimerA- Precautions for use

When using TimerA, set DrvTMA_Open(0,0) and DrvTMA_Open(1,0) as the counter function, you will find the phenomenon of inaccurate and unstable counting. The HY16F CPU in and out interrupt consumes about 200 mechanical instruction cycles, If CPU=8MHz, the total consumption time is (1/8000000)*200=25us. When set to execute DrvTMA_Open(0,0), the interrupt time for one entry is 8000000/32(ENTAD=1b)/2(TAS=0000b)=125kHz=8us, the time of 8us is far less than 25us, the real situation will see that the program has been stuck in the TimerA interrupt and cannot enter the main execution

Similarly

DrvTMA_Open(1,0), the interrupt time for one entry is 16us

DrvTMA_Open(2,0), the interrupt time for one entry is 32us

32us>25us, stable output can be seen, therefore, when using TimerA for counting, the fastest recommended use is DrvTMA_Open(2,0).

2.11. DAC

The DAC of the HY16F is alone, and has no driver capability, about 15uA. If it is DAC+OP, the maximum is 1mA (in the case of VDDA=3V), 0.5mA (in the case of VDDA=2.4V). The user should pay attention to the size of the load driven by the DAC , to avoid the situation that the voltage of the DAC output is abnormally pulled down when the DAC output is under heavy load.

2.12. R2ROP

For HY16F series products, R2ROP is a commonly used IP function. Here is an introduction to the precautions for the IP function of R2ROP

2.12.1. R2ROP as unit gain buffer- Precautions for use

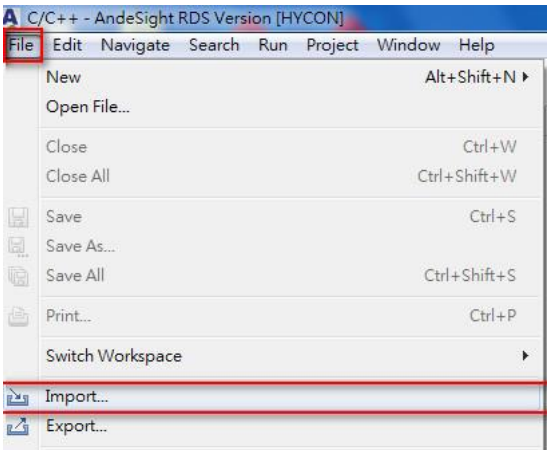
R2ROP When the unit gain buffer is applied, there will be an offset voltage when the input is from 0 to 5mV, and within this range, the voltage change cannot be observed from the output end, and the voltage output will not start until the voltage is about 6mV. If you want better linearity, it is recommended that the working voltage be within the range of VSSA+0.1V~VDDA-0.1V. Because of this limitation, a reference solution is provided here. The working voltage of the entire measurement system is raised, and the REFO pin of HY16F can be used to output 1.2V as the Bias voltage. The reference voltage point is changed from 0V to 1.2 V.

3. HY16F series development tool application description

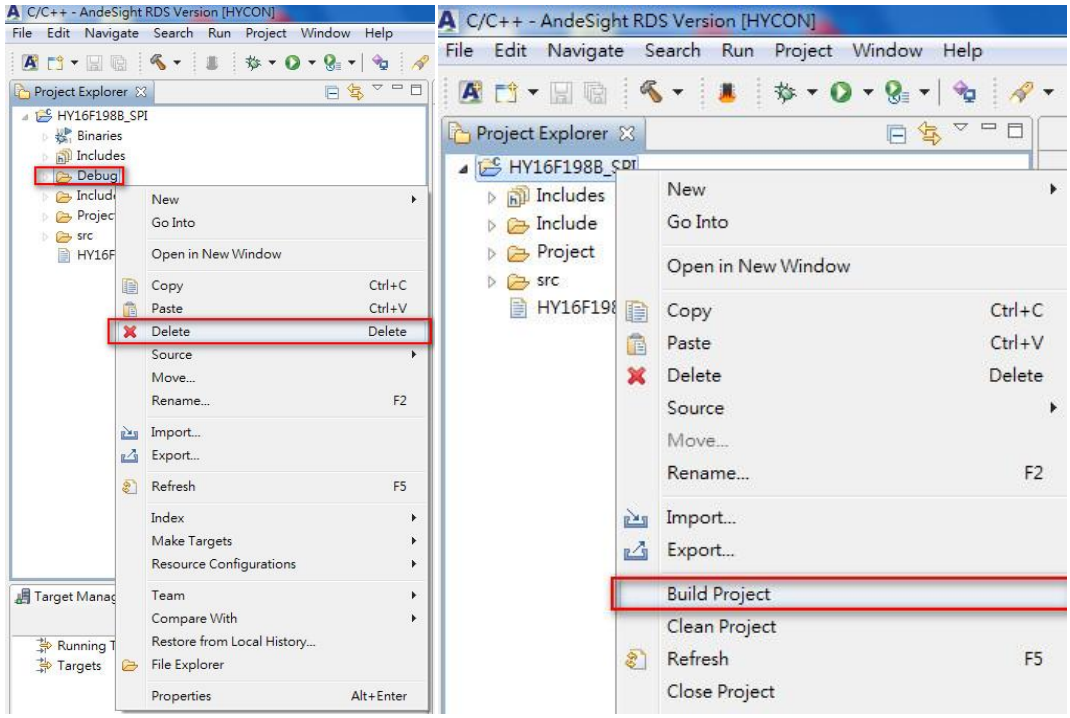
3.1.1. Convert AndeSightRDS V2.0.1 to AndeSightRDS V2.1.1

Before 2017, the standard development tool used was IDE: AndeSight RDS V2.0.1 with HY-Protool, after 2017, the updated development tool was IDE: AndeSight RDS V2.1.1 with HY16F Mini Link. The user should use the correct hardware development tools and IDE software version, so that the HY16F program development and debugging can be performed normally. In addition, it should also be noted that if the old AndeSight RDS V2.0.1 development project package is to be migrated to the AndeSight RDS V2.1.1 environment for continuous design and use, the following steps such as Step1~Step4 need to be done first to ensure that It is no problem to convert the old RDS V2.0.1 project package in the RDS V2.1.1 environment, and you can normally perform single-step debugging actions such as Debug.

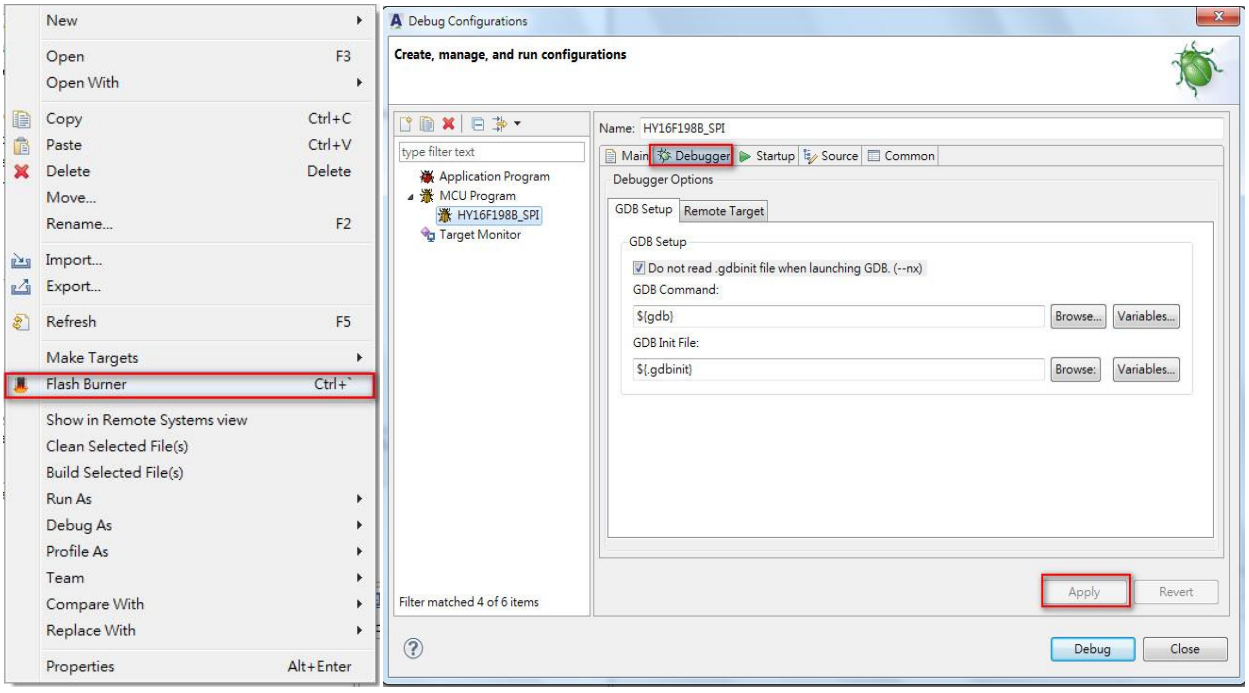
Step1 : Import RDS V2.0.1 project package under RDSV2.1.1 environment



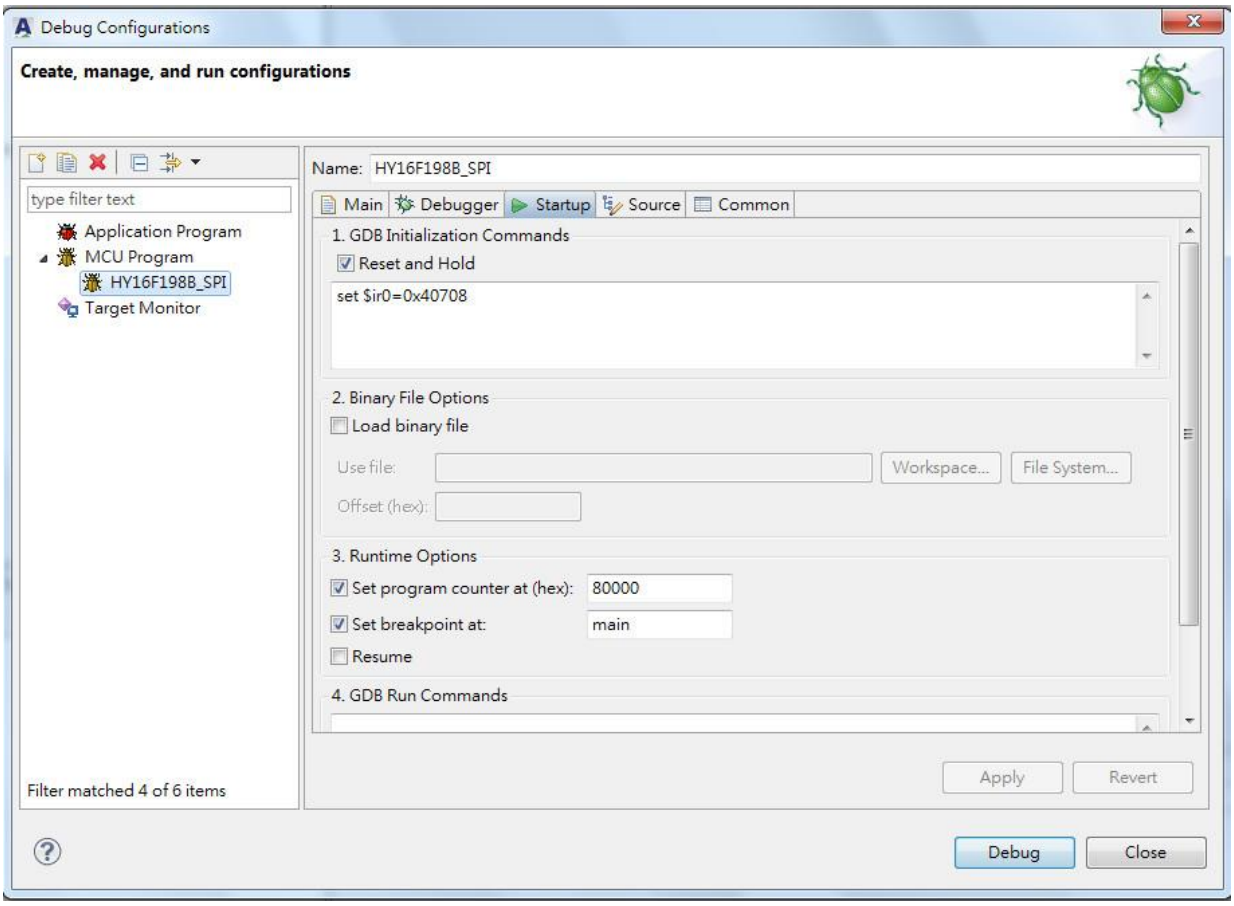
Step2 : After deleting the Debug folder Delete, rebuild the Project, create and generate a new Debug folder.



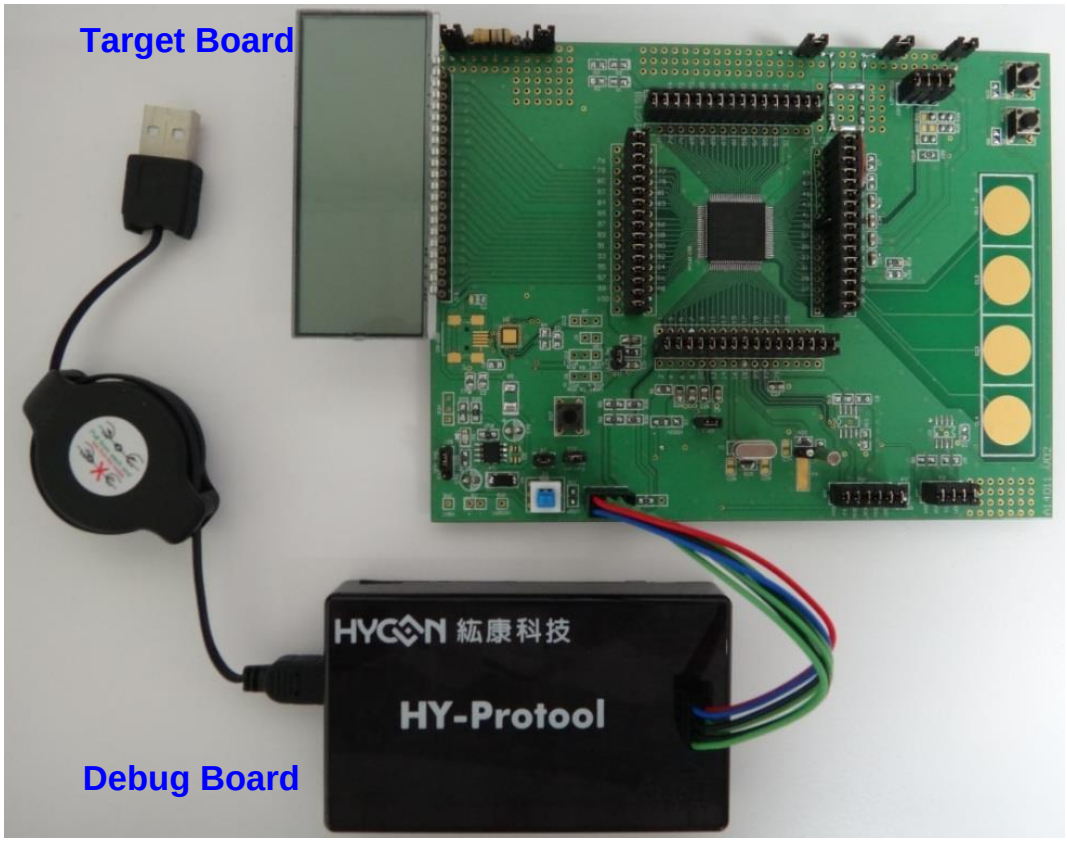
Step3 : After Build Project, execute Flash Burner to burn Code, click Debug Configurations to make sure the Debugger environment settings are exactly the same as the picture below.



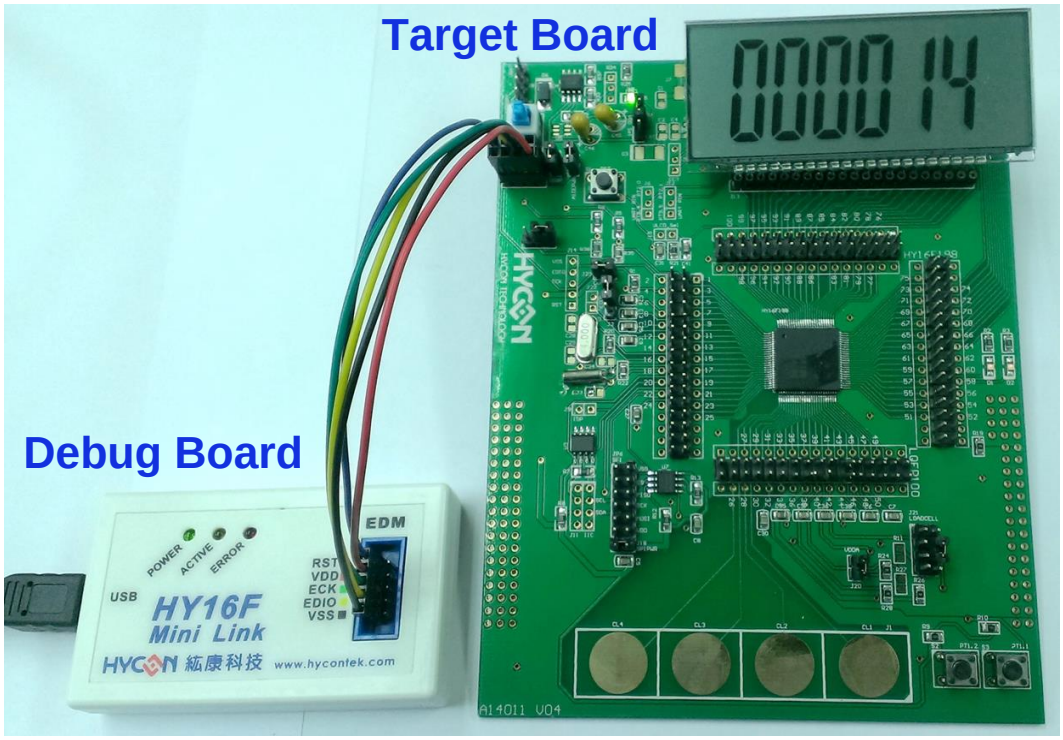
Step4 : Confirm that the Startup settings in the Debug Configurations environment are also the same as the following figure.


Debug Configurations
Create, manage, and run configurations
type filter text
Application Program
MCU Program
HY16F198B_SPI
Target Monitor
Filter matched 4 of 6 items
Name: HY16F198B_SPI
Main
Debugger
Startup
Source
Common
1. GDB Initialization Commands
Reset and Hold
set $ir0=0x40708
2. Binary File Options
Load binary file
Use file:
Workspace...
File System...
Offset (hex):
3. Runtime Options
Set program counter at (hex):
80000
Set breakpoint at:
main
Resume
4. GDB Run Commands
Apply
Revert
Debug
Close

The picture below shows HY16F19xB with HY-Protool hardware development kit (HY16F19x-DK02), the actual use should be with IDE:AndeSight RDS V2.0.1 :



The picture below shows HY16F19xB with HY16F Mini Link hardware development kit (HY16F19x-DK04), the actual use should be with IDE: AndeSight RDS V2.1.1 :



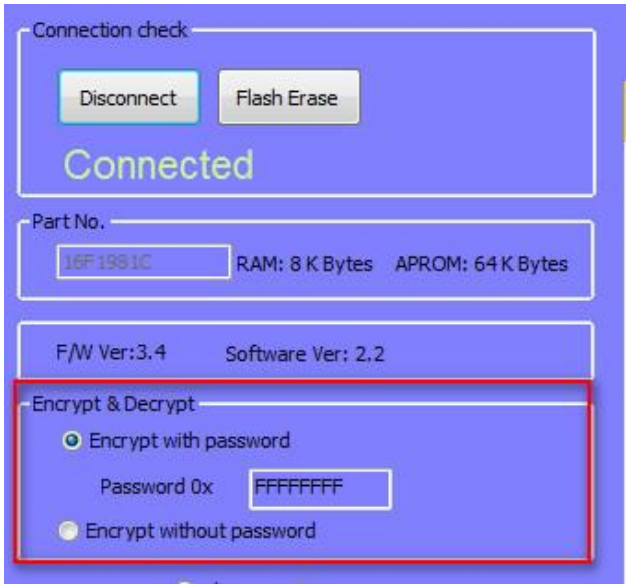
3.1.2. How much SRAM space does Stack occupy

The composition of SRAM consists of four elements data+bss+heap+stack. Among them, the starting position of the stack is 0x1fC0, which is dynamically configured, depending on how the program is written to dynamically configure and grow. If the program writes more layers of call functions, Then the stack will grow bigger and bigger. The stack grows back slowly from the tail position of SRAM 0x1fc0 --> 0x1fbf-->0x1fbe, while bss and data grow slowly from the starting position of 0x40 of SRAM. Until it follows bss If the variables in the data block overlap with the stack, then there may be a problem that the declared variables are messed up, resulting in program errors.

For example: SRAM uses 7.5kB space (data=522, bss=7239), which means that the stack only has 8128-7239-522=367 space left to use. If you continue to develop programs in this case, it will be easy for stack and bss/ The data of the data block overlaps, causing unexpected errors to occur in the program. Because the current Andes CPU N801 does not provide the function of stack protection, the program cannot file this problem during the compile process. When the user develops the program, the SRAM Memory planning requires special attention.

4. HY16F series encryption & decryption function description

HY16F series products can perform chip encryption and decryption operations through HY16F Writer, which can prevent the code in the chip from being read out. The encryption and decryption behavior of HY16F18x/HY16F19x/HY16F19xB/HY16F3981 series products is a little function difference, the following will strengthen the description function, the picture below is the encryption operation screen of HY16F Writer.



1. Encrypt with password function: (default is 0xFFFFFFFF, you can freely set the password for protection, even if you enter the correct password, HY16F19xB/HY16F3981 will force to erase part of the Flash, but HY16F19x/HY16F18x will not)

When setting Encrypt with password, if the password is entered correctly, the Code will be erased, and the erase range of the Code is based on the range of the password-protected programming APP at that time.

EX : Assuming that the APP size is 6KB Flash, select Encrypt with password and enter the password 0x12345678. When you want to connect again, you will be asked to enter the password. When the password is entered correctly, the range of 0x90000~0x91800 will be erased by Erase becomes 0xFF, At this time, the password status will be released to 0xFFFFFFFF, enter the password to erase the Flash correctly, this is the IC design behavior of HY16F19xB/HY16F3981, but this behavior will not happen in HY16F19x/HY16F18x.

For HY16F19xB/HY16F3981, when choosing Encrypt with password and setting a password, you can choose to enter the correct password as the method to connect and erase the Flash APP size and password, or choose FlashErase for the brute force method (no password required). To clear all 64KB Flash

For HY16F18x/HY16F19x, when you select Encrypt with password and set a password, enter the correct password, you can connect normally, but the Flash will not be erased, and the password status still exists, unless you press Flash Erase or re-burn Record a new set of passwords to unlock the password. But if the password is forgotten, press Flash Erase, the Flash still cannot be erased, and the unlocking action can be performed only when the password is known.

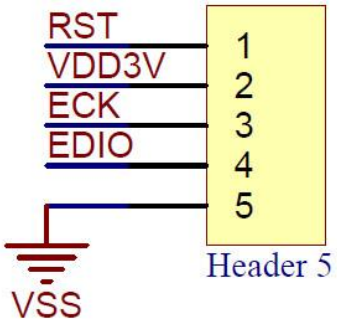
2. Encrypt without password function: After setting, the Flash content cannot be read out. Only Flash Erase can be used to erase the 64KB Flash to 0xFF, so that the chip can return to the original state. This is a method for unlocking the password. This function , HY16F18x/HY16F19x/ HY16F19xB/HY16F3981 are all the same, and there is no difference.

5. Precautions for HY16F series hardward design

HYCON HY16F series chips are ΣΔ ADC+MCU products, with high resolution and high precision capability, and are particularly sensitive to tiny leakage current and signal interference due to the resolution capability of the minimum 65nVrms signal. So here are some basic chip related The concept of circuit design and PCB wiring allows users to develop products more easily.

5.1.1. Precautions for schematic design

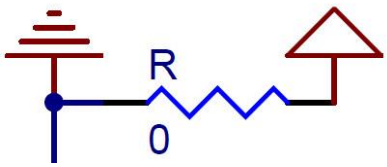
1. When designing and planning the circuit, it is best to reserve a dedicated 5pin Connector (2.54mm pitch) for programming and Debug, and the pin arrangement order should be the same. During product development and mass production, it can be directly connected with the HY16F programmer or The HY16F Mini Link is directly connected, which is convenient for development and programming.



2. When the ADC Output rate is less than 1k, the ADC measurement channels AIO0-AIO1 and AIO2-AIO3 and other ADC input pins are externally connected with 100nF capacitors. When the ADC Output rate is greater than 1k, the external 10nF capacitors are connected to the two ADC measurement channels. External capacitors between pins can enhance anti-noise interference

3. VDDA is connected to 10uF to ground, VDD18 is connected to 1uF to ground, and VPP remains NC.

4. When planning the circuit, the analog ground and the digital ground should be marked with different symbols, and a 0 ohm short-circuit resistor should be designed between the analog ground and the digital ground.



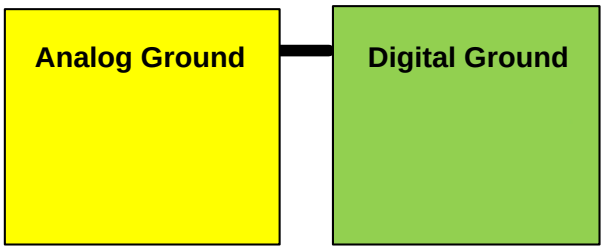
5.1.2. Precautions for PCB layout design

Be sure to follow general PCB layout rules and knowledge. For example, right-angle traces will cause trouble for EMI, and 45-degree corner traces are better.

5.1.2.1. Power Layout :

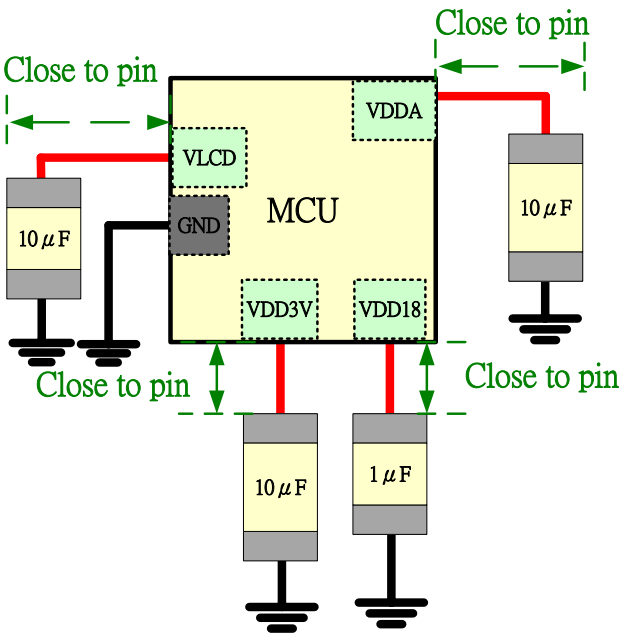
1. The GND of analog signal and digital signal must be separated and independent :

The most direct impact is that when the button switch is pressed, there will be a current loop flowing into the VSS to generate a potential difference (PCB wiring resistance). This potential difference is likely to cause measurement errors in the application of high ADC resolution products, ranging from a few ADC Count to several ten ADC Counts. Therefore, it is recommended to use separate analog and digital grounds to avoid measurement errors. At the same time, in order to enhance the anti-interference ability, the two ground trace are connected by a short-circuit trace, and the short-circuit position is preferably close to the battery VSS position for short-circuit.



2. The power traces should be as short as possible; the shorter the traces, the lower the impedance, the better:

The stabilizing capacitor at the pin end should be placed close to the chip. Such as pins: VDD, VDDA, VLCD, VDD18, REFO.

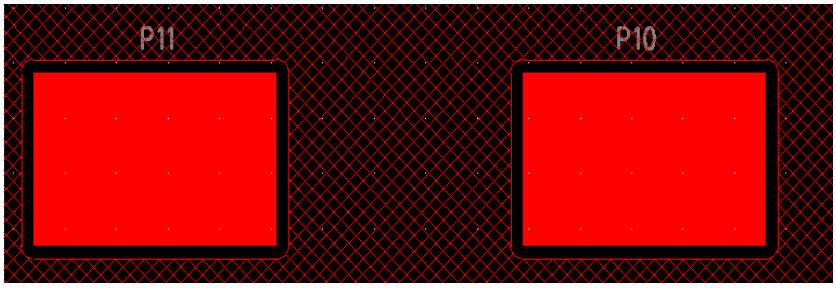


3. Copper pour:

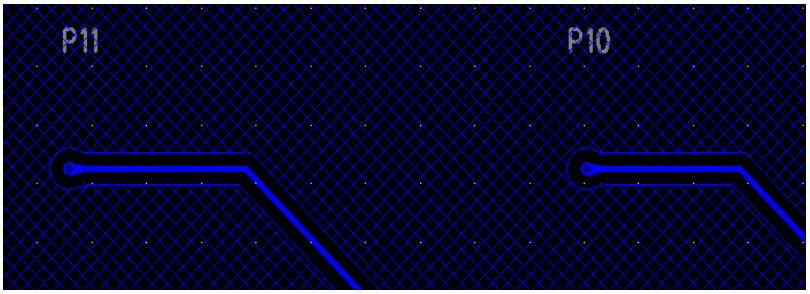
Ground copper is required on both the top and bottom layers of the PCB. Applying ground copper to the trace will increase noise immunity. We define the width of the ground copper to the trace is 5mil, the line spacing is 20mil, the grid spacing is 20mil, and the top and bottom layers have ground copper. Due to the strategy of the PCB factory, the line width must be set to 10 mil or more. The line width of the ground copper is set to 10 mil, the line spacing is 20 mil, and the grid spacing is 40 to meet the limit.

Please refer to the top and bottom layer diagrams below.

Copper pour to the top layer :



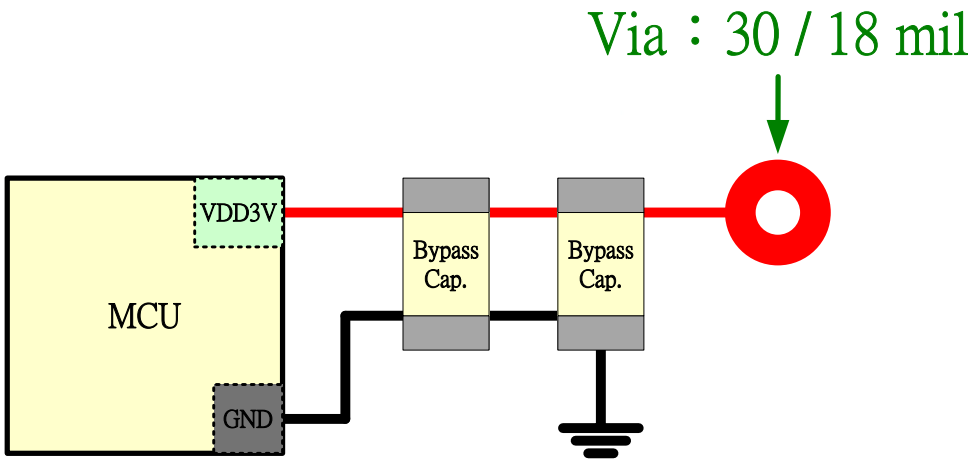
Copper pour to the button layer :



4. VDD3V/GND line and power supply through hole:

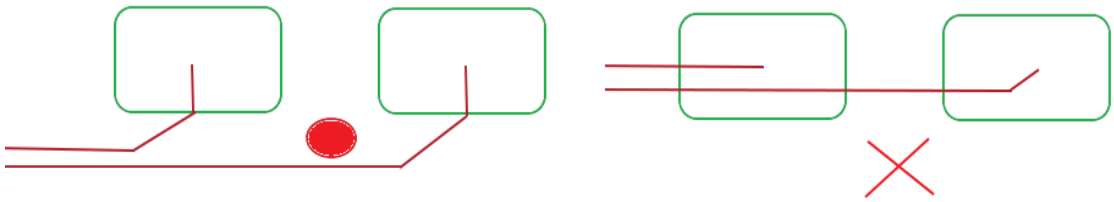
It is recommended to use 25~30mil for VDD3V/GND. The through hole of the power supply should be added to the decoupling capacitor. It is recommended to place it as shown in the figure below to provide proper decoupling capability, the noise from the power source will be decoupled through the capacitor to ground and flow back to the power source. The size of the through hole used for VDD3V/GND is recommended to be 30/18mil to reduce the equivalent inductance of the through hole structure. Internal LDO bypass capacitor lines (eg: VDDA and REFO output pins), internal LDO bypass capacitors are recommended to use 10~20mil wide PCB lines to provide stable power

VDD3V through holes and lines:



5. 2-Layer PCB design :

In the 2-layer PCB design, it is recommended to use 5~10mil wide traces for design. The spacing between traces is recommended to be twice the trace width (10~20mil recommended) to avoid interference. Examples of good and bad traces are as follows: The pad in this example represents the ADC sensor pin, and there should be no traces crossing the sensor pin.

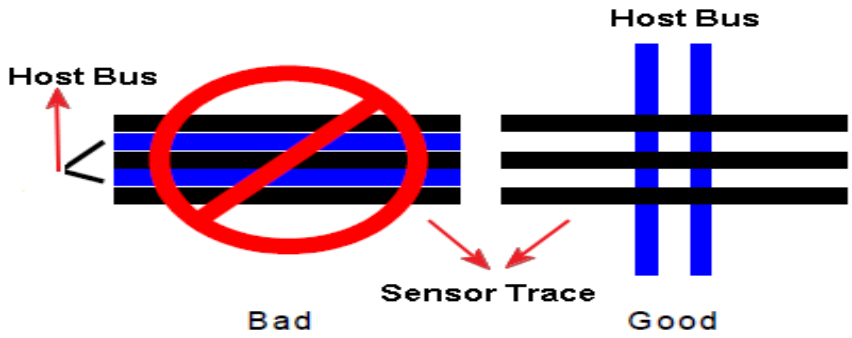


6. The digital signal trace between the host and the sensor controller:

The digital signal is the communication line with the host. Compared with other sensing traces, the switching frequency is relatively high. It is recommended to design the digital signal line with a 5~10mil wide line for the clock and data pins. Clock and other signals (power, The spacing between data, control, sensor lines) is recommended to be at least twice the line width (should be 10~20mil).

It is forbidden to route these digital signal lines in parallel with the analog lines. The parallel structure will cause a lot of crosstalk. If it is unavoidable that the digital signal lines are routed close to the sensor lines, it is recommended to use a 90-degree right-angle line for the interleaved part to reduce crosstalk effect.

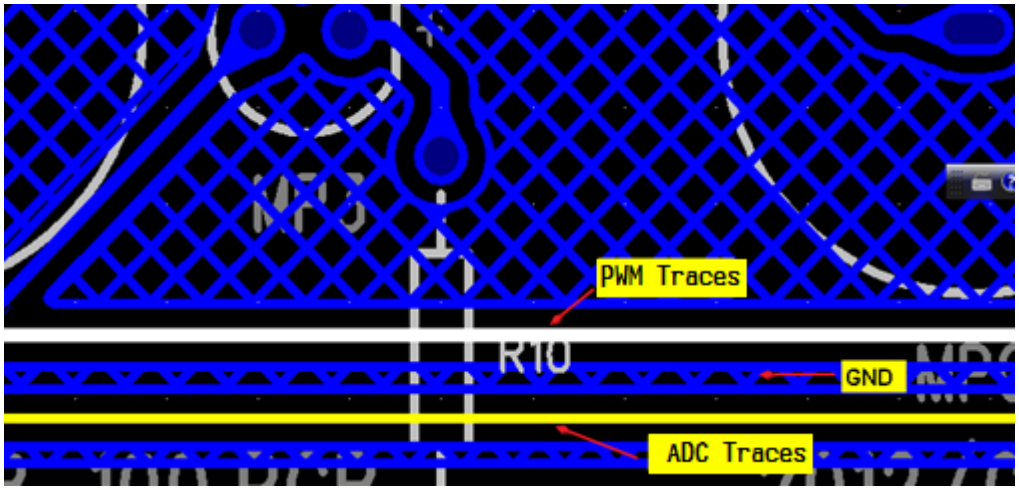
Bad and good host bus and analog signal routing:



7. Digital signal (PWM) circuit and analog signal (ADC) circuit:

Please note that it is forbidden to run the PWM control trace and the ADC trace in parallel. Please insert ground copper between the digital control trace and the analog trace. If the ground copper is not inserted between the digital control trace and the analog trace, the recommended distance is at least 50mil

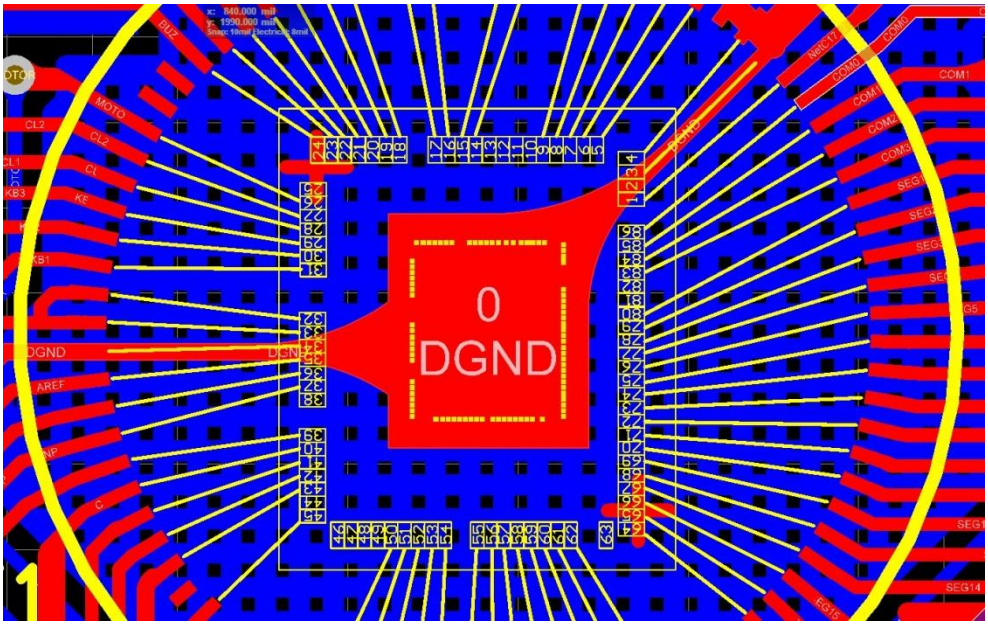
Please note: The inserted ground should not be grounded only on one side, otherwise a Uni Polar Antenna will be formed, which will affect the overall performance during EFT interference. The grounding between the PWM circuit and the analog signal circuit can be referred to the following figure:



Please note: If the PWM control line crosses the analog line vertically, SMT (Surface Mount Mount) components shall not be used to avoid the vertical crossover distance being too close, which will cause the analog signal to be disturbed. Ensure that the PWM control circuit and the analog circuit are kept at a distance of the board thickness (1.6mm).

8. Dice or COB Layout :

Please connect the metal surface on which the chip is placed to DGND (Digital GND). For detailed connection methods, please refer to the figure below.



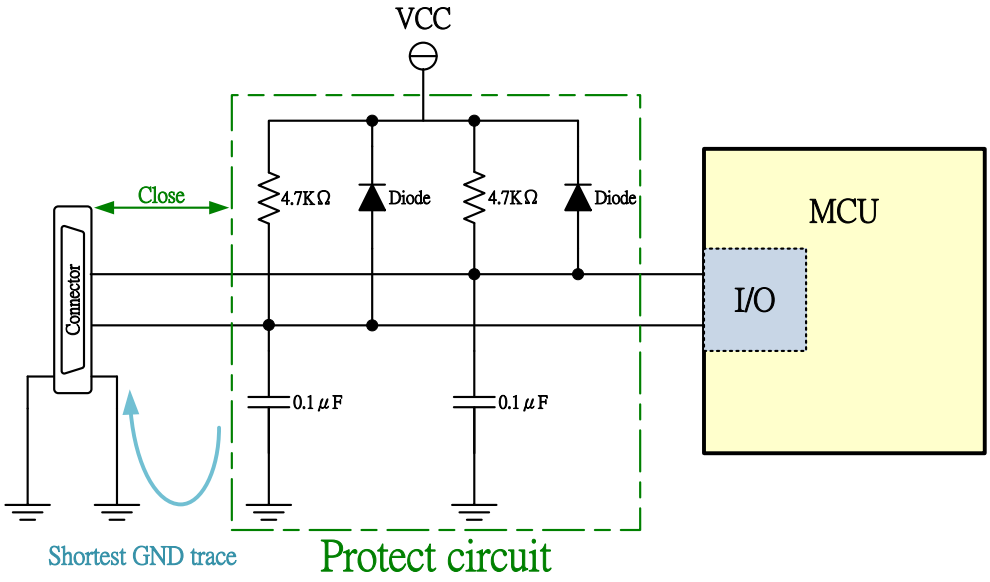
5.1.2.2. Analog Layout :

1. The input capacitors (0.1uF) of the analog input AIO0 and AIO1, AIO2 and AIO3, etc., should be as close to the pins as possible. When external signals are input, the traces should pass through the filter capacitors before connecting to the analog input pins of the chip.
2. For AIOx input pin traces, please run the traces in parallel and as short as possible. Avoid other horizontal or vertical cross traces on the upper and lower layers of the AIOx pin traces.
3. AIOx input pin, if possible, it is recommended to layout ground between AIOx pins

5.1.2.3. Digital Layout :

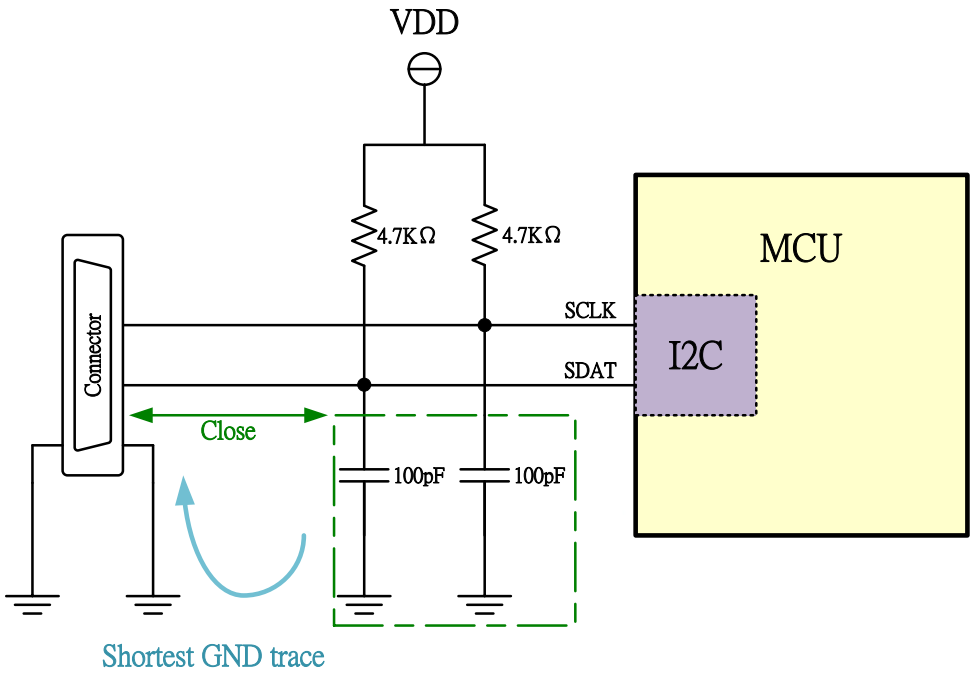
1. External 32768Hz oscillator pin (RTC), the traces should be as short as possible, and the grounding must be used to isolate the AC signal generated by other I/Os, so as to avoid the influence of the frequency generated by the RTC due to signal interference.
2. External 32768Hz oscillator pin (RTC), avoid (AIOx pin) too close.
3. External 32768Hz oscillator pin (RTC), avoid the power pin layout passing through
4. I/O port :

When using any I/O port to communicate with the host or power board, a protection circuit needs to be added. The protection circuit should be placed close to the connector port. If the capacitor is too far from the connector, the protection effect will be lost. Please note: the ground return of the ground capacitor The path to the power strip must be as short as possible.



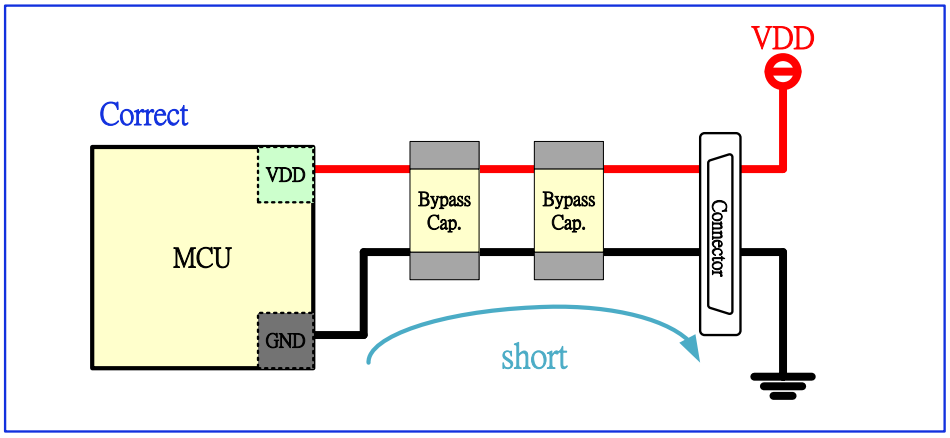
5. I2C Iinterface:

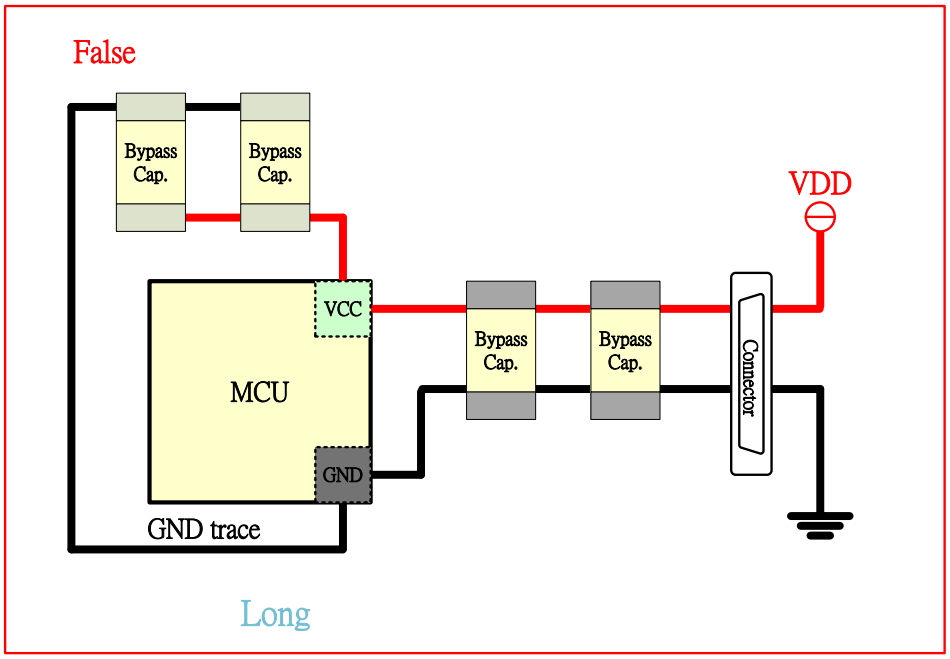
When using I2C as the host interface, SCLK/SDAT requires 4.7KΩ pull-up resistors for proper electrical characteristics. There may be slight differences in different applications and signal loads. Users can use external Pull-up resistor. Use a decoupling capacitor less than 100 pF externally, which can be used to reduce power supply noise and data processing noise (Noise). The decoupling capacitor should be placed close to the connector connected to the host side (Connector), and the ground loop should be as short as possible. Return directly to the ground (GND) of the Connector side.

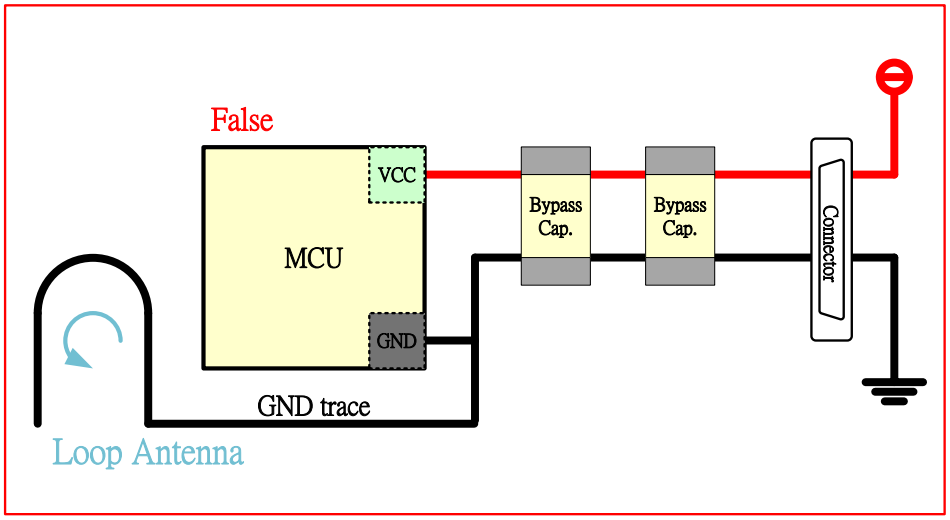


6. IC ground return path:

The ground return path of the MCU needs to pass through the ground point of the VDD/VDD18 filter capacitor. The traces when flowing back to the power connector port should be as short as possible to avoid excessive wiring. Also avoid becoming a “Loop Antenna”.


VDD
Correct
VDD
MCU
GND
Bypass Cap.
Bypass Cap.
Connector
short


False
Bypass Cap.
Bypass Cap.
VDD
VCC
MCU
GND
Bypass Cap.
Bypass Cap.
Connector
GND trace
Long


False
VCC
MCU
GND
Bypass Cap.
Bypass Cap.
Connector
GND trace
Loop Antenna

5.1.3. Precautions for RS protection design

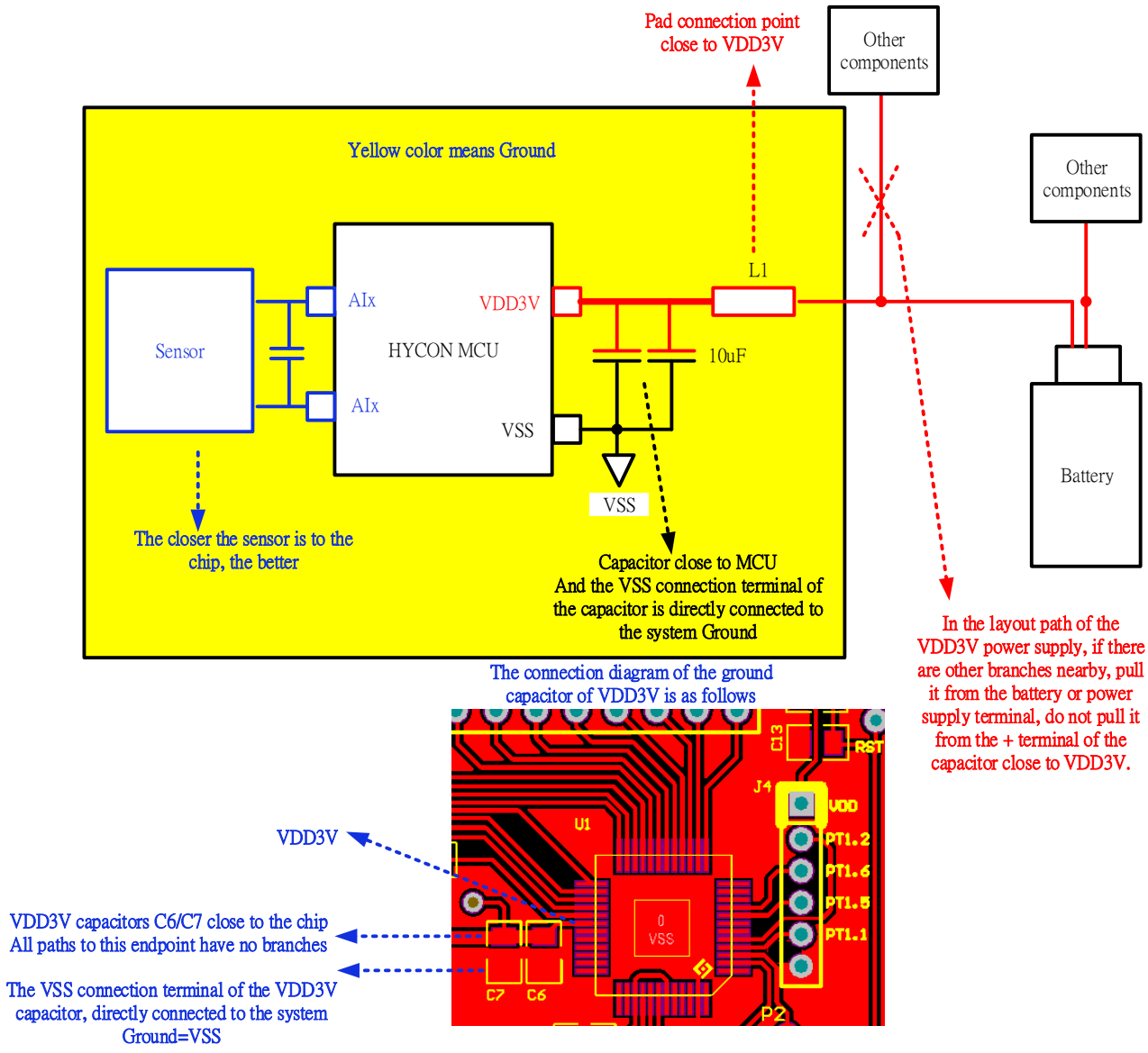
RS anti-interference, PCB Layout setting recommended teaching:

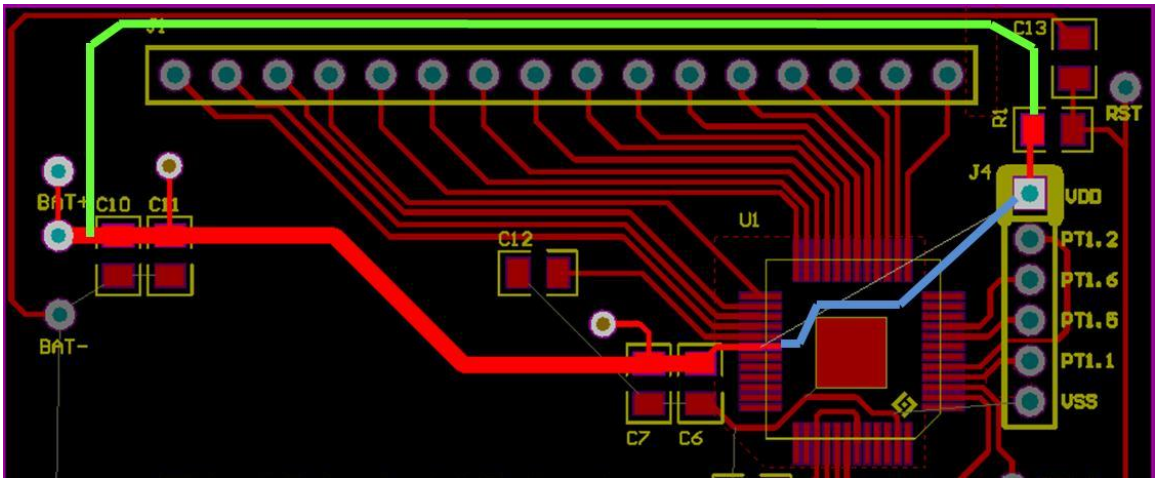
- Traces between Sensor and Aix don't go too far or go through communication traces.

- VDD power, if you want to add protection element magnetic beads, you need to connect the magnetic beads first and then connect to VDD3V. This VDD3V needs to be connected to 10uF and then 104pF (0.1uF) before it can be connected to the VDD3V pin of the MCU.

-The capacitor between VDD3V and ground should have the shortest path, and the path between VDD3V and ground capacitor should not be separated as far as possible.

Branch path. If there are other branch path requirements, please refer to the following diagram.



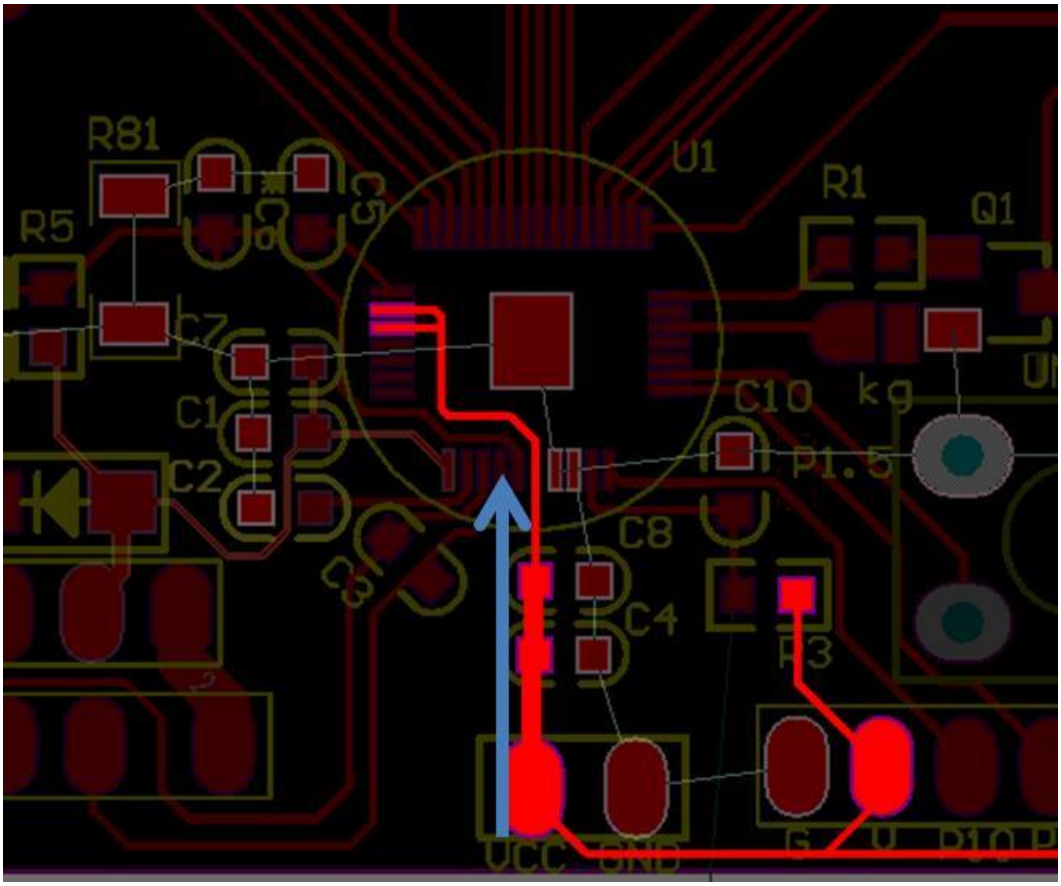


The example above, two notes

Note 1: **C7 and C6 are correct** for VDD capacitors, and **C10 and C11 are wrong examples**

Note 2 : There are two paths for chip connection to VDD: **blue line** and **green line**, **green line is correct, blue line is bad example**

When the external power supply is directly poured from the VDD pad, the blue line path is equivalent to the VDD3V pin of the chip, which is directly connected to the VDD pad first, and then goes through the capacitors C10 and C11, and finally reaches the capacitors C6 and C7.



The example above,

Note: After the Power enters the PCB, it goes to the VDD3V pin of the IC after passing through C4 and C8.

This is a correct demonstration

- Layout avoidance loop antenna effect

Figure 1

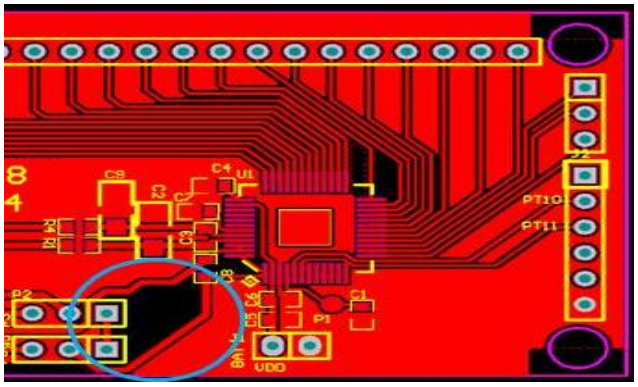
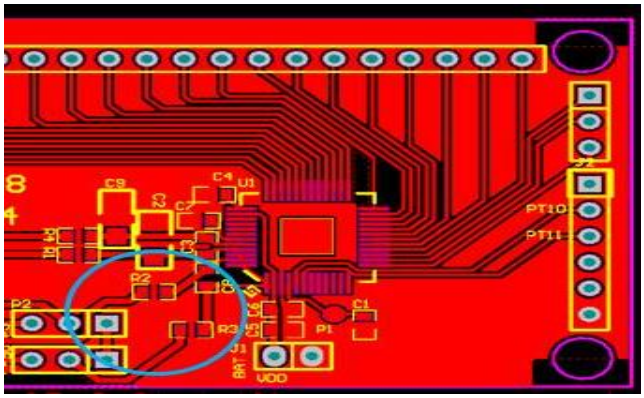


Figure 2

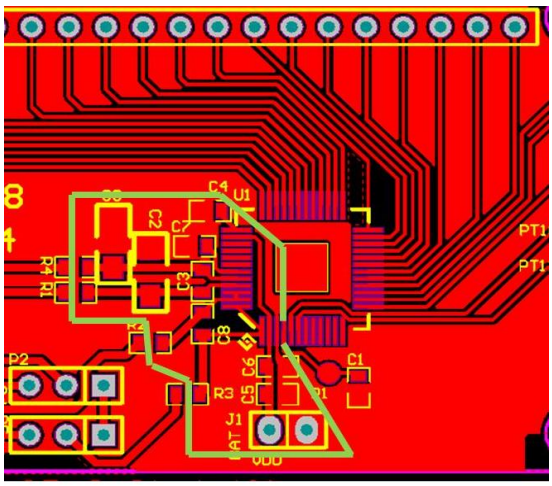


The examples of Figure 1 and Figure 2 above are similar PCBs, but the only difference is whether two resistors (R2, R3) are connected in series before the IC

Figure 1 can avoid loop antenna effect, Figure 1 is a correct demonstration

Figure 2 will have a loop antenna effect, Figure 2, it can be connected to GND from the middle of R2 and R3 resistors, but it will cause a loop antenna effect

The following figure shows a PCB with a series resistor. VSS generates a loop antenna, and the path is traced as a green line.

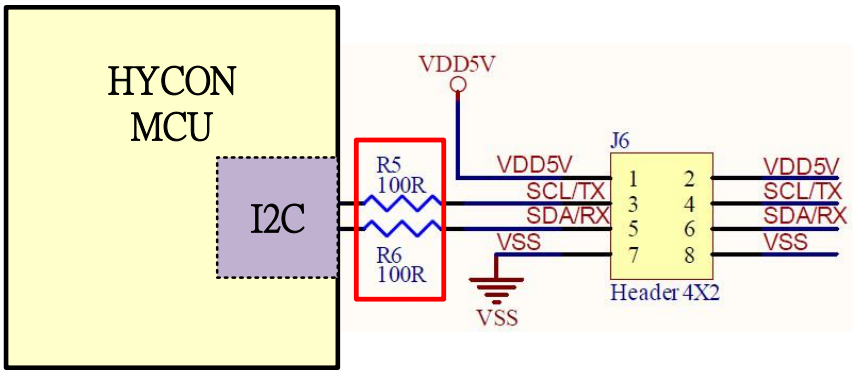


5.1.4. Precautions for ESD protection design

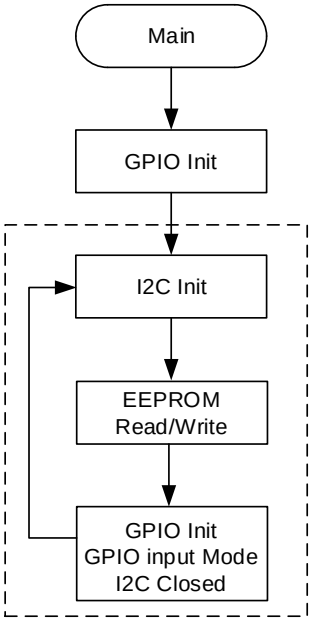
ESD protection and mechanism design are related to the PCB Layout routing method, but setting from the HY16F firmware can partially improve and strengthen the ESD capability.

1. The operating frequency of the HY16F main chip is set to HAO/2, which is better than HAO/1 in terms of anti-ESD noise.
2. For GPIO pins that are not used, it is best to set them to output low.
3. If the I2C Port is used in the application, you can start to strengthen the ESD protection from the I2C hardware and software settings

Hardware: Both SCL and SDA are connected with 100 ohm current limiting resistors (line current resistors are added near the main chip of HY16F)



Software: The I2C program is modified to close the I2C IP after each read/write to the EEPROM, and set the I/O state to GPIO Input Mode, only before each read/write to the EEPROM Redo the I2C initial action again



6. HY16F series software design precautions

This chapter provides the matters needing attention when designing software & firmware for HY16F.

6.1. Judgment of VDD3V power-on voltage stable of HY16F

In order to ensure a more stable operation of HY16F, on the software design side, it is recommended to add voltage regulation judgment to VDD3V of HY16F (ie, the first line of main), to ensure that VDD3V is stable after the operating voltage of the system (recommended VDD3V=2.75V or more), make sure VDD3V is stable before the program continues to run. The following will provide an example, using the CMP comparator of HY16F198B to do VDD3V voltage regulation judgment.

Code description: When the chip is powered on, the function VDD3V_2_75_Check() is used to determine whether VDD3V is greater than 2.75V (using the variable _timeout, the maximum waiting time for voltage regulation of VDD3V is about 8 seconds). If VDD3V is less than 2.75V, the LCD displays 0, the program while(1) is stuck. If VDD3V is greater than 2.75V, the LCD displays 1, and the program can continue to execute. The following is the code for reference:

```
int main(void)
{
   unsigned char x;
   unsigned int x_timeout=5000;
   //8S timeout
   while(x_timeout--)
   {
      x=VDD3V_2_75_Check();
      if(x==1)
      {
         x_timeout=0;
      }
   }
   if(x==0)
   {
      DisplayInit();
      ClearLCDframe();
      LCD_DATA_DISPLAY(x);    //if x=0 means failure
      while(1);
   }
   if(x==1)
   {
      DisplayInit();
      ClearLCDframe();
      LCD_DATA_DISPLAY(x);    //if x=1 means success
   }
   return 0;
}


unsigned int VDD3V_2_75_Check()
{
   unsigned char i=0;
```

```
    unsigned char j=0;
    unsigned char k=0;
    outw(0x40300,0x00002101);    //ENHAO + HAO=2M
    outw(0x41104,0x10000000);    //select precise voltage
    outw(0x40400,0x03031010);    //ENLDO
    //outw(0x41804,0x08083333);    //CMP, 0808 means VDD3V>2.4V
    outw(0x41804,0x07073333);    //CMP, 0808 means VDD3V>2.75V
    outw(0x41800,0x01010303);    //CMP
    outw(0x41808,0x01011212);    //CMP
    //Delay a while for CMP stable
    for(j=0;j<200;j++)
    {
       asm("nop");
    }
    for(j=0;j<10;j++)                    //compare 10 times
    {
       i=((inw(0x41800)&(1<<16))>>16);    //read CMPO
       if(i==0)
       {
          k++;                                //VDD3V > goal voltage
       }
       if(i==1)
       {
                                           //VDD3V < goal voltage
       }
    }
    if(k>=5) //that means VDD3V is stable >=2.4V
    {
        return 1;
    }
    else
    {
       return 0;
    }
}
```

7. Revision History

Version	Page	Date	Revision Summary
V02	All	2022/06/07	First edition