

HY-ADC ENOB Test User's Manual



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1. ENOB and Noise Free Description



RMS Noise that generated from Sigma Delta ADC is the minimum voltage value of distinguishable sampling signal. Hence, ENOB (Effective Number of Bits) is calculated by RMS Noise and Full Scale Range ratio. However, RMS Noise must be calculated by many average times. Insufficient sampling times can only represent RMS Noise for a specific period of time instead of the RMS Noise of the entire ADC operation. Therefore, RMS Noise operation times cannot be less than 1024 times.

However, Noise Free Bit represents that ADC output value count is not rolling. Noise Free Bits are stable ADC output performance. Bit operation is defined as Peak-to-Peak Noise and Full Scale Range ratio.

RMS Noise Calculation:

Average Counts
$$\Rightarrow$$
 Average $= \frac{\sum_{k=1}^{n} ADC[k]}{n}$ Equation 3
 $n = Total ADC sampling times.$
 $RMS Noise = \frac{V_{REF} \times \sqrt{\frac{\sum_{k=1}^{n} (ADC[k] - Average)^{2}}{n}}}{2^{Scale}}$ Equation 4

Scale = Total ADC Output Bits

Peak-to-Peak Noise Calculation:

Peak - to - Peak Noise =
$$\frac{V_{REF} \times (ADC_{Max} - ADC_{Min})}{2^{Scale}}$$
 Equation 5

ADCMax = Maximum ADC value of total sample ADCMin = Minimum ADC value of total sample



2. Software Description

IN Hy-ENOBIEST V1.5
Option USB Scan Read RAM ENOB Test
USB ENOB and Noise Free Test
Read
OTP Registers
Tregisters

Figure 1

2.1 Option



Figure 2



2.1.1 Setup





1. IC Selection

Choose OTP IC, OTP IC program needs to add-in SPI or Special communication program.

2. Communication Interface Selection

Only SPI or Special is selectable. The function is not supportive for other interface.

3. Optical coupler Selection

The option used when choosing optical coupler as isolator of communication interface.

2.1.2 RAM Panel

WW T										X						
-	0	1	2	3	4	5	6	7	8	9	A	в	С	D	E	F
000	02	02	02	02	02	02	06	06	02	02	-	-	-	-	-	00
010	10	00	92	-	-	-	07	ЗC	04	-	00	00	-	09	7Å	7D
020	60	00	18	4A	04	-	00	00	-	00	01	01	10	17	02	-
030	ΕO	01	01	08	02	02	00	00	-	EE	74	CF	9E	05	ΕO	6C
040	4C	СО	86	00	FF	00	00	FF	00	00	FF	FF	FF	FF	-	30
050	-	FF	DC	60	00	7Å	5B	7B	7Å	7D	10	00	00	00	83	-
060	00	00	-	-	-	-	-	-	-	-	-	-	-	99	20	00
070	DF	00	04	-	1F	ΕO	-	1F	00	00	-	-	-	-	-	-
080	95	92	8B	OA	00	10	00	03	09	05	03	00	01	03	00	00
090	00	00	00	8C	08	00	00	00	00	00	00	00	00	00	00	00
OAO	00	00	OE	OE	05	00	01	00	ЗC	00	00	00	00	06	ΕE	D2
OBO	74	ΕE	A 6	73	FF	00	AO	00	00	00	00	00	00	00	00	00
oco	00	00	00	00	01	00	00	00	00	00	00	00	AA	00	00	00
ODO	00	00	50	FD	98	74	EE	98	74	EE	99	74	ΕE	B8	74	EE
OEO	D5	74	ΕE	CF	74	ΕE	D4	74	EE	07	75	ΕE	00	04	00	00
OFO	08	00	A6	73	01	13	FF	00	F8	00	со	ЗD	95	00	95	00
В																

Figure 4

Please refer to Chapter 3.2 RAM Window Operation of HY-IDE Software User's Manual.



2.1.3 REG Panel

📷 暫存器 - 11P13 (4K) 📃 🗖 🔀									
IND0: M[010]= 10 Program Counter: 0									
[IND1: M[092]=00 Work: 00 Cycle: FE9C0000									
				n .					
	Byte								
INDFU	POINCU	PODECU	PRINCU	PLUSWU	INDFI	POINCI	PODECI	PRINCI	
02	02	02	02	02	02	06	06	02	
PLUSWI	WREG	BSR	ADCORH	ADCURM	ADCORL	TMAR	PRC	TMCR	
02	00	01	EE	74	CF	86	FF	00	
PWMR	SSPBUF	LCD0	LCD1	LCD2	LCD3	LCD4	LCDS	LCD6	
FF	00	00	7A	SB	7B	7A	7D	10	
LCD7	LCD8	LCD9							
00	00	00							
				Word					
FSRO	FSR1	TOS	PCLAT	TBLPTR	TBLD	PROD	TMBR	CCPOR	
0010	0092	073C	0000	097A	7D60	0018	FF00	FFFF	
CCP1R									
FFFF									
PAGE	E 1	PAGE2	PAG	GE3					
STKPTR	STKFL	STKUN	STKOV	-	STKPRT3	STKPRT2	STKPRT1	STKPRTO	
INTE1	GIE	ADCIE	TMCIE	TMBIE	TMAIE	WDTIE	EIIE	EOIE	
INTE2	-	-	-	-	-	SSPIE	CCPIIE	CCPOIE	
INTF1	-	ADCIF	TMCIF	TMBIF	TMAIF	WDTIF	EllF	EOIF	
INTF2	-	-	-	-	-	SSPIF	CCP1IF	CCPOIF	
STATUS	-	-	-	с	DC	N	OV	Z	
PSTAUS	PD	то	IDLEB	POR	SVS	SKERR		-	
SVSCN	ENPOR	SVSFG	SVSOP	SVSON	VLDX3	VLDX2	VLDX1	VLDX0	
SBMSET1	SKRST	NORADC	RCFTRS	RCFTR4	RCFTR3	RCFTR2	RCFTR1	RCFTRO	
PWRCN	ENVDDA	VDDAX1	VDDAX0	ENREF	-	-		-	
MCKCN1	ADCS2	ADCS1	ADCS0	ADCCK	XTHSP	XTSP	ENXT	ENRC2M	
MCKCN2	-	-	LSCK	HSCK	HSS1	HSSO	CPUCK1	CPUCKO	
MCKCN3	LCDS2	LCDS1	LCDSO	-	PERCK	BZS1	BZS1	BZSO	

Figure 5

Please refer to Chapter 3.3 Register Window Operation of HY-IDE Software User's Manual.

2.1.4 ADC Panel



Figure 6

Please refer to Chapter 3.6 ADC Window Operation of HY-IDE Software User's Manual.



2.1.5 OP Panel





Please refer to Chapter 3.7 OP Window Operation of HY-IDE Software User's Manual.

2.1.6 CMP Panel





Please refer to Chapter 3.8 Comparator Window Operation of HY-IDE Software User's Manual.

2.2 USB Scan

USB scan function help to detect whether USB scan communication port is connected to ENOB Control Board. If it is connected, the status, USB On Line, will be shown in left corner, as Figure 9



displayed.

USB On Line

Figure 9

If it is not connected, the status, USB not Connect, will be shown in left corner, as Figure 10 displayed.

USB not Connect !!!

Figure 10

PC program will scan once in every minute.

2.3 Read RAM

After USB Scan is executed, make sure USB is On Line. Then executes Read RAM, OTP Chip RAM and Registers at this moment, will be written into PC buffer. This will influence RMS Noise and Peak-to-Peak Noise operation of ENOB Test.

2.4 ENOB Test

Hana Ana	lyse <i>I</i>	ADC.																					(×
Sample	Point	1024	-	EN	IOB	Noise Fre	ee	Averag	ge Vp	o∙p Noi:	se	RM	S Noise	Catch	ADC			Save to	Cha	ang to C	Chart p	ef Volt	Avr	Times	
Sc	e	24	•							1							1	CSV	Cł	iange F	FT 1	2 V		•	
	00	T	01		02	03	04		05 /	06	/	07		08	09	04	\checkmark	OB	0C		0D	OE	OF		^
0000		A	ЬС	٦		1/	17.	_		_															
0001		Ou	tput		Dis	splay		Pe	ak-to-				Res	l time	Sav	e file	e to:		F	ET] Inp	ut Ref.			
0002		E	Bit		Nois	e Free		Ň	oise				Ca	pture	(HyA	DC.0	CSV)	/	Sv	vitch	Vol	t. Value			
0003							/	(nV)		1		and	Read					Dis	splay			-		
0004				Dist	olav	/						5	A	DC			Value	and							
0005				EN	OB	Displa	ay Al	DC		RMS	Nois	se					Ch	art			Colle		مريادر	then	1
0006			5			Sa	mple)		(n	V)						Swi	tch			avi	erage so	me o	fit	
0007	S	amol				AVE	erage	e	L	-		P					Disp	blay							1
8000	F	Point				(Co	ount)																		
0009	-																								
000A									T																
000B																									
000C									Value																
000D								1	Display	/															
000E									Block																



1. Sample Point

"Catch ADC" and "Ca.Flash" function of ADC sample point. The minimum OTP ADC sampling output amount is 256, the maximum is 1024.

2. Scale

ADC output bits. The minimum of ADC output is 8-bit, maximum is 24-bit.

3. ENOB

Display ENOB (Effective Number of Bits). The Calculation is shown as Equation 1. The unit is Bit.

4. Noise Free

Display Noise Free Bits. The Calculation is shown as Equation 2. The unit is Bit.

5. Average



Display ADC sampling average value. The Calculation is shown as Equation 3. The unit is Count.

6. Vp-p Noise

Display Peak-to-Peak Noise. The Calculation is shown as Equation 3. The unit is nV.

7. RMS Noise

Display RMS Noise. The Calculation is shown as Equation 4. The unit is nV.

8. Catch ADC

Real time catch and display ADC value in sequence in value display block.

9. Save to CSV

Save the value of display block into HyADC.CSV file, including ENOB, Noise Free, Average, Vp-p Noise and RMS Noise.

10. Change To Chart

Change to display chart and value in value display block.

11. Change FFT

Chart switch, displaying frequency domain and time domain.

12. Ref Volt

Input Reference Voltage value (unit is V).

13. Avr. Times

Select software average. Values in the value display block will be averaged based on the selected times, then to be shown in the block.



3. Hardware Description

3.1 Communication Structure





The whole structure starts from PC sending Command or Data to USB ENOB Test Board. The PC can read/write HYCON OTP SRAM Data or Flash Memory through USB ENOB Test Board.

3.2 USB ENOB Test Board Description





1. J2, J3: SPI Communication Port

J2 Description

PIN 1 \rightarrow VDDIN supplies U1power.

J3 open→HYCON OTP powered by external

J3 short→HYCON OTP powered from ENOB test Board

- PIN 2 \rightarrow ICESDI_Q, DI signal line of SPI.
- PIN 3 \rightarrow ICESCK_Q, CK signal line of SPI.
- PIN 4 \rightarrow ICESDO_Q, DO signal line of SPI.
- PIN 5 \rightarrow ICECS_Q, CS signal line of SPI.



 $\mathsf{PIN} \: 6 \to \mathsf{VSS}$

- PIN 7 → ICEIRQ_Q, signal line for detecting whether HYCON OTP writing into Flash Memory is accomplished.
- 2. J4, J5, J8 : Optical Coupler Communication Port
 - J4 Description

PIN 1 \rightarrow VP supplies power to optical coupler IC (U9~U13).

J5 & J8 open → thoroughly separate the power of optical coupler IC and HYCON OTP.

- J5 & J8 short→ optical coupler IC and HYCON OTP uses the same power
- PIN 2 \rightarrow SPIDI_Q, DI signal line of optical coupler.
- PIN 3 \rightarrow SPICK_Q, CK signal line of optical coupler.
- PIN 4 \rightarrow SPIDO_Q, DO signal line of optical coupler.
- PIN 5 \rightarrow SPICS_Q, CS signal line of optical coupler.
- PIN 6 \rightarrow VSSP, optical coupler ground.
- PIN 7 → SPIIRQ_Q, signal line (optical coupler) for detecting whether HYCON OTP writing into Flash Memory is accomplished.
- 3. J9, J10, J11 and U8

U8 is Flash Memory that capacitates 512K byte memory.

J10 and J11 is Flash Memory power source.

J10 & J11 pin1-2 short → powered by External (J5-pin1 and J8-pin2)

J10 & J11 pin2-3 short→ power is regulated from U3 (J5-pin2 and J8-pin1)

J9 Description:

PIN 1 \rightarrow VDD_X, supplying U8 power.

PIN 2 \rightarrow FLDI, controlling DI signal line of U8.

- PIN 3 \rightarrow FLCK, controlling CK signal line of U8.
- PIN 4 \rightarrow FLDO, controlling DO signal line of U8.

PIN 5 \rightarrow FLCS, controlling CS signal line of U8.

- PIN 6 \rightarrow VSS_X, U8 ground.
- 4. JP1, JP2, J6 and U3

JP1 and JP2 supplies external power to U3 in order to generate VDD power

J6 open \rightarrow using external power (5V) that inputted from JP1 and JP2.

J6 short \rightarrow using USB power.

The regulator composed by U3, R1, R2 and R3 generates VDD power. The output voltage can be amended through R1, R2 and R3. The equation is described in below:

$$VDD = 1.240V \times (1 + \frac{R1 + R2}{R3}))$$



4. Revision History

Major differences are stated thereinafter:

Version	Page	Revision Summary
V01	ALL	First edition
V02	9	Delete 2.5 Switch test information.
	ALL	Update all the figures