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**HY11P41**  
**Datasheet**  
**8-Bit RISC-like Mixed Signal Microcontroller**  
**Embedded 18-Bit  $\Sigma\Delta$ ADC**

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## 1. Features

- 8-bit RISC, 66 instructions included.
- Operating voltage range: 2.2V to 3.6V, operation temperature range:  $-40^{\circ}\text{C}\sim 85^{\circ}\text{C}$ .
- External Crystal Oscillator and Internal High Precision RC Oscillator, 6 CPU clock rates enable users to have the most power-saving plan.
  - Active Mode 300uA@2MHz
  - Standby Mode 3uA@28KHz
  - Sleep Mode 1uA
- 2K Word OTP (One Time Programmable) Type program memory, 128 Byte Data Memory.
- Brownout detector and Watch dog Timer, prevents CPU from Crash.
- 18-bit fully differential input Sigma-Delta Analog-to-Digital Converter (A/D)
  - Built-in PGA (Programmable Gain Amplifier) 1/4x · 1/2x · 1x. ... 128x · 10 input signal gain selection.
  - Built-in Input zero point adjustment can increase measurement range according to different application.
  - Programmable data output rate: 8SPS~2K SPS
- Built-in absolute temperature sensor
- 1.0V and 1.2V internal analog circuit common ground that equips with Push-Pull drive ability to provide sensor driving voltage.
- LVD low voltage detection function has 14 steps of voltage detection configuration and external input voltage detection function.
- VDDA can select 4 different output voltages that equips with 10mA low dropout regulator and fast start function.
- 8-bit Timer A
- 16-bit Timer B module equips with Capture function
- 8-bit Timer C module can generate PWM/PFD waveform.
- Built-in EPROM (BIE)
- Support 6 stack level

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## 2. Pin Definition

### 2.1 SSOP16 Pin Diagram

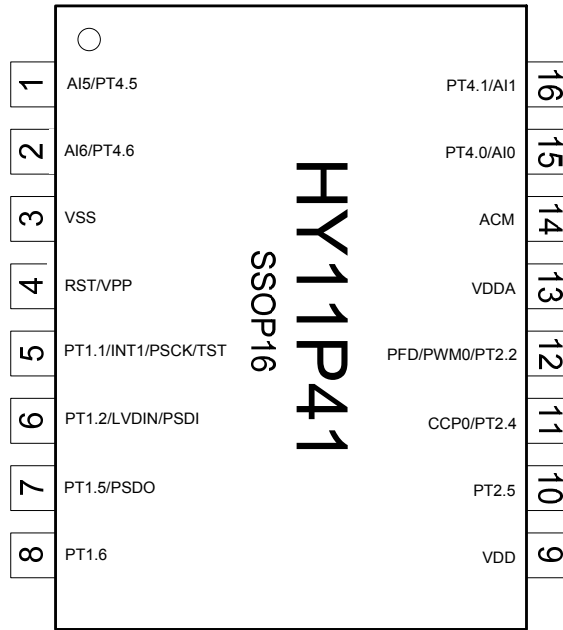


Figure 2-1 HY11P41 SSOP16 Pin Diagram

### 2.2 SOP16 Pin Diagram

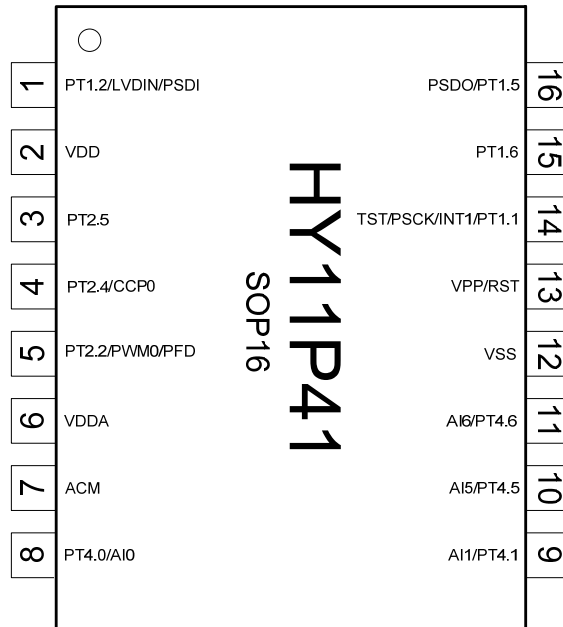


Figure 2-2 HY11P41 SOP16 Pin Diagram

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## 2.3 QFN16 Pin Diagram

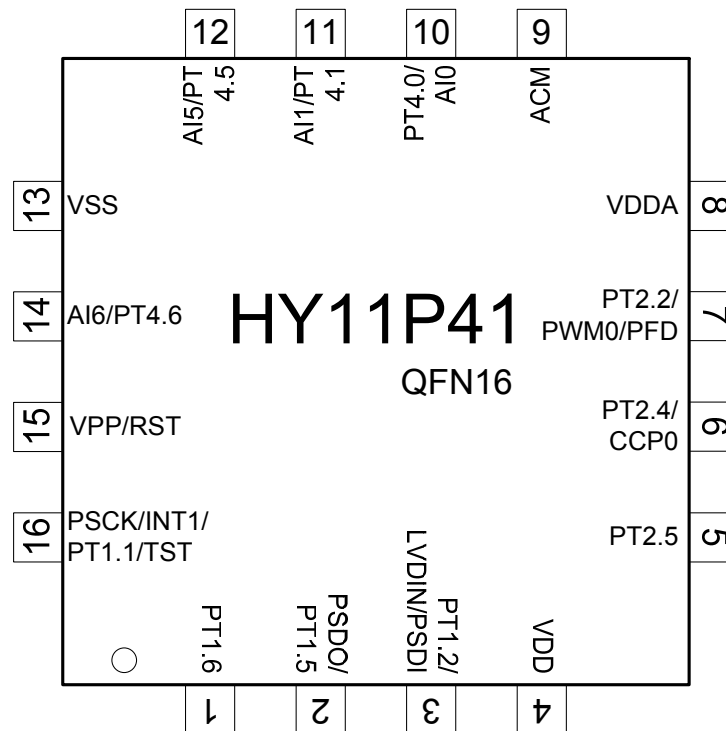


Figure 2-3 HY11P41 QFN16 Pin Diagram

Note 1 : VPP and RST use the same pin. Input voltage cannot exceed 5.8V when not programming EPROM.

Note 2 : TST and PT1.1 use the same pin. Input voltage cannot exceed VDD+0.3V while operating.

Note 3 : If PT1.1 is not configured as external button pin, the anti-interference ability will be enhanced.

## 2.4 SSOP16 Pinout I/O Description

"I/O" input/output, "I" input, "O" output, "S" Smith Trigger, "C" CMOS features compatible input/output, "P" power supply, "A" analog channel

No.	Pin Name	Pin Characteristics		Function Description	
		Pin Type	Buffer Type		
1	A15/PT4.5	A15	A	Analog input channel	
		PT4.5	I	Digital input	
2	A16/PT4.6	A16	A	Analog input channel	
		PT4.6	I	Digital input	
3	VSS		P	Ground pin for IC operation voltage	
4	RST/VPP	RST	I	Reset the chip	
		VPP	P	EPROM read/write power source	
5	PT1.1/INT1/PSCK/TST				
	PT1.1		I	Digital input	
	INT1		I	Interrupt source, INT1	
	PSCK		I	PSCK port of OTP read/write	
	TST		I	Test mode enable input (invalid)	
6	PT1.2/LVDIN/PSDI				
		PT1.2	I	Digital input	
		LVDIN	A	LVD external signal input port	
	PSDI	I	S	PSDI port of OTP read/write	
7	PT1.5/PSDO				
		PT1.5	I/O	S	Digital input/output
		PSDO	I/O	C	PSDO port of OTP read/write
8	PT1.6				
		PT1.6	I/O	S	Digital input/output
9	VDD		P	Chip operation power source	
10	PT2.5				
		PT2.5	I/O	S	Digital input/output
11	PT2.4/CCP0				
		PT2.4	I/O	S	Digital input/output
		CCP0	I	S	Capture mode signal port
12	PT2.2/PWM0/PFD				
		PT2.2	I/O	C	Digital input/output



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		PWM0	O	C	PWM output port
		PFD	O	C	PFD output port
13	VDDA		P	P	Regulator output Analog circuit voltage source
14	ACM		P	P	Internal analog circuit grounding pin
15	A10/PT4.0	A10	A	A	Analog input channel
		PT4.0	I	C	Digital input
16	A11/PT4.1	A11	A	A	Analog input channel
		PT4.1	I	C	Digital input

Table 2-1 Pin Definition and Function Description

## 2.5 SOP16 Pinout I/O Description

"I/O" input/output, "I" input, "O" output, "S" Smith Trigger, "C" CMOS features compatible input/output, "P" power supply, "A" analog channel

No.	Pin Name	Pin Characteristics		Function Description
		Pin Type	Buffer Type	
1	PT1.2/LVDIN/PSDI			
	PT1.2	I	S	Digital input
	LVDIN	A	A	LVD external signal input port
	PSDI	I	S	PSDI port of OTP read/write
2	VDD	P	P	Chip operation power source
3	PT2.5			
	PT2.5	I/O	S	Digital input/output
4	PT2.4/CCP0			
	PT2.4	I/O	S	Digital input/output
	CCP0	I	S	Capture mode signal port
5	PT2.2/PWM0/PFD			
	PT2.2	I/O	C	Digital input/output
	PWM0	O	C	PWM output port
	PFD	O	C	PFD output port
6	VDDA	P	P	Regulator output Analog circuit voltage source
7	ACM	P	P	Internal analog circuit grounding pin
8	AI0/PT4.0			
	AI0	A	A	Analog input channel
	PT4.0	I	C	Digital input
9	AI1/PT4.1			
	AI1	A	A	Analog input channel
	PT4.1	I	C	Digital input
10	AI5/PT4.5			
	AI5	A	A	Analog input channel
	PT4.5	I	C	Digital input
11	AI6/PT4.6			
	AI6	A	A	Analog input channel
	PT4.6	I	C	Digital input
12	VSS	P	P	Chip operation power source grounding pin

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13	RST/VPP	RST VPP	I P	S P	Reset the chip EPROM read/write power source
14	PT1.1/INT1/PSCK/TST	PT1.1 INT1 PSCK TST	I I I I	S S S S	Digital input Interrupt source, INT1 PSCK port of OTP read/write Test mode enable input (invalid)
15	PT1.6	PT1.6	I/O	S	Digital input/output
16	PT1.5/PSDO	PT1.5 PSDO	I/O I/O	S C	Digital input/output PSDO port of OTP read/write

Table 2-2 Pin Definition and Function Description

## 2.6 QFN16 Pinout I/O Description

"I/O" input/output, "I" input, "O" output, "S" Smith Trigger, "C" CMOS features compatible input/output, "P" power supply, "A" analog channel

No.	Pin Name	Pin Characteristics		Function Description	
		Pin Type	Buffer Type		
1	PT1.6	PT1.6	I/O	S	Digital input/output
2	PT1.5/PSDO	PT1.5	I/O	S	Digital input/output
		PSDO	I/O	C	PSDO port of OTP read/write
3	PT1.2/LVDIN/PSDI	PT1.2	I	S	Digital input
		LVDIN	A	A	LVD external signal input port
		PSDI	I	S	PSDI port of OTP read/write
4	VDD		P	P	Chip operation power source
5	PT2.5	PT2.5	I/O	S	Digital input/output
6	PT2.4/CCP0	PT2.4	I/O	S	Digital input/output
		CCP0	I	S	Capture mode signal port
7	PT2.2/PWM0/PFD	PT2.2	I/O	C	Digital input/output
		PWM0	O	C	PWM output port
		PFD	O	C	PFD output port
8	VDDA		P	P	Regulator output Analog circuit voltage source
9	ACM		P	P	Internal analog circuit grounding pin
10	AI0/PT4.0	AI0	A	A	Analog input channel
		PT4.0	I	C	Digital input
11	AI1/PT4.1	AI1	A	A	Analog input channel
		PT4.1	I	C	Digital input
12	AI5/PT4.5	AI5	A	A	Analog input channel
		PT4.5	I	C	Digital input

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13	VSS		P	P	Chip operation power source grounding pin
14	A16/PT4.6	A16 PT4.6	A I	A C	Analog input channel Digital input
15	RST/VPP	RST VPP	I P	S P	Reset the chip EPROM read/write power source
16	PT1.1/INT1/PSCK/TST	PT1.1 INT1 PSCK TST	I I I I	S S S S	Digital input Interrupt source, INT1 PSCK port of OTP read/write Test mode enable input (invalid)

Table 2-3 Pin Definition and Function Description

### 3. Application Circuit

#### 3.1 Bridge Sensor I

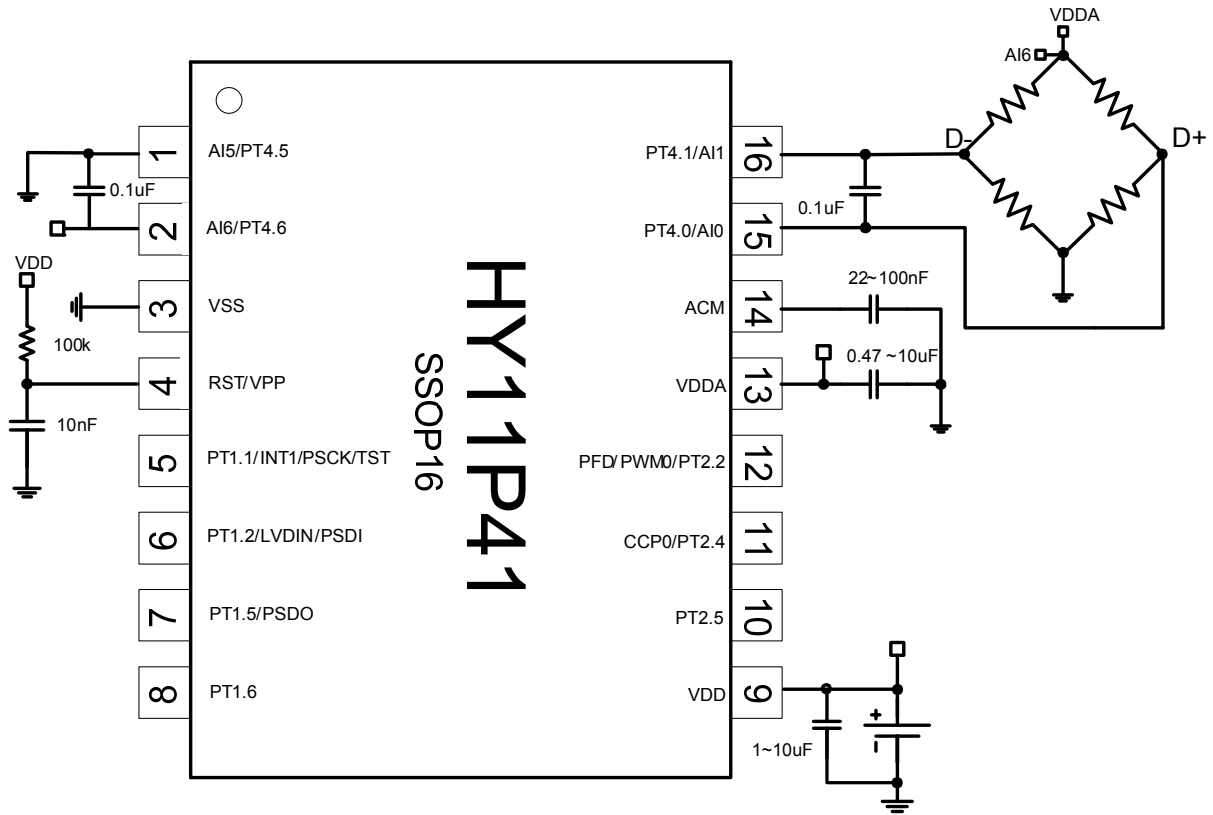


Figure 3-1 Application Circuit for Bridge Sensors

Note 1: DCSET[2:0] can conduct bias adjustment of Load Cell zero point voltage address

Note 2: BIE function can be used to save calibration parameters.

**3.2 Bridge Sensor II**

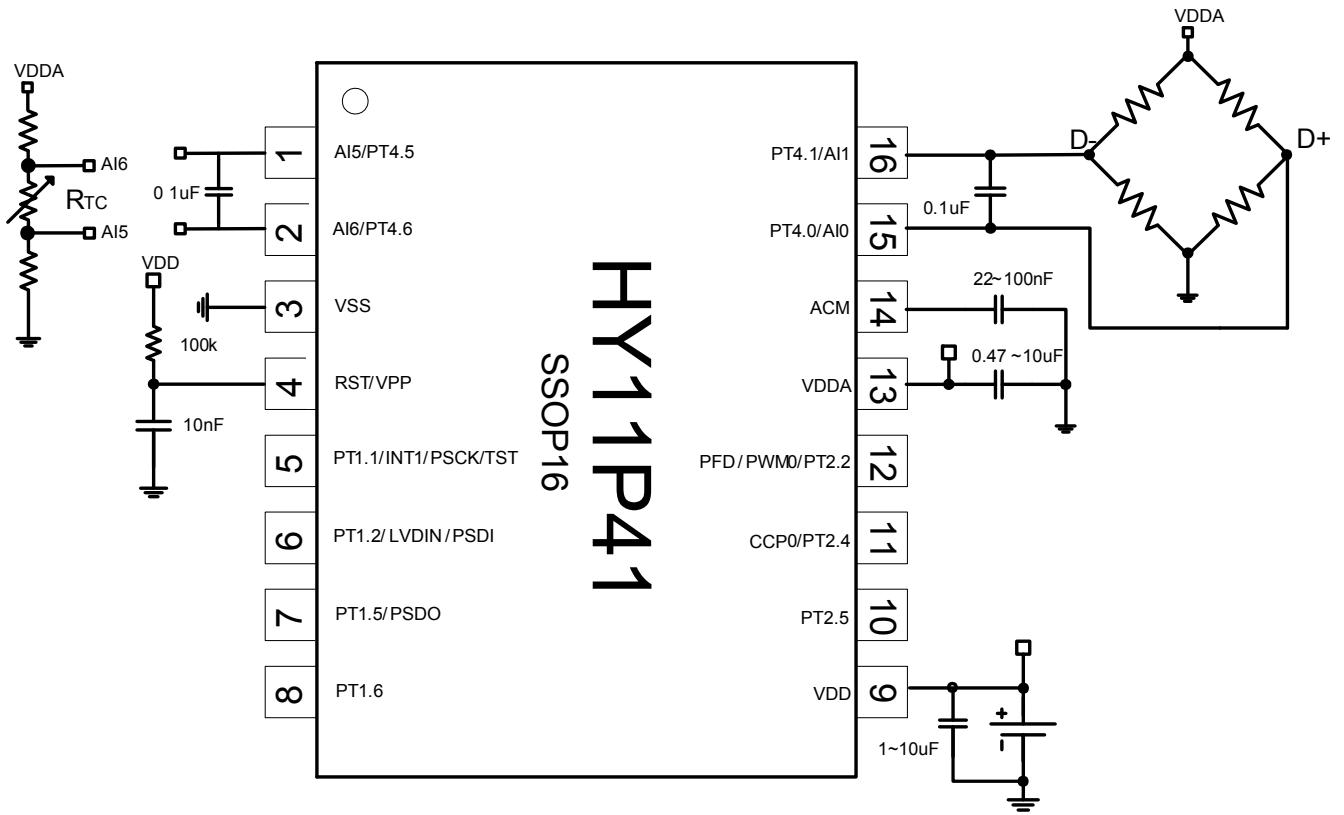


Figure 3-2 Application Circuit of Temperature Compensation Bridge Sensor

Note 1: Using external reference voltage to design temperature compensation resistor NTC basic circuit

Note 2: DCSET[2:0] can conduct bias adjustment of Load Cell zero point voltage address

Note 3: BIE function can be used to save calibration parameters.

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## 3.3 4-20mA Two-Wire Current Panel Meter

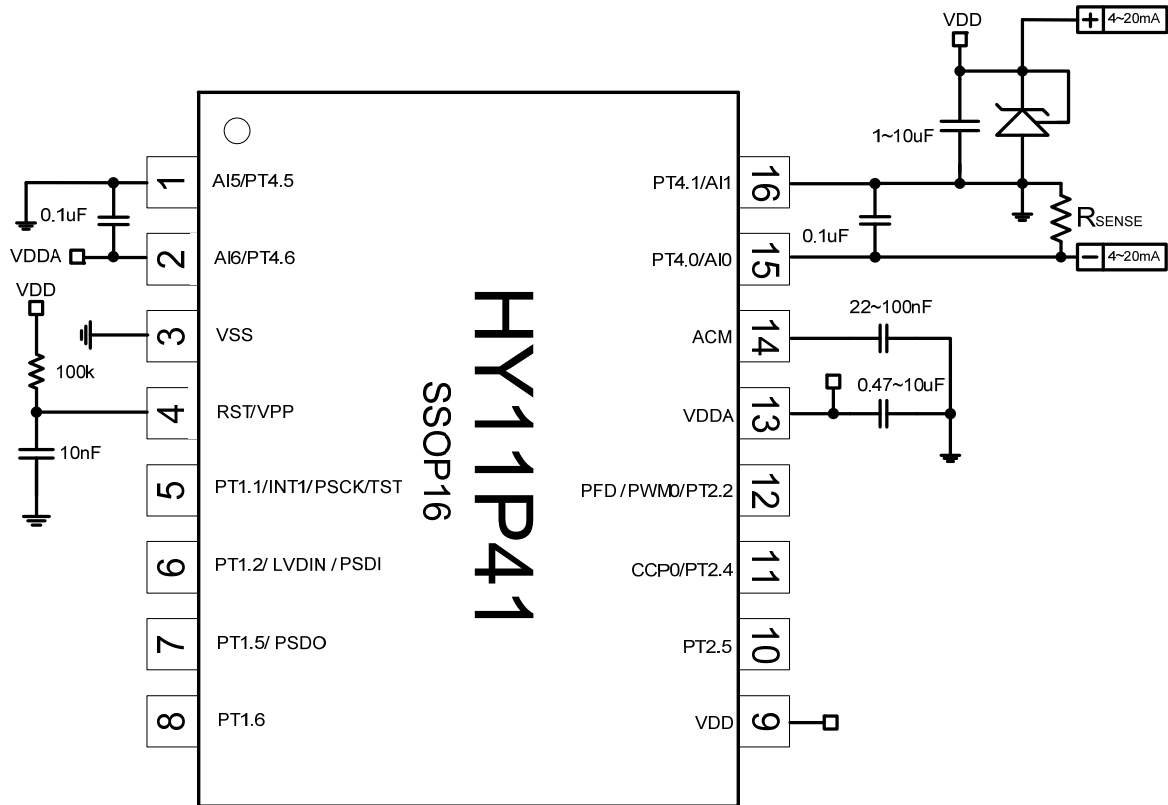


Figure 3-3 4-20mA Panel Meter that Unneeded to Connect External Power Supply

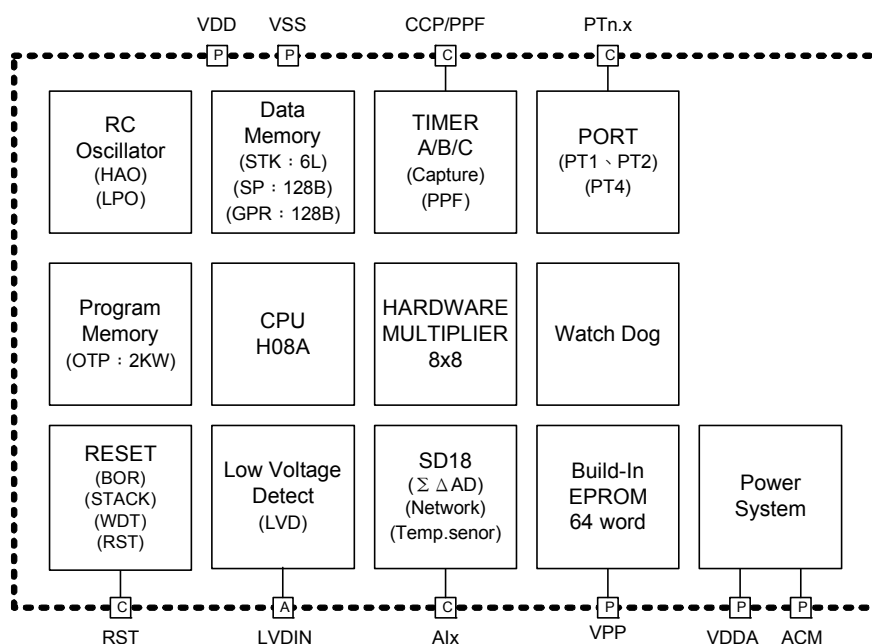
Note 1: DCSET[2:0] can carry out bias adjustment of Load Cell zero point voltage address

Note 2: BIE function can be used to save calibration parameters.



## 4. Function Outline

### 4.1 Internal Block Diagram



P Power Pad  
 D Digital Pad  
 A Analog Pad  
 C Common I/O Pad

Figure 4-1 HY11P41 Internal Block Diagram

### 4.2 Related Description and Supporting Documents

#### IC Function Related Operating Instruction

DS-HY11P41	HY11P41 Data Sheet
UG-HY11S14	HY11P Series Users' Manual
APD-CORE002-Vxx	H08A Instruction Description

#### Development Tool Related Operating Instruction

APD-HYIDE006-Vxx	HY11xxx Series Development Tool Software Instruction Manual
APD-HYIDE005-Vxx	HY11xxx Series Development Tool Hardware Instruction Manual
APD-OTP001-Vxx	OTP Products Programming Pin Manual Product

#### Production Related Operating Instruction

APD-HYIDE004-Vxx	HY1xxxx Series Production Line Specialized Programmer Manual
BDI-HY11P41-Vxx	HY11P41 Individual Product Die Bonding Information

**4.3 SD18 Network**

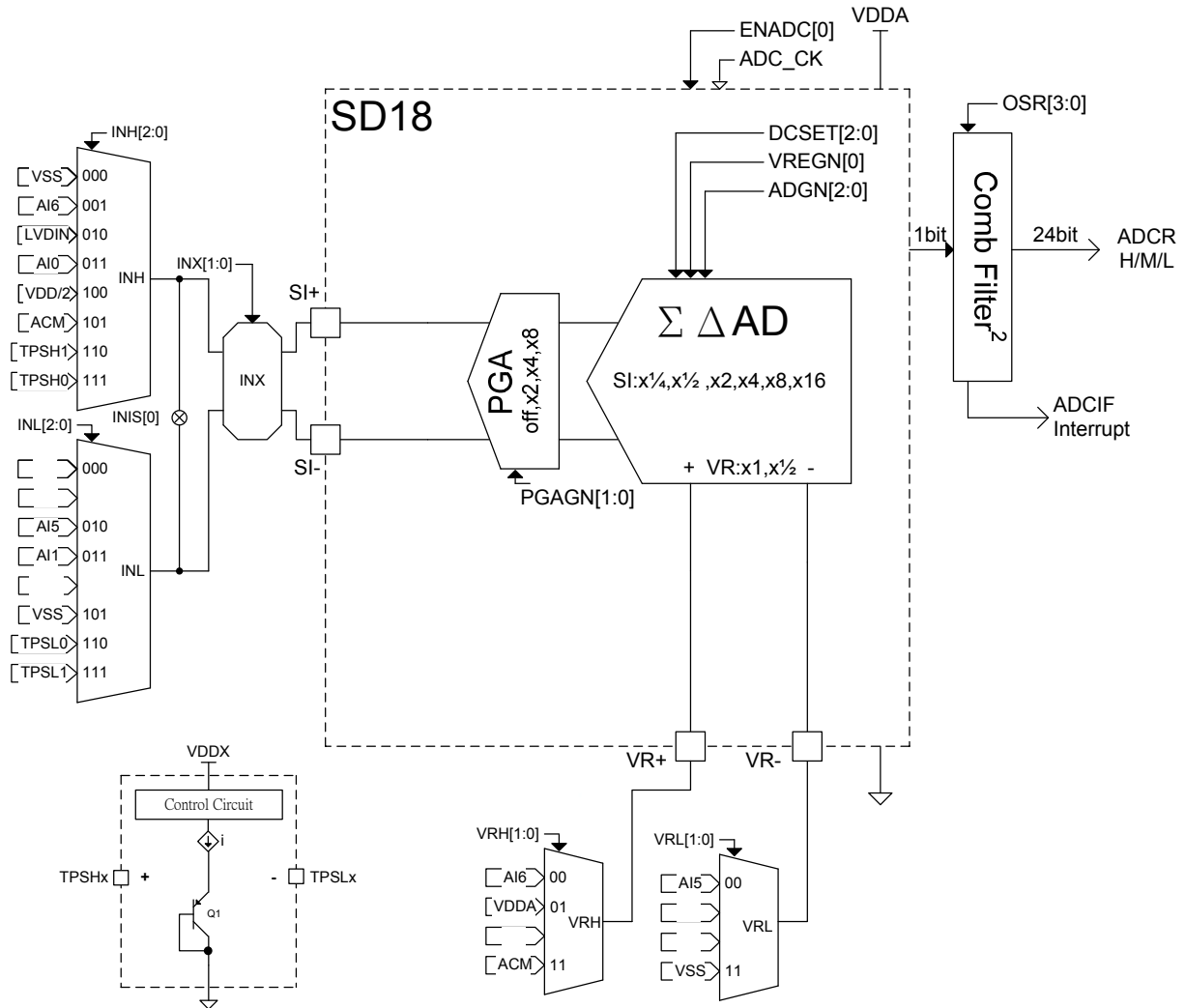


Figure 4-2 SD18 Network

Note: If ADC reference voltage end used AI6-AI5 network to connect external VDDA-VSS power, higher stability would be achieved.

Note: When using development kit (HY11S14-DK02) for emulation, users need to connect AI8 analog network to VDDA power in order to achieve VRH input as VDDA power source under VRH[1:0]=01b configuration. Connecting AI2 analog network to VSS power to achieve INH input as VSS power source under INH[2:0]=000b configuration. Connecting AI4 analog network to PT1.2 pin (LVDIN) to achieve INH input as LVDIN input source under INH[2:0]=010b configuration.

Note: Users can connect HY11P41 AD Net Board (PCB No.: T10009-2) to Analog Port: JP3 of development kit (HY11S14-DK02) as to accomplish power configuration of AI8 and AI2 analog network.

### 5. Register List

“-”no use, “r”read/write, “w”write, “r”read, “r0”only read 0, “r1”only read 1, “w0”only write 0, “w1”only write 1													
“-”unimplemented bit, “x”unknown, “u”unchanged, “d”depends on condition													
Address	File Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A-RESET	I-RESET	R/W	
00H	INDF0	Contents of FSR0 to address data memory value of FSR0 not changed								N/A	N/A	*****	
01H	POINC0	Contents of FSR0 to address data memory value of FSR0 post-incremented								N/A	N/A	*****	
02H	PODEC0	Contents of FSR0 to address data memory value of FSR0 post-decremented								N/A	N/A	*****	
03H	PRINC0	Contents of FSR0 to address data memory value of FSR0 pre-incremented								N/A	N/A	*****	
04H	PLUSW0	Contents of FSR0 to address data memory value of FSR0 offset by W								N/A	N/A	*****	
05H	INDF1	Contents of FSR1 to address data memory value of FSR0 not changed								N/A	N/A	*****	
06H	POINC1	Contents of FSR1 to address data memory value of FSR0 post-incremented								N/A	N/A	*****	
07H	PODEC1	Contents of FSR1 to address data memory value of FSR0 post-decremented								N/A	N/A	*****	
08H	PRINC1	Contents of FSR1 to address data memory value of FSR0 pre-incremented								N/A	N/A	*****	
09H	PLUSW1	Contents of FSR1 to address data memory value of FSR0 offset by W								N/A	N/A	*****	
0FH	FSR0H	FSR0[8]								....x	....u	*****	
10H	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*****	
11H	FSR1H	FSR1[8]								....x	....u	*****	
12H	FSR1L	Indirect Data Memory Address Pointer 1 Low Byte,FSR1[7:0]								xxxx xxxx	uuuu uuuu	*****	
16H	TOSH	TOS[10] TOS[9] TOS[8]								....000	....000	*****	
17H	TOSL	Top-of-Stack Low Byte (TOS<7:0>)								0000 0000	0000 0000	*****	
18H	STKPTR	STKFL	STKUN	STKOV	STKPR[2:0]				000.000	000.000	r,rw0,rw0,-,r,r,r		
1AH	PCLATH	PC[10] PC[9] PC[8]								....000	....000	*****	
1BH	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	*****	
1DH	TBLPTRH	TBLPTR[10] TBLPTR[9] TBLPTR[8]								....000	....000	*****	
1EH	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								0000 0000	0000 0000	*****	
1FH	TBLDH	Program Memory Table Latch High Byte								0000 0000	0000 0000	*****	
20H	TBLDL	Program Memory Table Latch Low Byte								0000 0000	0000 0000	*****	
21H	PRODH	Product Register of Multiply High Byte								xxxx xxxx	uuuu uuuu	r,r,r,r,r,r,r,r	
22H	PRODL	Product Register of Multiply Low Byte								xxxx xxxx	uuuu uuuu	r,r,r,r,r,r,r,r	
23H	INTE1	GIE	ADCFIE	TMCIE	TMBIE	TMAIE	WDTIE	E1IE	CCP0IE		0000 000.	000.000.	*****
24H	INTE2	CCP0IF								....0	....0	*****	
26H	INTF1	ADCFIF	TMCIF	TMBIF	TMAIF	WDTIF	E1IF	CCP0IF		.000 000.	.00.000.	*****	
27H	INTF2	CCP0IF								....0	....0	*****	
29H	WREG	Working Register								xxxx xxxx	uuuu uuuu	*****	
2AH	BSRCN	BSR[0]								....0	....0	*****	
2BH	STATUS	C DC N OV Z								...x xxxx	...u uuuu	*****	
2CH	PSTATUS	PD	TO	IDLEB	BOR	SKERR		uduu .d.		000d .0.	uduu .d.	rw0,rw0,rw0,rw0,-,rw0,-	
2DH	LVDCN	LVDFG	LVD	LVDON	VLDX[3:0]			.000 0000		.000 uuuu	*****		
30H	PWRCN	ENVDDA	VDDAX[1:0]	ENACM	ENHAO		0000 ....		0000 ....	*****			
31H	MCKCN1	ADCS[2:0]		ADCK	HSS[1:0]		CPUCK[1:0]	0000 ...1	0000 ...1	*****			
32H	MCKCN2	PERCK								....0000	....0000	*****	
33H	MCKCN3	0...								....0...	....0...	*****	
39H	ADCRH	ADC conversion memory HighByte								xxxx xxxx	uuuu uuuu	r,r,r,r,r,r,r,r	
3AH	ADCRM	ADC conversion memory Middle Byte								xxxx xxxx	uuuu uuuu	r,r,r,r,r,r,r,r	
3BH	ADCRL	ADC conversion memory Low Byte								xxxx xxxx	uuuu uuuu	r,r,r,r,r,r,r,r	
3CH	ADCCN1	ENADC	ENHIGN	ENCHP	PGAGN[1:0]	ADGN[2:0]		0000 0000		0000 0000	*****		
3DH	ADCCN2	VREGN DCSET[2:0]								....0000	....0000	*****	
3EH	ADCCN3	OSR[2:0] OSR[3]								000. ...0.	000. ...0.	*****	
3FH	AINET1	INH[2:0]		INL[2:0]		INIS		0000 000.		0000 000.	*****		
40H	AINET2	VRH[1:0]		INX[1:0]		VRL[1:0]		.000 000.		.000 000.	*****		
41H	TMACN	ENTMA	TMACK	TMAS[1:0]	ENWDT	WDTSS[2:0]		0000 0000		0000 0000	***** w1,***		
42H	TMAR	TimerA data register								xxxx xxxx	uuuu uuuu	r,r,r,r,r,r,r,r	
43H	TMBCN	ENTMB	TMBCK	TMBS[1:0]	TMBSYC	TMBR2R		0000 00.		0000 00.	*****		
44H	TMBRH	TimerB High Byte data register								xxxx xxxx	uuuu uuuu	*****	
45H	TMBRL	TimerB Low Byte data register								xxxx xxxx	uuuu uuuu	*****	
46H	TMCCN	ENTMC	TMCK[1:0]	TMCS1[2:0]		TMCS0[1:0]		0000 0000		0000 0000	*****		
47H	PRC	TimerC programmable register								1111 1111	1111 1111	*****	
48H	TMCR	TimerC register								0000 0000	0000 0000	r,r,r,r,r,r,r,r	
49H	CCPCN	CCP0M[3:0]								....0000	....0000	*****	
4AH	CCP0RH	CCP0 High Byte data register								xxxx xxxx	uuuu uuuu	*****	
4BH	CCP0RL	CCP0 Low Byte data register								xxxx xxxx	uuuu uuuu	*****	
4FH	PWMCN	ENPWM	ENPFD	PWMRL[1:0]		0000 ....		0000 ....		0000 ....	*****		
51H	PWMR	PWM MSB Byte register								xxxx xxxx	uuuu uuuu	*****	
6AH	PT4	PT4.6		PT4.5		PT4.1		PT4.0		.xx .xx	.uu .uu	-r,r,-,r,r,-	
6BH	PT4DA	DA4.6		DA4.5		DA4.1		DA4.0		.11 .11	.11 .11	*****	
6CH	PT4PU	PU4.6		PU4.5		PU4.1		PU4.0		.00 .00	.00 .00	*****	
6DH	PT1	PT1.6		PT1.5		PT1.2		PT1.1		.xx .xx	.uu .uu	-r,r,-,r,r,-	
6EH	TRISC1	TC1.6		TC1.5		DA1.2		PU1.2		.00 .00	.00 .00	*****	
6FH	PT1DA	PU1.6 PU1.5								....0.	....0.	*****	
70H	PT1PU	PU1.6 PU1.5								.00 .00.	.00 .00.	*****	
71H	PT1M1	INTEG1[1:0]								....00.	....00.	*****	
72H	PT1M2	PM1.6[0] PM1.5[0]								...0 .0.	...0 .0.	*****	
74H	PT2	PT2.5		PT2.4		PT2.2		PT2.1		.xx .x.	.uu .uu	*****	
75H	TRISC2	TC2.5		TC2.4		TC2.2		TC2.1		.00 .0.	.00 .0.	*****	
77H	PT2PU	PU2.5 PU2.4 PU2.2								.00 .0.	.00 .0.	*****	
78H	PT2M1	PM2.2[1]		PM2.2[0]		PM2.2[0]		PM2.2[0]		.00 ....	.00 ....	*****	
80H ~ FFH	GPR0	General Purpose Register as 128Byte								xxxx xxxx	uuuu uuuu	*****	
195H	BICTRL	VPP_HIGH BIEWR BIERD								1000 d000	1000 d000	***** r0,***	
196H	BIEPTRH	w0,w0,W0,W0 W0,W0,W0,W0								0000 0000	0000 0000	*****	
197H	BIEPTRL	0	0	BIE_ADDR[5:0]				0000 0000		0000 0000	w0,w0,*****		
198H	BIEDH	BIE_DATA[15:8]								xxxx xxxx	xxxx xxxx	*****	
199H	BIEDL	BIE_DATA[7:0]								xxxx xxxx	xxxx xxxx	*****	

Table 5-1 HY11P41 Register List

## 6. Electrical Characteristics

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at $V_{DD}$ to $V_{SS}$	-0.2 V to 4.0 V
Voltage applied to any pin	-0.2 V to $V_{DD} + 0.3$ V
Voltage applied to RST/VPP pin	-0.2 V to 6.9 V
Voltage applied to TST/PT1.1 pin	-0.2 V to $V_{DD} + 1$ V
Diode current at any device terminal	$\pm 2$ mA
Storage temperature, Tstg: (unprogrammed device)	-55°C to 150°C
(programmed device)	-40°C to 85°C
Total power dissipation	0.5w
Maximum output current sink by any PORT1 to PORT2 I/O pin	.25mA

### 6.1 Recommended Operating Conditions

$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$ , unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
$V_{DD}$	Supply Voltage	All digital peripherals and CPU	2.2		3.6	V
		Analog peripherals	2.4		3.6	
$V_{SS}$	Supply Voltage		0		0	

## 6.2 Internal RC Oscillator

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}$ , unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1	1.8	2.0	2.2	MHz
LPO	Low Power Oscillator frequency	$V_{DD}$ supply voltage be enable LPO	22	28	35	KHz

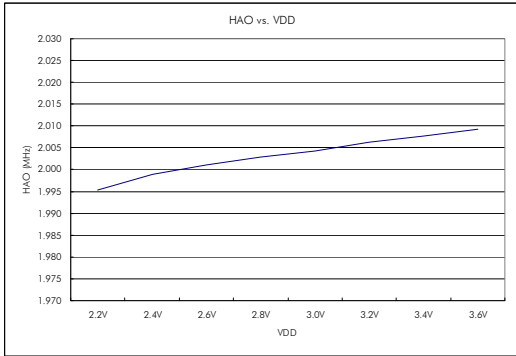


Figure 6.2-1 HAO vs. VDD

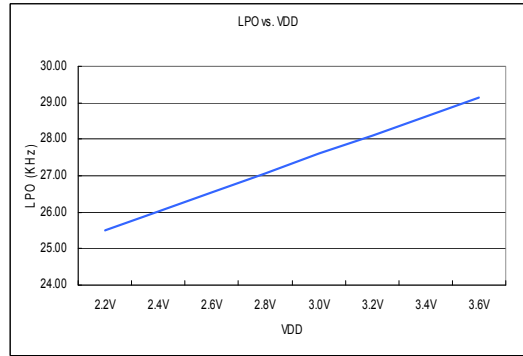


Figure 6.2-2 LPO vs. VDD

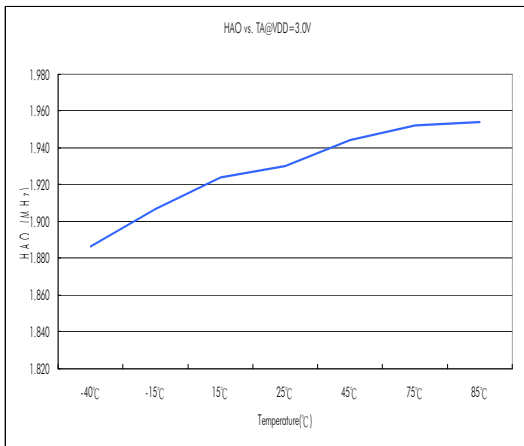


Figure 6.2-3 HAO vs. Temperature

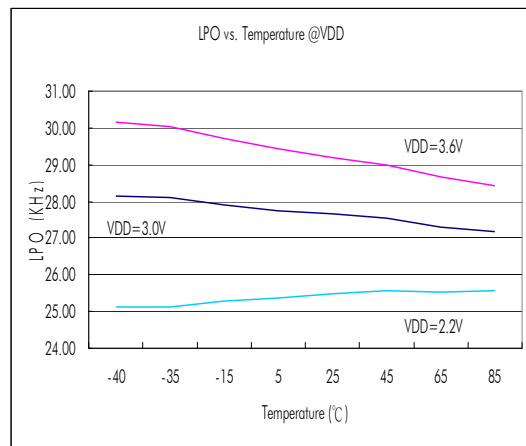


Figure 6.2-4 LPO vs. Temperature

### 6.3 Supply Current into VDD Excluding Peripherals Current

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, \text{OSC\_LPO} = 28\text{KHz}$ , unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
$I_{AM2}$	Active mode 2	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 2MHz		0.32	0.55	mA
$I_{AM3}$	Active mode 3	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 1MHz		0.18	0.3	mA
$I_{LP2}$	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		1.65	3	$\mu\text{A}$
$I_{LP3}$	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.65	1.2	$\mu\text{A}$

OSC\_HAO : Internal High Accuracy Oscillator frequency.

CPU\_CK : CPU core work frequency.

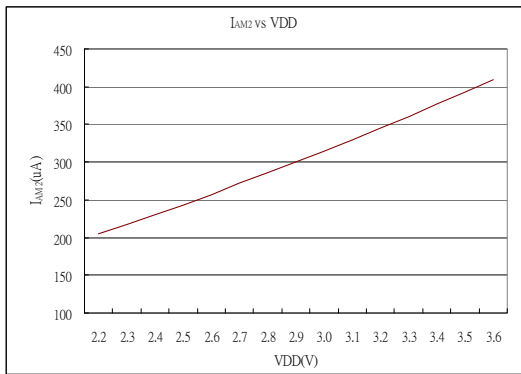


Figure 6.3-1  $I_{AM2}$  vs. VDD

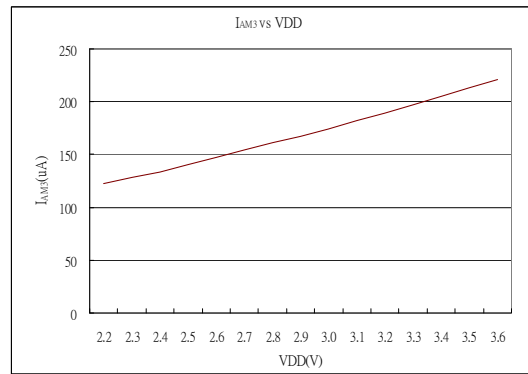


Figure 6.3-2  $I_{AM3}$  vs. VDD

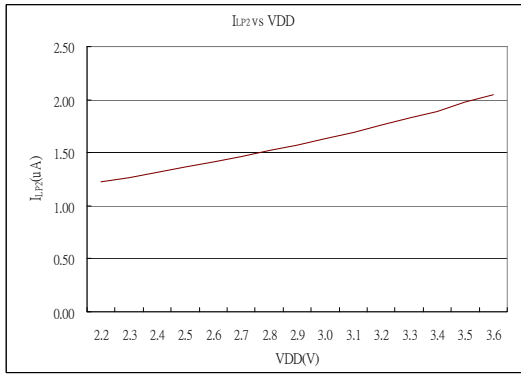


Figure 6.3-3  $I_{LP2}$  vs. VDD

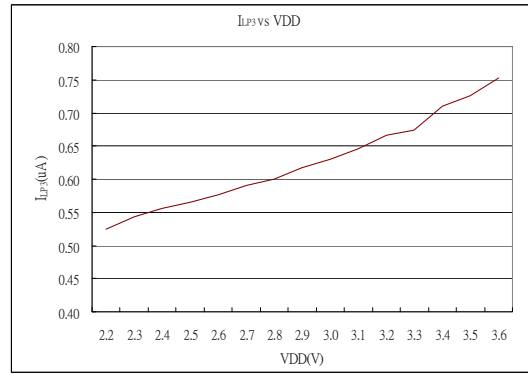


Figure 6.3-4  $I_{LP3}$  vs. VDD

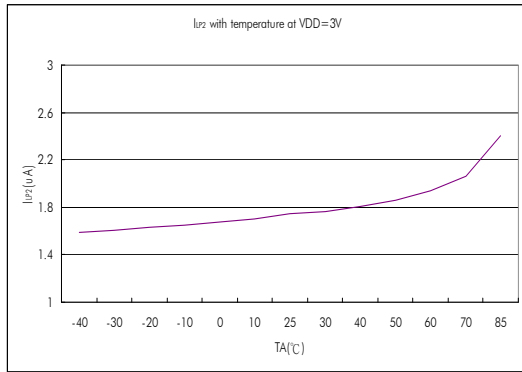


Figure 6.3-5  $I_{LP2}$  vs. Temperature

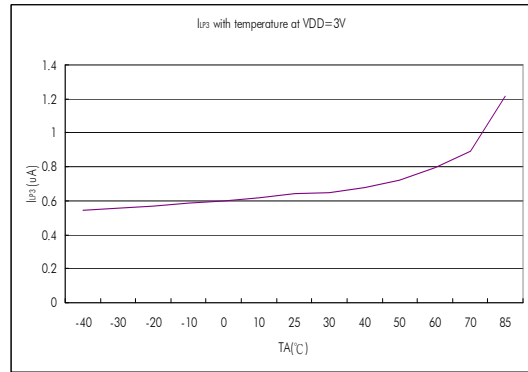


Figure 6.3-6  $I_{LP3}$  vs. Temperature

## 6.4 Port1~4

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}$ , unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
<b>Input voltage and Schmitt trigger and leakage current and timing</b>						
$V_{IH}$	High-Level input voltage		$0.7 \cdot V_{DD}$		$V_{DD}$	V
$V_{IL}$	Low-Level input voltage		VSS		$0.3 \cdot V_{DD}$	
$V_{hys}$	Input Voltage hysteresis( $V_{IH} - V_{IL}$ )			0.8		V
$I_{LKG}$	Leakage Current				0.1	$\mu\text{A}$
$R_{PU}$	Port pull high resistance			180		$\text{k}\Omega$
<b>Output voltage and current and frequency</b>						
$V_{OH}$	High-level output voltage	$I_{OH} = 10\text{mA}$	$V_{DD} - 0.3$			V
$V_{OL}$	Low-level output voltage	$I_{OL} = -10\text{mA}$			$V_{SS} + 0.3$	

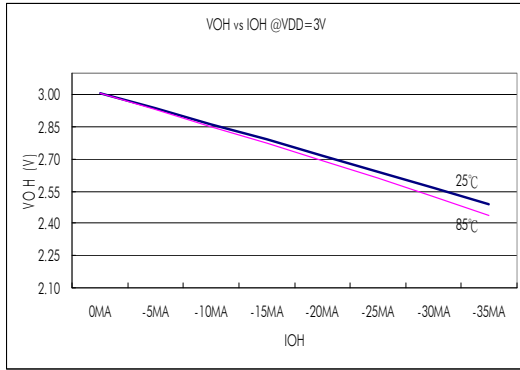


Figure 6.4-1  $V_{OH}$  vs.  $I_{OH}$  @  $V_{DD} = 3.0\text{V}$

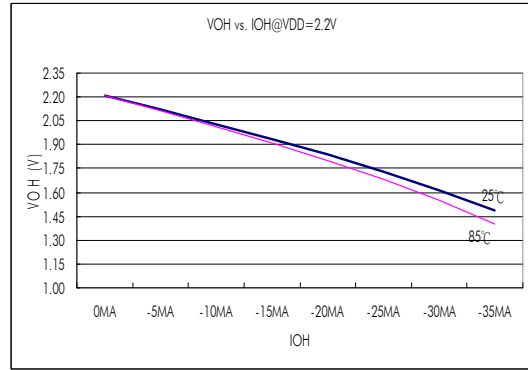


Figure 6.4-2  $V_{OH}$  vs.  $I_{OH}$  @  $V_{DD} = 2.2\text{V}$

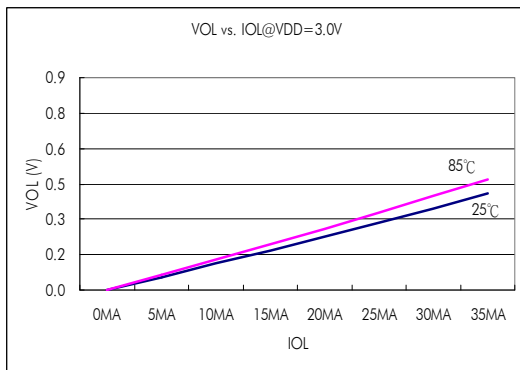


Figure 6.4-3  $V_{OL}$  vs.  $I_{OL}$  @  $V_{DD} = 3.0\text{V}$

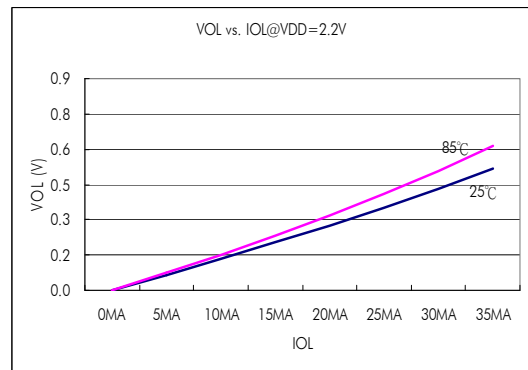


Figure 6.4-4  $V_{OL}$  vs.  $I_{OL}$  @  $V_{DD} = 2.2\text{V}$



### 6.5 Reset (Brownout, External RST Pin, Low Voltage Detect)

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}$ , unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit	
BOR	Pulse length needed to accepted reset internally, $t_{d-LVR}$		2			us	
	$V_{DD}$ Start Voltage to accepted reset internally (L $\rightarrow$ H), $V_{LVR}$		1.6	1.85	2.1	V	
	Hysteresis, $V_{HYS-LVR}$			70		mV	
RST	Pulse length needed as RST/VPP pin to accepted reset internally, $t_{d-RST}$		2			us	
	Input Voltage to accepted reset internally		0.9			V	
	Hysteresis, $V_{HYS-RST}$			0.8		V	
LVD	Operation current, $I_{SVS}$			10	15	uA	
	External input voltage to compare reference voltage			1.2		V	
	Compare reference voltage temperature drift	$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$		100		ppm/ $^\circ\text{C}$	
	Detect $V_{DD}$ voltage rang by user option, $V_{SVS} VLDx[3:0]=1110b$			3.3		V	
	Detect $V_{DD}$ voltage rang by user option, $V_{SVS} VLDx[3:0]=1101b$			3.2			
	Detect $V_{DD}$ voltage rang by user option, $V_{SVS} VLDx[3:0]=1100b$			3.1			
	Detect $V_{DD}$ voltage rang by user option, $V_{SVS} VLDx[3:0]=1011b$			3.0			
	Detect $V_{DD}$ voltage rang by user option, $V_{SVS} VLDx[3:0]=1010b$			2.9			
	Detect $V_{DD}$ voltage rang by user option, $V_{SVS} VLDx[3:0]=1001b$			2.8			
	Detect $V_{DD}$ voltage rang by user option, $V_{SVS} VLDx[3:0]=1000b$			2.7			
	Detect $V_{DD}$ voltage rang by user option, $V_{SVS} VLDx[3:0]=0111b$			2.6			
	Detect $V_{DD}$ voltage rang by user option, $V_{SVS} VLDx[3:0]=0110b$			2.5			
	Detect $V_{DD}$ voltage rang by user option, $V_{SVS} VLDx[3:0]=0101b$			2.4			
	Detect $V_{DD}$ voltage rang by user option, $V_{SVS} VLDx[3:0]=0100b$			2.3			
	Detect $V_{DD}$ voltage rang by user option, $V_{SVS} VLDx[3:0]=0011b$			2.2			
	Detect $V_{DD}$ voltage rang by user option, $V_{SVS} VLDx[3:0]=0010b$			2.1			
Detect $V_{DD}$ voltage rang by user option, $V_{SVS} VLDx[3:0]=0001b$			2.0				
BOR : Brownout Reset LVR : Low Voltage Reset of BOR LVD : Low Voltage Detect RST : External Reset pin							

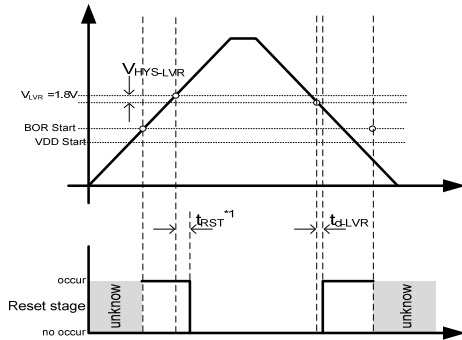


Figure 6.5-1 BOR Reset Diagram

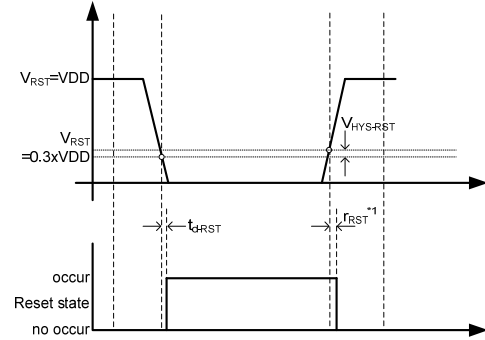


Figure 6.5-2 RST Reset Diagram

\*1  $t_{RST}$  : Please see BOR Introduce of HY11Pxx series User's Guide (UG-HY11S14-Vxx).

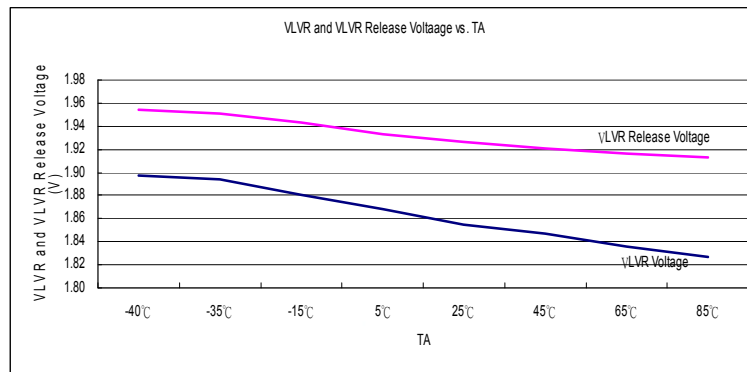


Figure 6.5-3 LVR vs. Temperature

## 6.6 Power System

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}$ , unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit	
VDDA	VDDA operation current, $I_{VDDA}$	$I_L = 0\text{mA}$	VDDAX[1:0]=00b		22		$\mu\text{A}$	
	Select VDDA output voltage	$I_L = 0.1\text{mA}$ , $V_{DD} \geq V_{DDA} + 0.2\text{V}$	VDDAX[1:0]=00b		3.4		V	
			VDDAX[1:0]=01b		3.0		V	
			VDDAX[1:0]=10b		2.6		V	
			VDDAX[1:0]=11b		2.4		V	
	Dropout voltage	$I_L = 10\text{mA}$	VDDAX[1:0]=00b			135		mV
			VDDAX[1:0]=01b			150		mV
VDDAX[1:0]=10b					165		mV	
VDDAX[1:0]=11b					180		mV	
Temperature drift	VDDAX[1:0]=11b	$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$		50		ppm/ $^\circ\text{C}$		
$V_{DD}$ Voltage drift	$I_L = 0.1\text{mA}$	$V_{DD} = 2.5\text{V} \sim 3.6\text{V}$		$\pm 0.2$		%/V		
ACM	ACM operation current, $I_{ACM}$	$I_L = 0\text{mA}$			20		$\mu\text{A}$	
	Output voltage, $V_{ACM}$	ENACM[0]=1, *1	$I_L = 0\mu\text{A}$		1.0		V	
	Output voltage with Load		$I_L = \pm 200\mu\text{A}$	0.98		1.02	$V_{ACM}$	
	Output voltage, $V_{ACM}$	ENACM[0]=1, *2	$I_L = 0\mu\text{A}$		1.2		V	
	Output voltage with Load		$I_L = \pm 200\mu\text{A}$	0.98		1.02	$V_{ACM}$	
	Temperature drift	ENACM[0]=1,	$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$		50		ppm/ $^\circ\text{C}$	
	VDDA Voltage drift	$I_L = 10\mu\text{A}$			100		$\mu\text{V}/\text{V}$	

VDDA : Adjust Voltage Regulator  
ACM : Analog Common Mode Voltage

\*1:  $V_{ACM} = 1.0\text{V}$  is just at A/D differential voltage reference < 1.4V ( if delta VR:  $(V_{DDA}-V_{SS})/2$  )  
\*2:  $V_{ACM} = 1.2\text{V}$  is just at A/D differential voltage reference > 1.4V ( if delta VR:  $(V_{DDA}-V_{SS})/2$  )

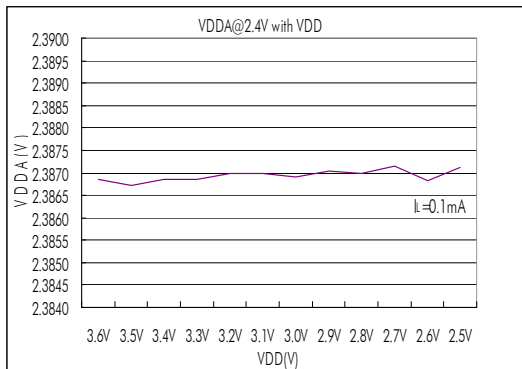


Figure 6.6-1 VDDA  $I_L=0.1\text{mA}$  vs. VDD

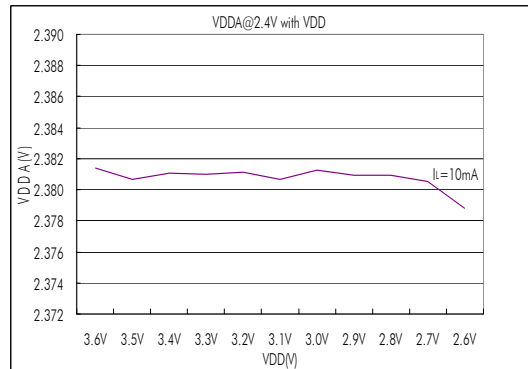


Figure 6.6-2 VDDA  $I_L=10\text{mA}$  vs. VDD

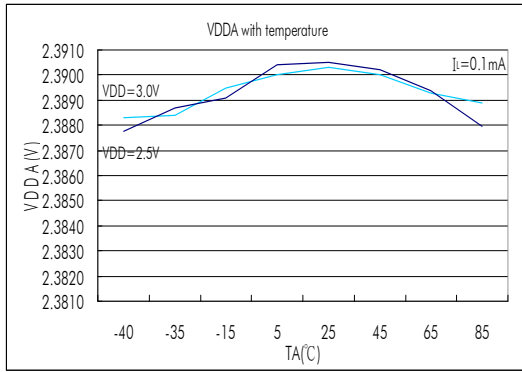


Figure 6.6-3 VDDA  $I_L=0.1\text{mA}$  vs. Temperature

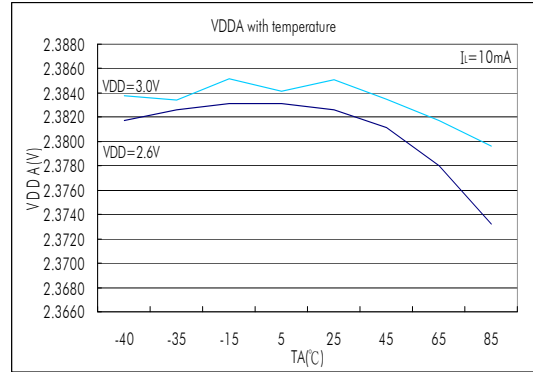


Figure 6.6-4 VDDA  $I_L=10\text{mA}$  vs. Temperature

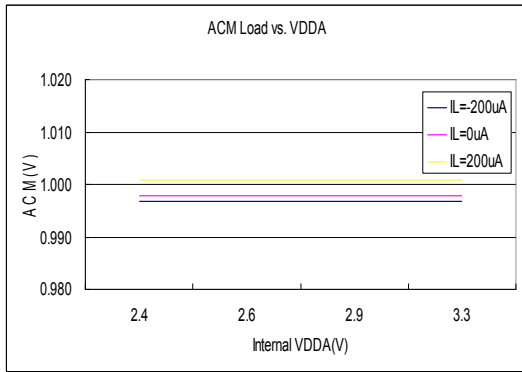


Figure 6.6-5 ACM Load vs. VDDA (a)

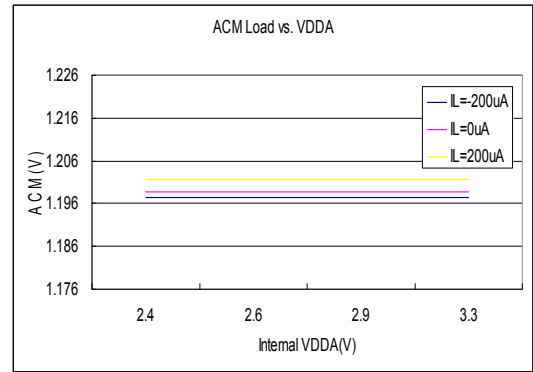


Figure 6.6-5 ACM Load vs. VDDA (b)

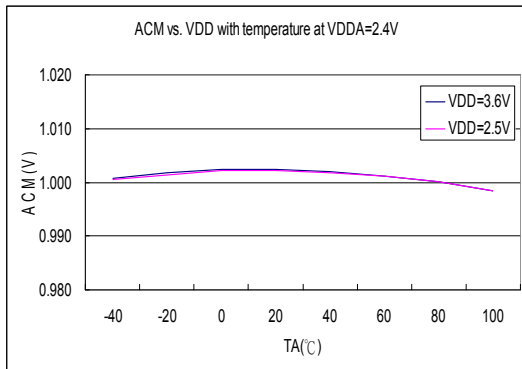


Figure 6.6-6 ACM vs. Temperature (a)

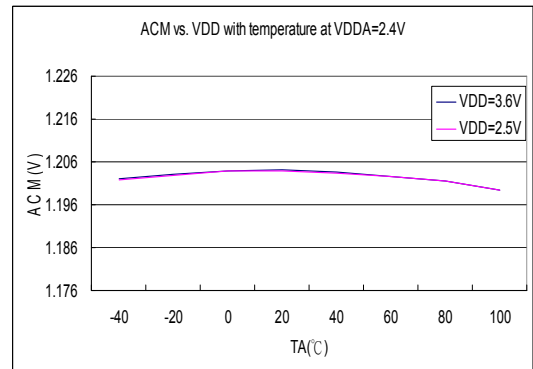


Figure 6.6-6 ACM vs. Temperature (b)

### 6.7 SD18, Power Supply and Recommended Operating Conditions

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA}=2.4\text{V}$ , unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
$V_{SD18}$	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
$f_{SD18}$	Modulator sample frequency, ADC_CK			25	250	300	KHz
	Over Sample Ratio, OSR			256		32768	
$I_{SD18}$	Operation supply current without PGA	ENADC[0]=1	GAIN =4, ADC_CK=250KHz		120		$\mu\text{A}$

\*1, OSR=128, setting by ADCCN3[ OSR[3] ] bit.  
OSR[3:0]=1010, OSR=128; OSR[3:0]=0xxx, OSR=256 ~ 32768

#### 6.7.1 PGA, Power Supply and Recommended Operating Conditions

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA}=2.4\text{V}$ , unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
$V_{PGA}$	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
$I_{PGA}$	Operation supply current	PGAGN[1:0]=<01> or <1x>			320		$\mu\text{A}$
$G_{PGA}$	Gain temperature drift	$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$	GAIN=128		5		ppm/ $^\circ\text{C}$

#### 6.7.2 SD18, Performance II ( $f_{SD18}=250\text{KHz}$ )

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA}=2.9\text{V}, V_{VR}=1.0\text{V}, \text{GAIN}=1$  without PGA, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
INL	Integral Nonlinearity(INL)	$V_{DDA}=2.4\text{V}, V_{VR}=1.0\text{V}, \Delta\text{SI}=\pm 450\text{mV}$			$\pm 0.003$	$\pm 0.01$	%FSR
	No Missing Codes <sup>3</sup>	ADC_CK=250KHz, OSR[2:0]=010b		23			Bits
$G_{SD18}$	Temperature drift Gain 1~x16		$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$		2		ppm/ $^\circ\text{C}$
$E_{OS}$	Offset error of Full Scale Rang input voltage range with Chopper without PGA	$\Delta\text{AI}=0\text{V}$ $\Delta\text{VR}=0.9\text{V}$ DCSET[2:0]=<000> * $\Delta\text{AI}$ is external short	Gain=2			1	%FSR
	Offset temperature drift with chopper without PGA		GAIN=1		2		$\mu\text{V}/^\circ\text{C}$
			GAIN=2		1		
			GAIN=4		0.5		
			GAIN=16		0.15		
			GAIN=128		0.02		
$\text{CM}_{SD18}$	Common-mode rejection	$V_{CM}=0.7\text{V}$ to $1.7\text{V}$ , $V_{VR}=1.0\text{V}$ , without PGA	$V_{SI}=0\text{V}$ , GAIN=1		90		dB

# HY11P41

## Embedded 18-Bit $\Sigma\Delta$ ADC

### 8-Bit RISC-like Mixed Signal Microcontroller

		$V_{CM}=0.7V$ to $1.7V$ , $V_{VR}=1.0V$ ,	$V_{SI}=0V$ , GAIN=16	75	
PSRR	DC power supply rejection	$V_{DDA}=3.0V, \Delta V_{DDA}=\pm 100mV$ , $V_{VR}=1.0V, V_{SI}=V_{SL}=1.2V$ ,	GAIN=1 PGA=off	75	dB
			GAIN=16		

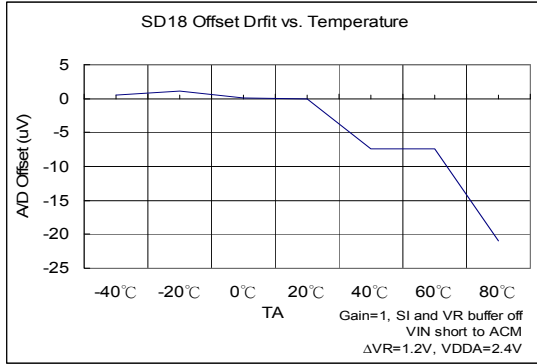


Figure 6.7-1(a) SD18 Offset Temperature Drift

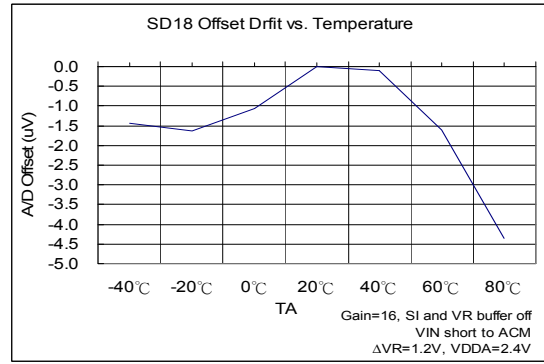


Figure 6.7-1(b) SD18 Offset Temperature Drift

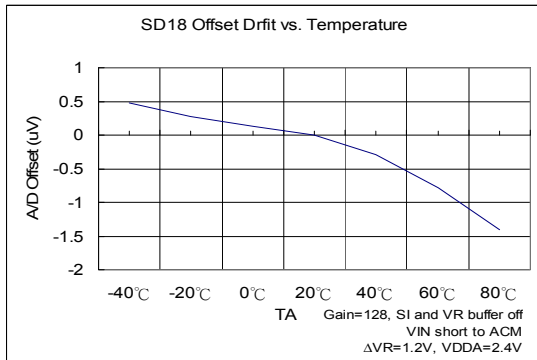


Figure 6.7-1(c) SD18 Offset Temperature Drift

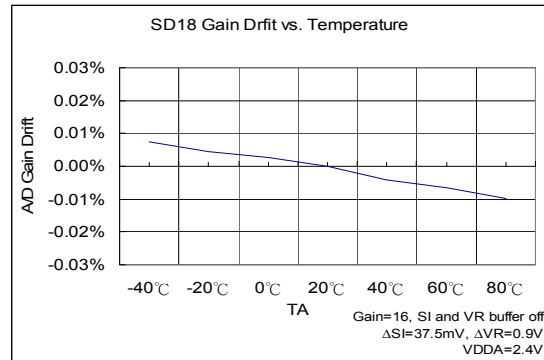


Figure 6.7-2(b) SD18 Gain Drift with Temperature

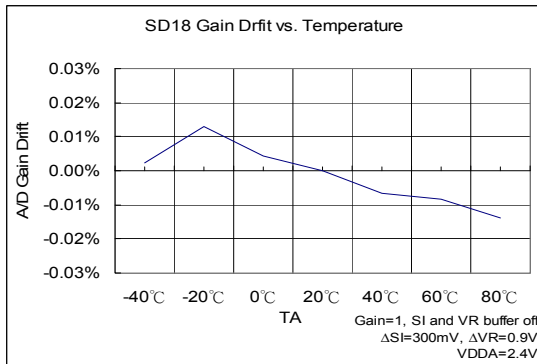


Figure 6.7-2(a) SD18 Gain Drift with Temperature

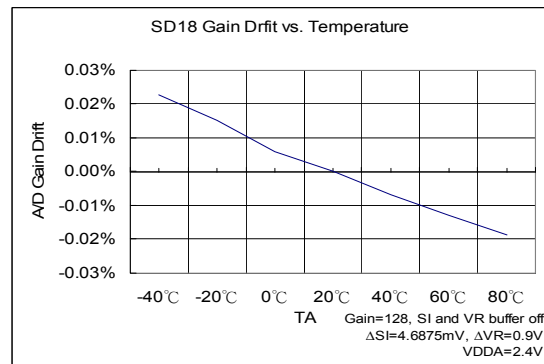


Figure 6.7-2(c) SD18 Gain Drift with Temperature

### 6.7.3 SD18, Temperature Sensor

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{V}$ ,  $V_{DDA} = 2.4\text{V}$ , unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
$TC_S$	Sensor temperature drift			178		$\mu\text{V}/^\circ\text{C}$
KT	Absolute Temperature Scale $0^\circ\text{K}$	INBUF[0]=1		-289		$^\circ\text{C}$
$TC_{ERR}$	One point calibrate error temperature	Calibration at $25^\circ\text{C}$ of $-40^\circ\text{C} \sim 85^\circ\text{C}$		$\pm 2$		$^\circ\text{C}$

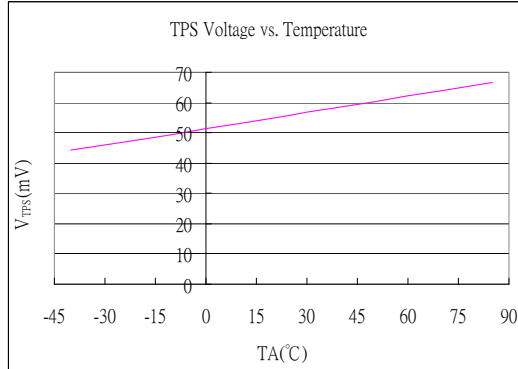


Figure 6.7-3 TPS Output Voltage vs. Temperature Drift

## 6.7.4 SD18 Noise Performance

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA} = 2.4\text{V}$ , unless otherwise noted

HY11P41 provides important input noise specification that aims at SD18. Table 6.7-4(a) and Table 6.7-4(b) lists out the relations of typical noise specification, Gain, Output rate, and maximum input voltage of single end. Test condition configuration and external input signal short, voltage reference: 1.2V and 1024 records were sampled.

<b>ENOB(RMS) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V</b>														
Max. Vin(mV) =0.9*VREF <sup>(1)</sup>	OSR				128	256	512	1024	2048	4096	8192	16384	32768	
	Output rate(HZ)				1953	977	488	244	122	61	31	15	8	
	Gain	=	PGA	×	ADGN									
±2400	0.25	=	1	×	0.25	14.0	16.3	17.6	18.3	18.9	19.4	19.8	20.3	20.7
±2160	0.5	=	1	×	0.5	13.9	16.2	17.5	18.2	18.8	19.3	19.7	20.2	20.6
±1080	1	=	1	×	1	14.0	16.2	17.4	18.1	18.6	19.1	19.5	19.9	20.4
±540	2	=	1	×	2	13.9	16.1	17.3	17.9	18.4	18.9	19.4	19.8	20.2
±270	4	=	1	×	4	13.9	16.0	17.0	17.7	18.1	18.6	19.1	19.6	20.0
±135	8	=	1	×	8	13.9	15.9	16.7	17.3	17.8	18.2	18.8	19.2	19.7
±68	16	=	1	×	16	13.8	15.6	16.3	16.8	17.3	17.8	18.3	18.8	19.3
±34	32	=	2	×	16	13.5	14.8	15.4	15.9	16.4	16.9	17.4	17.9	18.4
±17	64	=	4	×	16	13.4	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.1
±8	128	=	8	×	16	13.1	14.1	14.6	15.1	15.6	16.1	16.6	17.1	17.6

(1) Max. Vin (mV) is the max. input voltage of single end to ground (VSS).

Table 6.7-4(a) SD18 ENOB Table

<b>RMS Noise(uV) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V</b>														
Max. Vin(mV) =0.9*VREF	OSR				128	256	512	1024	2048	4096	8192	16384	32768	
	Output rate(HZ)				1953	977	488	244	122	61	31	15	8	
	Gain	=	PGA	×	ADGN									
±2400	0.25	=	1	×	0.25	680.48	122.16	47.79	29.08	20.02	14.45	10.35	7.55	5.90
±2160	0.5	=	1	×	0.5	355.63	63.41	25.72	15.67	10.78	7.66	5.63	3.99	2.97
±1080	1	=	1	×	1	166.02	31.71	13.93	8.63	5.99	4.35	3.22	2.41	1.76
±540	2	=	1	×	2	85.85	16.80	7.72	4.96	3.49	2.49	1.81	1.33	0.98
±270	4	=	1	×	4	43.52	9.19	4.53	2.93	2.12	1.51	1.08	0.78	0.59
±135	8	=	1	×	8	22.18	5.10	2.83	1.91	1.33	0.97	0.67	0.49	0.35
±68	16	=	1	×	16	11.97	3.08	1.88	1.30	0.91	0.66	0.46	0.33	0.23
±34	32	=	2	×	16	6.75	2.63	1.79	1.24	0.87	0.62	0.44	0.32	0.22
±17	64	=	4	×	16	3.75	1.68	1.12	0.80	0.56	0.42	0.28	0.20	0.14
±8	128	=	8	×	16	2.16	1.09	0.78	0.55	0.38	0.27	0.19	0.13	0.10

Table 6.7-4(b) SD18 RMS Noise Table



The RMS noise is referred to the input. The Effective Number of Bits (ENOB (RMS Bit)) is defined as:

$$\text{ENOB(RMS)} = \frac{\ln\left(\frac{\text{FSR}}{\text{RMS Noise}}\right)}{\ln(2)}$$

$$\text{RMS Noise} = \frac{\left(2 \times \text{VREF} \times \sqrt{\sum_{k=1}^{1024} (\text{ADO}[k] - \text{Average})^2}\right)}{2^{23}}$$

Where FSR (Full - Scale Range) =  $2 \times \text{VREF}/\text{Gain}$ .

$$\text{Average} = \frac{\sum_{k=1}^{1024} (\text{ADO}[k])}{1024}$$

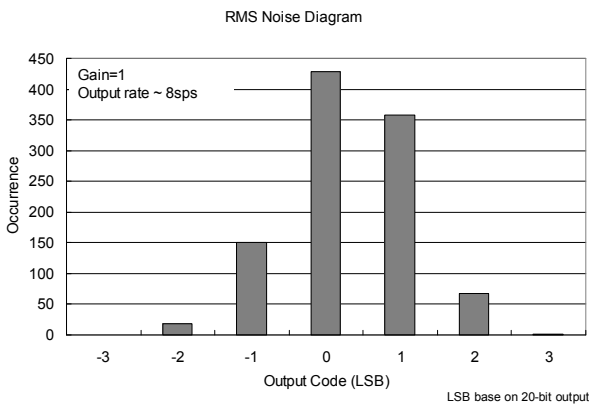


Figure 6.7-4(a) RMS Noise Diagram

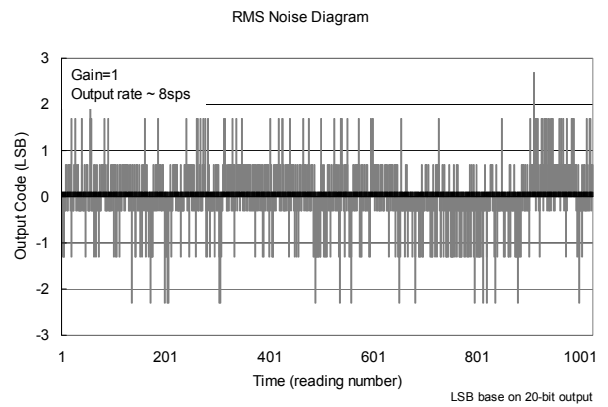


Figure 6.7-4(b) Output Code Diagram

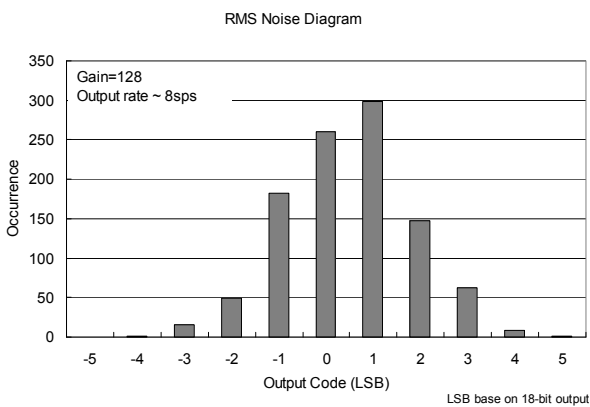


Figure 6.7-4(c) RMS Noise Diagram

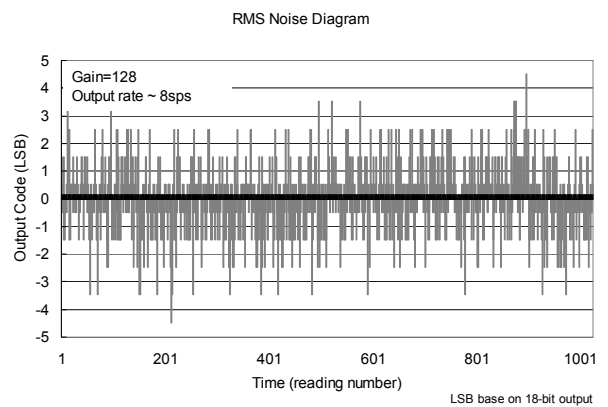


Figure 6.7-4(d) Output Code Diagram

#### 6.8 Built-in EPROM (BIE)

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{V}$ , unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
$V_{BIE}$	Supply Voltage			6.0	6.5	V
$I_{BIE}$	Operation supply current			5		mA
$V_{SS}$	Supply Voltage			0		V

## 7. Ordering Information

Device No. <sup>1</sup>	Package Type	Pins	Package Drawing		Code <sup>2</sup>	Shipment Packing Type	Unit Q'ty	Material Composition	MSL <sup>3</sup>
HY11P41-D000	Die	-	D	000	000	-	250	Green <sup>4</sup>	-
HY11P41-E016	SSOP	16	E	016	000	Tube	100	Green <sup>4</sup>	MSL-3
HY11P41-E016	SSOP	16	E	016	000	Tape & Reel	2500	Green <sup>4</sup>	MSL-3
HY11P41-S016	SOP	16	S	016	000	Tube	50	Green <sup>4</sup>	MSL-3
HY11P41-S016	SOP	16	S	016	000	Tape & Reel	2500	Green <sup>4</sup>	MSL-3
HY11P41-N016	QFN	16	N	016	000	Tape & Reel	5000	Green <sup>4</sup>	MSL-3

<sup>1</sup> **Device No.:** Model No. – Package Type Description – Code (Blank Code/ Standard/ Customized Programming Code)

Ex: Your customized programming code is 008 and you require die shipment.

The device No. will be HY11P41-D000-008

Ex: You request blank code in die package.

The device No. will be HY11P41-D000

Ex: You request blank code in SSOP16 package.

The device No. will be HY11P41-E016

And please clearly indicate the shipment packing type when placing orders.

Ex: Your customized programming code is 009 and you require products in SOP16 package.

The device No. will be HY11P41-S016-009.

And please clearly indicate the shipment packing type when placing orders.

<sup>2</sup> **Code:**

“001”~ “999” is standard or customized programming code. Blank code does not have these numbers.

<sup>3</sup> **MSL:**

The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

<sup>4</sup> **Green (RoHS & no Cl/Br):**

HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br/Cl<0.1%)

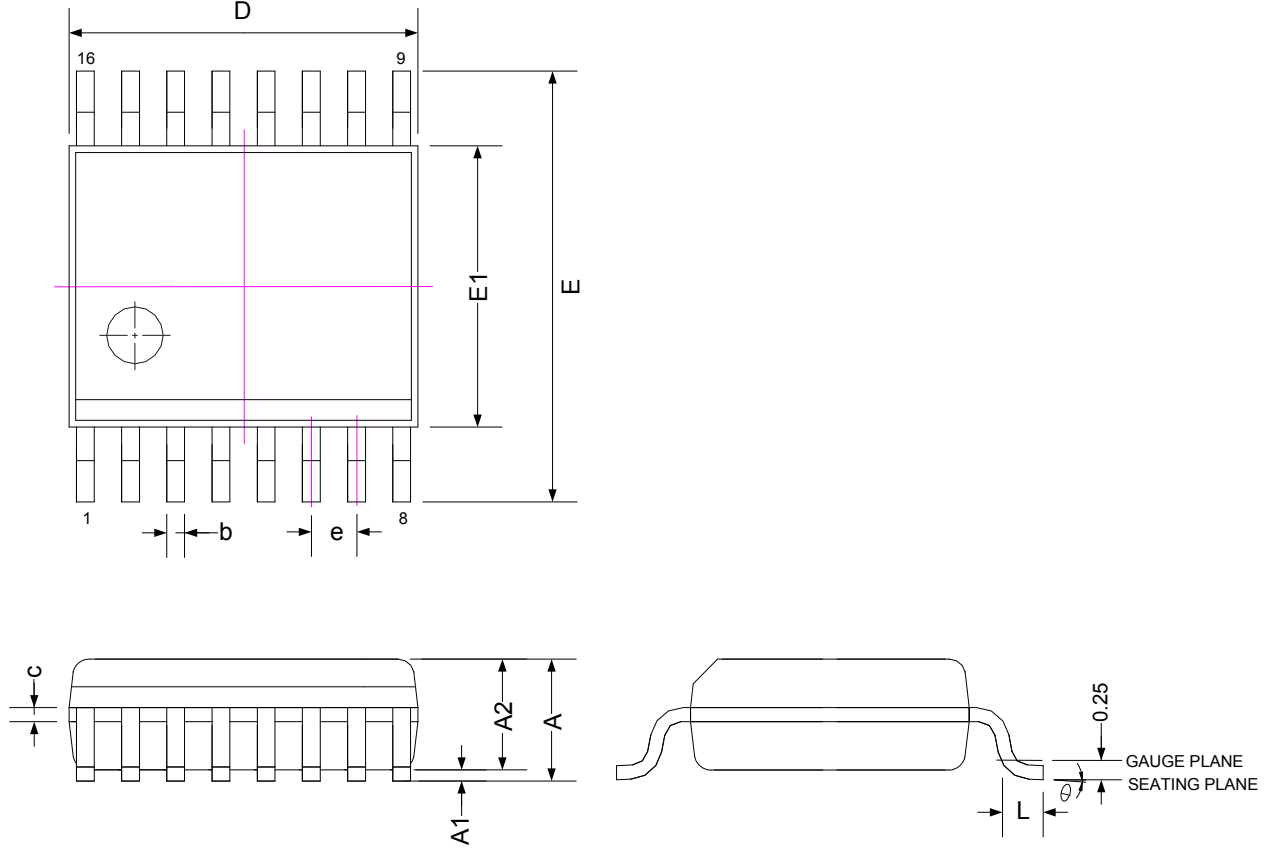
# HY11P41

Embedded 18-Bit  $\Sigma\Delta$ ADC  
8-Bit RISC-like Mixed Signal Microcontroller

## 8. Package Information

### 8.1 SSOP16 (E016)

#### 8.1.1 Package Dimensions

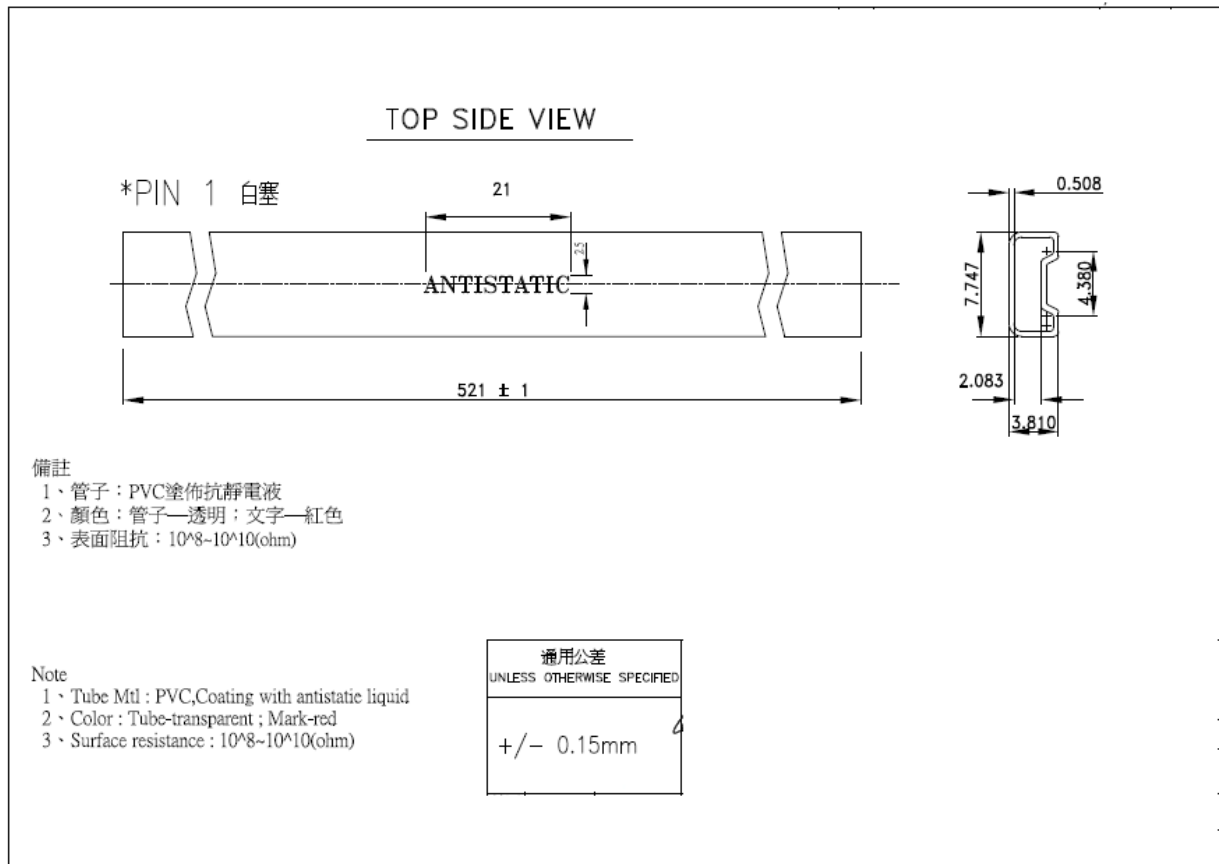


SYMBOLS	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	0.15	0.25
A2	-	-	1.50
b	0.20	-	0.30
c	0.18	-	0.25
D	4.80	4.90	5.00
E1	3.81	3.91	3.99
E	5.79	5.99	6.20
L	0.41	-	1.27
e	0.635 BASIC		
$\theta^\circ$	0	-	8

Note:

1. All dimensions refer to JEDEC OUTLINE MO-137.
2. Do not include Mold Flash or Protrusions.
3. Unit : mm.

### 8.1.2 Tube Dimensions

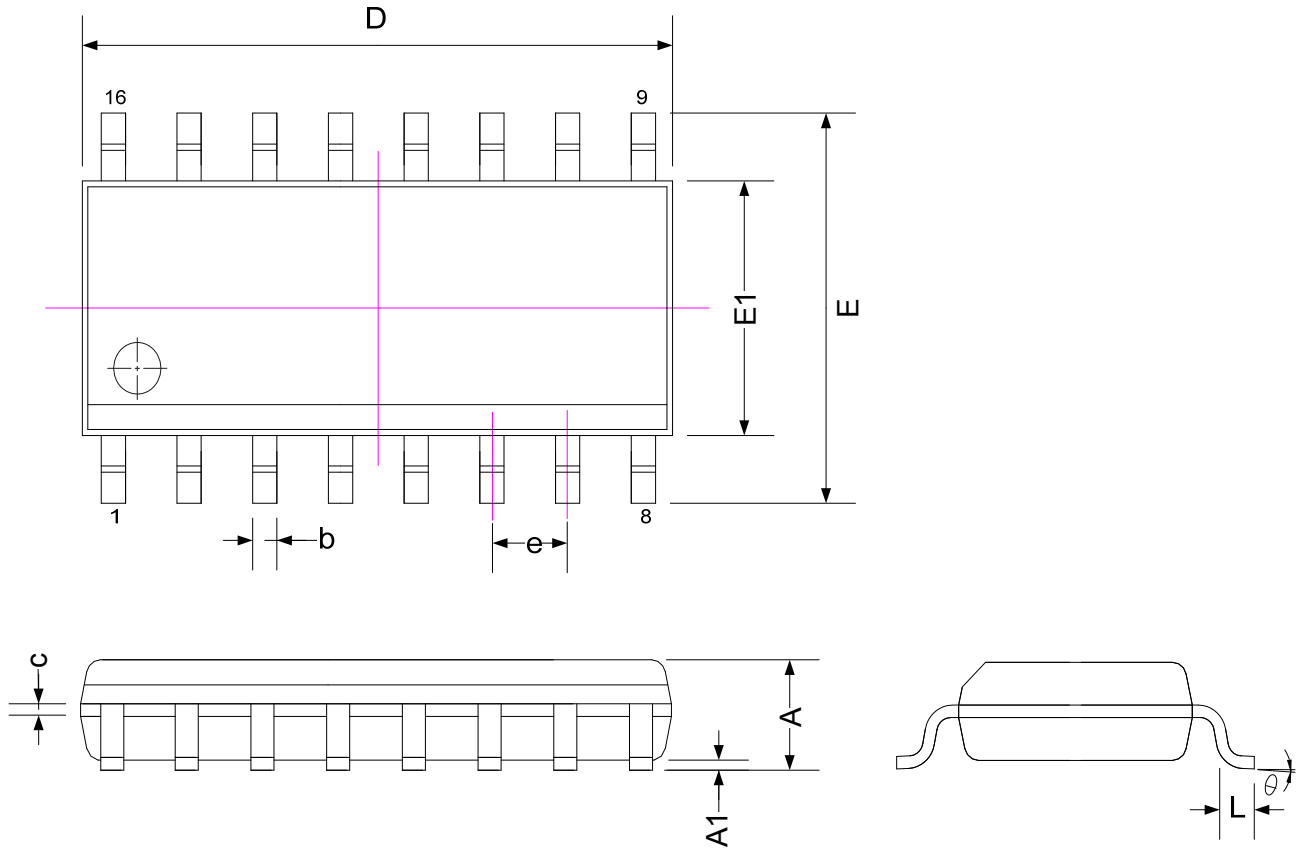


# HY11P41

Embedded 18-Bit  $\Sigma\Delta$ ADC  
8-Bit RISC-like Mixed Signal Microcontroller

## 8.2 SOP16 (S016)

### 8.2.1 Package Dimensions



SYMBOLS	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	-	0.25
b	0.31	-	0.51
c	0.10	-	0.25
D	9.90 BASIC		
E1	3.90 BASIC		
E	6.00 BASIC		
L	0.40	-	1.27
e	1.27 BASIC		
$\theta$	0	-	8

Note:

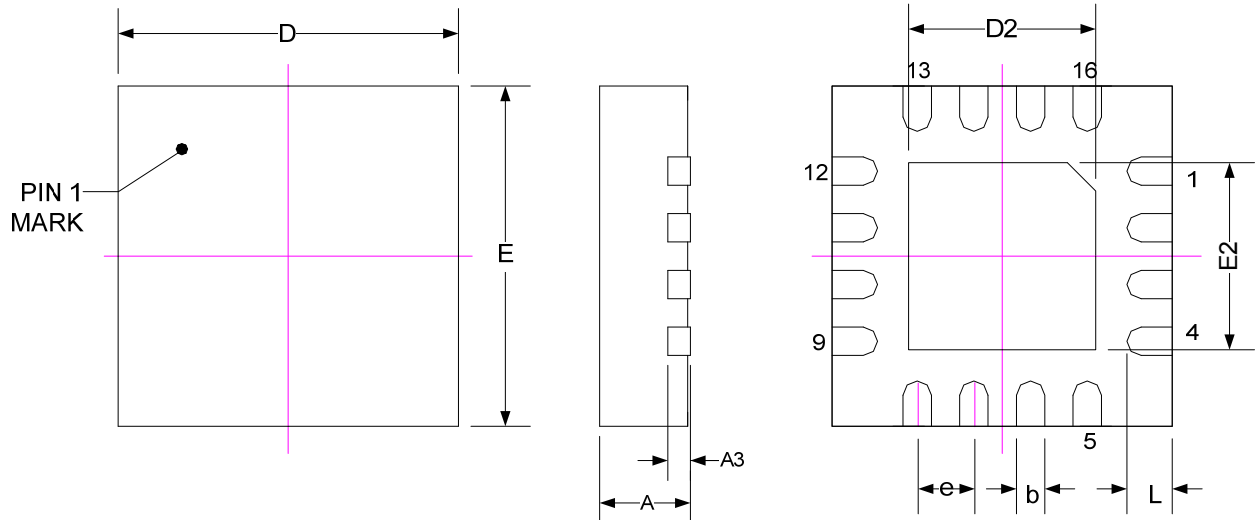
1. All dimensions refer to JEDEC OUTLINE MS-012.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.



## 8.3 QFN16(N016)

### 8.3.1 Package Dimensions

Unit : mm



SYMBOLS	MIN	NOM	MAX
A	0.70	0.75	0.80
A3	0.203 REF.		
b	0.20	0.25	0.30
D	2.925	3.000	3.075
E	2.925	3.000	3.075
D2	1.625	1.725	1.825
E2	1.625	1.725	1.825
L	0.30	0.35	0.40
e	0.50 BASIC		

Note: All dimensions refer to JEDEC OUTLINE MO-220



## 9. Revision Record

Major differences are stated thereafter:

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Version	Page	Revision Summary
V06	All	First Edition
V07	13	Add in note of SD18 Network
V08	7,10~13,35,38	Add in QFN16 package type related information
V10	5~17, 19	Delete the related description and figures of Serial communication SPI module.
V11	5	Add the description of fast start function
	14~16	Update the application circuits
	29	Delete the description related to INBUF and VRBUF function of ADC
	36~37	Update the package information of SSOP16 and SOP16
V12	6~16, 20	Update PT1.1/TST pin description
V13	35	HY11P41-N016 ordering information (3000/Reel revise to 5000/Reel)