



HY11P23
Datasheet
8-Bit RISC-Like Mixed Signal Microcontroller
Embedded Low Noise Amplifier
18-Bit $\Sigma\Delta$ ADC

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1. Features

- 8-bit RISC, 66 instructions included.
- Operating voltage range: 2.0V to 3.6V, operation temperature range: -40°C~85°C.
- External Crystal Oscillator and Internal High Precision RC Oscillator, 6 CPU clock rates enable users to have the most power-saving plan.
 - Active Mode 300uA@2MHz
 - Standby Mode 3uA@32KHz
 - Sleep Mode 1uA
- 4K Word OTP (One Time Programmable) Type program memory, 256 Byte Data Memory.
- Brownout detector and Watch dog Timer, prevents CPU from Crash.
- 18-bit fully differential input Sigma-Delta Analog-to-Digital Converter (A/D)
 - Build-in PGA (Programmable Gain Amplifier) 1/4x \ 1/2x \ 1x. ...128x, 10 input signal gain selection.
 - Build-in Input zero point adjustment can increase measurement range according to different application.
 - Built-in high impedance input buffer (Not suitable for 4x or upwards input gain).
 - Build-in absolute temperature sensor
- Ultra-Low Input Noise (<1uVpp) OP provides high output impedance, small signal amplification and low current voltage transformation
- 1.0V and 1.2V internal analog circuit common ground that equips with Push-Pull drive ability to provide sensor driving voltage.
- LVD low voltage detection function has 14 steps of voltage detection configuration and external input voltage detection function.
- VDDA can select 4 different output voltage that equips with 10mA low dropout regulator function.
- 8-bit Timer A
- 16-bit Timer B module has Capture/ Compare function.
- 8-bit Timer C module can generate PWM/ PFD waveform.
- Serial communication SPI, EUART module.
- Support 6 stack level

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Device No.	Package	ADC* (SD 18)	LNOP*	I/O	Program Memory (word)	Data Memory (byte)	Serial Interface	Timer*	Instruction Set*	Stack Level
HY11P23-L032	LQFP32	10	1	22	4k	256	SPI+EUART	A,B,C	H08A	6
HY11P23-N032	QFN32	10	1	22	4k	256	SPI+EUART	A,B,C	H08A	6
HY11P23-E028	SSOP28	7	-	19	4k	256	SPI+EUART	A,B,C	H08A	6

*ADC: SD 18: Sigma Delta ADC, 18bit $\Sigma\Delta$ ADC

*LNOP: Low noise operational amplifier

*Timer: Timer A (8-bit) has several interrupt time configurations ;

Timer B (16-bit) has Capture/Compare function;

Timer C (8-bit) has PWM/PFD function.

*Instruction Set: Main differences of instruction set: H08A has 8x8 hardware multiplier,

16-bit look-up-table instruction, condition jump instruction, stack operation instruction ...etc.

2. Pin Definition

2.1 32Pin Diagram LQFP32

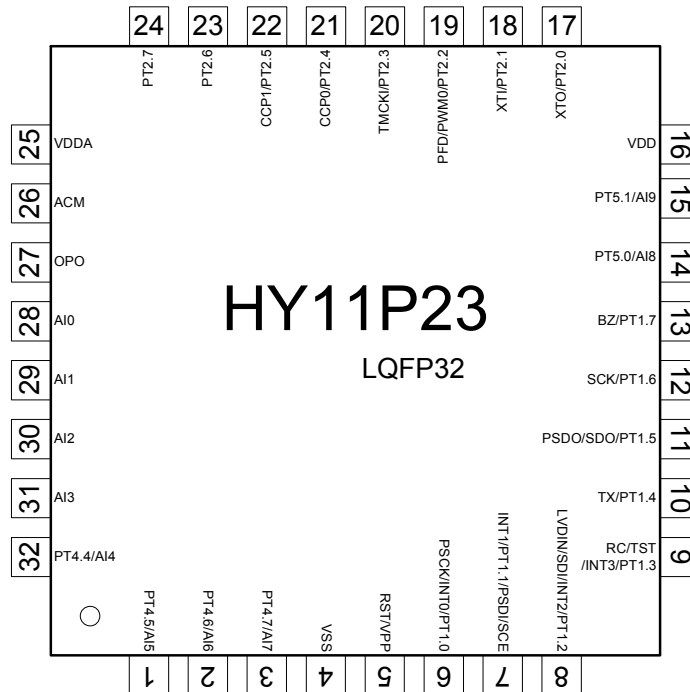


Figure 2-1 HY11P23 LQFP32 Pin Diagram

2.2 32Pin Diagram QFN32

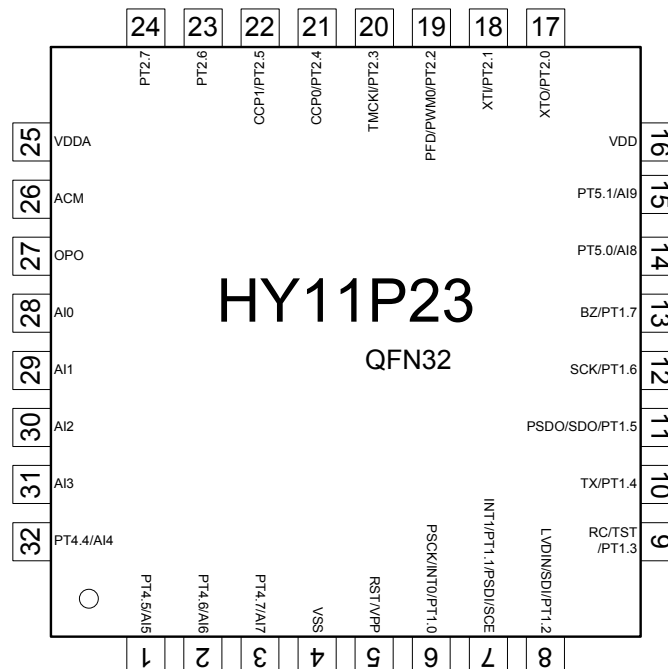


Figure 2-2 HY11P23 QFN32 Pin Diagram

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2.3 28Pin Diagram SSOP28

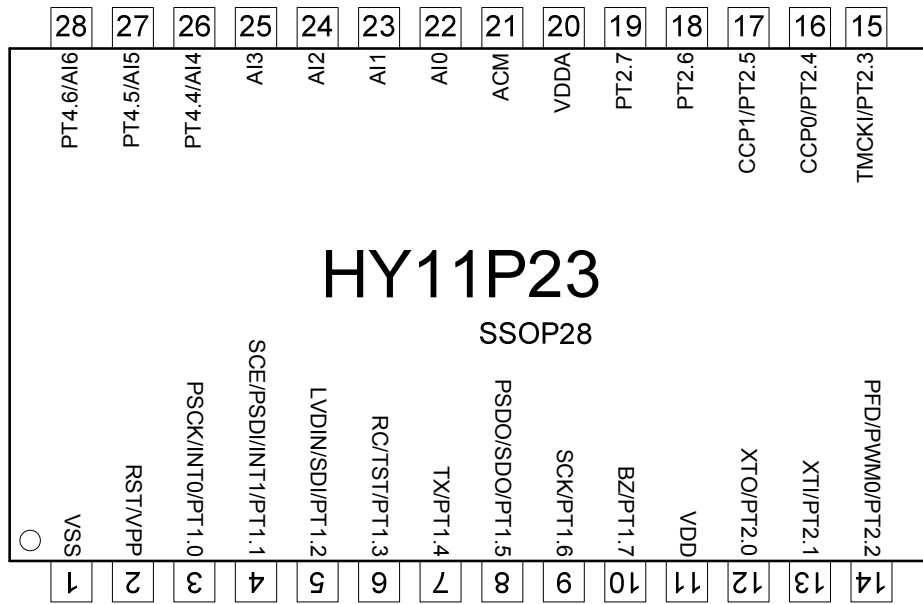


Figure 2-3 HY11P23 SSOP28 Pin Diagram

Note 1 : VPP and RST use the same pin. Input voltage cannot exceed 5.8V when not programming EPROM.

Note 2 : TST and PT1.3 use the same pin. Input voltage cannot exceed VDD+0.3V while operating.

Note 3 : If PT1.3 is not configured as external button pin, the anti-interference ability will be enhanced.

2.4 LQFP32/QFN32 Pinout I/O Description

"I/O" input/output, "I" input, "O" output, "S" Smith Trigger, "C" CMOS features compatible input/output, "P" power supply, "A" analog channel

NO.	Pin Name	Pin Characteristic		Description	
		Pin Type	Buffer Type		
1	PT4.5/AI5	PT4.5	I	C	Digital input
		AI5	A	A	Analog input channel
2	PT4.6/AI6	PT4.6	I	C	Digital input
		AI6	A	A	Analog input channel
3	PT4.7/AI7	PT4.7	I	C	Digital input
		AI7	A	A	Analog input channel
4	VSS		P	P	Grounding pin for IC operation voltage
5	RST/VPP	RST	I	S	Reset IC
		VPP	P	P	EPROM programming voltage input
6	PT1.0/INT0/PSCK	PT1.0	I	S	Digital input
		INT0	I	S	Interrupt input INT0
		PSCK	I	S	OTP programming interface SCK
7	PT1.1/INT1/PSDI/SCE	PT1.1	I	S	Digital input
		INT1	I	S	Interrupt input INT1
		PSDI	I	S	OTP programming interface SDI
		SCE	I/O	S	SPI communication interface SCE
8	PT1.2/SDI/LVDIN	PT1.2	I	S	Digital input
		SDI	I/O	S	SPI communication interface SDI
		LVDIN	A	A	LVD external signal input port
9	PT1.3/TST/RC	PT1.3	I	S	Digital input
		RC	I/O	S	EUART communication interface RC
		TST	I	S	Test Mode input pin (invalid)
10	PT1.4/TX				

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		PT1.4	I/O	S	Digital I/O
		TX	I/O	S	EUART communication interface TX
11	PT1.5/PSDO/SDO	PT1.5	I/O	S	Digital I/O
		PSDO	I/O	C	OTP programming interface SDO
		SDO	I/O	S	SPI communication interface SDO
12	PT1.6/SCK	PT1.6	I/O	S	Digital I/O
		SCK	I/O	S	SPI communication interface SCK
13	PT1.7/BZ	PT1.7	I/O	S	Digital I/O
		BZ	O	C	Buzzer output
14	PT5.0/AI8	PT5.0	I	C	Digital input
		AI8	A	A	Analog input channel
15	PT5.1/AI9	PT5.1	I	C	Digital input
		AI9	A	A	Analog input channel
16	VDD		P	P	IC operation power source
17	PT2.0/XTO	PT2.0	I/O	S	Digital I/O
		XTO	A	A	External oscillator output
18	PT2.1/XTI	PT2.1	I/O	S	Digital I/O
		XTI	A	A	External oscillator output
19	PT2.2/PWM0/PFD	PT2.2	I/O	C	Digital I/O
		PWM0	O	C	PWM output
		PFD	O	C	PFD output
20	PT2.3/TMCKI	PT2.3	I/O	S	Digital I/O
		TMCKI	I	S	TIMERC clock source input
21	PT2.4/CCP0	PT2.4	I/O	S	Digital I/O
		CCP0	I	S	Capture/compare mode signal port
22	PT2.5/CCP1	PT2.5	I/O	S	Digital I/O
		CCP1	I	S	Capture/compare mode signal port

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23	PT2.6	I/O	C	Digital I/O	
24	PT2.7	I/O	C	Digital I/O	
25	VDDA	P	P	Regulator output Analog circuit voltage source	
26	ACM	P	P	Internal analog circuit common ground pin	
27	OPO	A	A	OP output	
28	AI0	A	A	Analog channel pin	
29	AI1	A	A	Analog channel pin	
30	AI2	A	A	Analog channel pin	
31	AI3	A	A	Analog channel pin	
32	PT4.4/AI4	PT4.4	I	C	Digital input
		AI4	A	A	Analog input channel

Table 2-1 Pin Definition and Function description

2.5 SSOP28 Pinout I/O Description

"I/O" input/output, "I" input, "O" output, "S" Smith Trigger, "C" CMOS features compatible input/output, "P" power supply, "A" analog channel

NO.	Pin Name	Pin Characteristic		Description
		Pin Type	Buffer Type	
1	VSS	P	P	Grounding pin for IC operation voltage
2	RST	I	S	Reset IC
	VPP	P	P	EPROM programming voltage input
3	PT1.0	I	S	Digital input
	INT0	I	S	Interrupt input INT0
	PSCK	I	S	OTP programming interface SCK
4	PT1.1	I	S	Digital input
	INT1	I	S	Interrupt input INT1
	PSDI	I	S	OTP programming interface SDI
	SCE	I/O	S	SPI communication interface SCE
5	PT1.2	I	S	Digital input
	SDI	I/O	S	SPI communication interface SDI
	LVDIN	A	A	LVD external signal input port
6	PT1.3	I	S	Digital input
	RC	I/O	S	EUART communication interface RC
	TST	I	S	Test Mode input pin (invalid)
7	PT1.4	I/O	S	Digital I/O
	TX	I/O	S	EUART communication interface TX
8	PT1.5	I/O	S	Digital I/O
	PSDO	I/O	C	OTP programming interface SDO
	SDO	I/O	S	SPI communication interface SDO
9	PT1.6	I/O	S	Digital I/O
	SCK	I/O	S	SPI communication interface SCK

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10	PT1.7/BZ	PT1.7 BZ	I/O O	S C	Digital I/O Buzzer output
11	VDD		P	P	IC operation power source
12	PT2.0/XTO	PT2.0 XTO	I/O A	S A	Digital I/O External oscillator output
13	PT2.1/XTI	PT2.1 XTI	I/O A	S A	Digital I/O External oscillator output
14	PT2.2/PWM0/PFD	PT2.2 PWM0 PFD	I/O O O	C C C	Digital I/O PWM output PFD output
15	PT2.3/TMCKI	PT2.3 TMCKI	I/O I	S S	Digital I/O TIMERC clock source input
16	PT2.4/CCP0	PT2.4 CCP0	I/O I	S S	Digital I/O Capture/compare mode signal port
17	PT2.5/CCP1	PT2.5 CCP1	I/O I	S S	Digital I/O Capture/compare mode signal port
18	PT2.6		I/O	C	Digital I/O
19	PT2.7		I/O	C	Digital I/O
20	VDDA		P	P	Regulator output Analog circuit voltage source
21	ACM		P	P	Internal analog circuit common ground pin
22	A10		A	A	Analog channel pin
23	A11		A	A	Analog channel pin
24	A12		A	A	Analog channel pin
25	A13		A	A	Analog channel pin
26	PT4.4/A14	PT4.4 A14	I A	C A	Digital input Analog input channel
27	PT4.5/A15	PT4.5	I	C	Digital input

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		A15	A	A	Analog input channel
28	PT4.6/A16				
		PT4.6	I	C	Digital input
		A16	A	A	Analog input channel

Table 2-2 Pin Definition and Function Description

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3. Application Circuit

3.1 Four Sets Bridge Sensor I

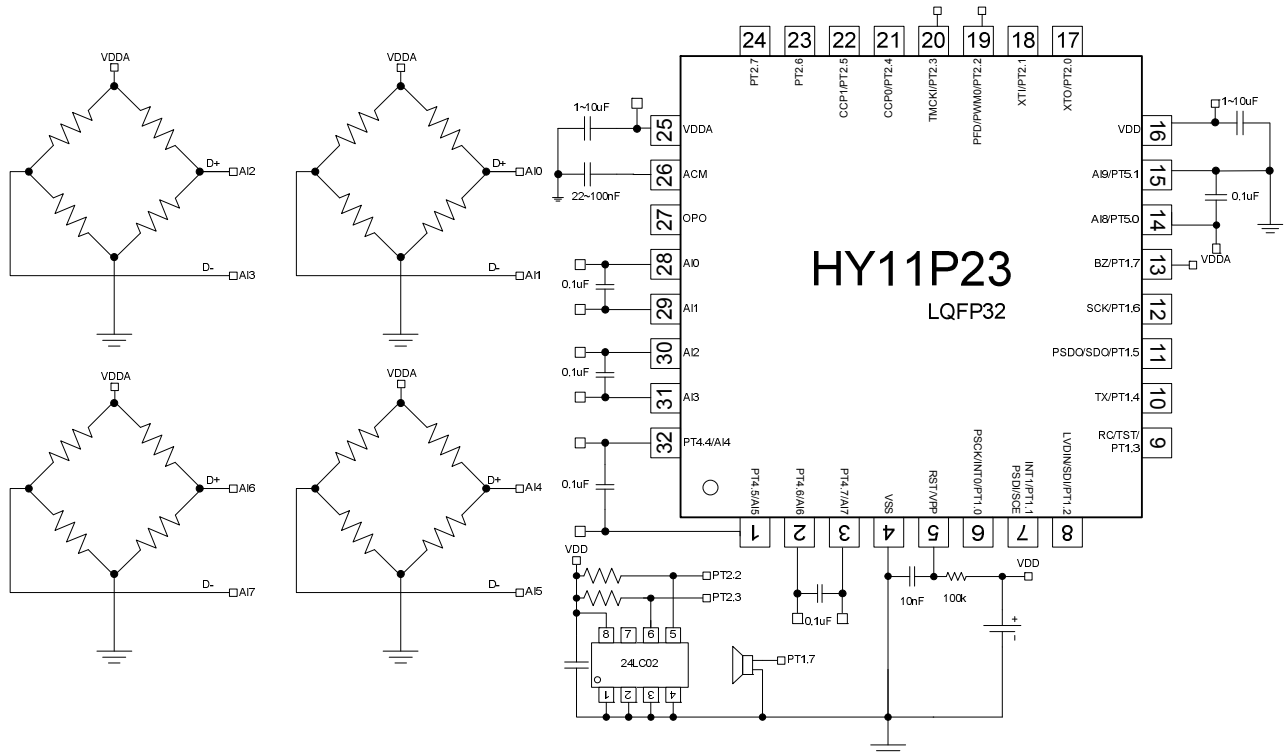


Figure 3-1 Application Circuit of Bridge Sensor

Note : DCSET[2:0] can conduct bias adjustment of Load Cell zero point voltage address

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3.3 Two-Wire 4-20mA Current Panel Meter

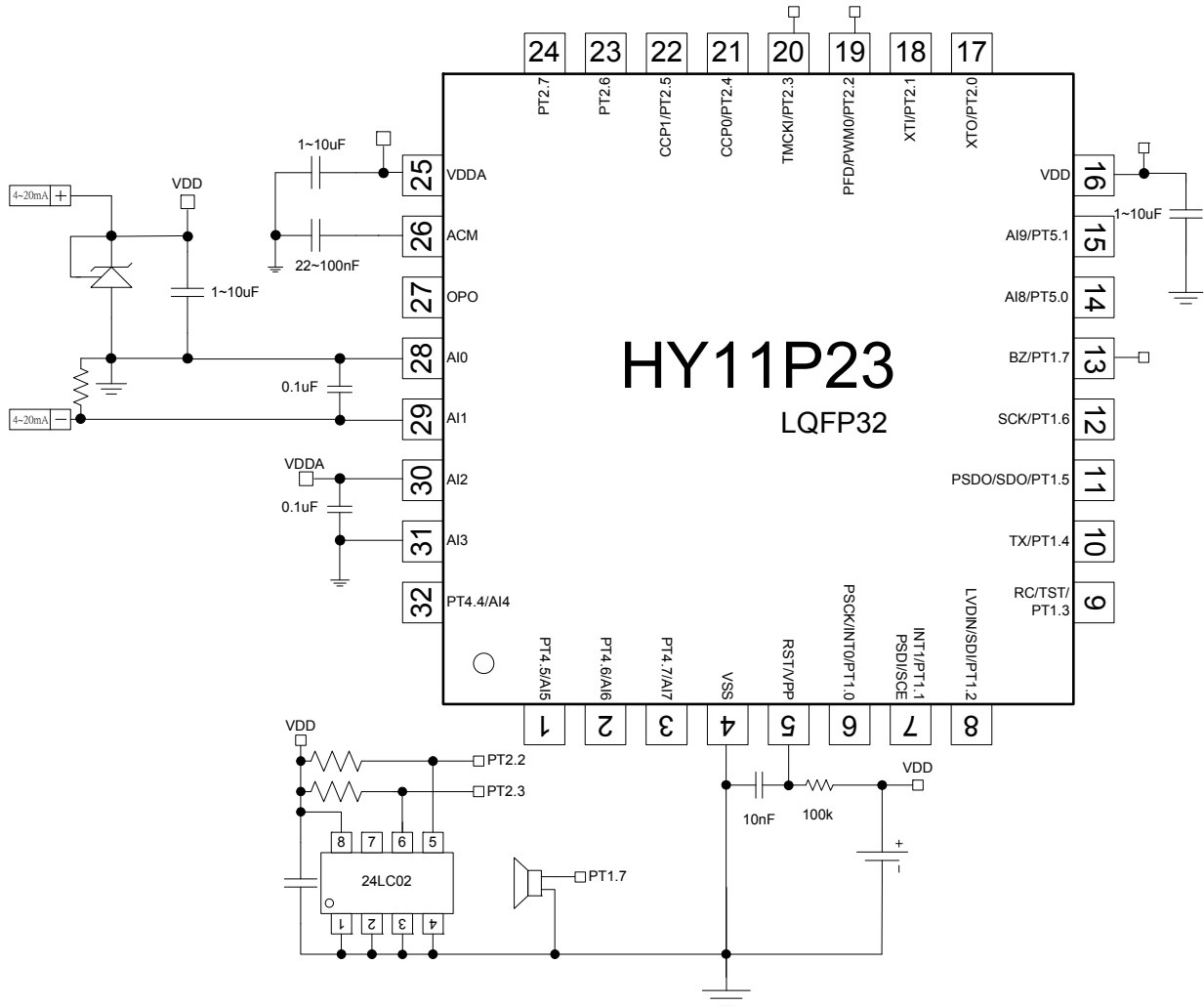
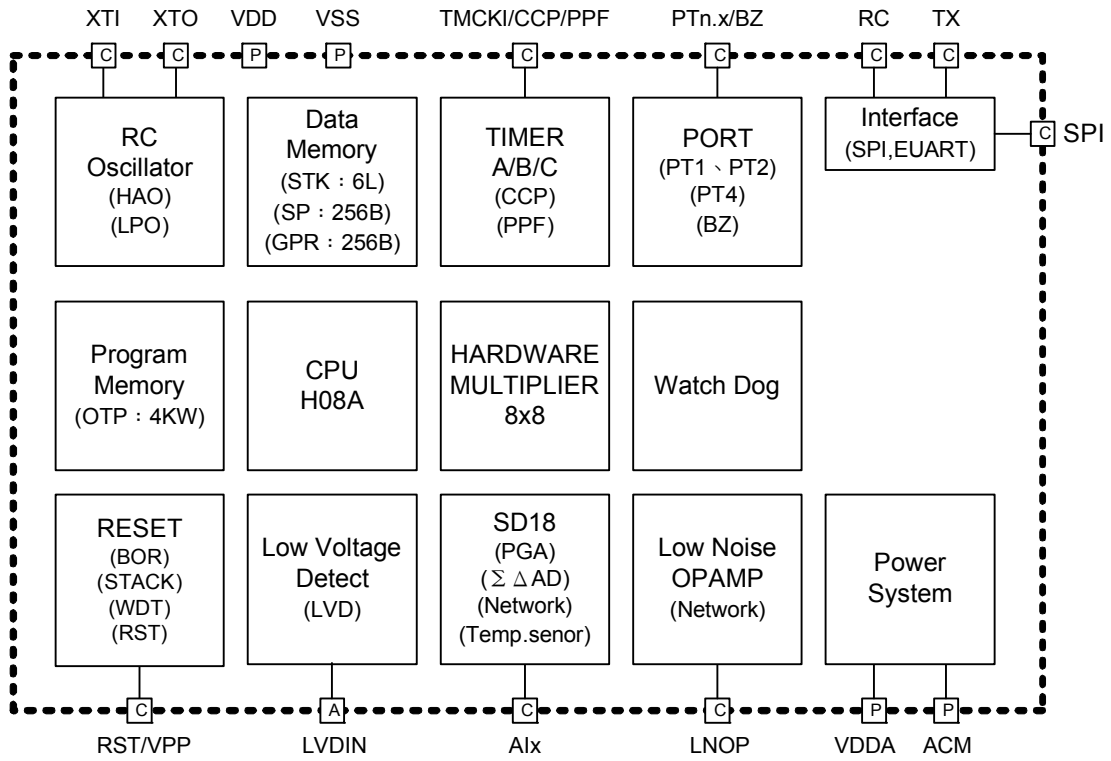


Figure 3-3 4-20mA Panel Meter that Unneeded to Connect External Power Supply

4. Function Outline

4.1 Internal Block Diagram



[P] Power Pad [D] Digital Pad [A] Analog Pad [C] Common I/O Pad

Figure 4-1 HY11P23 Internal Block Diagram

4.2 Related Description and Supporting Document

IC Function Related Operating Instruction

DS-HY11P23-Vxx	HY11P23 Data Sheet
UG-HY11S14-Vxx	HY11P Series Users' Manual
APD-CORE002-Vxx	H08A Instruction Description

Development Tool Related Operating Instruction

APD-HYIDE006-Vxx	HY11xxx Series Development Tool Software Instruction Manual
APD-HYIDE005-Vxx	HY11xxx Series Development Tool Hardware Instruction Manual
APD-OTP001-Vxx	OTP Products Programming Pin Manual

Product Production Related Operating Instruction

APD-HYIDE004-Vxx	HY1xxxx Series Production Line Specialized Programmer Manual
BDI-HY11P23-Vxx	HY11P23 Individual Product Die Bonding Information

4.3 SD18 Network

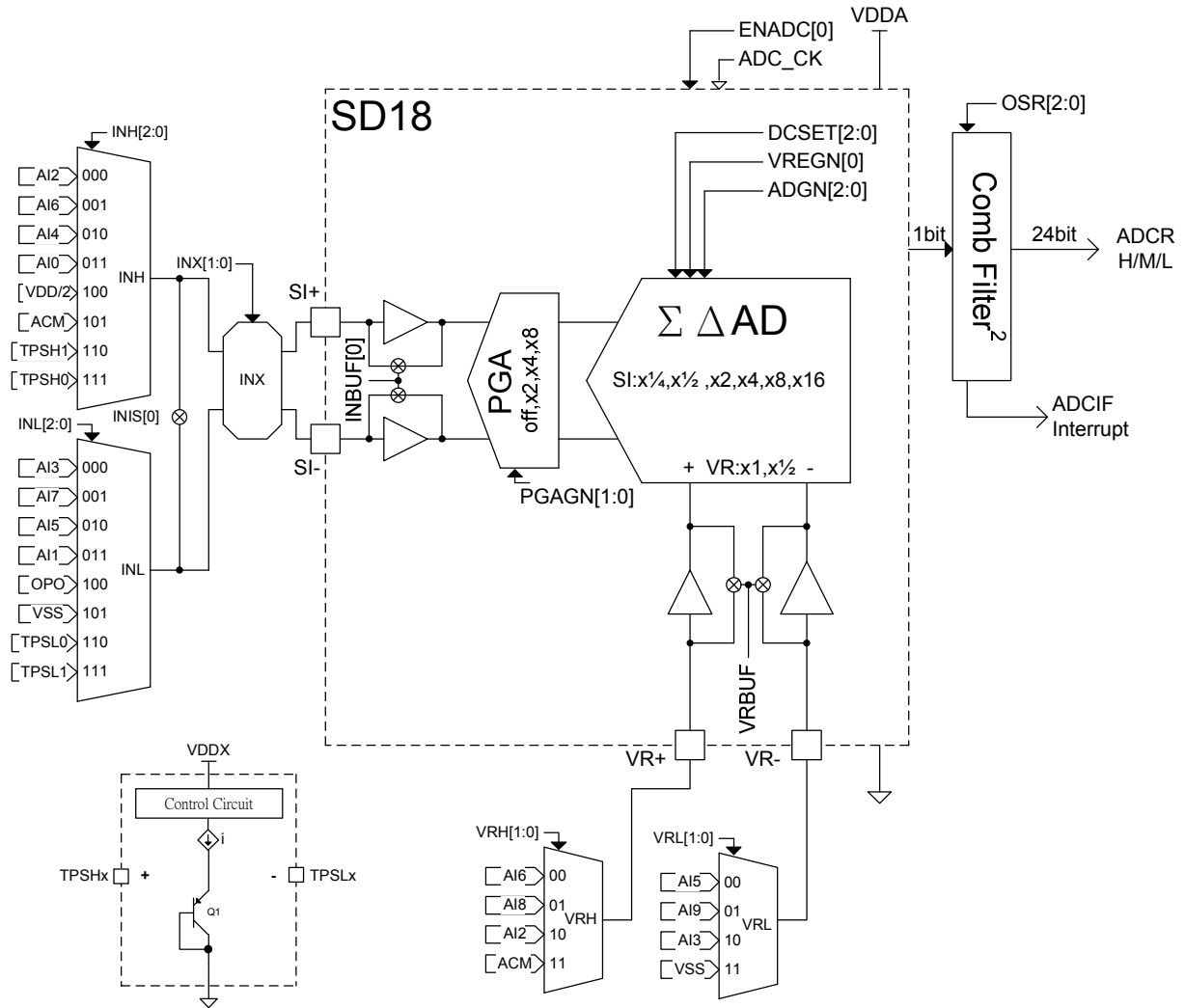


Figure 4-2 SD18 Network

4.4 Low Noise OPAMP Network

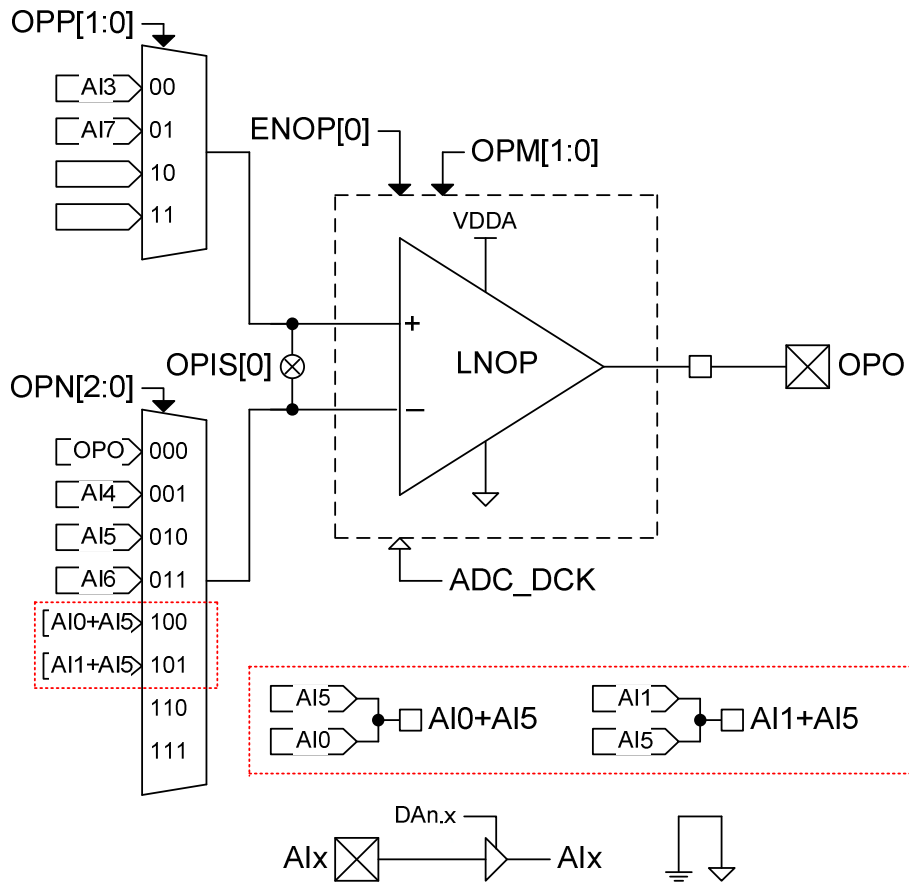


Figure 4-3 Low Noise OPAMP Network

5. Register List

“.”no use,“*”read/write,“w”write,“r”read,“r0”only read 0,“r1”only read 1,“w0”only write 0,“w1”only write 1 “.”unimplemented bit,“x”unknown,“u”unchanged,“d”depends on condition														
Address	File Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A-RESET	i-RESET	R/W		
00H	INDF0	Contents of FSR0 to address data memory value of FSR0 not changed								N/A	N/A	*****		
01H	POINC0	Contents of FSR0 to address data memory value of FSR0 post-incremented								N/A	N/A	*****		
02H	PODEC0	Contents of FSR0 to address data memory value of FSR0 post-decremented								N/A	N/A	*****		
03H	PRINC0	Contents of FSR0 to address data memory value of FSR0 pre-incremented								N/A	N/A	*****		
04H	PLUSW0	Contents of FSR0 to address data memory value of FSR0 offset by W								N/A	N/A	*****		
05H	INDF1	Contents of FSR1 to address data memory value of FSR0 not changed								N/A	N/A	*****		
06H	POINC1	Contents of FSR1 to address data memory value of FSR0 post-incremented								N/A	N/A	*****		
07H	PODEC1	Contents of FSR1 to address data memory value of FSR0 post-decremented								N/A	N/A	*****		
08H	PRINC1	Contents of FSR1 to address data memory value of FSR0 pre-incremented								N/A	N/A	*****		
09H	PLUSW1	Contents of FSR1 to address data memory value of FSR0 offset by W								N/A	N/A	*****		
0FH	FSR0H									FSR0[8]xu	*****	
10H	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*****		
11H	FSR1H									FSR1[8]xu	*****	
12H	FSR1L	Indirect Data Memory Address Pointer 1 Low Byte,FSR1[7:0]								xxxx xxxx	uuuu uuuu	*****		
16H	TOSH					TOS[11]	TOS[10]	TOS[9]	TOS[8]00000000	*****		
17H	TOSL	Top-of-Stack Low Byte (TOS<7:0>)												
18H	STKPTR	STKFL	STKUN	STKOV				STKPRT[2]	STKPRT[1]	STKPRT[0]	000...000	000...000	r,rw0,rw0,-,r,r,r	
1AH	PCLATH					PC[11]	PC[10]	PC[9]	PC[8]00000000	*****		
1BH	PCLATL	PC Low Byte for PC<7:0>												
1DH	TBLPTRH					TBLPTR[11]	TBLPTR[10]	TBLPTR[9]	TBLPTR[8]00000000	*****		
1EH	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)												
1FH	TBLDH	Program Memory Table Latch High Byte												
20H	TBLDL	Program Memory Table Latch Low Byte												
21H	PRODH	Product Register of Multiply High Byte												
22H	PRODL	Product Register of Multiply Low Byte												
23H	INTE1	GIE	ADCIE	TMCIE	TMBIE	TMAIE	WDTIE	E1IE	E0IE	0000 0000	0000 0000	*****		
24H	INTE2	TXIE	RCIE				SSPIE	CCP1IE	CCP0IE000000	*****		
26H	INTF1			ADCIF	TMCIF	TMBIF	TMAIF	WDTIF	E1IF	E0IF	.000 0000	.000 0000	*****	
27H	INTF2	TXIF	RCIF				SSPIF	CCP1IF	CCP0IF000000	*****		
29H	WREG	Working Register												
2AH	BSRCN									BSR[0]00	*****	
2BH	STATUS					C	DC	N	OV	Z	...x xxxx	...u uuuu	*****	
2CH	PSTATUS	PD	TO	IDLEB	BOR	SKERR			000d.0..	uduu .d..	rw0,rw0,rw0,rw0,-,-			
2DH	LVDON	LVDFG		LVD	LVDON	VLDX[3:0]			.000 0000	.000 0000	*****			
30H	PWRCN	ENVDDA	VDDAX[1:0]		ENACM				0000	0000	*****			
31H	MCKCN1	ADCS[2:0]			ADOCK	XTHSP	XTSP	ENXT	ENHAO	0000 0001	0000 0001	*****		
32H	MCKCN2			LSCK	HSCK	HSS[1:0]		CPUCK[1:0]	.00 0000	.00 0000	*****			
33H	MCKCN3					PERCK	BZS[2:0]		00000000	*****		
37H	OPCN1	ENOP	OPM[1:0]		OPP[1:0]		OPN[2:0]			0000 0000	0000 0000	*****		
39H	ADCRH	ADC conversion memory HighByte												
3AH	ADCRM	ADC conversion memory Middle Byte												
3BH	ADCRL	ADC conversion memory Low Byte												
3CH	ADCCN1	ENADC	ENHIGN	ENCHP	PGAGN[1:0]			ADGN[2:0]			0000 0000	0000 0000	*****	
3DH	ADCCN2				INBUF	VRBUF	VREGN	DCSET[2:0]			.00 0000	.00 0000	*****	
3EH	ADCCN3	OSR[2:0]												
3FH	AINET1	INH[2:0]			INL[2:0]			INIS	OPIS	0000 0000	0000 0000	*****		
40H	AINET2	VRH[1:0]			INX[1:0]		VRL[1:0]			.000 000.	.000 000.	*****		
41H	TMACN	ENTMA	TMACK	TMAS[1:0]		ENWDT	WDT[2:0]			0000 0000	0000 0000	**** w1,***		
42H	TMAR	TimerA data register												
43H	TMBCN	ENTMB	TMACK	TMBS[1:0]		TMBSYC	TMBR2R			0000 00..	0000 00..	*****		
44H	TMBRH	TimerB High Byte data register												
45H	TMBRL	TimerB Low Byte data register												
46H	TMCCN	ENTMC	TMCCK[1:0]		TMCS1[2:0]		TMCS0[1:0]			0000 0000	0000 0000	*****		
47H	PRC	TimerC programmable register												
48H	TMCR	TimerC register												
49H	CCPCN	CCP1M[3:0]					CCP0M[3:0]					0000 0000	0000 0000	*****
4AH	CCPORH	CCP0 High Byte data register												
4BH	CCP0RL	CCP0 Low Byte data register												
4CH	CCP1RH	CCP1 High Byte data register												
4DH	CCP1RL	CCP1 Low Byte data register												
4EH	PASC	PASF	PASC[1:0]							0.00	0.00	*****		
4FH	PWMCN	ENPWM	ENPFD	PWMRL[1:0]							0000	0000	*****	
51H	PWMR	PWM MSB Byte register												

Table 5-1(a) HY11P23 Register List

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Embedded 18-Bit Σ ADC 8-Bit RISC-Like Mixed Signal Microcontroller



"..."no use, "w"read/write, "w"write, "r"read, "r0"only read 0, "r1"only read 1, "w0"only write 0, "w1"only write 1
"..."unimplemented bit, "x"unknown, "u"unchanged, "d"depends on condition

Address	File Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A-RESET	I-RESET	R/W		
5EH	SSPCON1	SSPEN	CKP	CKE	SMP	—	—	SSPM<1:0>		0000 ..00	uuuu ..uu	***r***		
60H	SSPSTA	SSPBUY	SSPOV							BF	00...0	00...0	r,r,r,r,r,r,r	
61H	SSPBUF	SSP Receive Buffer/Transmit Register												
63H	URCON	ENSP	ENTX	TX9	TX9D	PARITY			WUE	0000 0..0	0000 0..0	***r***		
64H	URSTA		RC9D	PERR	FERR	OERR	RCIDL	TRMT	ABDOVF	.000 0110	.000 0110	-r,r,r,r,r,r,rw0		
65H	BAUDCON					ENCR	RC9	ENADD	ENABD 0000 0000	-r,r,r,r,r,r,r		
66H	BRGRH	Baud Rate Generator Register High Byte												
67H	BRGRL	Baud Rate Generator Register Low Byte												
68H	TXREG	UART Transmit Register												
69H	RCREG	UART Receive Register												
6AH	PT4	PT4.7	PT4.6	PT4.5	PT4.4							xxxx	uuuu	r,r,r,r,r,r,r,r
6BH	PT4DA	DA4.7	DA4.6	DA4.5	DA4.4							1111	1111	***r***
6CH	PT4PU	PU4.7	PU4.6	PU4.5	PU4.4							0000	0000	***r***
6DH	PT1	PT1.7	PT1.6	PT1.5	PT1.4	PT1.3	PT1.2	PT1.1	PT1.0	xxxx xxxx	uuuu uuuu	***r,r,r,r,r		
6EH	TRISC1	TC1.7	TC1.6	TC1.5	TC1.4							0000	0000	***r***
6FH	PT1DA							DA1.2		 0.. 0..	-r,r,r,r,r,r,-	
70H	PT1PU	PU1.7	PU1.6	PU1.5	PU1.4	PU1.3	PU1.2	PU1.1	PU1.0	0000 0000	0000 0000	***r***		
71H	PT1M1					INTEG1[1:0]		INTEG0[1:0]			 0000 0000	-r,r,r,r,r,r,-
72H	PT1M2		PM1.7[0]		PM1.6[0]		PM1.5[0]		PM1.4[0]	.0.0 .0.0	.0.0 .0.0	-r,r,r,r,r,r,-		
74H	PT2	PT2.7	PT2.6	PT2.5	PT2.4	PT2.3	PT2.2	PT2.1	PT2.0	xxxx xxxx	uuuu uuuu	***r***		
75H	TRISC2	TC2.7	TC2.6	TC2.5	TC2.4	TC2.3	TC2.2	TC2.1	TC2.0	0000 0000	0000 0000	***r***		
77H	PT2PU	PU2.7	PU2.6	PU2.5	PU2.4	PU2.3	PU2.2	PU2.1	PU2.0	0000 0000	0000 0000	-r,r,r,r,r,r,-		
78H	PT2M1			PM2.2[1]	PM2.2[0]							..0000	***r***
79H	PT2M2	PWMTR[1:0]					PM2.5[1]	PM2.5[0]	PM2.4[1]	PM2.4[0]	00.. 0000	00.. 0000	***r***	
192H	PT5								PT5.1	PT5.0xxuu	-r,r,r,r,r,r,f	
193H	PT5DA								DA5.1	DA5.01111	-r,r,r,r,r,r,f	
194H	PT5PU								PU5.1	PU5.00000	-r,r,r,r,r,r,f	
80H ~ FFH		GENERAL PURPOSE REGISTER @ 128Byte								xxxx xxxx	uuuu uuuu	***r***		
100H~17FH		GENERAL PURPOSE REGISTER @ 128Byte								xxxx xxxx	uuuu uuuu	***r***		

Table 5-1(b) HY11P23 Register List (continued)

6. Electrical Characteristics

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at V_{DD} to V_{SS}	-0.2 V to 4.0 V
Voltage applied to any pin	-0.2 V to $V_{DD} + 0.3$ V
Voltage applied to RST/VPP pin	-0.2 V to 6.9 V
Voltage applied to TST/PT1.3 pin	-0.2 V to $V_{DD} + 1$ V
Diode current at any device terminal	± 2 mA
Storage temperature, Tstg: (unprogrammed device)	-55°C to 150°C
(programmed device)	-40°C to 85°C
Total power dissipation	0.5w
Maximum output current sink by any PORT1 to PORT3 I/O pin25mA

6.1 Recommended Operating Conditions

$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$, unless otherwise noted

Sym.	Parameter		Test Conditions	Min.	Typ.	Max.	unit
V_{DD}	Supply Voltage		All digital peripherals and CPU	2.2		3.6	V
			Analog peripherals	2.4		3.6	
V_{SS}	Supply Voltage			0		0	
XT	External	Watch crystal	$V_{DD} = 2.2\text{V}$, ENXT[0]=1			32.768K	Hz
	Oscillator	Ceramic resonator			450K	8M	
	Frequency	Crystal			1M	8M	

6.2 Internal RC Oscillator

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1	1.7	2.0	2.3	MHz
LPO	Low Power Oscillator frequency	V_{DD} supply voltage be enable LPO	22	28	35	KHz

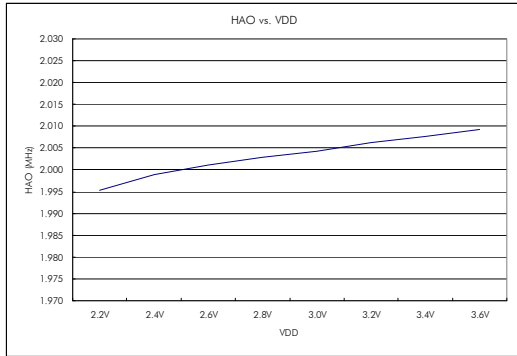


Figure 6.2-1 HAO vs. VDD

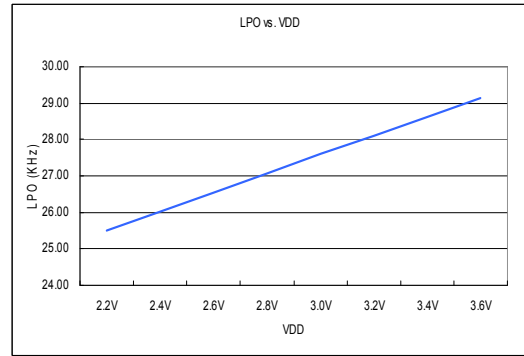


Figure 6.2-2 LPO vs. VDD

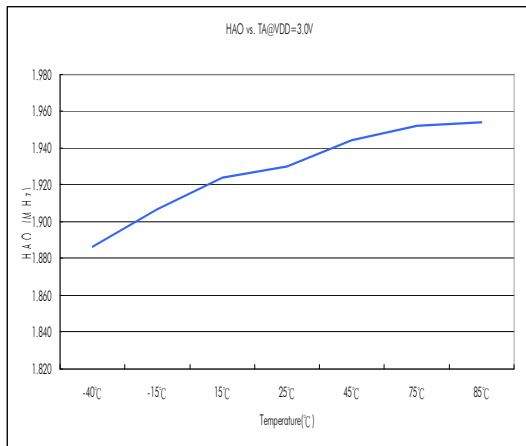


Figure 6.2-3 HAO vs. Temperature

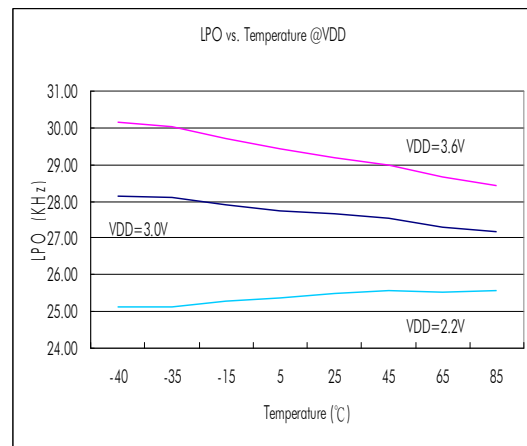


Figure 6.2-4 LPO vs. Temperature

6.3 Supply Current into VDD Excluding Peripherals Current

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, \text{OSC_LPO} = 28\text{KHz}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM1}	Active mode 1	OSC_CY = 8MHz, OSC_HAO = off, CPU_CK = 8MHz		1.2	2	mA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 2MHz		0.32	0.55	mA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 1MHz		0.18	0.3	mA
I_{LP1}	Low Power 1	OSC_CY = 32768Hz, OSC_HAO = off, CPU_CK = 16384Hz		7	12	uA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		1.65	3	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.65	1.2	uA

OSC_CY : External Oscillator frequency.

OSC_HAO : Internal High Accuracy Oscillator frequency.

CPU_CK : CPU core work frequency.

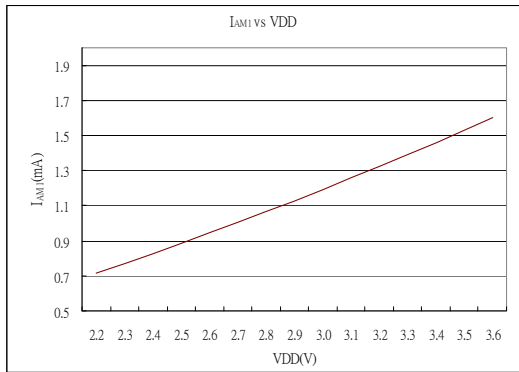


Figure 6.3-1 I_{AM1} vs. VDD

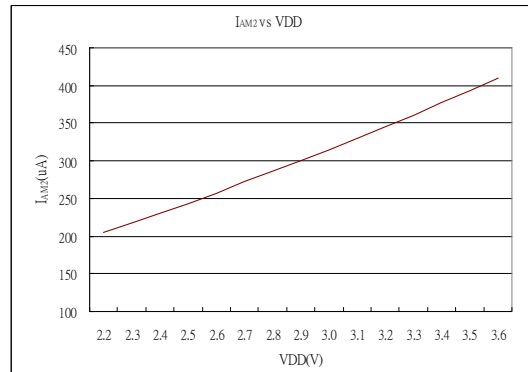


Figure 6.3-2 I_{AM2} vs. VDD

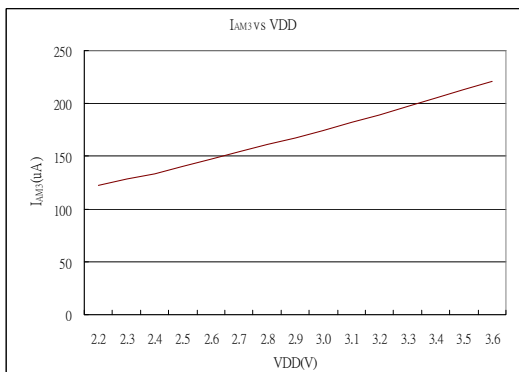


Figure 6.3-3 I_{AM3} vs. VDD

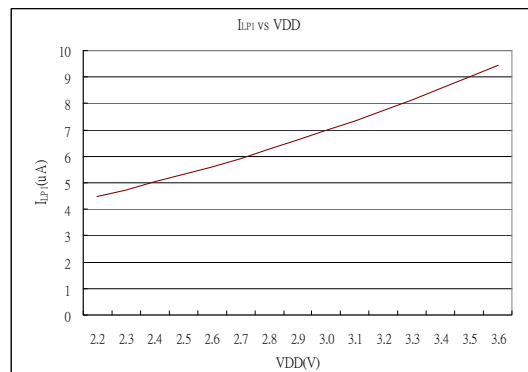


Figure 6.3-4 I_{LP1} vs. VDD

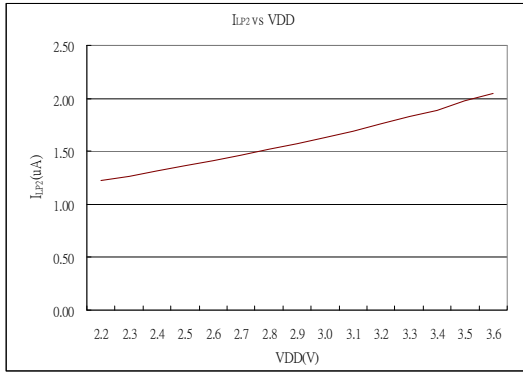


Figure 6.3-5 I_{LP2} vs. VDD

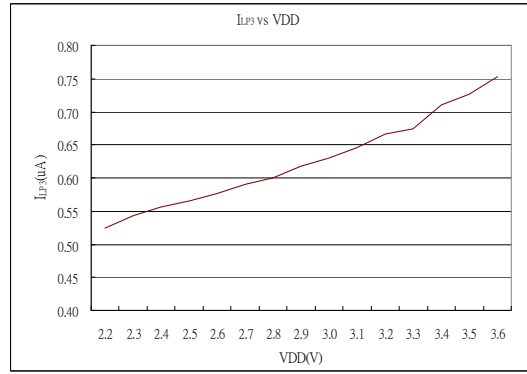


Figure 6.3-6 I_{LP3} vs. VDD

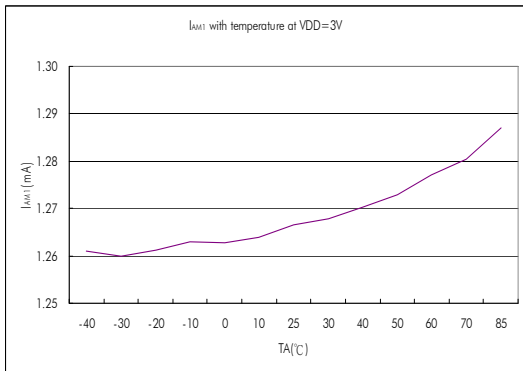


Figure 6.3-7 I_{AM1} vs. Temperature

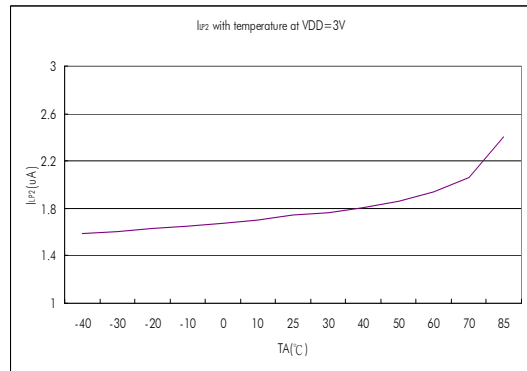


Figure 6.3-8 I_{LP2} vs. Temperature

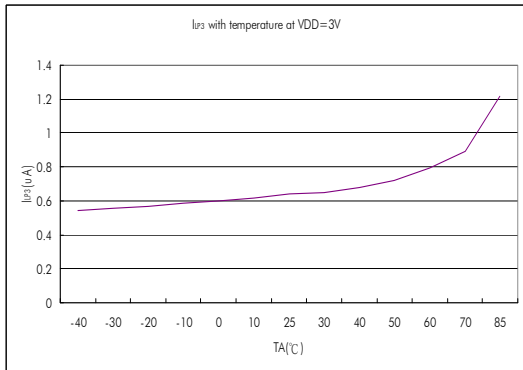


Figure 6.3-9 I_{LP3} vs. Temperature

6.4 Port 1~5

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				2.1	V
V_{IL}	Low-Level input voltage		0.9			
V_{hys}	Input Voltage hysteresis($V_{IH} - V_{IL}$)			0.8		V
I_{LKG}	Leakage Current				0.1	μA
R_{PU}	Port pull high resistance			180		$\text{k}\Omega$
Output voltage and current and frequency						
V_{OH}	High-level output voltage	$I_{OH}=10\text{mA}$	$V_{DD}-0.3$			V
V_{OL}	Low-level output voltage	$I_{OL}=-10\text{mA}$			$V_{SS}+0.3$	

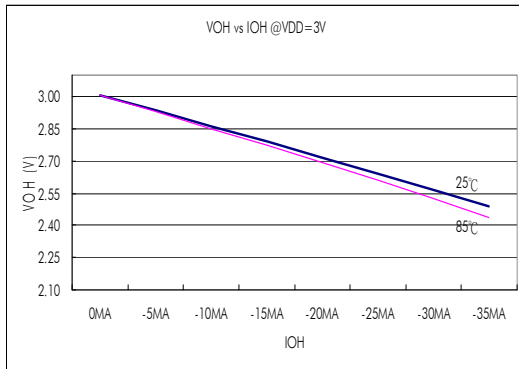


Figure 6.4-1 V_{OH} vs. I_{OH} @ $V_{DD}=3.0\text{V}$

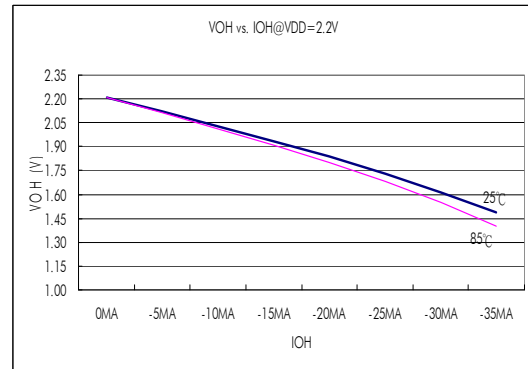


Figure 6.4-2 V_{OH} vs. I_{OH} @ $V_{DD}=2.2\text{V}$

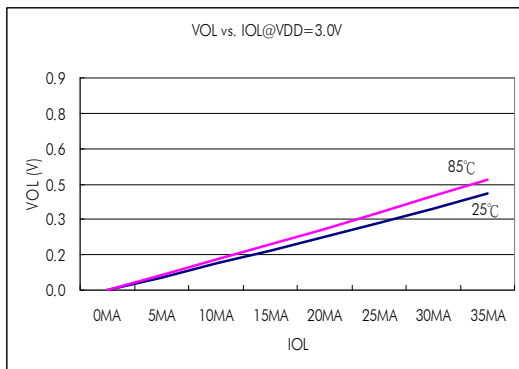


Figure 6.4-3 V_{OL} vs. I_{OL} @ $V_{DD}=3.0\text{V}$

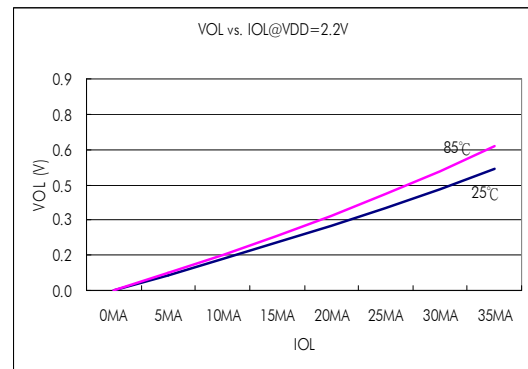


Figure 6.4-4 V_{OL} vs. I_{OL} @ $V_{DD}=2.2\text{V}$

6.5 Reset (Brownout, External RST Pin, Low Voltage Detect)

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit	
BOR	Pulse length needed to accepted reset internally, t_{d-LVR}		2			us	
	V_{DD} Start Voltage to accepted reset internally (L→H), V_{LVR}		1.6	1.85	2.1	V	
	Hysteresis, $V_{HYS-LVR}$			70		mV	
RST	Pulse length needed as RST/VPP pin to accepted reset internally, t_{d-RST}		2			us	
	Input Voltage to accepted reset internally		0.9			V	
	Hysteresis, $V_{HYS-RST}$			0.8		V	
LVD	Operation current, I_{LVD}			10	15	uA	
	External input voltage to compare reference voltage			1.2		V	
	Compare reference voltage temperature drift	$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$		100		ppm/ $^\circ\text{C}$	
	Detect V_{DD} voltage rang by user option, $V_{LVD} VLDx[3:0]=1110b$			3.3		V	
	Detect V_{DD} voltage rang by user option, $V_{LVD} VLDx[3:0]=1101b$			3.2			
	Detect V_{DD} voltage rang by user option, $V_{LVD} VLDx[3:0]=1100b$			3.1			
	Detect V_{DD} voltage rang by user option, $V_{LVD} VLDx[3:0]=1011b$			3.0			
	Detect V_{DD} voltage rang by user option, $V_{LVD} VLDx[3:0]=1010b$			2.9			
	Detect V_{DD} voltage rang by user option, $V_{LVD} VLDx[3:0]=1001b$			2.8			
	Detect V_{DD} voltage rang by user option, $V_{LVD} VLDx[3:0]=1000b$			2.7			
	Detect V_{DD} voltage rang by user option, $V_{LVD} VLDx[3:0]=0111b$			2.6			
	Detect V_{DD} voltage rang by user option, $V_{LVD} VLDx[3:0]=0110b$			2.5			
	Detect V_{DD} voltage rang by user option, $V_{LVD} VLDx[3:0]=0101b$			2.4			
	Detect V_{DD} voltage rang by user option, $V_{LVD} VLDx[3:0]=0100b$			2.3			
	Detect V_{DD} voltage rang by user option, $V_{LVD} VLDx[3:0]=0011b$			2.2			
	Detect V_{DD} voltage rang by user option, $V_{LVD} VLDx[3:0]=0010b$			2.1			
	Detect V_{DD} voltage rang by user option, $V_{LVD} VLDx[3:0]=0001b$			2.0			
BOR : Brownout Reset LVR : Low Voltage Reset of BOR LVD : Low Voltage Detect RST : External Reset pin							

HY11P23

Embedded 18-Bit $\Sigma\Delta$ ADC
8-Bit RISC-Like Mixed Signal Microcontroller

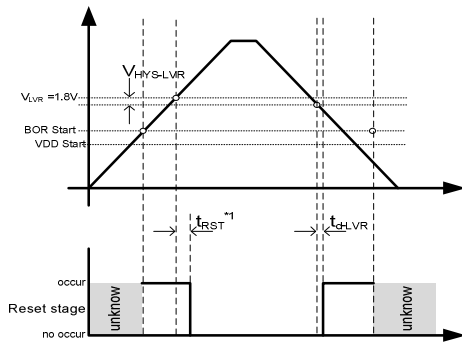


Figure 6.5-1 BOR Reset Diagram

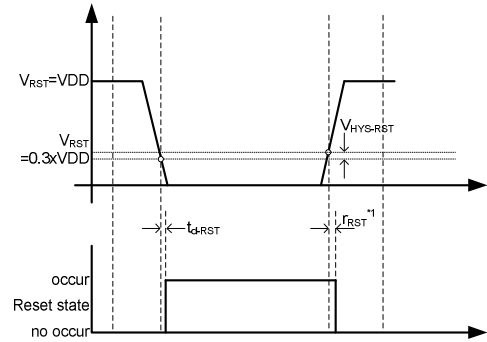


Figure 6.5-2 RST Reset Diagram

*1 t_{RST} : Please see BOR Introduce of HY11Pxx series User's Guide (UG-HY11S14-Vxx).

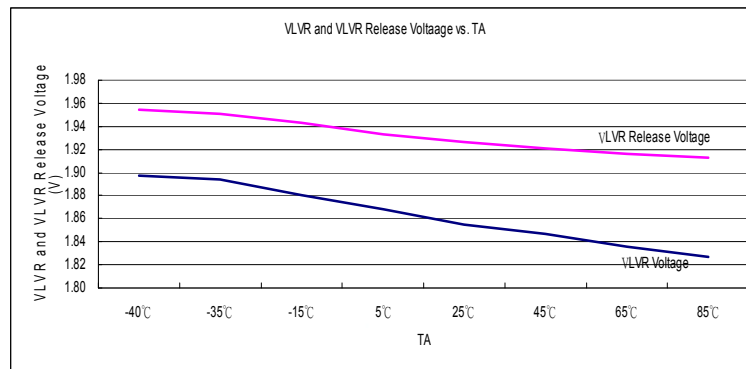


Figure 6.5-3 LVR vs. Temperature

6.6 Power System

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
VDDA	VDDA operation current, I_{VDDA}	$I_L = 0\text{mA}$	VDDAX[1:0]=00b	22			μA
	Select VDDA output voltage	$I_L = 0.1\text{mA}$, $V_{DD} \geq V_{VDDA} + 0.2\text{V}$	VDDAX[1:0]=00b	3.3			V
			VDDAX[1:0]=01b	2.9			V
			VDDAX[1:0]=10b	2.6			V
			VDDAX[1:0]=11b	2.4			V
	Dropout voltage	$I_L = 10\text{mA}$	VDDAX[1:0]=00b	135			mV
			VDDAX[1:0]=01b	150			mV
			VDDAX[1:0]=10b	165			mV
VDDAX[1:0]=11b			180			mV	
Temperature drift	VDDAX[1:0]=11b	$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$	50			ppm/ $^\circ\text{C}$	
V_{DD} Voltage drift	$I_L = 0.1\text{mA}$	$V_{DD} = 2.5\text{V} \sim 3.6\text{V}$	± 0.2			%/V	
ACM	ACM operation current, I_{ACM}	$I_L = 0\text{mA}$		20			μA
	Output voltage, V_{ACM}	ENACM[0]=1, ^{*1}	$I_L = 0\mu\text{A}$	1.0			V
	Output voltage with Load		$I_L = \pm 200\mu\text{A}$	0.98	1.02		V_{ACM}
	Output voltage, V_{ACM}	ENACM[0]=1, ^{*2}	$I_L = 0\mu\text{A}$	1.2			V
	Output voltage with Load		$I_L = \pm 200\mu\text{A}$	0.98	1.02		V_{ACM}
	Temperature drift	ENACM[0]=1,	$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$	50			ppm/ $^\circ\text{C}$
	V_{DDA} Voltage drift	$I_L = 10\mu\text{A}$		100			$\mu\text{V}/\text{V}$

VDDA : Adjust Voltage Regulator
ACM : Analog Common Mode Voltage

*1: $V_{ACM} = 1.0\text{V}$ is just for VDDAX[1:0]=1xb mode. (at A/D differential voltage reference < 1.4V)
*2: $V_{ACM} = 1.2\text{V}$ is just for VDDAX[1:0]=0xb mode. (at A/D differential voltage reference > 1.4V)

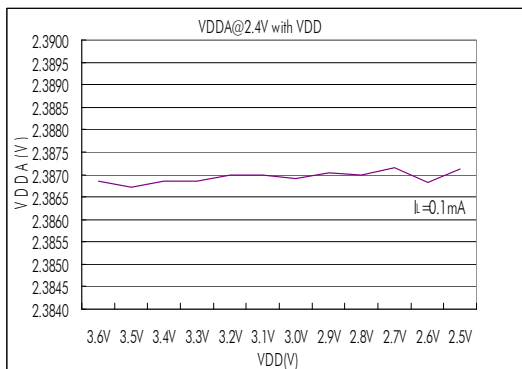


Figure 6.6-1 VDDA $I_L=0.1\text{mA}$ vs. VDD

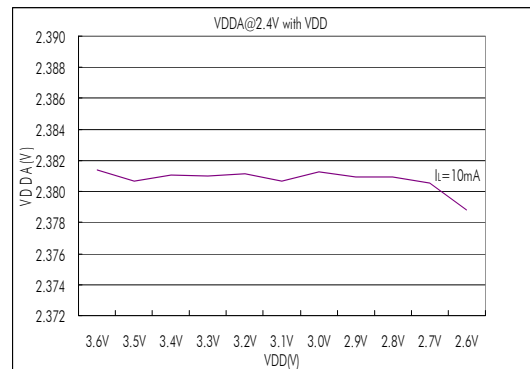


Figure 6.6-2 VDDA $I_L=10\text{mA}$ vs. VDD

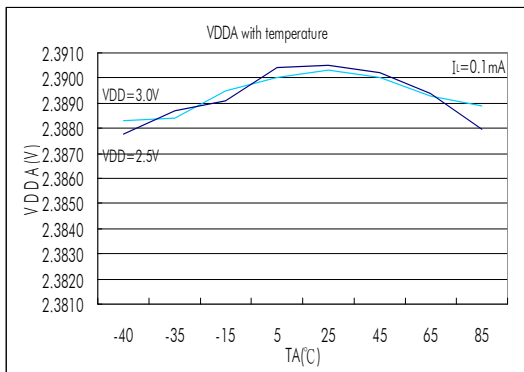


Figure 6.6-3 VDDA $I_L=0.1\text{mA}$ vs. Temperature

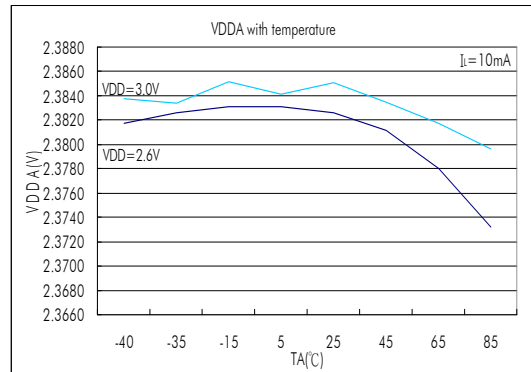


Figure 6.6-4 VDDA $I_L=10\text{mA}$ vs. Temperature

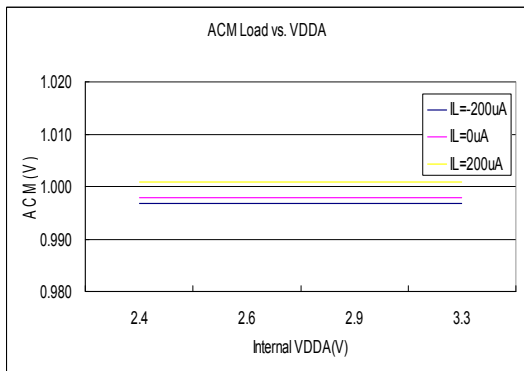


Figure 6.6-5 ACM Load vs. VDDA (a)

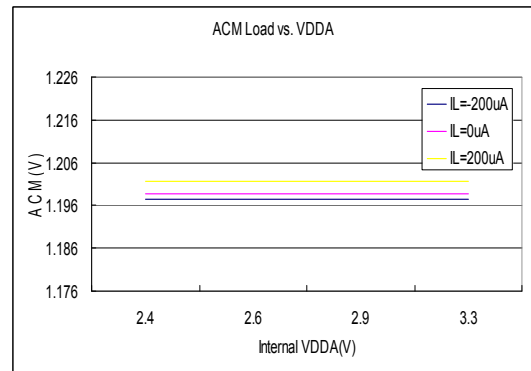


Figure 6.6-5 ACM Load vs. VDDA (b)

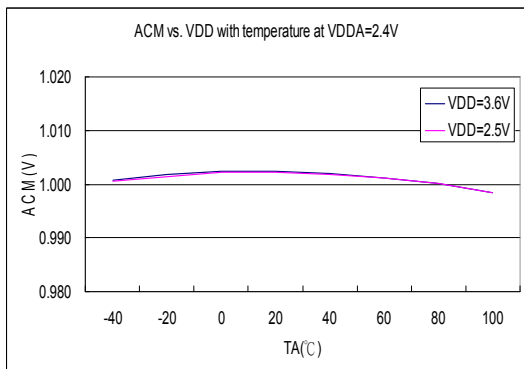


Figure 6.6-6 ACM vs. Temperature (a)

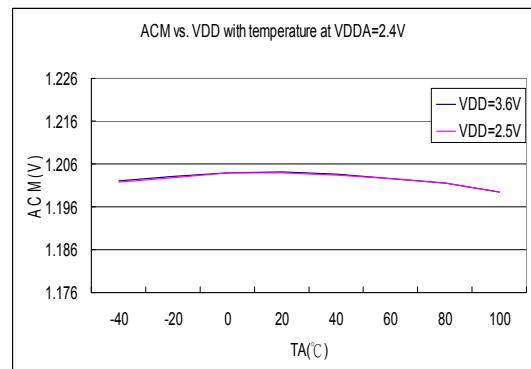


Figure 6.6-6 ACM vs. Temperature (b)

6.7 Low Noise OPAMP

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA}=2.4\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{LNOP}	Supply voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
I_{LNOP}	Operation supply current		OPM[1:0]=xxb		200		μA
V_{OS-OP}	Input offset voltage without chopper.		OPM[1:0]=1xb	-2		2	mV
	Input offset voltage with chopper		OPM[1:0]=0xb		20		μV
	Input offset voltage temperature drift.	OPM[1:0]=00b OPM[1:0]=10	$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$		0.1 2		$\mu\text{V}/^\circ\text{C}$
V_{OLR}	Unit gain load regulation	$V_O=1.2\text{V},$ $V_{DDA}=2.4\text{V}$	$I_L=+1\text{mA}$ $I_L=-1\text{mA}$		0.1		$\%V_O$
CMVR	Common-mode voltage input range		OPM[1:0]=xxb	0.1		$V_{DDA}-1.1$	V
CMRR	Common-mode rejection ratio		OPM[1:0]=xxb		90		dB

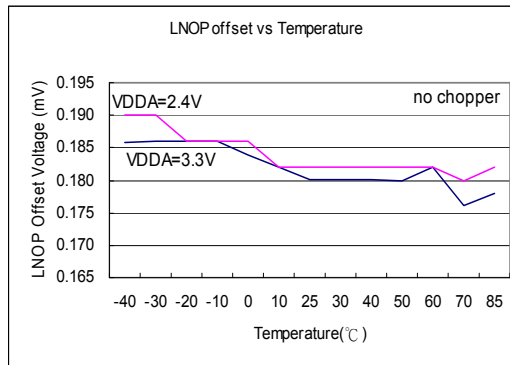


Figure 6.7-1 LNOP Offset Temperature

6.8 SD18, Power Supply and Recommended Operating Conditions

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA}=2.4\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{SD18}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
f_{SD18}	Modulator sample frequency, ADC_CK			25	250	300	KHz
	Over Sample Ratio, OSR			256		32768	
I_{SD18}	Operation supply current without PGA	ENADC[0]=1 INBUF[0]=1,VRBUF[0]=0	GAIN=4, ADC_CK=250KHz	168		uA	
		ENADC[0]=1 INBUF[0]=0,VRBUF[0]=1		150			
		ENADC[0]=1 INBUF[0]=0,VRBUF[0]=0		120			

6.8.1 PGA, Power Supply and Recommended Operating Conditions

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA}=2.4\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{PGA}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
I_{PGA}	Operation supply current	PGAGN[1:0]=<01>or<1x>			320		uA
G_{PGA}	Gain temperature drift	$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$	GAIN=128		5		ppm/°C

6.8.2 SD18, Performance II ($f_{SD18}=250\text{KHz}$)

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA}=2.9\text{V}, V_{VR}=1.0\text{V}, \text{GAIN}=1$ without PGA, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
INL	Integral Nonlinearity(INL)	$V_{DDA}=2.4\text{V}, V_{VR}=1.0\text{V}, \Delta SI = \pm 200\text{mV}$		± 0.003		± 0.01	%FSR
		$V_{DDA}=2.4\text{V}, V_{VR}=1.0\text{V}, \Delta SI = \pm 450\text{mV}$					
	No Missing Codes ³	ADC_CK=250KHz, OSR[2:0]=010b		23			Bits
G_{SD18}	Temperature drift Gain 1~x16 (INBUF[0]=0b,) Gain 1~x4 (INBUF[0]=1b,)	INBUF[0]=0b,VRBUF[0]=0b	$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$	2		ppm/°C	
		INBUF[0]=1b,VRBUF[0]=0b					
		INBUF[0]=0b,VRBUF[0]=1b					
		INBUF[0]=1b,VRBUF[0]=1b					
E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper and Buffer(INBUF,VRBUF) without PGA	$\Delta AI=0\text{V}$ $\Delta VR=0.9\text{V}$ DCSET[2:0]=<000>	Gain=2	1		%FSR	
	Offset error of Full Scale Rang input voltage range with Chopper without PGA and Buffer(INBUF,VRBUF)	* ΔAI is external short	Gain=2	1			

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CM _{SD18}	Offset temperature drift with chopper without PGA and Buffer (INBUF,VRBUF).		GAIN=1	2	uV/°C
			GAIN=2	1	
			GAIN=4	0.5	
	Offset temperature drift with chopper and Buffer (INBUF,VRBUF) without PGA.		GAIN=1	2	
			GAIN=2	1	
			GAIN=4	0.5	
	Offset temperature drift with chopper without Buffer (INBUF,VRBUF).		GAIN=128	0.02	
CM _{SD18}	Common-mode rejection	V _{CM} =0.7V to 1.7V, V _{VR} =1.0V, without PGA	V _{SI} =0V, GAIN=1	90	dB
		V _{CM} =0.7V to 1.7V, V _{VR} =1.0V, without PGA	V _{SI} =0V, GAIN=16	75	
PSRR	DC power supply rejection	VDDA=3.0V, Δ VDDA= \pm 100mV, V _{VR} =1.0V, V _{SI} =1.2V, V _{SI} =1.2V,	GAIN=1 PGA=off	75	dB
			GAIN=16 PGA=8		

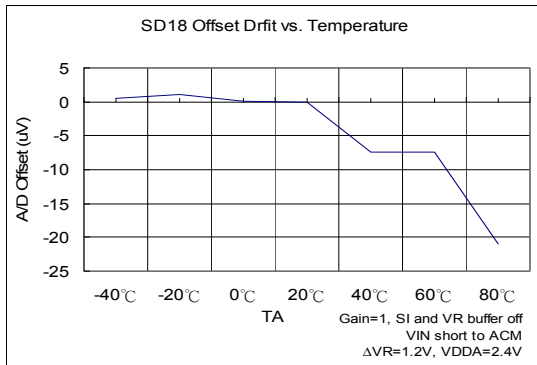


Figure 6.8-1(a) SD18 Offset Temperature Drift

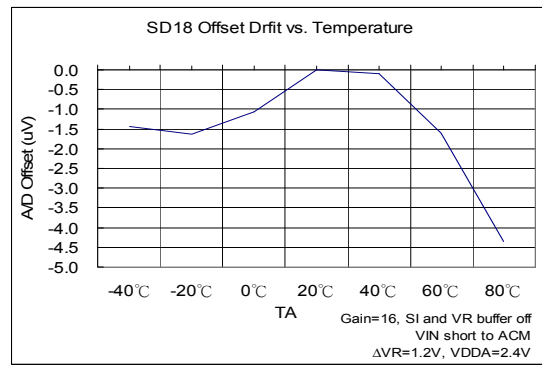


Figure 6.8-1(b) SD18 Offset Temperature Drift

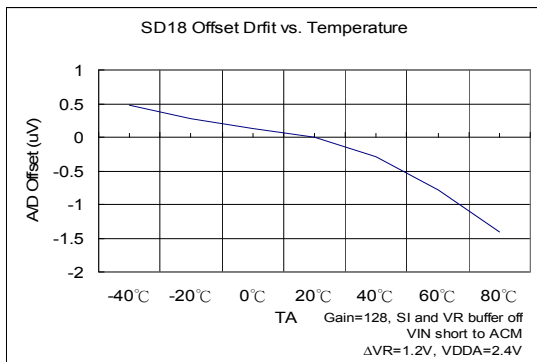


Figure 6.8-1I SD18 Offset Temperature Drift

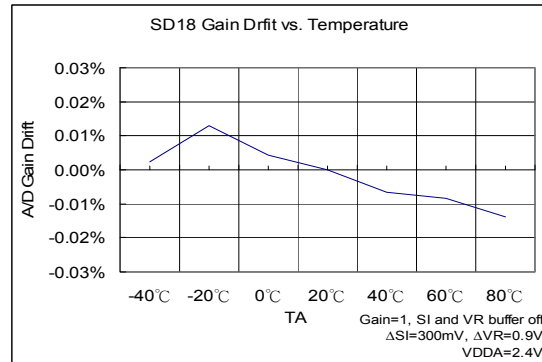


Figure 6.8-2(a) SD18 Gain Drift with Temperature

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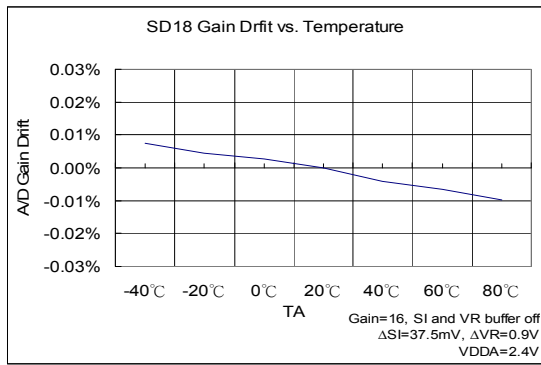


Figure 6.8-2(b) SD18 Gain Drift with Temperature

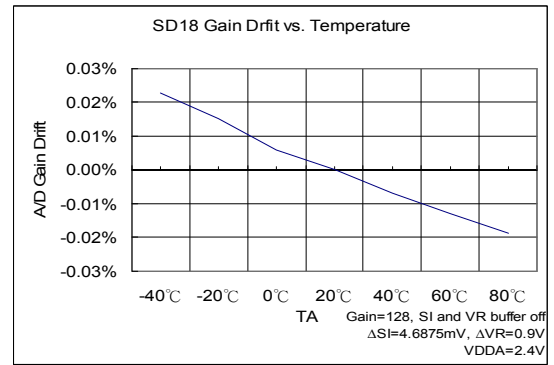


Figure 6.8-2(c) SD18 Gain Drift with Temperature

6.8.3 SD18, Temperature Sensor

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA} = 3.3\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
TC_S	Sensor temperature drift			178		$\mu\text{V}/^\circ\text{C}$
KT	Absolute Temperature Scale 0°K	INBUF[0]=1		-289		$^\circ\text{C}$
TC_{ERR}	One point calibrate error temperature	Calibration at 25°C of $-40^\circ\text{C}\sim 85^\circ\text{C}$		± 2		$^\circ\text{C}$

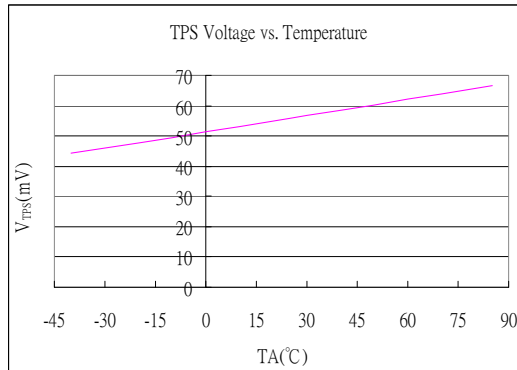


Figure 6.8-3 TPS Output Voltage vs. Temperature Drift

6.8.4 SD18 Noise Performance

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{V}$, $V_{DDA} = 2.4\text{V}$, unless otherwise noted

HY11P23 provides important input noise specification that aims at SD18. Table 6.8-4 (a) and Table 6.8-4 (b) lists out the relations of typical noise specification, Gain, Output rate, and maximum input voltage of single end. Test condition configuration and external input signal short, voltage reference: 1.2V and 1024 records were sampled.

ENOB(RMS) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V													
Max. Vin(mV) =0.9*VREF ⁽¹⁾	OSR					256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					977	488	244	122	61	31	15	8
	Gain	=	PGA	x	ADGN								
± 2400	0.25	=	1	x	0.25	16.3	17.4	17.9	18.5	19.0	19.5	20.0	20.4
± 2160	0.5	=	1	x	0.5	16.3	17.3	17.9	18.4	18.9	19.4	19.8	20.2
± 1080	1	=	1	x	1	16.2	17.2	17.8	18.3	18.8	19.3	19.7	20.1
± 540	2	=	1	x	2	16.1	17.1	17.6	18.2	18.7	19.2	19.6	20.0
± 270	4	=	1	x	4	16.0	16.9	17.5	18.0	18.5	18.9	19.4	19.8
± 135	8	=	1	x	8	15.9	16.6	17.2	17.7	18.2	18.7	19.2	19.6
± 68	16	=	1	x	16	15.6	16.3	16.8	17.3	17.7	18.3	18.8	19.3
± 34	32	=	2	x	16	14.8	15.3	15.9	16.4	16.9	17.4	17.8	18.3
± 17	64	=	4	x	16	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0
± 8	128	=	8	x	16	14.0	14.6	15.1	15.6	16.0	16.6	17.0	17.5

(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).

Table 6.8-4(a) SD18 ENOB Table

RMS Noise(uV) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V													
Max. Vin(mV) =0.9*VREF	OSR					256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					977	488	244	122	61	31	15	8
	Gain	=	PGA	x	ADGN								
± 2400	0.25	=	1	x	0.25	121.08	57.40	38.74	26.66	18.39	13.21	9.49	6.98
± 2160	0.5	=	1	x	0.5	61.63	29.23	19.21	13.51	9.78	7.02	5.12	3.91
± 1080	1	=	1	x	1	32.21	15.70	10.25	7.31	5.19	3.77	2.80	2.13
± 540	2	=	1	x	2	16.59	8.54	5.91	4.06	2.86	2.06	1.48	1.12
± 270	4	=	1	x	4	9.00	4.84	3.33	2.37	1.67	1.19	0.87	0.65
± 135	8	=	1	x	8	5.04	2.97	2.02	1.44	1.01	0.73	0.51	0.39
± 68	16	=	1	x	16	3.03	1.84	1.29	0.92	0.70	0.46	0.33	0.24
± 34	32	=	2	x	16	2.61	1.81	1.27	0.89	0.62	0.45	0.32	0.23
± 17	64	=	4	x	16	1.66	1.13	0.80	0.56	0.41	0.29	0.20	0.14
± 8	128	=	8	x	16	1.13	0.77	0.55	0.38	0.28	0.19	0.14	0.10

Table 6.8-4(b) SD18 RMS Noise Table

The RMS noise is referred to the input. The Effective Number of Bits (ENOB (RMS Bit)) is defined as:

$$\text{ENOB(RMS)} = \frac{\ln\left(\frac{\text{FSR}}{\text{RMS Noise}}\right)}{\ln(2)}$$

$$\text{RMS Noise} = \frac{\left(2 \times \text{VREF} \times \sqrt{\sum_{k=1}^{1024} (\text{ADO}[k] - \text{Average})^2}\right)}{2^{23}}$$

Where FSR (Full - Scale Range) = $2 \times \text{VREF}/\text{Gain}$.

$$\text{Average} = \frac{\sum_{k=1}^{1024} (\text{ADO}[k])}{1024}$$

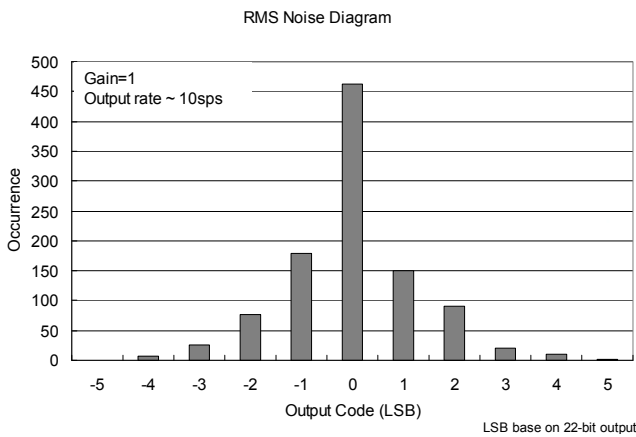


Figure 6.8-4(a) RMS Noise Diagram

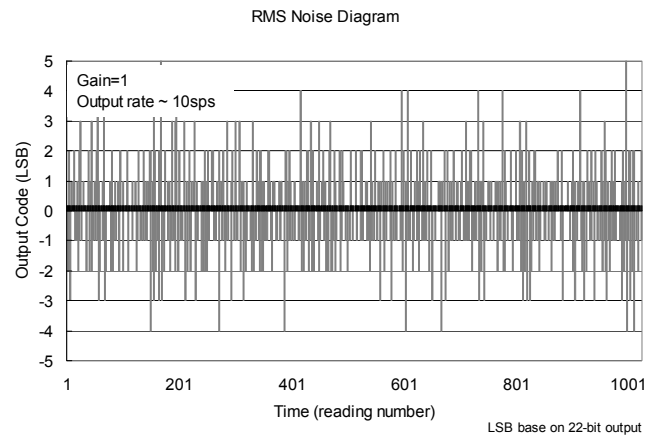


Figure 6.8-4(b) Output Code Diagram

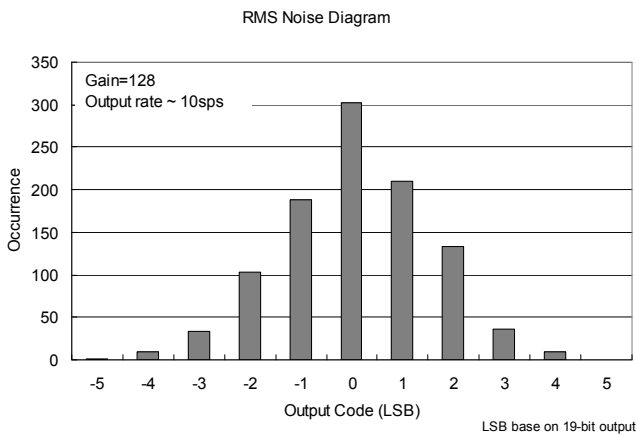


Figure 6.8-4(c) RMS Noise Diagram

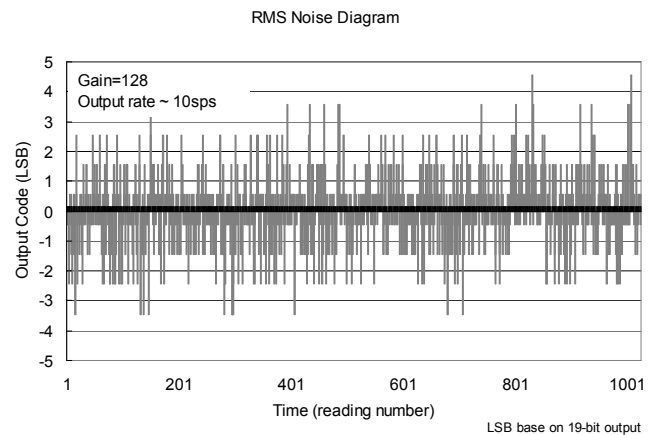


Figure 6.8-4(d) Output Code Diagram

7. Ordering Information

Device No. ¹	Package Type	Pins	Package Drawing		Code ²	Shipment Packing Type	Unit Q'ty	Material Composition	MSL ³
HY11P23-D000	Die	-	D	000	000	-	200	Green ⁴	-
HY11P23-L032	LQFP	32	L	032	000	Tray	250	Green ⁴	MSL-3
HY11P23-N032	QFN	32	N	032	000	Tray	490	Green ⁴	MSL-3
HY11P23-E028	SSOP	28	E	028	000	Tube	48	Green ⁴	MSL-3
HY11P23-E028	SSOP	28	E	028	000	Tape & Reel	2000	Green ⁴	MSL-3

¹ **Device No.:** Model No. – Package Type Description – Code (Blank Code/ Standard/ Customized Programming Code)

Ex: Your customized programming code is 008 and you require die shipment.

The device No. will be HY11P23-D000-008.

Ex: You request blank code in die package.

The device No. will be HY11P23-D000.

Ex: You request blank code in LQFP 32package.

The device No. will be HY11P23-L032.

And please clearly indicate the shipment packing type when placing orders.

Ex: Your customized programming code is 009 and you require products in QFN32 package.

The device No. will be HY11P23-N032-009.

And please clearly indicate the shipment packing type when placing orders.

² **Code:**

“001”~ “999” is standard or customized programming code. Blank code does not have these numbers.

³ **MSL:**

The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

⁴ **Green (RoHS & no Cl/Br):**

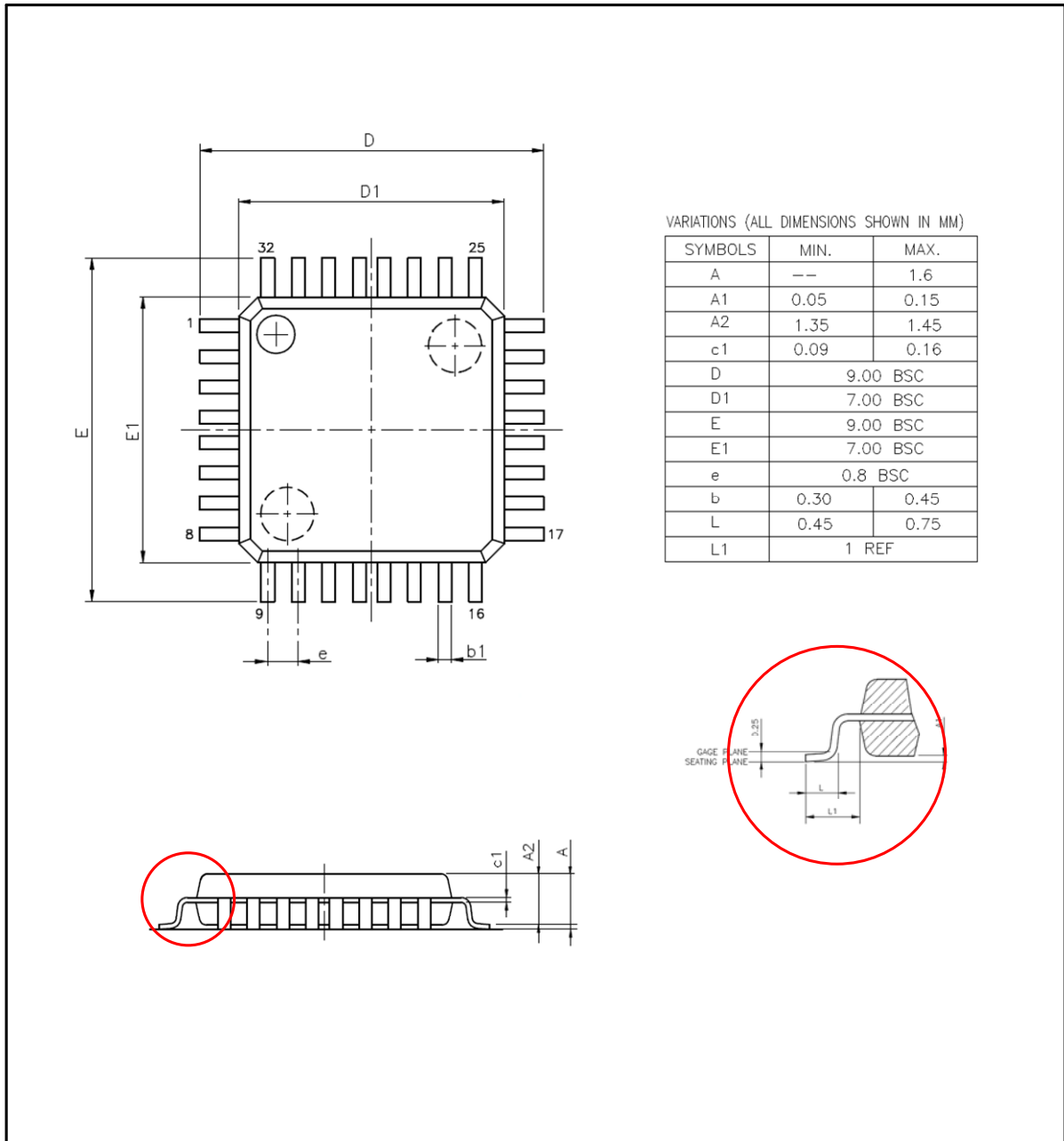
HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br/Cl<0.1%).

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8. Package Information

8.1 LQFP32(L032)

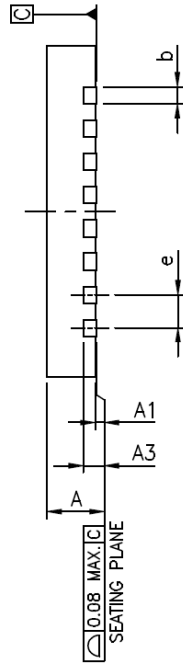
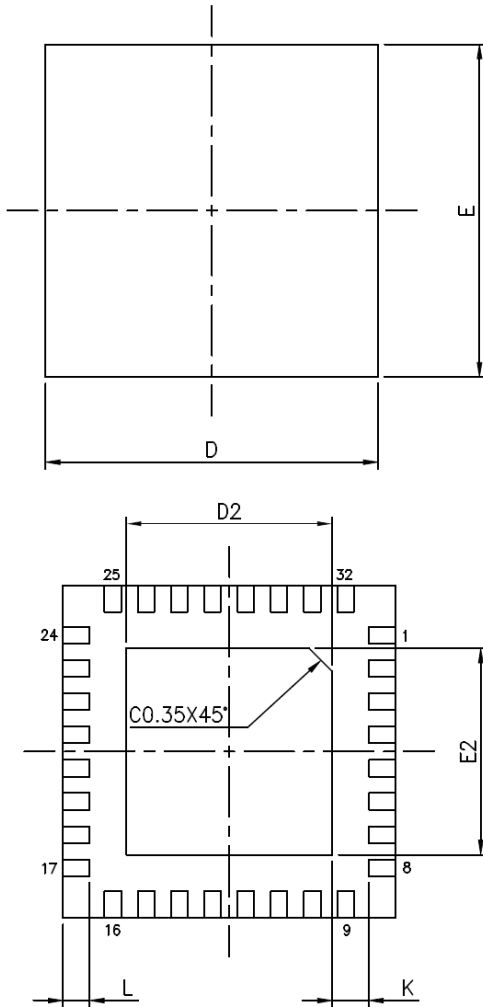


JEDEC MS-026 compliant

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8.2 QFN32 (N032)



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.18	0.25	0.30
D	5.00 BSC		
E	5.00 BSC		
e	0.50 BSC.		
L	0.35	0.40	0.45
K	0.20	—	—

UNIT : mm

PAD SIZE	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
134X134 MIL	3.10	3.20	3.30	3.10	3.20	3.30

UNIT : mm

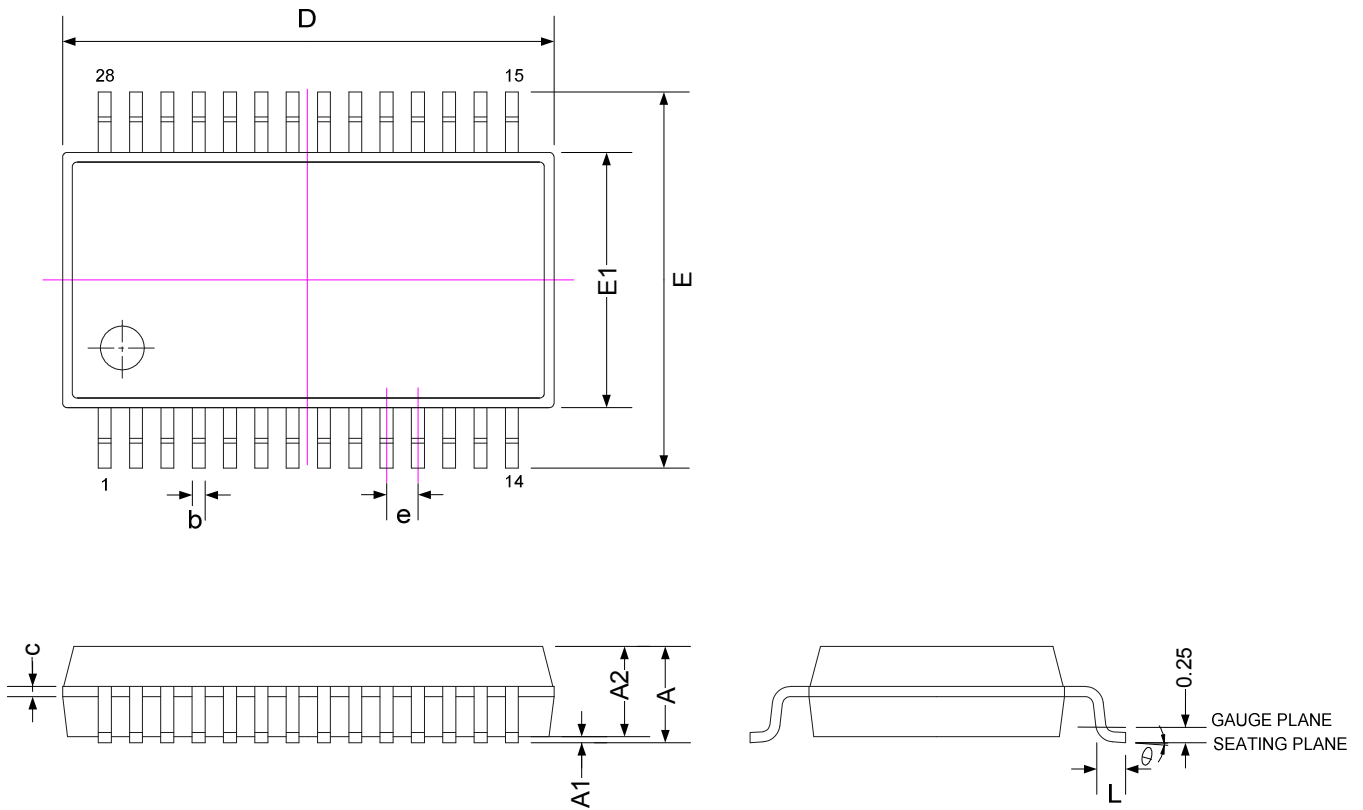
JEDEC MO-220 compliant

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8.3 SSOP28(E028)

Unit : mm



SYMBOLS	MIN	NOM	MAX
A	-	-	2.00
A1	0.05	-	-
A2	1.65	1.75	1.85
b	0.22	-	0.38
c	0.09	-	0.25
D	10.05	10.20	10.50
E1	5.00	5.30	5.60
E	7.65	7.80	7.90
L	0.55	0.75	0.95
e	0.65 BASIC		
θ°	0	4	8

Note:

1. All dimensions refer to JEDEC OUTLINE MO -150.
2. Do not include Mold Flash or Protrusions.

9. Revision History

Major differences are stated thereafter:

Version	Page	Revision Summary
V04	ALL	First edition
V07		With reference to documentation: DS-HY11P23-V07_TC
	4	Features revision
	5~8	Chapter 2 Pin Definition revision
	9~11	Chapter 3 Application Circuit revision
	13~14	Chapter 5 Register List revision
	22~23	Chapter 6.6 Power System revision
	24	Chapter 6.7 Low Noise OPAMP revision
	25~27	Chapter 6.8.2 SD18, Performance II revision
V08	13	Chapter 5 Register List revision
V10	4	Features revision
	5	Delete P-DIP32 package type, add in QFN32 package type
	7	Chapter 2 Pin Definition revision
	22~23	Chapter 6.6 Power System revision
	29	Delete HY11P23-P032 ordering information, add in QFN32 ordering information
	31	Delete HY11P23-P032 package information, add in QFN32 package information
V11	4	Revised features content
	5	Add in Note 3 description
	9~11	Revised application circuit, add in RC circuit of RST
	12	Revised Internal Block Diagram
V15	5	Features revision
	13	Revised 4.2 Development Tool Related Operating Instruction serial numbers
	14	Add 4.3 SD18 Network
	17	Chapter 6 Electrical Characteristics revision
	24	Chapter 6.6 Power System revision
	25	Revised the background color of diagrams
	31~32	Add 6.8.4 SD18 Noise Performance
	33	Chapter 7 Ordering information revision
	35	Revised QFN32 (N032) package type
V16	7	Added in QFN32 Pinout I/O Description (LQFP32/QFN32)
	15	Added in 4.4 Low Noise OPAMP Network
V17	6	Added in Comparison Sheet
	8	Added in SSOP28 Pin Definition

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	9	Chapter 2.4 LQFP32/QFN32 pins name revision.
	12~14	Added in SSOP28 Pinout I/O Description
	39	Chapter 7 Ordering Information revision
	42	Added in SSOP28(E028) package type
V18	24	Revise HAO specification