HYCON TECHNOLOGY

HY3130/HY3131
Datasheet

5,000/50,000 Counts DMM Analog Front End

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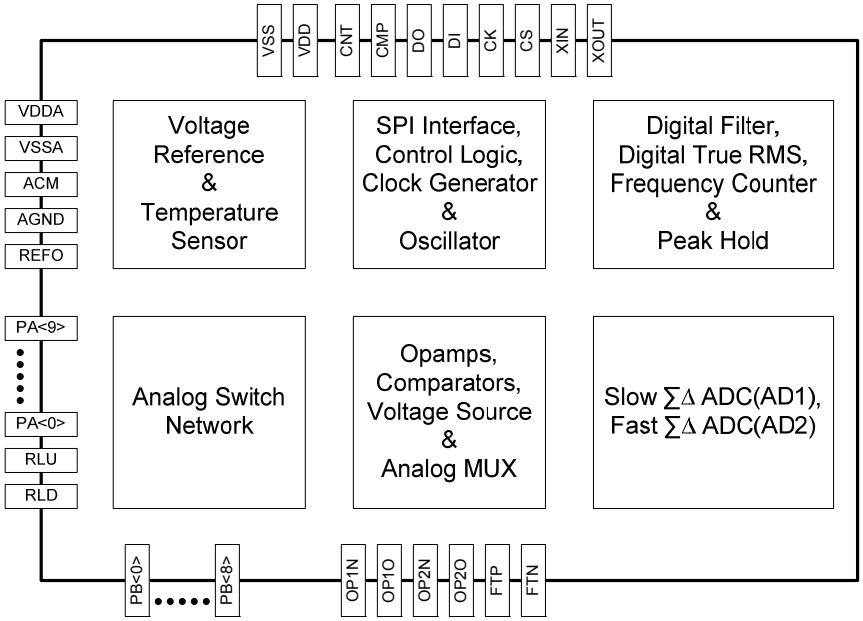
1. Features

- Operating voltage: 3.6V
- Built-in crystal oscillation circuit and 4.9152MHz operation clock source
- Programmable multifunctional network
  - Voltage/resistor/capacitor auto range measurement
  - Fixed voltage/current output
  - Self calibration components
  - Positive/negative electrode differential
- Multifunctional comparator
  - Hysteresis and latch function eliminates glitch
  - Programmable comparison voltage
  - Enable short circuit test, frequency measurement or capacitor discharge/charge frequency measurement
- Operational amplifier
  - Amplify small signal with external components
  - Programmable AC buffer
  - AC full-wave rectification circuit can be formed with combination of external components
- High Resolution ΣΔADC (AD1)
  - 5,000/50,000 Counts @ 5Hz Output rate
  - Zero input, Zero Output
  - High Impedance Input (with input buffer)
- High Speed ΣΔADC (AD2 & AD3)
  - Digital true RMS converter can be formed with combination of internal digital circuit.
  - Peak hold measurement can be achieved with combination of internal digital circuit.
  - Power Measurement can be achieved with combination of internal digital circuit (HY3131 only).
- Built-in absolute temperature sensor
- SPI Interface connect to microprocessor
- 44-pin & 48-pin LQFP Package

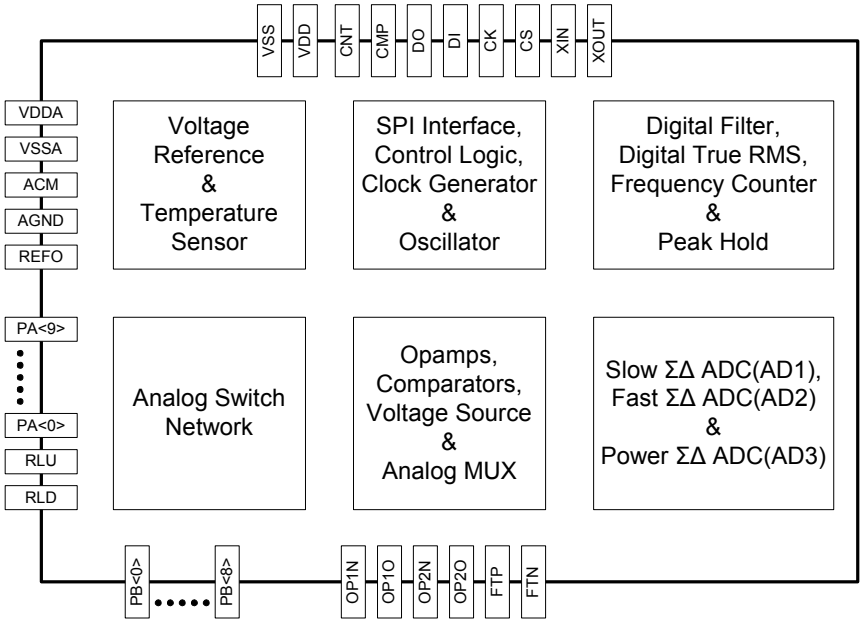
Model No.	PA Network	PB Channel	High Precision ADC	High Speed ADC	OPA	Cap. Array	Digital RMS	Peak Hold	Serial Port	Package
HY3130	10	9	16Bits*1	16Bits*1	2	Yes	Yes	Digital	SPI	LQFP48
HY3131	10	9	24Bits*1	19Bits*2	2	Yes	Yes	Digital	SPI	LQFP48

2. Block Diagram

HY3130:

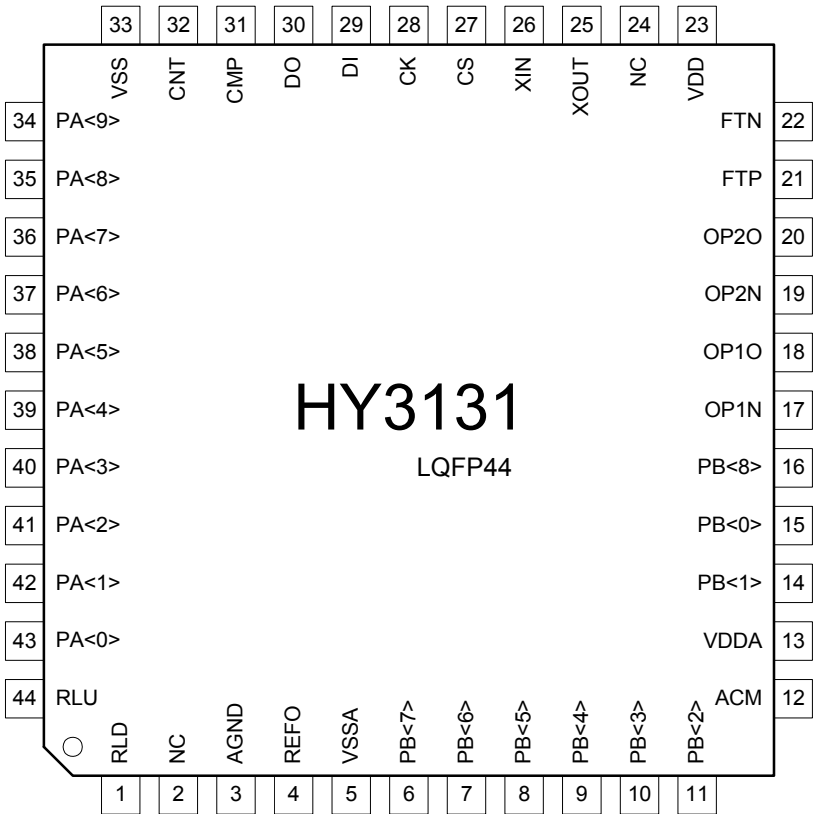


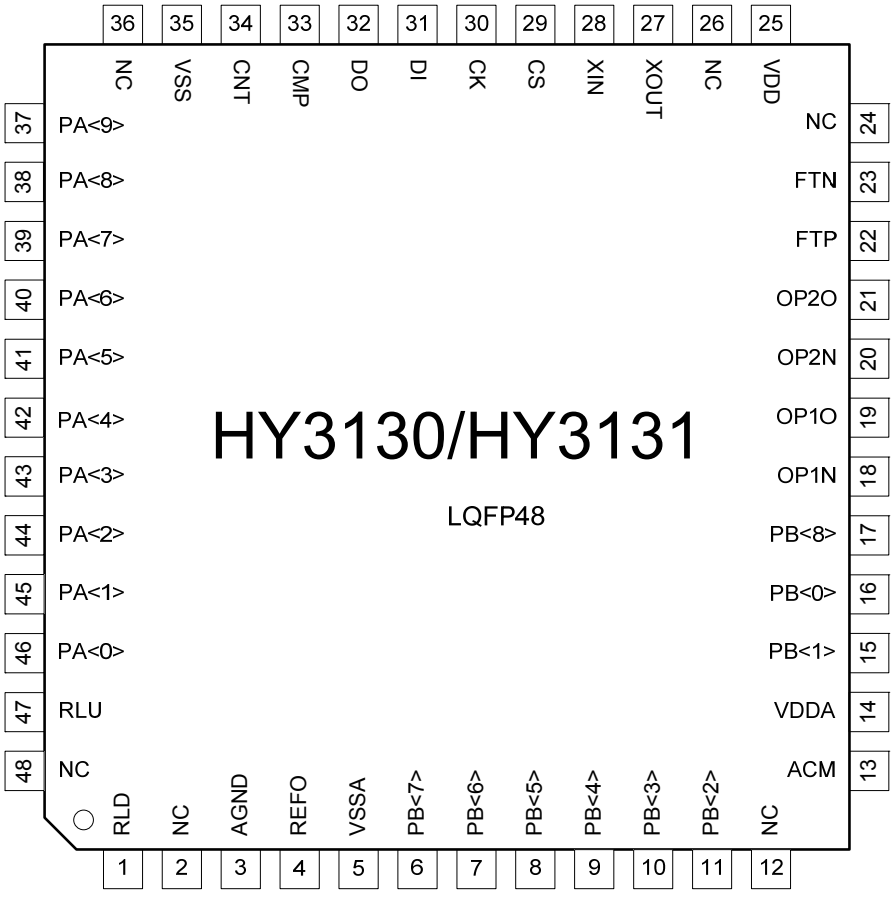
HY3131:



3. Package And Pin

3.1. Pin Definition





3.2. Pin Description

LQFP44:"I/O" Input/Output, "I" Input, "O" Output, "S" Schmitt Trigger, "C" CMOS, "P" Power, "A" Analog

Pin		Characteristic		Description
No.	Name	I/O	Type	
1	RLD	I/O	A	Analog switch network terminal
2	NC			No Connect
3	AGND	I/O	A	Internal analog circuit common ground pin
4	REFO	I/O	A	Voltage reference terminal
5	VSSA	I	P	Analog power supply ground
6 ~ 11	PB<7> ~ PB<2>	I	A	Analog input terminal
12	ACM[1]	I/O	A	ADC common ground
13	VDDA	I	P	Analog power supply
14 ~ 15	PB<1> ~ PB<0>	I	A	Analog input terminal
16	PB<8>	I	A	Analog input terminal
17	OP1N	I	A	OPAMP(OP1) negative input terminal
18	OP1O	O	A	OPAMP(OP1) output terminal
19	OP2N	I	A	OPAMP(OP2) negative input terminal
20	OP2O	O	A	OPAMP(OP2) output terminal
21 ~ 22	FTP, FTN	I/O	A	Pre-filter capacitor terminal
23	VDD	I	P	Digital power supply
24	NC			No Connect
25 ~ 26	XOUT, XIN	I/O	C	Crystal oscillator terminal
27	CS	I	S	SPI interface chip select
28	CK	I	S	SPI interface clock input
29	DI	I	S	SPI interface data input
30	DO	O	C	SPI interface data output
31	CMP	O	C	Comparator output
32	CNT	I	S	Frequency counter input terminal
33	VSS	I	P	Digital power supply ground
34 ~ 43	PA<9> ~ PA<0>	I/O	A	Analog switch network terminal
44	RLU	I/O	A	Analog switch network terminal

[1] ACM pin can only be connected to external capacitors; otherwise it may lead to error action.

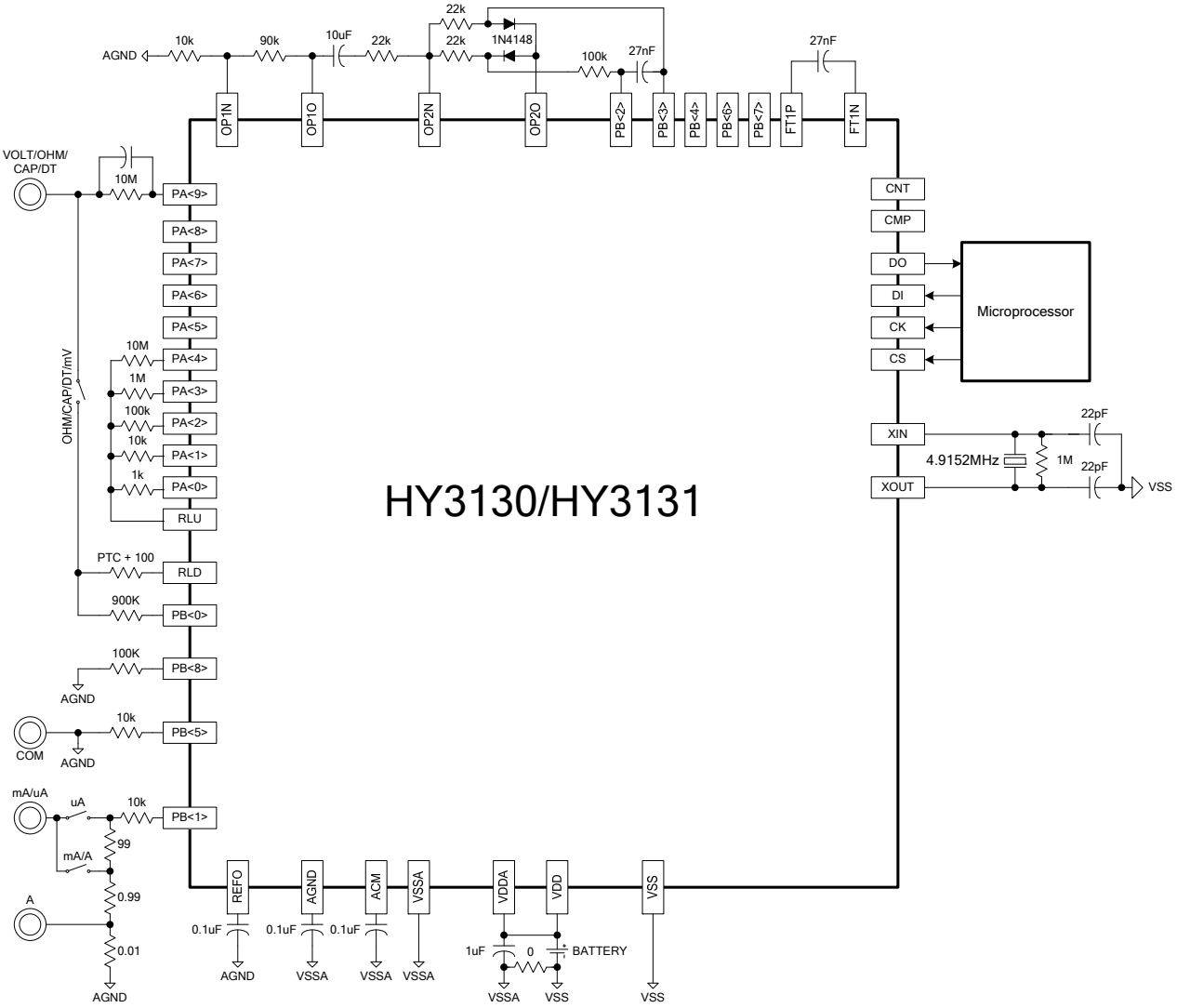
LQFP48:

"I/O" Input/Output, "I" Input, "O" Output, "S" Schmitt Trigger, "C" CMOS, "P" Power, "A" Analog

Pin		Characteristic		Description
No.	Name	I/O	Type	
1	RLD	I/O	A	Analog switch network terminal
2	NC			No Connect
3	AGND	I/O	A	Internal analog circuit common ground pin
4	REFO	I/O	A	Voltage reference terminal
5	VSSA	I	P	Analog power supply ground
6 ~ 11	PB<7> ~ PB<2>	I	A	Analog input terminal
12	NC			No Connect
13	ACM[2]	I/O	A	ADC common ground
14	VDDA	I	P	Analog power supply
15 ~ 16	PB<1> ~ PB<0>	I	A	Analog input terminal
17	PB<8>	I	A	Analog input terminal
18	OP1N	I	A	OPAMP(OP1) negative input terminal
19	OP1O	O	A	OPAMP(OP1) output terminal
20	OP2N	I	A	OPAMP(OP2) negative input terminal
21	OP2O	O	A	OPAMP(OP2) output terminal
22 ~ 23	FTP, FTN	I/O	A	Pre-filter capacitor terminal
24	NC			No Connect
25	VDD	I	P	Digital power supply
26	NC			No Connect
27 ~ 28	XOUT, XIN	I/O	C	Crystal oscillator terminal
29	CS	I	S	SPI interface chip select
30	CK	I	S	SPI interface clock input
31	DI	I	S	SPI interface data input
32	DO	O	C	SPI interface data output
33	CMP	O	C	Comparator output
34	CNT	I	S	Frequency counter input terminal
35	VSS	I	P	Digital power supply ground
36	NC			No Connect
37 ~ 46	PA<9> ~ PA<0>	I/O	A	Analog switch network terminal
47	RLU	I/O	A	Analog switch network terminal
48	NC			No Connect

[2] ACM pin can only be connected to external capacitors; otherwise it may lead to error action.

4. Typical Application Circuit



5. Absolute Maximum Ratings

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at VDD(VDDA) to VSS(VSSA)	**−0.2 V to 4.0 V**
Voltage applied to any pin	**−0.2 V to VDD + 0.3 V**
Diode current at any device terminal	**±2 mA**
Storage temperature range, Tstg	**−55℃ to 150℃**
Total power dissipation	**0.5w**
Lead temperature (soldering, 10s)	**300℃**

6. Electrical Characteristics

(VDD=VDDA=3.6V, VSS=VSSA=0V, TA=+25℃, unless otherwise noted)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	VDD-VSS, VDDA-VSSA	3.6-0.05	3.6	3.6+0.05	V
Power On Reset Voltage	VDD-VSS		1.9		V
External Oscillator Frequency			4.9158	8	Mhz
AD1 Zero Input Reading (HY3131 only)	V_{IN}=0V, Full Scale 50,000 counts	-1	0	+1	Counts
AD1 Zero Reading Drift (HY3131 only)	V_{IN}=0V, Full Scale 50,000 counts, TA=0℃ ~ 70℃	-0.03	0	+0.03	Counts /℃
AD1 Linearity (HY3131 only)	Full Scale (50,000 counts) at 30,000 counts Calibration			±(0.01%+ 2Counts)	% + Counts
Input Leakage Current	V_{IN}=0V		1	10	pA
ADC1 Gain Temperature drift (HY3131 only)	TA=-40℃ ~ 85℃ AD1 Gain=0.9,VR Gain=1, INBUF=off, VRBUF=off		2.5		PPM/℃
ADC2 &AD3 Gain Temperature drift (HY3131 only)	TA=-40℃ ~ 85℃ AD2 & AD3 Gain=1,VR Gain=1,		10	30[3]	PPM/℃
Bandwidth of OP1 or OP2			2		MHz
DC Gain of OP1 or OP2			130		dB
OP1 or OP2 Current Consumption			190		μA
OP3 Source Capability	OP3 positive input=3.5V, ΔV_O =-0.1V		600		μA
OP3 Source Capability	OP3 positive input=0.0 ~ 3.4V, ΔV_O =-0.1V		900		μA
OP3 Sink Capability	OP3 positive input=0.2 ~ 3.5V, ΔV_O =+0.1V		900		μA
OP3 Sink Capability	OP3 positive input=0.1V, ΔV_O =+0.1V		600		μA
OP3 Current Consumption			30		μA
OP Input offset voltage 1	without chopper, OP1CHOP<1:0>=00b or 11b	-2		2	mV
OP Input offset voltage 2	with chopper, OP1CHOP<1:0>=01b or 10b		20		uV
OP Input offset temperature drift 1	without chopper, TA=-40℃ ~ 85℃		2		uV/℃
OP Input offset temperature drift 2	with chopper, TA=-40℃ ~ 85℃		0.1		uV/℃
OP Common-mode voltage input range	OP1CHOP<1:0>=XXb	0.1		VDDA - 1.1	V
Bandwidth of Comparator (CMPH & CMPL)	V_{IN}=600mV_{P-P} SIN V_{IN}=40mV_{P-P} SIN		6 2		MHz
Comparator Current Consumption	CMPH & CMPL		40		μA
Switch Resistance	PS9 ~ PS2		80		Ω

[3] By Design Guarantee

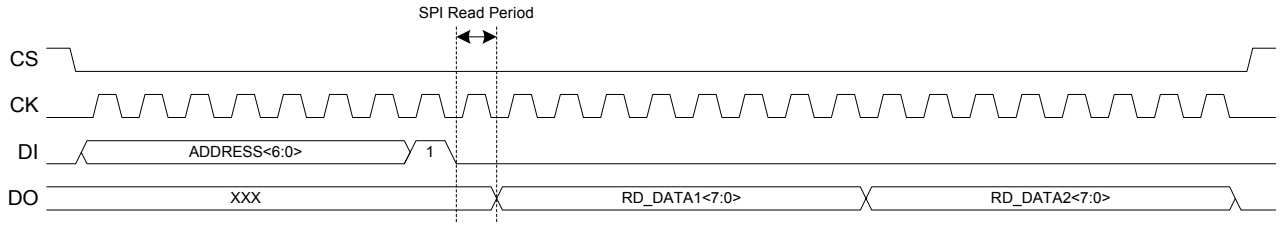
	PS1 ~ PS0 DS9 ~DS0 FS9 ~ FS0 SS9 ~ SS0		40 80 300 300		
AD1 Current Consumption	Without Input & Reference Buffer		90		μA
AD2 or AD3 Current Consumption (HY3131 only)			2160	4000[4]	μA
AD2 + AD3 Current Consumption			3100	6500[5]	μA
Low Pass Filter Current Consumption			50		μA
Digital True RMS Converter Current Consumption			210	3000[6]	μA
Sleep Current			1		μA
REFO Temperature Drift	TA=-40℃ ~ 85℃		70		PPM/℃
Normal Mode Rejection	Offset=500mV, AC 50mV, 50Hz/60Hz±1Hz, Output rate = 5sps Output rate = 10sps		 120 75		dB
Digital Output High	I_{OL}=+10mA	VDD-0.3			V
Digital Output Low	I_{OL}=-10mA			VSS+0.3	V
Digital Input High	CK, DI & CS Pin	1.8		VDD	V
Digital Input Low	CK, DI & CS Pin	VSS		0.5	V
Digital Input High	CNT Pin	2.4		VDD	V
Digital Input Low	CNT Pin	VSS		1.3	V
CK High Pulse Width Time(T_{CKHI})		20			ns
CK Low Pulse Width Time(T_{CKLO})		60			ns
DI Data Set Time(T_{DISET})		60			ns
DI Data Hold Time(T_{DIHOLD})		20			ns
DO Data Ready Time(T_{DODL})		60			ns

[4] By Design Guarantee
[5] By Design Guarantee
[6] By Design Guarantee

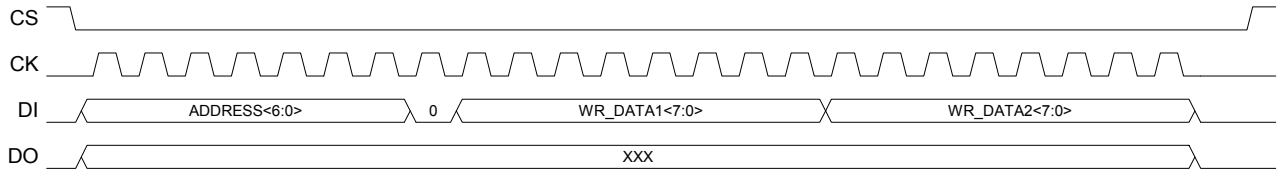
7. Digital Interface

7.1. SPI Protocol

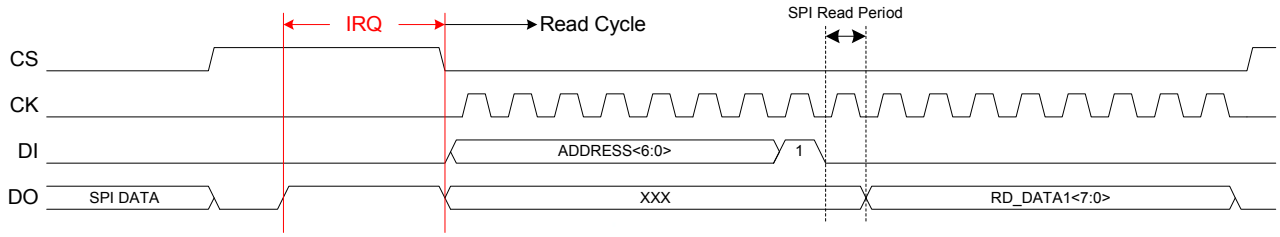
Read:



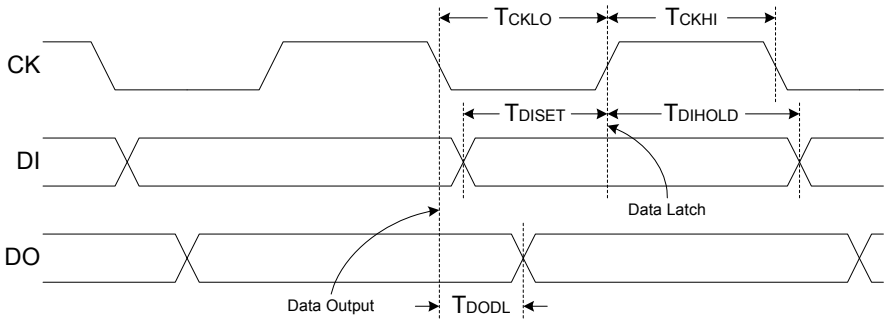
Write:



IRQ:



Timing:



7.2. Description

(1) Address：Register address includes 7 Bits. When SPI started communication and CS is Low, the first Data is Register Address[6…0] and R/W, totally 8 Bits. The output sequence is Address MSB(Bit6) first, then R/W. So Register Address must left shift 1 Bit and output.

(2) Read mode：Followed (1), if the eighth bit of DI is 1, then it enters Read mode. The ninth bit must be blank (SPI Read Period) to capture correct data after entering Read mode. The tenth to seventeenth bit of DO is address data and from this bit, address automatically adds 1. It is no need to wait SPI to capture data, every 8 bits afterward, is the content of address add 1. Readout action will stop when CS is configured high.

(3) Write mode：Continued (1), if the eighth bit of DI is 0, it is Write mode. The ninth bit does not need to be blank after entering Write mode. The ninth bit to sixteenth bit of DI is address data and from this bit, address automatically adds 1. It is no need to wait SPI to capture data, every 8 bits afterward, is the content of address add 1. Write-in action will stop when CS is configured high.

(4) IRQ output mode：After entering IRQ waiting mode, CS is set high. At this time, IRQ occurs and DO is high. Conversely, if DO is low, IRQ will not occur. After IRQ took place, sets CS as Low, then read/write data can be implemented. IRQ graph appears after IRQ occurrence, read action is activated. Please be noted that when CS is High, DO is IRQ output mode. CS is Low, DO is SPI output mode.

(5) Timing relation between DI, DO and CK and DI and DO is shown as the graph.

(6) CK signal must be low before CS is Low (CK line low in idle state).

(7) CK is in effective state under high potential while it's in idle state under low potential.

(8) DI and DO will be sent when CK turns idle state from effective state.

8. Register List

HY3130:

Address	File Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	AD1_DATA	AD1<7:0>=unknown							
01h		AD1<15:8>							
02h		AD1<23:16>							
03h	AD2_DATA	AD2<7:3>					AD2<2:0>=000		
04h		AD2<15:8>							
05h		AD2<23:16>							
06h	LPF_DATA	LPF<7:0>							
07h		LPF<15:8>							
08h		LPF<23:16>							
09h	RMS_DATA	RMS<7:0>							
0Ah		RMS<15:8>							
0Bh		RMS<23:16>							
0Ch		RMS<31:24>							
0Dh		RMS<39:32>							
0Eh	PKHMIN	PKHMIN<7:0>							
0Fh		PKHMIN<15:8>							
10h		PKHMIN<23:16>							
11h	PKHMAX	PKHMAX<7:0>							
12h		PKHMAX<15:8>							
13h		PKHMAX<23:16>							
14h	CTSTA	PCNTI	ACPO	CMPHO	CMPLO	-	-	-	CTBOV
15h	CTC	CTC<7:0>							
16h		CTC<15:8>							
17h		CTC<23:16>							
18h	CTB	CTB<7:0>							
19h		CTB<15:8>							
1Ah		CTB<23:16>							
1Bh	CTA	CTA<7:0>							
1Ch		CTA<15:8>							
1Dh		CTA<23:16>							
1Eh	INTF	BORF	-	-	RMSF	LPFF	AD1F	AD2F	CTF
1Fh	INTE	-	-	-	RMSIE	LPFIE	AD1IE	AD2IE	CTIE
20H	R20	SCMPI<2:0>			ENCMP	ENCNTI	ENPCMPO	ENCTR	O
21H	R21	SCMPRH<3:0>				SCMPRL<3:0>			
22H	R22	AD1OS<2:0>			AD1CHOP<1:0>		AD1OSR<2:0>		
23H	R23	ENAD1	-	O	AD1RG	AD1RHBUF	AD1RLBUF	AD1IPBUF	AD1INBUF
24H	R24	SAD1FP<3:0>				SDIO	SAD1FN<2:0>		
25H	R25	AD2IG<1:0>		AD1IG<1:0>		SACM<1:0>		OPS<2>	OPS<1>
26H	R26	ENAD2	0	ENCHOPAD	AD2RG	SAD2CLK	AD2OSR<2:0>		
27H	R27	SAD2IP<1:0>		SAD2IN<1:0>		SAD2RH<1:0>		SAD2RL<1:0>	
28H	R28	-	SAD1RH<2:0>			-	SAD1RL<2:0>		
29H	R29	ENRMS	ENLPF	LPFBW<2:0>			ENPKH	PKHSEL<1:0>	
2Ah	R2A	PS1	DS1	FS1	SS1	PS0	DS0	FS0	SS0
2Bh	R2B	PS3	DS3	FS3	SS3	PS2	DS2	FS2	SS2
2Ch	R2C	PS5	DS5	FS5	SS5	PS4	DS4	FS4	SS4
2Dh	R2D	PS7	DS7	FS7	SS7	PS6	DS6	FS6	SS6
2Eh	R2E	PS9	DS9	FS9	SS9	PS8	DS8	FS8	SS8
2Fh	R2F	ENVS	SMODE<6:0>						
30h	R30	SREFO	ACC<6:0>						
31h	R31	ENREFO	ENBIAS	SAGND<1:0>		SFUVR<3:0>			
32h	R32	ENOP2	SOP2P<2:0>			ENOP1	SOP1P<2:0>		
33h	R33	OP1CHOP<1:0>		ENOSC	ENXI	SFT1<1:0>		SAD1I<1:0>	
35h	R35	O	O	O	O	O	O	O	O
36h	R36	O	O	O	O	O	O	O	O
37h	R37	Testing Mode, Don't use or Write "0" only							

HY3131:

Address	File Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	AD1_DATA	AD1<7:0>							
01h		AD1<15:8>							
02h		AD1<23:16>							
03h	AD2_DATA	AD2<7:0>							
04h		AD2<15:8>							
05h		AD2<23:16>							
06h	LPF_DATA	LPF<7:0>							
07h		LPF<15:8>							
08h		LPF<23:16>							
09h	RMS_DATA	RMS<7:0>							
0Ah		RMS<15:8>							
0Bh		RMS<23:16>							
0Ch		RMS<31:24>							
0Dh		RMS<39:32>							
0Eh	PKHMIN	PKHMIN<7:0>							
0Fh		PKHMIN<15:8>							
10h		PKHMIN<23:16>							
11h	PKHMAX	PKHMAX<7:0>							
12h		PKHMAX<15:8>							
13h		PKHMAX<23:16>							
14h	CTSTA	PCNTI	ACPO	CMPHO	CMPLO	-	-	-	CTBOV
15h	CTC	CTC<7:0>							
16h		CTC<15:8>							
17h		CTC<23:16>							
18h	CTB	CTB<7:0>							
19h		CTB<15:8>							
1Ah		CTB<23:16>							
1Bh	CTA	CTA<7:0>							
1Ch		CTA<15:8>							
1Dh		CTA<23:16>							
1Eh	INTF	BORF	-	-	RMSF	LPFF	AD1F	AD2F	CTF
1Fh	INTE	-	-	-	RMSIE	LPFIE	AD1IE	AD2IE	CTIE
20H	R20	SCMPI<2:0>			ENCMP	ENCNTI	ENPCMPO	ENCTR	O
21H	R21	SCMPRH<3:0>				SCMPRL<3:0>			
22H	R22	AD1OS<2:0>			AD1CHOP<1:0>		AD1OSR<2:0>		
23H	R23	ENAD1	-	0	AD1RG	AD1RHBUF	AD1RLBUF	AD1IPBUF	AD1INBUF
24H	R24	SAD1FP<3:0>				SDIO	SAD1FN<2:0>		
25H	R25	AD2IG<1:0>		AD1IG<1:0>		SACM<1:0>		OPS<2>	OPS<1>
26H	R26	ENAD2	0	ENCHOPAD	AD2RG	SAD2CLK	AD2OSR<2:0>		
27H	R27	SAD2IP<1:0>		SAD2IN<1:0>		SAD2RH<1:0>		SAD2RL<1:0>	
28H	R28	-	SAD1RH<2:0>			-	SAD1RL<2:0>		
29H	R29	ENRMS	ENLPF	LPFBW<2:0>			ENPKH	PKHSEL<1:0>	
2Ah	R2A	PS1	DS1	FS1	SS1	PS0	DS0	FS0	SS0
2Bh	R2B	PS3	DS3	FS3	SS3	PS2	DS2	FS2	SS2
2Ch	R2C	PS5	DS5	FS5	SS5	PS4	DS4	FS4	SS4
2Dh	R2D	PS7	DS7	FS7	SS7	PS6	DS6	FS6	SS6
2Eh	R2E	PS9	DS9	FS9	SS9	PS8	DS8	FS8	SS8
2Fh	R2F	ENVS	SMODE<6:0>						
30h	R30	SREFO	ACC<6:0>						
31h	R31	ENREFO	ENBIAS	SAGND<1:0>		SFUVR<3:0>			
32h	R32	ENOP2	SOP2P<2:0>			ENOP1	SOP1P<2:0>		
33h	R33	OP1CHOP<1:0>		ENOSC	ENXI	SFT1<1:0>		SAD1I<1:0>	
34h	R34	ENAD3	O	ENCHOPAD	AD3RG	SVXI	SDO23	O	O
35h	R35	SAD3IP<1:0>		SAD3IN<1:0>		AD3IG<1:0>		O	O
36h	R36	SPHACAL<7:0>=unknown							
37h	R37	Testing Mode, Don't use or Write "0" only							

9. Data Register

(1) AD1<23:0>：Register for High Resolution ADC (AD1) output data. Max. value: 7FFFFFh, min. value: 800000h. AD1<23:8> is effective bit for HY3130, AD1<23:0> is effective bit for HY3131.

(2) AD2<23:0>：Register for High Resolution ADC (AD2) output data. Max. value: 03FFFFh, min. value:FC0000h. AD2<18:3> is effective bit for HY3130, AD2<18:0> is effective bit for HY3131, AD<23:19> and AD<18> is the same.

(3) LPF<23:0>：Register for Low Pass Filter output data. Max. value: 03FFFFh, min. value: FC0000h. LPF<18:3> is effective bit for HY3130, LPF<18:0> is effective bit, LPF<23:19> and LPF<18> is the same.

(4) RMS<39:0>：Register for RMS Converter output data. Max. value: 1FFFFFFFFFh, min. value: E000000000h. RMS<<37:6> is effective bit for HY3130, RMS<37:0> is effective bit for HY3131, RMS<39:38> and RMS<37> is the same.

(5) PKHMAX<23:0>：Register for Peak Hold max. output data. Max. value: 03FFFFh, min. value: FC0000h. PKHMAX<18:3> is effective bit for HY3130, PKHMAX<18:0> is effective bit for HY3131, PKHMAX<23:19> and PKHMAX<18> is the same.

(6) PKHMIN<23:0>：Register for Peak Hold min. output data. Max. value: 03FFFFh, min. value: FC0000h. PKHMIN<18:3> is effective bit for HY3130, PKHMIN<18:0> is effective bit for HY3131, PKHMIN<23:19> and PKHMIN<18> is the same.

(7) CTA<23:0>：Register for Frequency Counter data. Max. value: FFFFFFh, min. value: 000000h.

(8) CTB<23:0>：Register for Frequency Counter data. Max. value: FFFFFFh, min. value: 000000h.

(9) CTC<23:0>：Register for Frequency Counter data. Max. value: FFFFFFh, min. value: 000000h.

10. Interrupt

Address	Name	Bit<7>	Bit<6>	Bit<5>	Bit<4>	Bit<3>	Bit<2>	Bit<1>	Bit<0>
1Fh	INTE	-	-	-	RMSIE	LPFIE	AD1IE	AD2IE	CTIE
1Eh	INTF	BORF	-	-	RMSF	LPFF	AD1F	AD2F	CTF

10.1. INTE : IRQ Enable Register

(1) RMSIE：IRQ is generated when RMS event takes place. 1=Enable，0=Disable.

(2) LPFIE：IRQ is generated when Low Pass Filter event takes place. 1=Enable, 0=Disable.

(3) AD1IE：IRQ is generated when AD1event takes place. 1=Enable, 0=Disable.

(4) AD2IE：IRQ is generated when AD2 event takes place. 1=Enable, 0=Disable.

(5) CTIE：IRQ is generated when Frequency Counter event takes place. 1=Enable, 0=Disable.

(6) When XXIE is set 1, XXF is set 1; IRQ will be generated by DO of SPI Interface.

(7) When XXIE is set 0, XXF still will be set as 1 due to relative event occurrence, IRQ will not be generated.

10.2. INTF : IRQ Event Register

(1) BORF：When VDD lowers than 1.9V, BORF will be set 1. This bit has neither relative INTEx nor IRQ event.

(2) RMSF：RMSF will be set 1 when RMS event takes place.

(3) LPFF：LPFF will be set 1 when Low Pass Filter event takes place.

(4) AD1F：AD1F will be set 1 when AD1 event takes place.

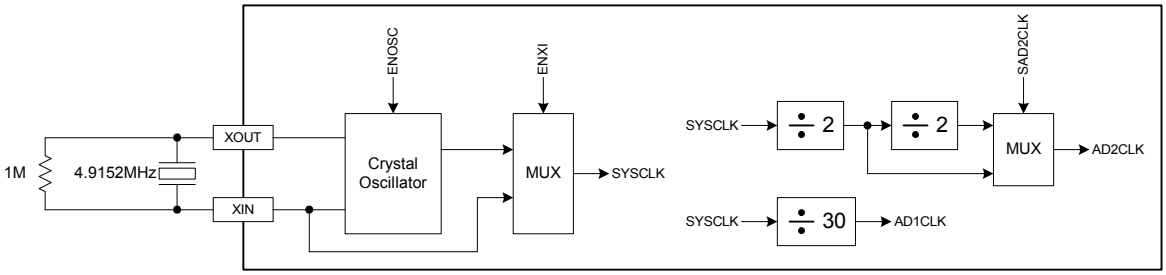
(5) AD2F：AD2F will be set 1 when AD2 event takes place.

(6) CTF：CTF will be set 1 when Frequency Counter event takes place.

(7) INTF register will be erased 0 when IC rest or after INTF register is read. INTF register can be written as 0 by SPI Interface, but not 1.

(8) Relative bit of INTF register will be set 1 when event takes place. It is suggested to erase INTF register as 0 before setting INTEx as 1 (SPI readout or write-in 0) to prevent unnecessary IRQ.

11. Clock System



Address	Name	Bit<7>	Bit<6>	Bit<5>	Bit<4>	Bit<3>	Bit<2>	Bit<1>	Bit<0>
33h	R33	OP1CHOP<1:0>		**ENOSC**	**ENXI**	SFT1<1:0>		SAD1I<1:0>	
26h	R26	ENAD2	0	ENCHOPAD2	AD2RG	**SAD2CLK**	AD2OSR<2:0>		

The IC has built-in Crystal Oscillator, which generates Clock for system usage. The pin of XIN and XOUT can be connected to external oscillator components. XIN can be used as input pin for system clock when no oscillator is being connected, as shown in the graph.

(1) ENOSC：Register bit that can enable Crystal Oscillator. 1=Enable；0=Disable。

(2) ENXI：Register bit that can select system clock. SYSCLK。0：SYSCLK=Crystal Oscillator output；1：SYSCLK =XIN.

(3) SYSCLK：System clock that provides for IC usage

(4) AD1CLK：Sampling signals of Modulator1 of AD1 that frequency is fixed at $F_{SYSCLK}/30$. F_{SYSCLK} is the frequency of SYSCLK.

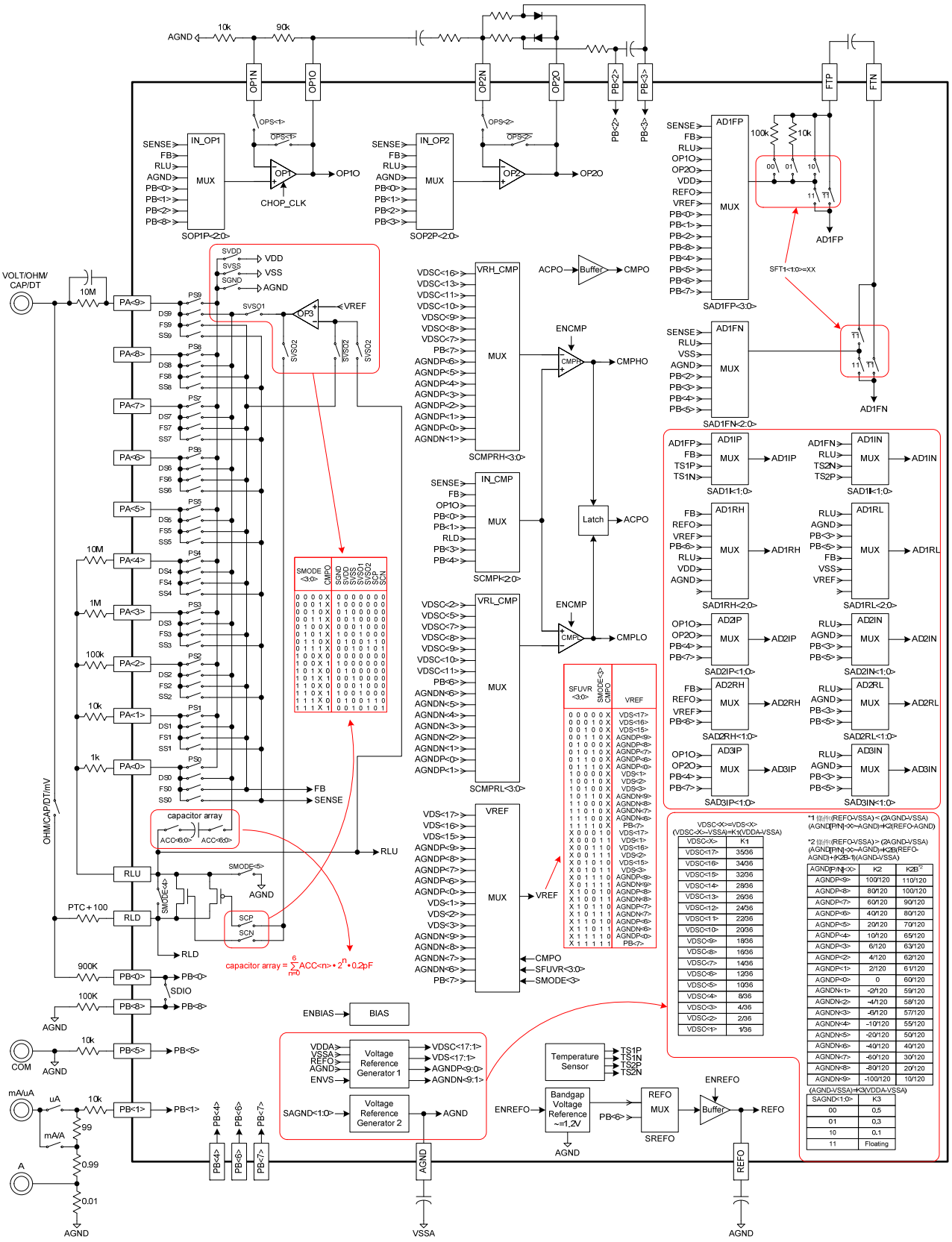
(5) AD2CLK：Sampling signals of Modulator2 of AD2 that frequency is selected by register bit SAD2CLK.

(6) SAD2CLK：Register bit, frequency of choosing AD2CLK.
0：$F_{AD2CLK}=F_{SYSCLK}/2$； 1：$F_{AD2CLK}=F_{SYSCLK}/4$。F_{SYSCLK} is the frequency of SYSCLK. F_{AD2CLK} is the frequency of AD2CLK.

(7) If register Address=37h, write-in Data=60h, the IC will Reset.

(8) If VDD<1.9V, the IC will Reset.

12. Function Network



SMODE <3:0>	CMPO	SGND	SVDD	SVSS1	SVSO2	SCP	SCN
0 0 0 0 X	0	0	0	0	0	0	0
0 0 0 1 X	1	0	0	0	0	0	0
0 0 1 0 X	0	1	0	0	0	0	0
0 0 1 1 X	1	1	0	0	0	0	0
0 1 0 0 X	0	0	1	0	0	0	0
0 1 0 1 X	1	0	1	0	0	0	0
0 1 1 0 X	0	1	1	0	0	0	0
0 1 1 1 X	1	1	1	0	0	0	0
1 0 0 X 0	0	0	0	1	0	0	0
1 0 0 X 1	1	0	0	1	0	0	0
1 0 1 X 0	0	1	0	1	0	0	0
1 0 1 X 1	1	1	0	1	0	0	0
1 1 0 X 0	0	0	1	1	0	0	0
1 1 0 X 1	1	0	1	1	0	0	0
1 1 1 X 0	0	1	1	1	0	0	0
1 1 1 X 1	1	1	1	1	0	0	0

SFUVR <3:0>	SMODE <3>	CMPO	VREF
0 0 0 0	0	X	VDS<17>
0 0 0 1	0	X	VDS<16>
0 0 1 0	0	X	VDS<15>
0 0 1 1	0	X	AGNDP<8>
0 1 0 0	0	X	AGNDP<8>
0 1 0 1	0	X	AGNDP<7>
0 1 1 0	0	X	AGNDP<6>
0 1 1 1	0	X	AGNDP<0>
1 0 0 0	X	0	VDS<1>
1 0 0 1	X	0	VDS<2>
1 0 1 0	X	0	VDS<3>
1 0 1 1	X	0	AGNDN<8>
1 1 0 0	X	0	AGNDN<8>
1 1 0 1	X	0	AGNDN<7>
1 1 1 0	X	0	AGNDN<6>
1 1 1 1	X	0	PB<7>
X 0 0 0	1	1	VDS<17>
X 0 0 1	1	1	VDS<1>
X 0 1 0	1	1	VDS<2>
X 0 1 1	1	1	VDS<15>
X 1 0 0	1	1	VDS<3>
X 1 0 1	1	1	AGNDP<8>
X 1 1 0	1	1	AGNDN<8>
X 1 1 1	1	1	AGNDP<7>
X 1 0 1	1	1	AGNDN<7>
X 1 1 0	1	1	AGNDP<6>
X 1 1 1	1	1	AGNDN<6>
X 1 1 1	1	0	AGNDP<0>
X 1 1 1	1	1	PB<7>

VDSC<X>=VDS<X>
(VDSC<X>-VSSA)=K1(VDDA-VSSA)

VDSC<X>	K1
VDSC<17>	35/36
VDSC<16>	34/36
VDSC<15>	32/36
VDSC<14>	28/36
VDSC<13>	26/36
VDSC<12>	24/36
VDSC<11>	22/36
VDSC<10>	20/36
VDSC<9>	18/36
VDSC<8>	16/36
VDSC<7>	14/36
VDSC<6>	12/36
VDSC<5>	10/36
VDSC<4>	8/36
VDSC<3>	4/36
VDSC<2>	2/36
VDSC<1>	1/36

*1 條件:(REFO-VSSA) < (2AGND-VSSA)
(AGND[P/N]-X<-AGND)=K2(REFO-AGND)

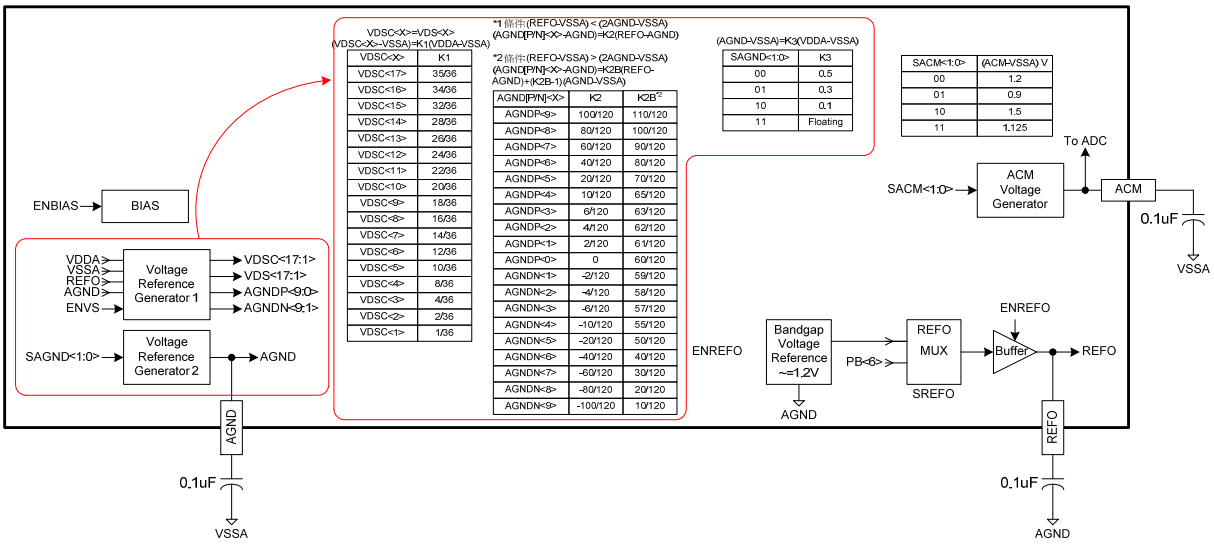
*2 條件:(REFO-VSSA) > (2AGND-VSSA)
(AGND[P/N]-X>-AGND)=K2B(REFO-AGND)+K2B-1)(AGND-VSSA)

AGND[P/N]<X>	K2	K2B*
AGNDP<9>	100/120	110/120
AGNDP<8>	80/120	100/120
AGNDP<7>	60/120	90/120
AGNDP<6>	40/120	80/120
AGNDP<5>	20/120	70/120
AGNDP<4>	10/120	65/120
AGNDP<3>	6/120	63/120
AGNDP<2>	4/120	62/120
AGNDP<1>	2/120	61/120
AGNDP<0>	0	60/120
AGNDN<1>	-2/120	59/120
AGNDN<2>	-4/120	58/120
AGNDN<3>	-6/120	57/120
AGNDN<4>	-10/120	55/120
AGNDN<5>	-20/120	50/120
AGNDN<6>	-40/120	40/120
AGNDN<7>	-60/120	30/120
AGNDN<8>	-80/120	20/120
AGNDN<9>	-100/120	10/120

(AGND-VSSA)=K3(VDDA-VSSA)

SAGND<1:0>	K3
00	0.5
01	0.3
10	0.1
11	Floating

12.1. Voltage Reference Generator



Address	Name	Bit<7>	Bit<6>	Bit<5>	Bit<4>	Bit<3>	Bit<2>	Bit<1>	Bit<0>
31h	R31	ENREFO	ENBIAS	SAGND<1:0>		SFUVR<3:0>			
30h	R30	SREFO	ACC<6:0>						
2Fh	R2F	ENVS	SMODE<6:0>						
25h	R25	AD2IG<1:0>		AD1IG<1:0>		SACM<1:0>		OPS<2>	OPS<1>

Voltage reference generator provides bias and voltage reference for ADC, Comparator and OPAMP usage.

(1) Voltage Reference Generator1：Generates VDS<17:1>，VDSC<17:1>，AGNDP<9:0> and AGNDN<9:1>. VDSC<N> is (VDDA,VSS) divided node, AGNDP<N> is (REFO,AGND) divided node, AGNDN<N> is (-REFO,AGND) divided node.

(2) Voltage Reference Generator2：Generates AGND pin voltage as the reference point of the measurement system

AGND pin needs to be connected with external capacitor, 0.1μF.

(3) Band gap Voltage Reference：Can generate relative AGND, approximate 1.2V voltage

(4) REFO Buffer：Buffer input is selected by SREFO. Band gap Voltage Reference or PB<6> voltage is selectable.

Buffer output, REFO pin needs to be connected with external capacitor, 0.1μF.

(5) ACM Voltage Generator：Generates ACM pin voltage as the reference point of common mode of the internal ADC

ACM pin needs to be connected with external capacitor, 0.1μF.

(6) ENBIAS：Register bit that can enable bias circuit, providing bias for all analog circuit. 1=Enable，0=Disable.

(7) ENVS：Register bit that can enable Voltage Reference Generator1. 1=Enable，0=Disable.

(8) SAGND<1:0>：Register bit that can select AGND voltage. When SAGND<1:0>=11, Voltage Reference Generator2 will be disabled and AGND pin is in Floating status. At this time, AGND can connect to external voltage.

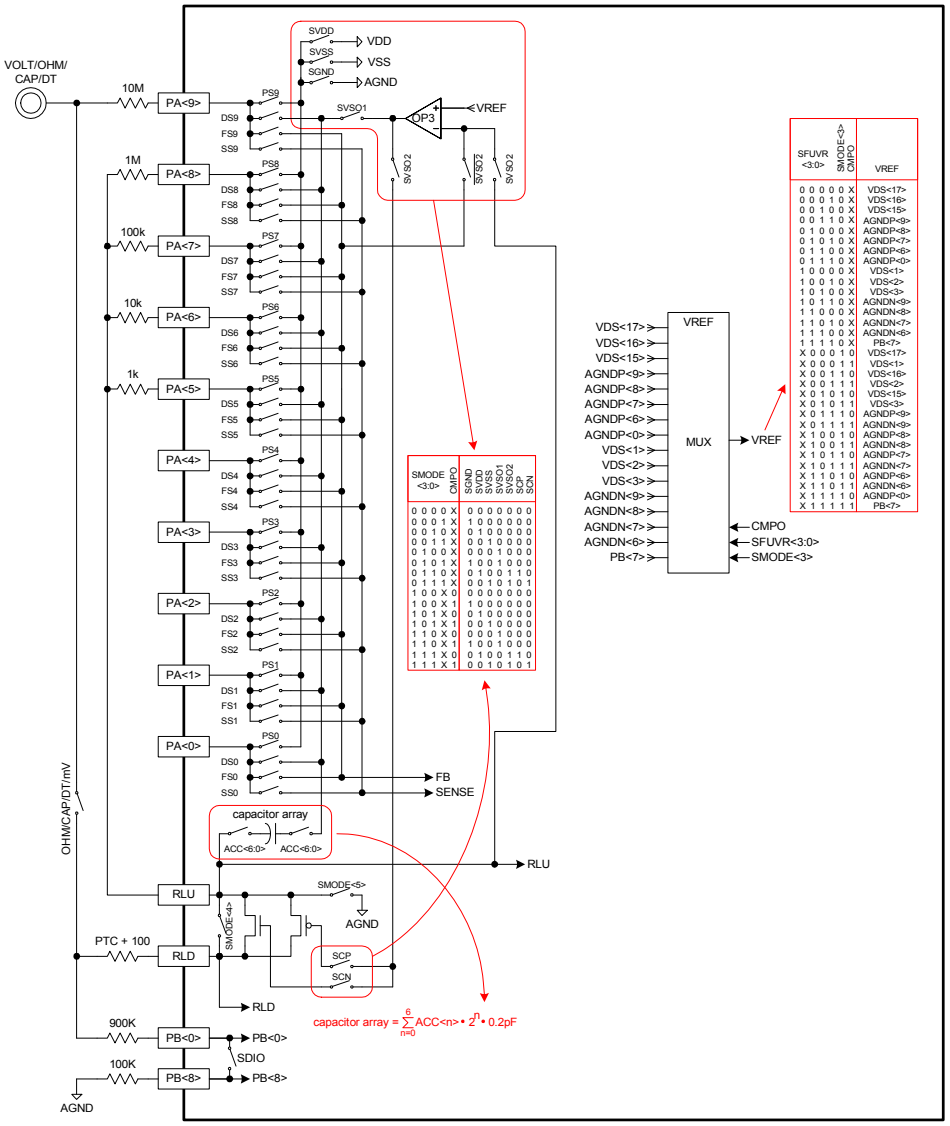
(9) ENREFO：Register bit that can enable approximately 1.2V voltage of relative AGND of the internal Band gap Voltage Reference and can enable REFO Buffer. 1=Enable, 0=Disable. When it is set 0, REFO pin is in Floating status.

(10) SREFO：Register bit that can select input source of REFO Buffer. ”0”: select relative AGND 1.2V voltage of the internal Band gap; ”1”: select PB<6> pin.

(11) SACM<1:0>：Register bit that can select ACM voltage. Recommend 1.5V voltage of the ACM.

(12) For all correlative voltages, please refer to the above graph.

12.2. Analog Switch Network



Address	Name	Bit<7>	Bit<6>	Bit<5>	Bit<4>	Bit<3>	Bit<2>	Bit<1>	Bit<0>
31h	R31	ENREFO	ENBIAS	SAGND<1:0>		SFUVR<3:0>			
30h	R30	SREFO	ACC<6:0>						
2Fh	R2F	ENVS	SMODE<6:0>						
2Eh	R2E	PS9	DS9	FS9	SS9	PS8	DS8	FS8	SS8
2Dh	R2D	PS7	DS7	FS7	SS7	PS6	DS6	FS6	SS6
2Ch	R2C	PS5	DS5	FS5	SS5	PS4	DS4	FS4	SS4
2Bh	R2B	PS3	DS3	FS3	SS3	PS2	DS2	FS2	SS2
2Ah	R2A	PS1	DS1	FS1	SS1	PS0	DS0	FS0	SS0
24h	R24	SAD1FP<3:0>				SDIO	SAD1FN<2:0>		

Analog switch network is described as in the graph. With combination of external resistances, it can constitute various networks to measure voltage, resistance and capacitance. The internal switch of PA<9:0> pin is

controlled by register bit PS9~PS0, DS9~DS0, FS9~FS0 and SS9~SS0 respectively. The value of controlled switch resistance is shown in below table：@VDDA=3.6V

Register Bit	PS9 ~ PS2	PS1 ~ PS0	DS9 ~ DS0	FS9 ~ FS0	SS9 ~ SS0
Switch Resistance(Ω)	80	40	80	300	300

(1) OP3 can be used as fixed voltage source. Combining with MOS that controlled by SCP/SCN, it can form fixed current source that provides current for measuring components.

(2) The positive input end of OP3 is VREF. VREF voltage selection is controlled by CMPO, register bit SFUVR<3:0> and SMODE<3> combination. For its voltage value, please refer to the above graph.

(3) register bit SMODE<3:0> and CMPO signal compose internal control signal, SGND, SVDD, SVSS, SVSO1, SVSO2, SCP and SCN. The value is shown in the above graph.

(4) CMPO is the output signal of comparator.

(5) Capacitor array can compensate ACV measurement bandwidth; the capacitance value is shown in the above graph. The capacitance value is controlled by register bit ACC<6:0>.

$$\text{capacitor array} = \sum_{n=0}^{6} \text{ACC<n>} \bullet 2^{n} \bullet 0.2\text{pF}$$

Capacitance value of every Bit: (Bit = 0 or 1) x 2^n x 0.2pF. Calculated capacitance value result of every Bit is shown in below table.

(unit：pF)

ACC<6:0> = n	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
ACC<n>	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Capacitance Value	12.8	6.4	3.2	1.6	0.8	0.4	0.2

Example 1:

Supposed ACC<6:0>=1010101,

Then total compensation capacitance value:

=(1*2^6*0.2)+(0*2^5*0.2)+(1*2^4*0.2)+(0*2^3*0.2)+(1*2^2*0.2)+(0*2^1*0.2)+(1*2^0*0.2)

=12.8 + 0 + 3.2 + 0 + 0.8 + 0 + 0.2

=17 pF

Example 2:

Supposed ACC<6:0>=1100011，

Then total compensation capacitance value:

=(1*2^6*0.2)+(1*2^5*0.2)+(0*2^4*0.2)+(0*2^3*0.2)+(0*2^2*0.2)+(1*2^1*0.2)+(1*2^0*0.2)

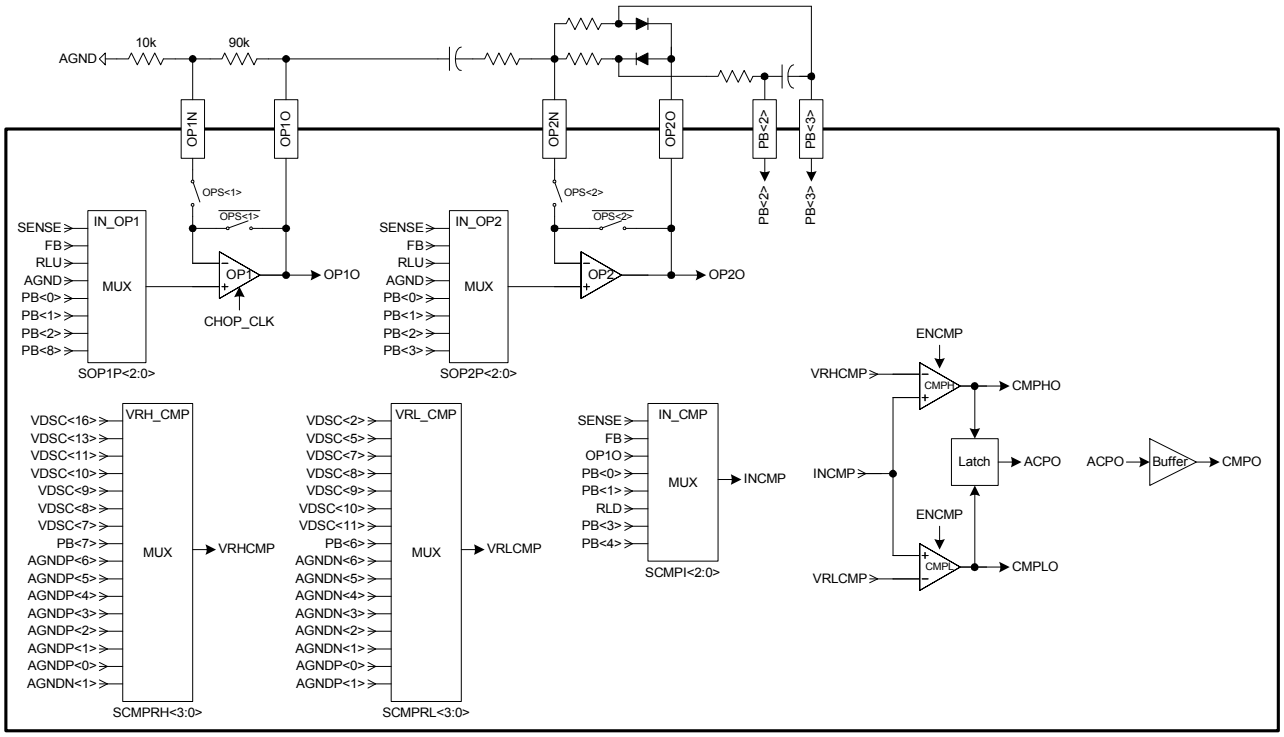
=12.8 + 6.4 + 0 + 0 + 0 + 0.4 + 0.2

=19.8 pF

(6) Register bit SDIO can connect PB<0> and PB<8> pin. This function is implemented to divide measurement voltage when measuring Diode.

(7) Node FB, SENSE, RLU, RLD and PB<8:0> can be measured by ADC through MUX.

12.3. OPAMP and Comparator



Address	Name	Bit<7>	Bit<6>	Bit<5>	Bit<4>	Bit<3>	Bit<2>	Bit<1>	Bit<0>
33h	R33	**OP1CHOP<1:0>**		ENOSC	ENXI	SFT1<1:0>		SAD1I<1:0>	
32h	R32	**ENOP2**	**SOP2P<2:0>**			**ENOP1**	**SOP1P<2:0>**		
25h	R25	AD2IG<1:0>		AD1IG<1:0>		SACM<1:0>		**OPS<2>**	**OPS<1>**
21h	R21	**SCMPRH<3:0>**				**SCMPRL<3:0>**			
20h	R20	**SCMPI<2:0>**			**ENCMP**	ENCNTI	ENPCMPO	ENCTR	0
14h	CTSTA	PCNTI	**ACPO**	**CMPHO**	**CMPLO**	-	-	-	CTBOV

OPAMP:

There are two OPAMP embedded in the IC, namely OP1 and OP2. With combination of external components, it can form amplifying circuit and full-wave rectification circuit.

(1) Register bit OPS<2:1> can determine the negative input pin of OPAMP to be OPXN or OPXO pin.

(2) Register bit ENOP1 and ENOP2 can Enable OP1 and OP2 respectively (it is not shown in the graph). 1=Enable, 0=Disable.

(3) The positive input pin of OPAMP is connected by MUX and is controlled by register bit SOP1P<2:0> and SOP2P<2:0>.

SOP1P<2:0>	000	001	010	011	100	101	110	111
OP1 Positive Input	SENSE	FB	RLU	AGND	PB<0>	PB<1>	PB<2>	PB<8>
SOP2P<2:0>	000	001	010	011	100	101	110	111
OP2 Positive Input	SENSE	FB	RLU	AGND	PB<0>	PB<1>	PB<2>	PB<3>

(4) CHOP_CLK is the chopper clock of OP1, the signal is controlled by register bit OP1CHOP<1:0> as follows：

OP1CHOP<1:0>	00	01	10	11
CHOP_CLK	0	1k Hz square wave	2k Hz Square wave	1

Comparator:

Internally, there are two analog comparator of the IC. CMPH and CMPL form comparators with function of delay and latch that can compare analog and digital signal.

(1) Comparator output, CMPHO, CMPLO and ACPO can be read by register CTSTA. The data can be transmitted and processed in digital units as to measurement frequency and duty cycle.

(2) Comparator input is separately connected by MUX and is controlled by register bit SCMPRH<3:0>, SCMPRL<3:0> and SCMPI<2:0>.

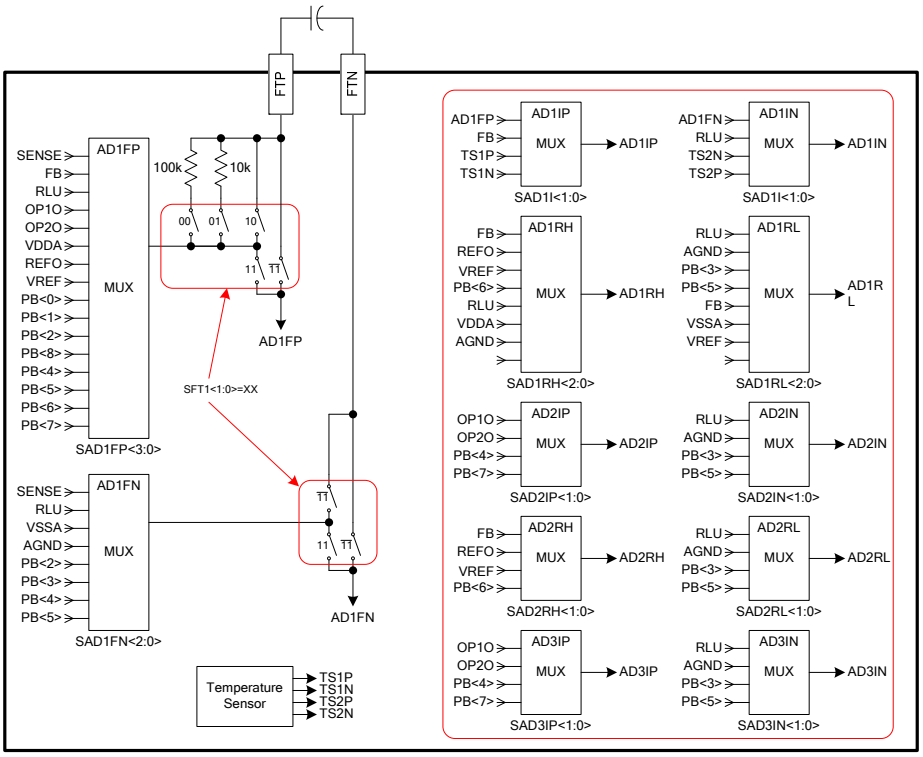
SCMPRH<3:0>	0000	0001	0010	0011	0100	0101	0110	0111
VRHCMP	VDSC<16>	VDSC<13>	VDSC<11>	VDSC<10>	VDSC<9>	VDSC<8>	VDSC<7>	PB<7>
SCMPRH<3:0>	1000	1001	1010	1011	1100	1101	1110	1111
VRHCMP	AGNDP<6>	AGNDP<5>	AGNDP<4>	AGNDP<3>	AGNDP<2>	AGNDP<1>	AGNDP<0>	AGNDN<1>
SCMPRL<3:0>	0000	0001	0010	0011	0100	0101	0110	0111
VRLCMP	VDSC<2>	VDSC<5>	VDSC<7>	VDSC<8>	VDSC<9>	VDSC<10>	VDSC<11>	PB<6>
SCMPRL<3:0>	1000	1001	1010	1011	1100	1101	1110	1111
VRLCMP	AGNDN<6>	AGNDN<5>	AGNDN<4>	AGNDN<3>	AGNDN<2>	AGNDN<1>	AGNDP<0>	AGNDP<1>
SCMPI<2:0>	000	001	010	011	100	101	110	111
INCMP	SENSE	FB	OP1O	PB<0>	PB<1>	RLD	PB<3>	PB<4>

(3) ACPO：ACPO is comparator output after latch.

(4) CMPO：This signal is ACPO output after Buffer. CMPO can control VREF or other switches of analog switch network unit.

(5) ENCMP：Register bit that can enable CMPH and CMPL comparator. 1=Enable, 0=Disable.

12.4. Pre-Filter, ADC Input MUX and Temperature Sensor



Address	Name	Bit<7>	Bit<6>	Bit<5>	Bit<4>	Bit<3>	Bit<2>	Bit<1>	Bit<0>
35h	R35	SAD3IP<1:0>		SAD3IN<1:0>		AD3IG<1:0>		-	0
33h	R33	OP1CHOP<1:0>		ENOSC	ENXI	SFT1<1:0>		SAD1I<1:0>	
28h	R28	-	SAD1RH<2:0>			-	SAD1RL<2:0>		
27h	R27	SAD2IP<1:0>		SAD2IN<1:0>		SAD2RH<1:0>		SAD2RL<1:0>	
24h	R24	SAD1FP<3:0>				SDIO	SAD1FN<2:0>		

ADC input signal and reference signal is connected by MUX. AD1 input stage can select if to pass pre-filter. Moreover, the IC has built-in temperature sensor that can measure IC temperature through AD1.

Pre-Filter:

(1) There is a resistance network of AD1 input stage. Filter is formed by connecting filter capacitor between FTP and FTN. It will help to filer noise and stabilize signal. The positive/negative input signal is connected by MUX. AD1FP and AD1FN represents the positive and negative output signal of the filter respectively and is controlled by register bit SAD1FP<3:0>, SAD1FN<2:0> and SFT1<1:0>.

SAD1FP<3:0>	0000	0001	0010	0011	0100	0101	0110	0111
Filter Positive Input	SENSE	FB	RLU	OP1O	OP2O	VDDA	REFO	VREF
SAD1FP<3:0>	1000	1001	1010	1011	1100	1101	1110	1111
Filter Positive Input	PB<0>	PB<1>	PB<2>	PB<3>	PB<4>	PB<5>	PB<6>	PB<7>
SAD1FN<2:0>	000	001	010	011	100	101	110	111
Filter Negative Input	SENSE	RLU	VSSA	AGND	PB<2>	PB<3>	PB<4>	PB<5>

(2) SFT1<1:0>：Register bit that can select filter resistor as 100K, 10K, 0 or nil, as shown in the above graph.

ADC Input MUX:

Input signal and reference signal of AD1 and AD2 is connected by MUX and is controlled by register bit.

(1) AD1IP and AD1IN：The positive/negative input signal of AD1, controlled by register bit SAD1I<1:0>.

(2) AD1RH and AD1RL：The positive/negative reference signal of AD1, controlled by register bit SAD1RH<2:0> and SAD1RL<2:0> respectively.

(3) AD2IP and AD2IN：The positive/negative input signal of AD2 that controlled by register bit SAD2IP<1:0 and SAD2IN<1:0> respectively.

(4) AD2RH and AD2RL：The positive/negative reference signal of AD2 that controlled by register bit SAD2RH<1:0> and SAD2RL<1:0> respectively.

(5) AD3IP and AD3IN (HY3131 only)：The positive/negative input signal of AD3, controlled by register bit SAD3IP<1:0> and SAD3IN<1:0>.

SAD1I<1:0>	00	01	10	11				
AD1IP	AD1FP	FB	TS1P	TS1N				
AD1IN	AD1FN	RLU	TS2N	TS2P				
SAD1RH<2:0>	000	001	010	011	100	101	110	111
AD1RH	FB	REFO	VREF	PB<6>	RLU	VDDA	AGND	X
SAD1RL<2:0>	000	001	010	011	100	101	110	111
AD1RL	RLU	AGND	PB<3>	PB<5>	FB	VSSA	VREF	X
SAD2IP<1:0>	00	01	10	11				
AD2IP	OP1O	OP2O	PB<4>	PB<7>				
SAD2IN<1:0>	00	01	10	11				
AD2IN	RLU	AGND	PB<3>	PB<5>				
SAD3IP<1:0>	00	01	10	11				
AD3IP	OP1O	OP2O	PB<4>	PB<7>				
SAD3IN<1:0>	00	01	10	11				
AD3IN	RLU	AGND	PB<3>	PB<5>				
SAD2RH<1:0>	00	01	10	11				
AD2RH	FB	REFO	VREF	PB<6>				
SAD2RL<1:0>	00	01	10	11				
AD2RL	RLU	AGND	PB<3>	PB<5>				

Temperature Sensor:

A temperature sensor is built-in in the IC. It has two output voltage sets, (TS1P, TS2N) and (TS1N, TS2P) that can be measured by AD1. The temperature calculation is as follows：

(1) Configure SAD1I<1:0>=10, a digital code: TCode1 is obtained after AD1 measurement.

(2) Configure SAD1I<1:0>=11, a digital code: TCode2 is obtained after AD1 measurement.

(3) Calculate TCode=(TCode2 - TCode1)/2. It helps to erase Temperature Sensor Offset.

(4) Supposed a single point is calibrated at 25℃, TCode@25℃ is obtained. One offset is added in because the temperature sensor itself has offset. The slope of a temperature curve G is obtained as follows：

$$G = \frac{TCode@25^{o}C}{25 + 273.15 + T_{OS}}$$, TOS is offset, approx. -3.15^{O}K.

(5) Supposed the temperature to be measured is TX℃ :

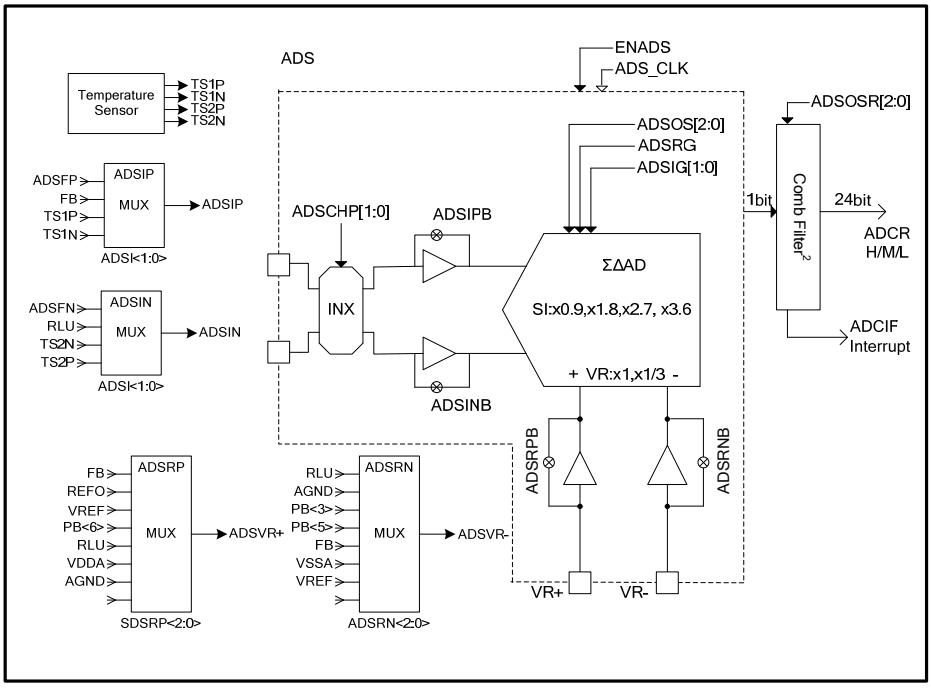
$$T_X = \frac{TCode@T_X{}^{o}C}{G} - [273.15 + T_{OS}] \quad {}^{o}C$$

ADC Set default value:

AD1RH: REFO; AD1RL: AGND; AD1IG: 3.6; AD1IPBUF disable; AD1INBUF disable; AD1RG: 1;

13. ΣΔADC, Low Pass Filter, RMS Converter and Peak Hold

13.1. High Resolution ADC(AD1)



Address	Name	Bit<7>	Bit<6>	Bit<5>	Bit<4>	Bit<3>	Bit<2>	Bit<1>	Bit<0>
25h	R25	AD2IG<1:0>		AD1IG<1:0>		SACM<1:0>		OPS<2>	OPS<1>
23h	R23	ENAD1	-	0	AD1RG	AD1RHBUF	AD1RLBUF	AD1IPBUF	AD1INBUF
22h	R22	AD1OS<2:0>			AD1CHOP<1:0>		AD1OSR<2:0>		

AD1 is High Resolution ADC. AD1IP and AD1IN is positive/negative input signal, AD1RH and AD1RL is positive/negative reference signal.

(1) ENAD1[7]：Register bit that can enable AD1. 1=Enable, 0=Disable and clear AD1<23:0> as 0.

(2) AD1CHOP<1:0>：Register bit that can configure Chop AD1 input signal, the result is reflected at the output AD1<23:0> of AD1.

Supposed VOS is the Offset output code of AD1, VX is the output code of AD1 Zero Offset. When using different AD1CHOP configuration, ADC output code is shown as below table. When AD1CHOP=1x, ADC switches input signal based on OSR configured time. To erase Offset function, ADC output rate will be one time slower at the same time.

AD1CHOP<1:0>	00	01	10	11
AD1<23:0>	VX+VOS	VX-VOS	VX	VX

(3) AD1IG<1:0>：Register bit that can configure Gain of AD1 input signal.

(4) AD1RG：Register bit that can configure Gin of AD1 reference signal.

AD1IG<1:0>	00	01	10	11
AD1 Input Gain	0.9	1.8	2.7	3.6

AD1RG	0	1
AD1 Reference Gain	1.0	0.333

(5) AD1OS<2:0>：Register bit that can configure DVOS of zero input voltage. If the signal to be measured is not symmetrical, using this function enables AD1 to operate in a better range.

[7] When AD1 and AD2/AD3 is on, users must not turn on/off AD to avoid different AD1 Offset problem.

AD1OS<2:0>	000	001	010	011	100	101	110	111
DCOS	0	0.25	0.5	0.75	0	-0.25	-0.5	-0.75

Supposed VIN is the input signal of AD1, VR is the reference signal of AD1, IG is the gain of AD1 input signal and RG is the Gain of AD1 reference signal. Then, $AD1<23:0>=\frac{IG \bullet VIN}{RG \bullet VR}+\frac{DCOS}{RG}$.

(6) AD1IPBUF：Register bit that can configure whether positive input signal of AD1 passes through Buffer. 1=Enable；0=Disable.

(7) AD1INBUF：Register bit that can configure whether negative input signal of AD1 passes through Buffer. 1=Enable；0=Disable.

(8) AD1RHBUF：Register bit that can configure whether positive input signal of AD1 passes through Buffer. 1=Enable；0=Disable.

(9) AD1RLBUF：Register bit that can configure whether negative input signal of AD1 passes through Buffer. 1=Enable；0=Disable.

(10) AD1CLK：Sampling signal of Modulator1, of which the frequency is fixed at FSYSCLK/30. FSYSCLK is the frequency of SYSCLK.

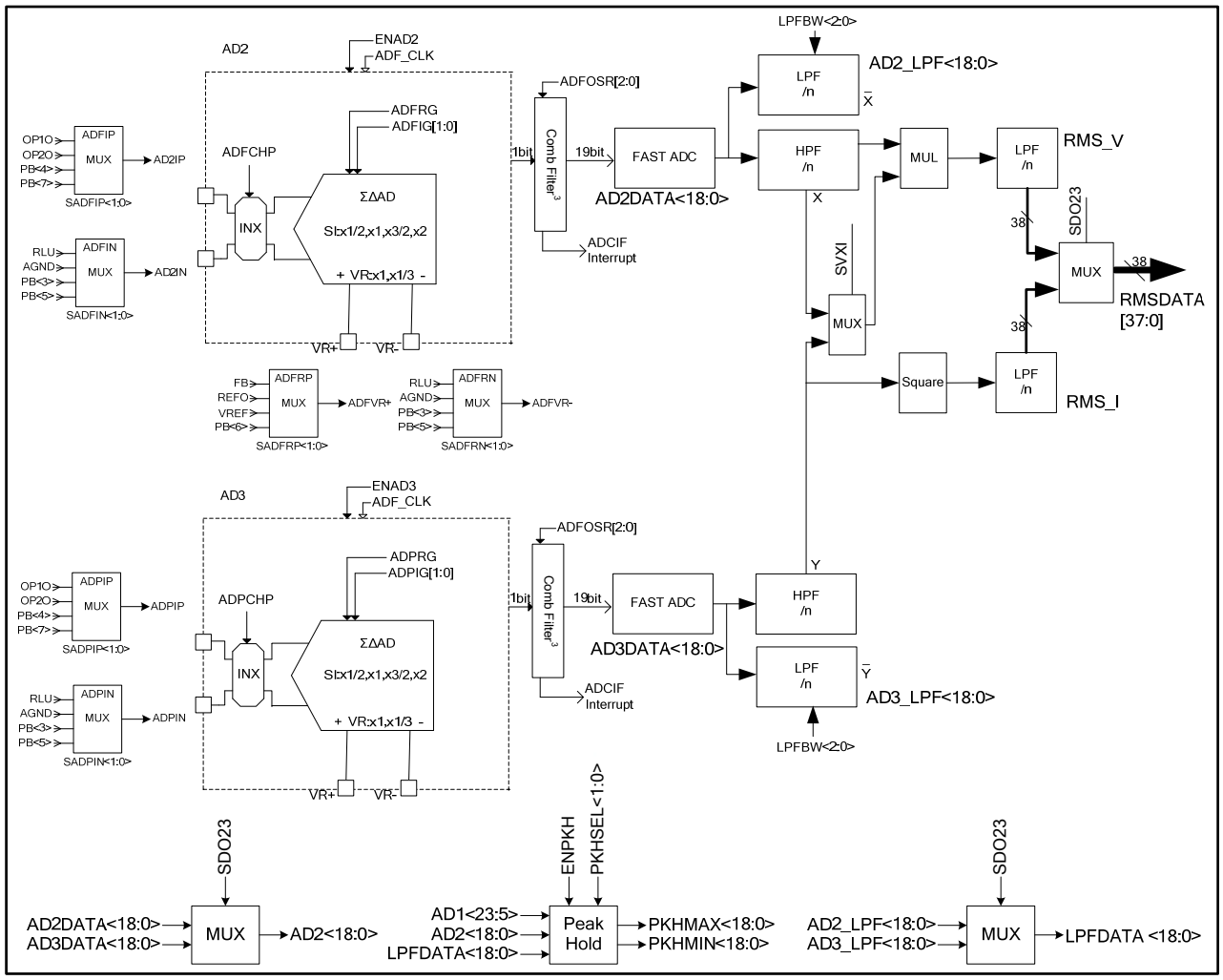
(11) AD1OSR<2:0>：Register bit that can configure Over Sampling Ratio (OSR1) of AD1 Comb Filter. AD1 data output rate=FAD1CLK/OSR1. FAD1CLK is the frequency of AD1CLK.

AD1OSR<1:0>	000	001	010	011	100	101	110	111
OSR1	256	512	1024	2048	4096	8192	16384	32768

(12) AD1<23:0>：Data register of AD1 output, totally there are 24 bits.

(13) AD1F：Flag of the occurred AD1 events, this signal will be transmitted to INTF register.

13.2. High Speed ADC(AD2 & AD3), Low Pass Filter, RMS Converter and Peak Hold



Address	Name	Bit<7>	Bit<6>	Bit<5>	Bit<4>	Bit<3>	Bit<2>	Bit<1>	Bit<0>
36h	R36	SPHACAL<7:0>							
35h	R35	SAD3IP<1:0>		SAD3IN<1:0>		AD3IG<1:0>		-	0
34h	R34	ENAD3	0	ENCHOPAD3	AD3RG	SVXI	SDO23	0	0
29h	R29	ENRMS	ENLPF	LPFBW<2:0>			ENPKH	PKHSEL<1:0>	
26h	R26	ENAD2	0	ENCHOPAD2	AD2RG	SAD2CLK	AD2OSR<2:0>		
25h	R25	AD2IG<1:0>		AD1IG<1:0>		SACM<1:0>		OPS<2>	OPS<1>

AD2:

AD2 is High Speed ADC. AD2IP and AD2IN is the positive/negative input signal[8] while AD2RH and AD2RL is the positive/negative reference signal.

(1) ENAD2：Register bit that can Enable AD2. 1=Enable；0=Disable and clear AD2<18:0> as 0.

(2) ENCHOPAD2：Register bit that can Enable Chop input signal of AD2.1=Enable, 0=Disable. When starting AD2 Chop configuration to realize Offset erase function, ADC output rate will be one time slower.

(3) AD2IG<1:0>：Register bit that can configure input signal gain of AD2.

(4) AD2RG：Register bit that can configure reference signal gain of AD2.

[8] When AD2 and AD3 is used at the same time, it is suggested to connect AD2IN and AD3IN to AGND or to different PB<x> input.

AD2IG<1:0>	00	01	10	11	AD2RG	0	1
AD2 Input Gain	0.5	1.0	1.5	2.0	AD2 Reference Gain	1.0	0.333

(5) AD2CLK：Sampling signal of Modulator2, of which frequency is selected by register bit SAD2CLK. SAD2CLK=0：FAD2CLK=FSYSCLK/2； SAD2CLK=1：FAD2CLK=FSYSCLK/4. FSYSCLK is the frequency of SYSCLK; FAD2CLK is the frequency of AD2CLK.

(6) AD2OSR<2:0>：Register bit that can configure Over Sampling Ratio (OSR2) of AD2 Comb Filter. AD2 data output rate=FAD2CLK/OSR2.

AD2OSR<2:0>	000	001	010	011	100	101	110	111
OSR2	32	64	128	256	512	1024	1024	1024

(7) AD2<18:0>：Output data of AD2, totally there are 19 bits.

(8) AD2F：Flag of the occurred AD2 events, this signal will be transmitted to INTF register.

(9) SPHACAL<7:0> (HY3131 only)：Register bit that can calibrate AD2 phase. This function is to measure Power, set AD2 and AD3 output in the same phase. When using this function, SPHACAL<7:0> must be set first, then set ENAD2 and ENAD3 as 1, otherwise the data would be stabilized later.

SPHACAL<7>：This bit can set to lead or to follow. 0：AD2 output will fall behind AD3 output；1：AD2 output will lead AD3 output.

SPHACAL<6:0>：This bit can set the time (T) of leading or following.

$$T = \sum_{n=0}^{6} 2^n \bullet SPHACAL<n> \bullet \frac{1}{F_{AD2CLK}}$$, F_{AD2CLK} is the frequency of AD2CLK.

AD3 (HY3131 only):

AD3 is the second High Speed ADC. AD3IP and AD3IN are the positive/negative input signal.AD2RH and AD2RL are the positive/negative reference signal, in common with AD2.

(1) ENAD3：Register bit that can enable AD3. 1=Enable；0=Disable and clear AD3DATA<18:0> to 0.

(2) ENCHOPAD3：Register bit that can enable Chop AD3 input signal.1=Enable, 0=Disable. When starting AD3 Chop configuration to realize Offset erase function, ADC output rate will be one time slower at the same time.

(3) AD3IG<1:0>：Register bit that can set AD3 input signal Gain.

(4) AD3RG：Register bit that can set AD3 reference signal Gain.

AD3IG<1:0>	00	01	10	11	AD3RG	0	1
AD3 Input Gain	0.5	1.0	1.5	2.0	AD3 Reference Gain	1.0	0.333

(5) AD2CLK：Modulator3 sampling signal, in common with AD2, can be selected by register bit, SAD2CLK. SAD2CLK=0：$F_{AD2CLK}=F_{SYSCLK}/2$；SAD2CLK=1：$F_{AD2CLK}=F_{SYSCLK}/4$. F_{SYSCLK} is the frequency of SYSCLK, F_{AD2CLK} is the frequency of AD2CLK.

(6) AD2OSR<2:0>：Register bit that can set Over Sampling Ratio(OSR3) of AD3 Comb Filter, in common with AD2.

AD3 data output rate=F_{AD2CLK}/OSR3.

AD2OSR<2:0>	000	001	010	011	100	101	110	111
OSR3	32	64	128	256	512	1024	1024	1024

(7) AD3DATA<18:0>：AD3 output data, 19 bits.

(8) AD2F：The flag when AD3 event occurred. This signal will be sent to INTF register, in common with AD2.

MUX (HY3131 only):

(1) SDO23：Register bit, can select data that enters into data register, AD2<18:0>, LPF<18:0> and RMS<37:0>.

(2) AD2<18:0>：Data register of High Speed ADC. This data can be selected as AD2DATA<18:0> or AD3DATA<18:0>, controlled by register bit, SDO23.

SDO23=0：AD2<18:0>= AD2DATA<18:0>；SDO23=1：AD2<18:0>= AD3DATA<18:0>.

Low Pass Filter:

(1) ENLPF：Register bit that can Enable Low Pass Filter. 1=Enable；0=Disable and clear LPF<18:0> as 0.

(2) SDO23： Register bit that can select Low Pass Filter output as LPF[AD2DATA<18:0>] or LPF[AD3DATA<18:0>].

0：LPF[AD2DATA<18:0>]；1：LPF[AD3DATA<18:0>].

(3) LPFBW<2:0>：Register bit that can configure Over Sampling Ratio (OSR4) of Low Pass Filter.

Low Pass Filter data output rate=data input rate/OSR4.

LPFBW<2:0>	000	001	010	011	100	101	110	111
OSR4	128	256	512	1024	2048	4096	8192	16384

(4) LPF<18:0>：Data register of Low Pass Filter output.

(5) LPFF：Flag of the occurred Low Pass Filter events, this signal will be transmitted to INTF register.

RMS Converter:

(1) ENRMS：Register bit that can Enable RMS Converter. 1=Enable；0=Disable and clear RMS<37:0> as 0.

(2) RMS<37:0>：Data register of RMS Converter output.

RMS data output rate=Low Pass Filter data output rate.

(3) SDO23 and SVXI (HY3131 only)：Register bit, the combination of both SDO23 and MULFP can select RMS Converter output data.

Supposed X=AD2DATA<18:0> is the data that passed High Pass Filter, Y=AD3DATA<18:0> is the data that passed High Pass Filter.

N=Low Pass Filter OSR, configured by LPFBW<2:0>, and:

SDO23	0	0	1	1
SVXI	0	1	0	1
RMS<37:0>	$\Sigma X^2/N$	$\Sigma XY/N$	$\Sigma Y^2/N$	$\Sigma Y^2/N$

To get the desired RMS value, it is necessary to square root by external MCU software.

(4) RMSF：Flag of the occurred RMS Converter events, this signal will be transmitted to INTF register.

Peak Hold:

(1) ENPKH：Register bit that can Enable Peak Hold. 1=Enable；0=Disable and clear PKHMAX<18:0> as 40000h, PKHMIN<18:0> as 3FFFFh.

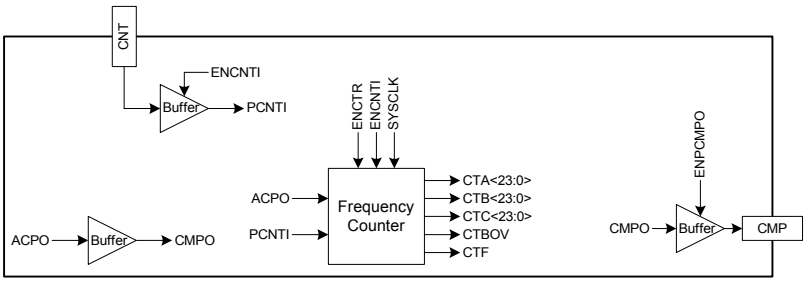
(2) PKHSEL<1:0>：Register bit that can select Peak Hold input to be AD1<23:5>, AD2<18:0> or LPF<18:0>.

PKHSEL<1:0>	00	01	10	11
Peak Hold Input	AD2<18:0>	AD1<23:5>	LPF<18:0>	LPF<18:0>

(3) PKHMAX<18:0>：Data register of Peak Hold max. output value. Default value=40000h.

(4) PKHMIN<18:0>：Data register of Peak Hold min. output value. Default value=3FFFFh.

14. Frequency Counter, CNT and CMP Pin



Address	Name	Bit<7>	Bit<6>	Bit<5>	Bit<4>	Bit<3>	Bit<2>	Bit<1>	Bit<0>
20h	R20	SCMPI<2:0>			ENCMP	ENCNTI	ENPCMPO	ENCTR	0
14h	CTSTA	PCNTI	ACPO	CMPHO	CMPLO	-	-	-	CTBOV

Frequency Counter:

Frequency Counter can select ACPO or PCNTI to be input source. Output data will be written to data register CTA<23:0>, CTB<23:0> and CTC<23:0>. By reading data register, it can calculate signal frequency and Duty Cycle.

(1) ENCTR：Register bit that can Enable Frequency Counter. 1=Enable；0=Disable and clear CTA<23:0>, CTB<23:0>, CTC<23:0> and CTBOV as 0.

(2) ENCNTI：Register bit that can Enable CNT Buffer and can select input source of Frequency Counter.

ENCNTI	0	1
Frequency Counter Input	ACPO	PCNTI

(3) PCNTI：CNT Buffer output, it will be transmitted to register CTSTA<7>.

(4) CTA<7:0>：Register bit. When ENCTR=0, CTA<7:0> will be cleared 0.

(5) CTA<23:8>：Register bit. When ENCTR=0, CTA<23:8> will not be cleared 0. When ENCTR=0, CTA<23:8> can write in data through SPI only. When ENCTR=1, CTA<23:8> can write in data through Frequency Counter.

(6) CTB<23:0>：Data register. When ENCTR=0, it will be cleared 0. When ENCTR=1 and interrupt occurred after counting complete, it will record the whole cycle amount of the signal to be measured. And can be implemented to calculate frequency of the signal to be measured.

(7) CTC<23:0>：Data register. When ENCTR=0, it will be cleared 0. When ENCTR=1 and interrupt occurred after counting complete, it will record SYSCLK amount of the signal to be measured while it is in High. And can be used to calculate Duty Cycle of the signal to be measured.

(8) CTBOV：Register bit. When CTB<23:0> is Over Flow, it will be set as 1. Reading CTSTA register or ENCTR=0, it will be set 0.

(9) CTF：Flag of the occurred Frequency Counter event; this signal will be transmitted to INTF register.

(10) SYSCLK is the system clock.

Frequency Counter is operated as follows：

(1) Configure ENCTR=0, CTA<7:0> will be set 0.

(2) Configure the initial value of counting at CTA<23:8>, the default counting time: Gate Time=[1000000h-CTA<23:0>]/FSYSCLK.

(3) Configure ENCTR=1, counting starts. When CTA<23:0> Over Flow, CTA<23:0> continues counting until CTB<23:0> records the whole cycle amount of signal to be measured, then it will stop counting.

(4) Waiting for interrupt.

(5) Ceased counting after interrupt occurrence.

(6) Readout CTA<23:0>, CTB<23:0>, CTC<23:0> and CTBOV.

(7) If CTBOV=1, it means Gate Time configuration is too long but the frequency of signal to be measured is high, so CTB<23:0> is Over Flow. This counting record is meaningless. It must restart from step (1) and reconfigure Gate Time and count again.

(8) If CTBOV=0, it means this counting record is meaningful. It can measure the Duty Cycle frequency of signal to be measured.

Total counting time T=[1000000h-CTA<23:0>Initial+ CTA<23:0>Final]/F_{SYSCLK}

Frequency of signal to be measured=CTB<23:0>/T

Duty Cycle of signal to be measure =CTC<23:0>/[1000000h-CTA<23:0>$_{Initial}$+ CTA<23:0>$_{Final}$]

FSYSCLK is the frequency of SYSCLK, CTA<23:0>Initial is the setup value before counting, CTA<23:0>$_{Finalis}$ is the readout value after counting finished.

CNT and CMP pin:

CNT Pin is digital input pin. Signals can be inputted through these pins and transmitted the signal to Frequency Counter for measurement. CMP Pin is digital output pin. CMPO signal of the IC can output to CMP Pin.

(1) ENCNTI：Register bit that can Enable CNT Buffer. 1=Enable；0=Disable. It can also select input source of Frequency Counter.

(2) PCNTI：CNT Buffer output and can be transmitted to register CTSTA<7>.

(3) ENPCMPO：Register bit that can Enable CMP Pin Buffer. 1=Enable；0=Disable.

15. Reference Documents

For HY313X Configurations, please refer to APD-DMM003_EN.

16. Ordering Information

Device No.[1]	Package Type	Pins	Package Drawing		Shipment Packing Type	Unit Q'ty	Material Composition	MSL[2]
HY3130-L048	LQFP	48	L	048	Tray	250	Green[3]	MSL-3
HY3131-L044	LQFP	44	L	044	Tray	160	Green[3]	MSL-3
HY3131-L048	LQFP	48	L	048	Tray	250	Green[3]	MSL-3

[1] **Device No.: Model No. – Package Type Description** (Standard Parts)

Ex: You request HY3131 in LQFP44 package.

The device no will be HY3131-L044.

And please clearly indicate the shipment packing type when placing orders.

Ex: You request HY3131 in LQFP48 package.

The device no will be HY3131-L048.

And please clearly indicate the shipment packing type when placing orders.

[2] **MSL:**

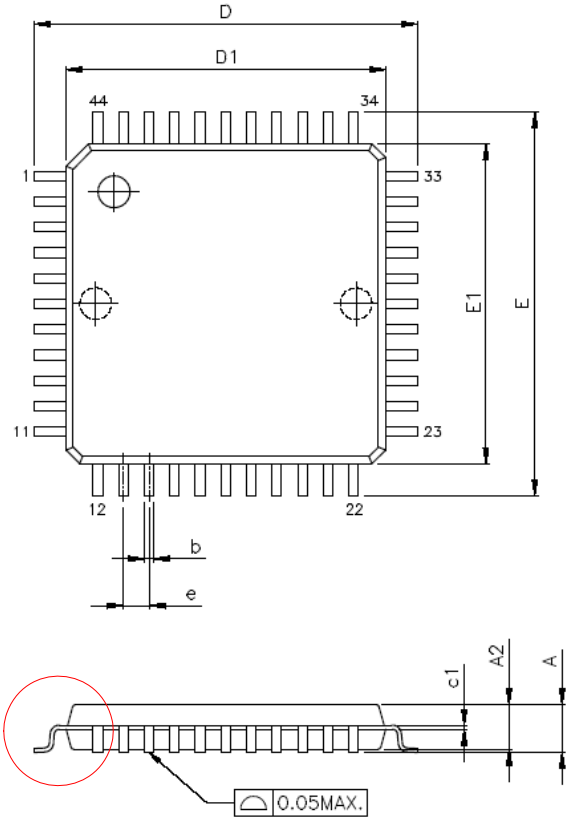
The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

[3] **Green (RoHS & no Cl/Br):**

HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br/Cl<0.1%).

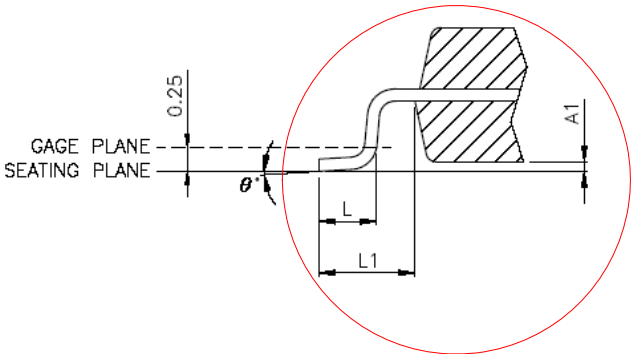
17. Packaging Information

LQFP44 (L044)



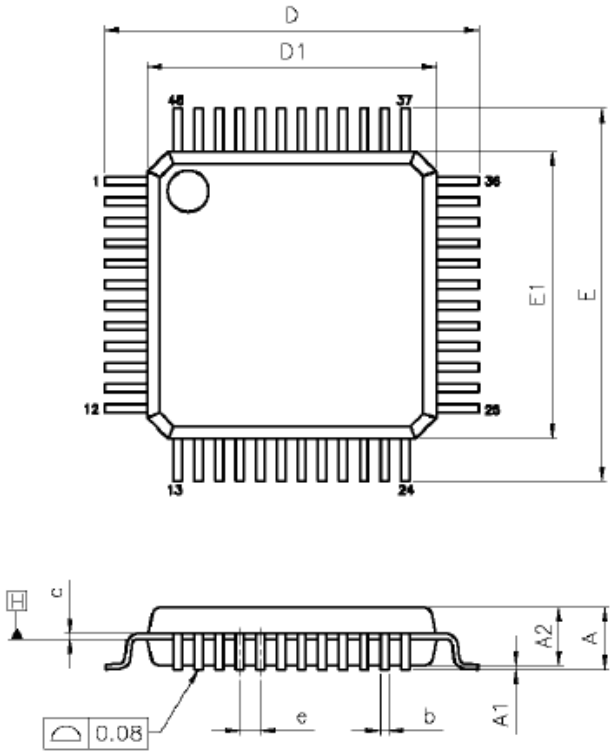
VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
c1	0.09	—	0.16
D		12.00 BSC	
D1		10.00 BSC	
E		12.00 BSC	
E1		10.00 BSC	
e		0.80 BSC	
b	0.30	0.37	0.45
L	0.45	0.60	0.75
L1		1.00 REF	
θ°	0°	3.5°	7°



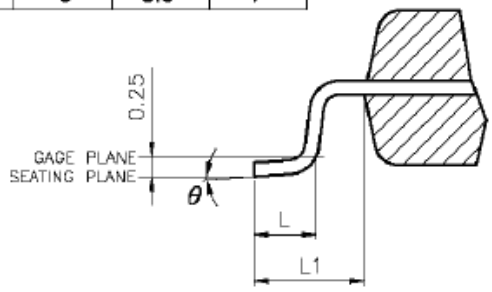
JEDEC MS-026 Compliant

LQFP48 (L048)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D		9.00 BSC	
D1		7.00 BSC	
E		9.00 BSC	
E1		7.00 BSC	
e		0.50 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°



JEDEC MS-026 Compliant

18. Revision Record

Major differences are stated thereinafter:

Version	Page	Revision Summary
V03	All	First edition
V05	5, 7~9	Revise ACM notice and add in new pin definition
	32	Remove Example circuit to reference documents: APD-DMM003_EN HY313X Configurations
	33	Revise Ordering information content
	35	Add in new package type
V06	All	Enhanced HY3131 functionality, adding High Speed ADC3 and function description
V07	11	Add in OP specification
	14~15	Supplement SPI communication description
	21	AGNDP<n> and AGNDN<n> description
	23	Add Capacitor Array description and example
	29	Add AD1CHOP description
	31	Revise AD2/AD3 internal Block diagram
	31~32	Add ENCHOPAD2 及 ENCHOPAD3 description
	29, 31	Application caution for AD1/AD2/AD3
V10	All	Add HY3130 Difference
	12	Revise AD Gain Temperature drift, Chapter 6
	12	Revise ADC1 Linearity Specification, Chapter 6
	12	Revise ADC Current Consumption, Chapter 6
	23	Recommend ACM Voltage
	21,22	VSS figure changed to VSSA, and VDD figure changed to VDDA
	27~30	