HYCON TECHNOLOGY

HY16F198/HY16F198B

規格書

高精密混合信號處理控制器

4X36 ~ 6X34 LCD Driver

32-bit 低功耗微控制器

21-bit ENOB ΣΔADC

64KB Flash ROM

目錄

1. 特性 5
2. 管腳名稱定義 7
2.1 HY16F198/HY16F198B系列管腳圖 7
2.2HY16F197/HY16F197B系列管腳圖 10
2.3 HY16F196/HY16F196B系列管腳圖 12
2.4 引腳功能描述 14
2.4.1 HY16F19x與HY16F19xB系列引腳定義 14
2.4.2 管腳複用功能及複用功能優先級 24
2.5 封裝片標記訊息 26
2.5.1 HY16F198/HY16F198B LQFP封裝片標記訊息 26
2.5.2 HY16F198/HY16F198B QFN封裝片標記訊息 27
3.1 橋式傳感器應用電路 28
3.2 血壓傳感器應用電路 29
3.3 電化學傳感器應用電路 30
3.4 觸控按鍵應用電路 31
3.5 三合一血糖計應用電路 32
4. 功能概述 33
4.1 內部框圖 33
4.2 中央處理器核心方框圖 34
4.3 相關的支援文檔 34
4.4 時鐘系統網絡 35
4.5 電源系統網絡 36
4.6 24-bit ΣΔADC 網絡 37
4.7 軌對軌運算放大器OPAMP網絡 38
4.8 8-bit Resistance Ladder網絡 39
4.9 多功能比較器CMP網絡 40
4.10 看門狗(WDT)網絡 41
4.11 定時計數器 A 網絡 42
4.12 定時計數器B 網絡 43
4.13 定時計數器C 網絡 44
4.14 定時計數器B2 網絡 45
4.15 32-bit SPI 網絡 46
4.16 UART 網絡 47
4.17 I2C 網絡 48
4.18 硬體時鐘RTC網絡 48

4.19 LCD網路 49
5. Electrical Characteristics 50
5.1 Recommended Operating Conditions 50
5.2 Clock System 53
5.3 Power Management System 55
5.4 Charge Pump System 57
5.5 Reset Management System 58
5.6 GPIO Port System 59
5.7 ΣΔADC ENOB and RMS Noise 60
5.8 ADC Management System 62
5.9 Internal Temperature Sensor 63
5.10 8-Bit Resistance Ladders 64
5.11 OPAMP Management System 66
5.12 CMP Management System 67
5.13 LCD System 68
6. 訂貨資訊 69
6.1 HY16F19x系列選型編碼 69
6.2 HY16F19xB系列選型編碼 69
7. 封裝尺寸資訊 71
7.1 LQFP100 封裝圖 71
7.2 LQFP64 封裝圖 72
7.3 QFN88 封裝圖 73
7.4 QFN68 封裝圖 75
8. HY16F19xB 性能升級說明 77
9. 修改記錄 79

注意：

1、本說明書中的內容，隨著產品的改進，有可能不經過預告而更改。請客戶及時到本公司網站下載更新 http://www.hycontek.com

2、本規格書中的圖形、應用電路等，因第三方工業所有權引發的問題，本公司不承擔其責任。

3、本產品在單獨應用的情況下，本公司保證它的性能、典型應用和功能符合說明書中的條件。當使用在客戶的產品或設備中，以上條件我們不作保證，建議客戶做充分的評估和測試。

4、請注意輸入電壓、輸出電壓、負載電流的使用條件，使 IC 內的功耗不超過封裝的容許功耗。對於客戶在超出說明書中規定額定值使用產品，即使是瞬間的使用，由此所造成的損失，本公司不承擔任何責任。

5、本產品雖內置防靜電保護電路，但請不要施加超過保護電路性能的過大靜電。

6、本規格書中的產品，未經書面許可，不可使用在要求高可靠性的電路中。例如健康醫療器械、防災器械、車輛器械、車載器械及航空器械等對人體產生影響的器械或裝置，不得作為其部件使用。

7、本公司一直致力於提高產品的品質和可靠度，但所有的半導體產品都有一定的失效概率，這些失效概率可能會導致一些人身事故、火災事故等。當設計產品時，請充分留意冗餘設計，採用安全指標，這樣可以避免事故的發生。

8、本規格書中內容，未經本公司許可，嚴禁用於其他目的之轉載或複製。

1. 特性

數字量

- 32-bit 1T Andes Core N801 內核
- 支援 C 開發環境指令集
- 寬工作電壓 2.2V to 3.6V.
- 工作溫度-40 to 85℃
- 低功耗:
  - 運行模式: 350uA/MIPS@3.3V
  - 低速運行模式: 10uA@17KHz & 3.3V
  - 休眠模式: 2.5uA@3.3V
- 64KB Flash ROM
- 8KB SRAM
- 16-bit Timer A, Timer B(X2), Timer C
- 16-bit PWM 控制器及訊號捕抓功能
- 硬體實現 I2C/32-bit SPI/UART(X2) 通訊介面
- 硬體實現時鐘 RTC
- 32 個可編程複用型 I/O
  - 16 個通用型數位輸出入埠
  - 16 個可選擇 LCD 埠或數位輸出入埠
- 4x36 ~ 6x34 LCD 液晶驅動器
  - 1/3、1/4、1/5、1/6 Duty 及 1/3 Bias 選擇
  - 支援 R Type 驅動方式
  - 內建 Charge Pump 穩壓線路，提供 4 段 VLCD 偏壓，3.3V, 3.0V, 2.8V, or 2.6V

模擬量

- 內建低雜訊 24-bit Σ ADC
  - 輸入參考雜訊低至 65nVrms
  - 轉換率高達 10KSPS
  - 輸入放大倍率高達 128
  - 工作電壓為 2.4V to 3.6V
- 外部高速晶震頻率高達 16MHz
- 外部低速晶震低至 32768Hz
- 內建 RC 高速震盪器頻率高達 16MHz
- 內建 RC 低速震盪器頻率低至 35KHz
- 電源模塊
  - 電荷泵升壓穩壓電源(CP_O)
  - 內建四段可調整穩壓電源(VDDA)
  - 1.2V 帶隙參考電壓(REFO)
- 8-BIT 可編程數位電阻器
  - 可編程電阻分壓計
  - 電阻保證單調性
- 軌對軌運算放大器 OPAMP
  - CMOS 輸入，1MHz 增益帶寬
  - 可用作比較器
- 多功能比較器 Comparator
  - 支持觸控按鍵測量
  - 低電壓檢測電路

Part No.	Flash ROM (kb)	SRAM (kb)	ΣΔADC VIN Ch.	I/O	Touch Key (Ch.)	LCD		Charge pump	ISP Mode	Package	Others: (All the products have the same IP)
						COM	SEG				
HY16F196-L064	16	2	8	20+22	6	4~6	24~22	Y	N	LQFP64	Analog Parts: One hardware RTC and calendar. One 8-bit resistance ladders for DAC. One rail-to-rail OPAMP. One multi-function comparator. One built-in temperature sensor. Digital Parts: One 32-bit programmable SPI One IIC(master and slave mode.) Two enhanced UART Four channels PWM function,
HY16F196-N068	16	2	8	20+26	6	4~6	28~26	Y	N	QFN68	
HY16F197-L064	32	4	5	20+24	6	4~6	26~24	Y	N	LQFP64	
HY16F197-N068	32	4	5	20+28	6	4~6	30~28	Y	N	QFN68	
HY16F198-L100	64	8	8	24+34	8	4~6	36~34	Y	N	LQFP100	
HY16F198-N088	64	8	8	24+34	8	4~6	36~34	Y	N	QFN88	
HY16F198-L064	64	8	6	24+24	8	4~6	26~24	N	N	LQFP64	
HY16F196B-L064	16	2	8	20+22	6	4~6	24~22	Y	Y	LQFP64	
HY16F196B-N068	16	2	8	20+26	6	4~6	28~26	Y	Y	QFN68	
HY16F197B-L064	32	4	5	20+24	6	4~6	26~24	Y	Y	LQFP64	
HY16F197B-N068	32	4	5	20+28	6	4~6	30~28	Y	Y	QFN68	
HY16F198B-L100	64	8	8	24+34	8	4~6	36~34	Y	Y	LQFP100	
HY16F198B-N088	64	8	8	24+34	8	4~6	36~34	Y	Y	QFN88	
HY16F198B-L064	64	8	6	24+24	8	4~6	26~24	N	Y	LQFP64	

Note: HY16F19xB 與 HY16F19x 為相同封裝，性能升級說明可參考章節 8

2. 管腳名稱定義

2.1 HY16F198/HY16F198B 系列管腳圖

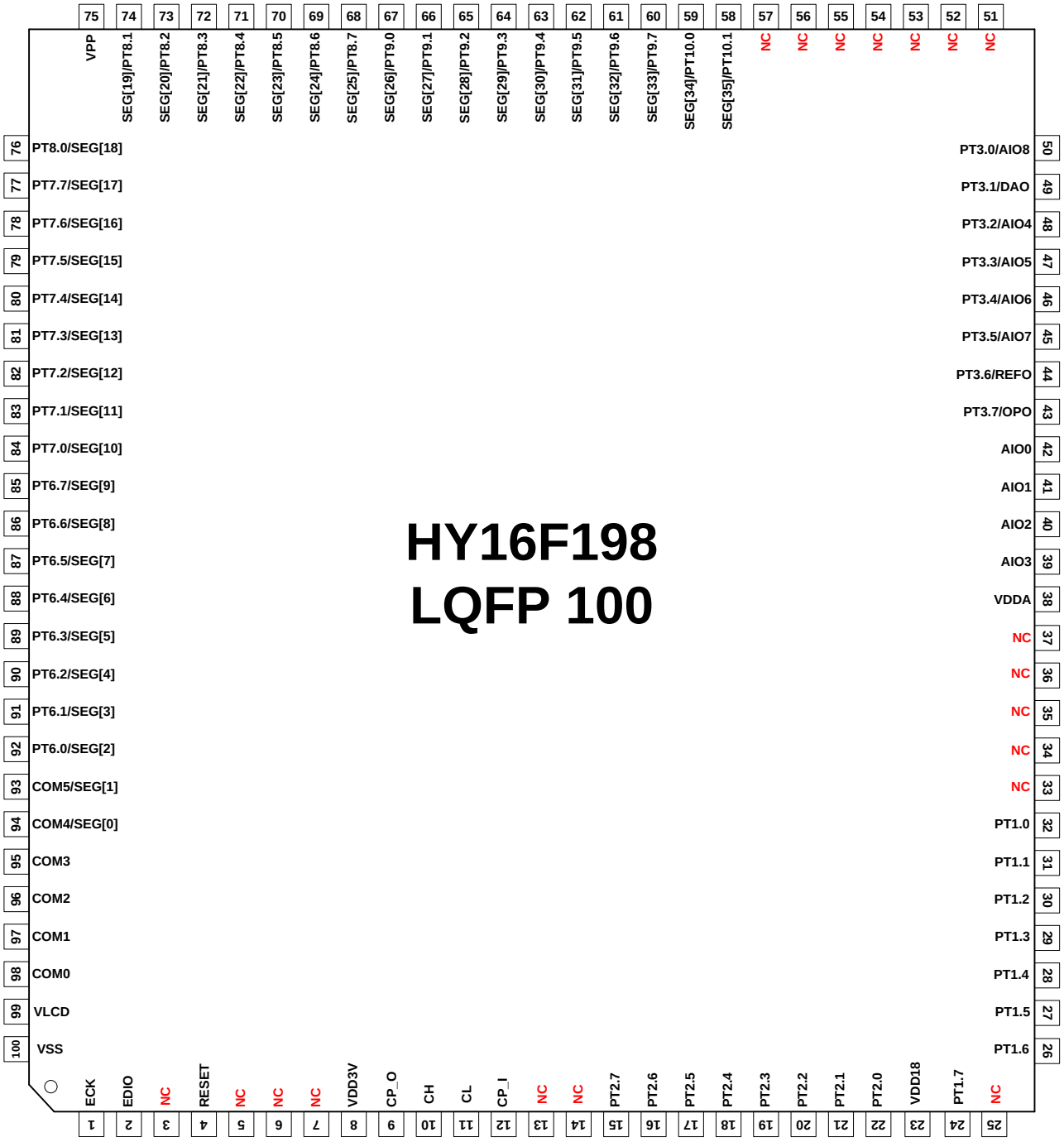


圖 2-1-1 HY16F198/HY16F198B LQFP 100 管腳圖

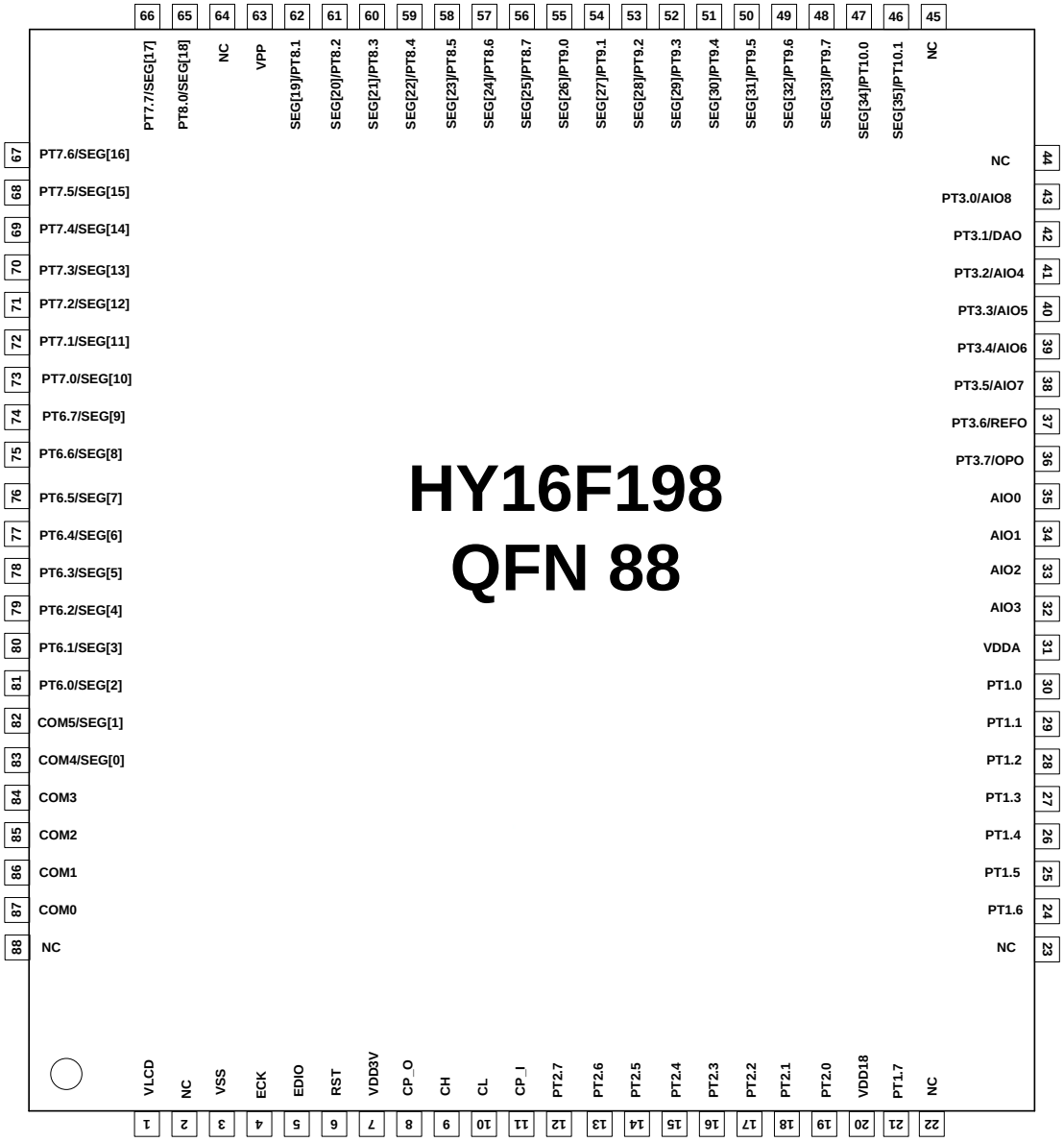


圖 2-1-2 HY16F198/HY16F198B QFN88 管腳圖

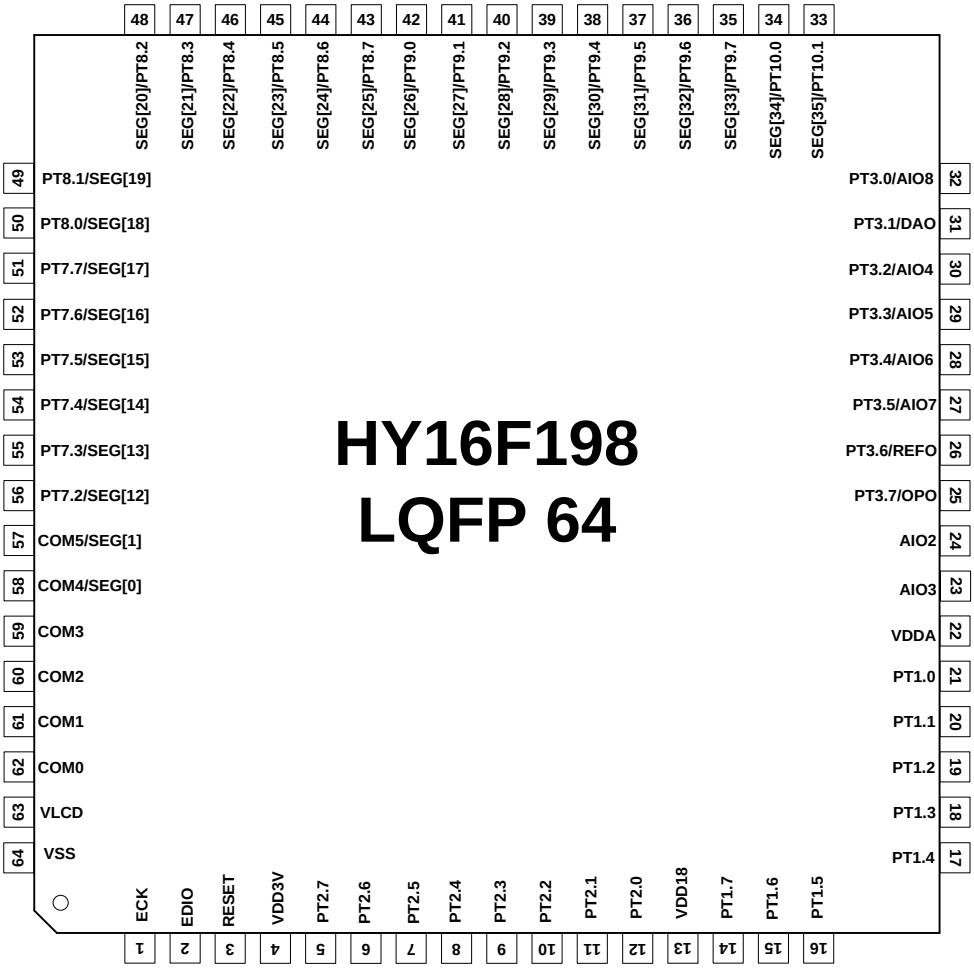


圖 2-1-3 HY16F198/HY16F198B LQFP64 管腳圖

2.2HY16F197/HY16F197B 系列管腳圖

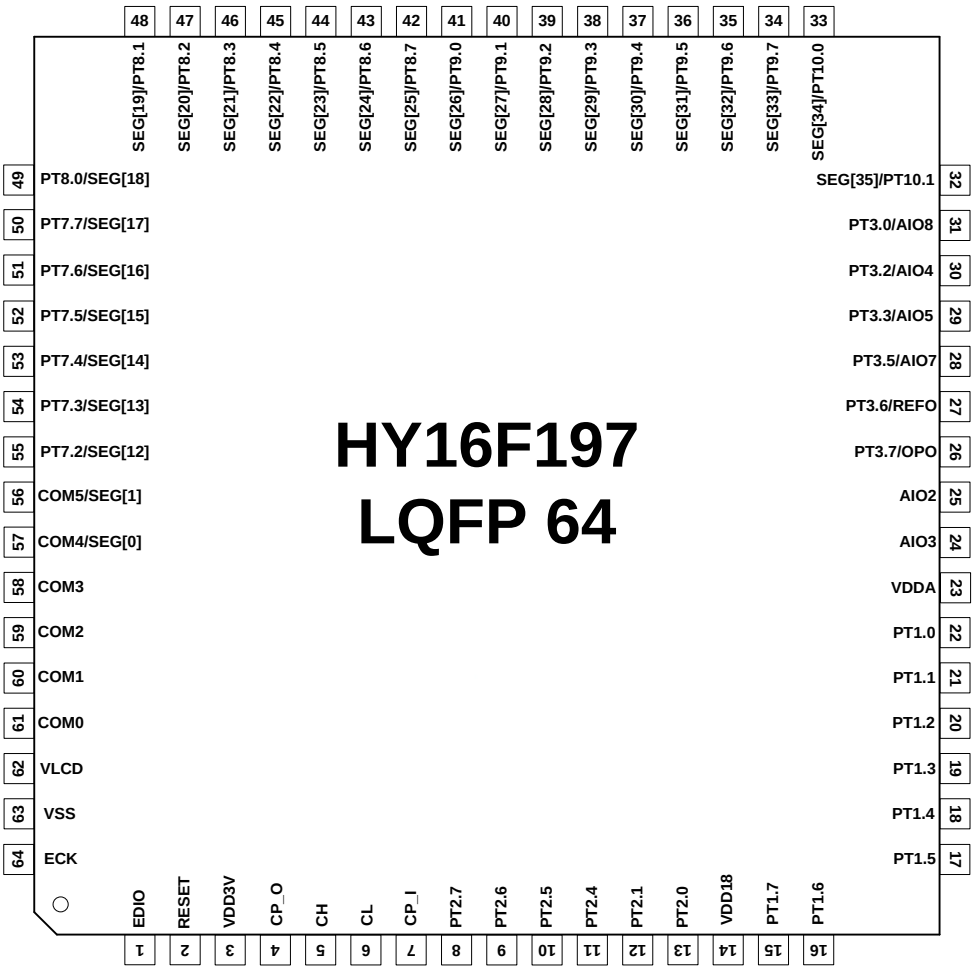


圖 2-2-1 HY16F197/HY16F197B LQFP 64 管腳圖

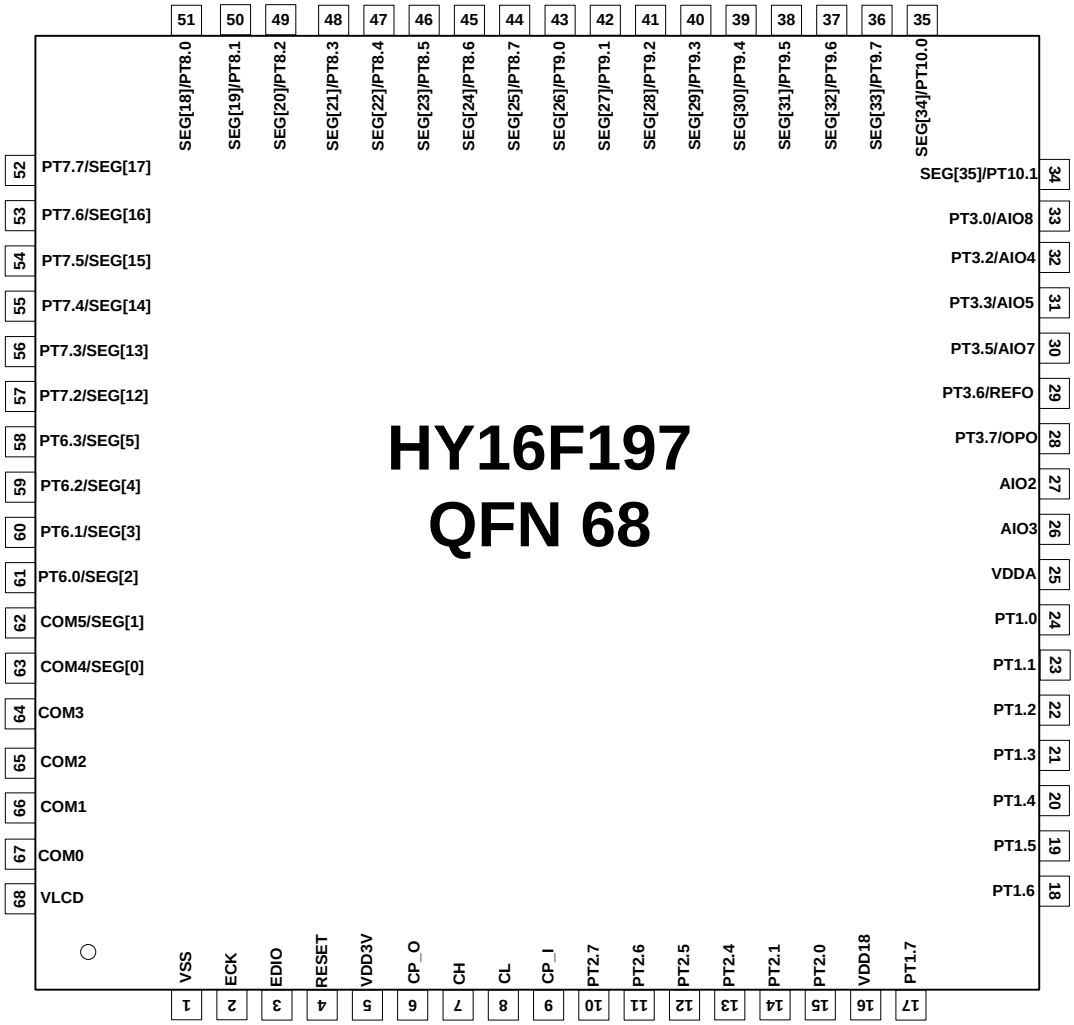


圖 2-2-2 HY16F197/HY16F197B QFN 68 管腳圖

2.3 HY16F196/HY16F196B 系列管腳圖

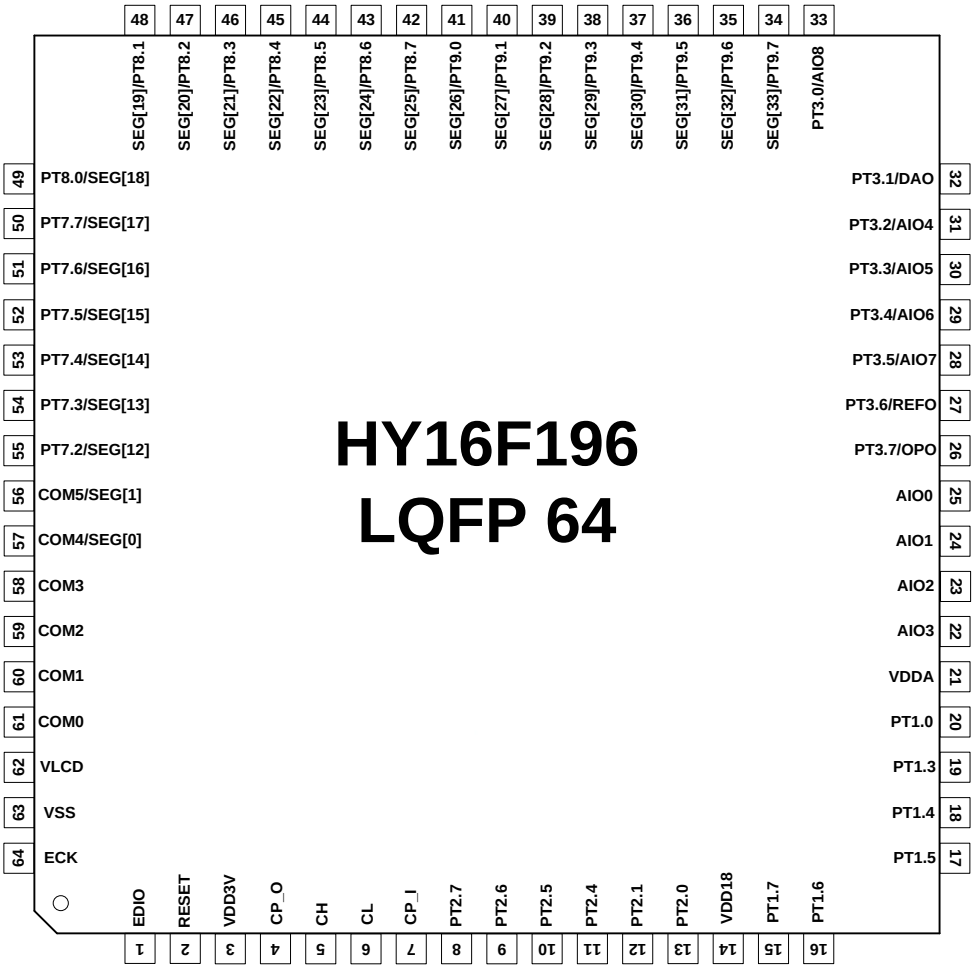


圖 2-3-1 HY16F196/HY16F196B LQFP64 管腳圖

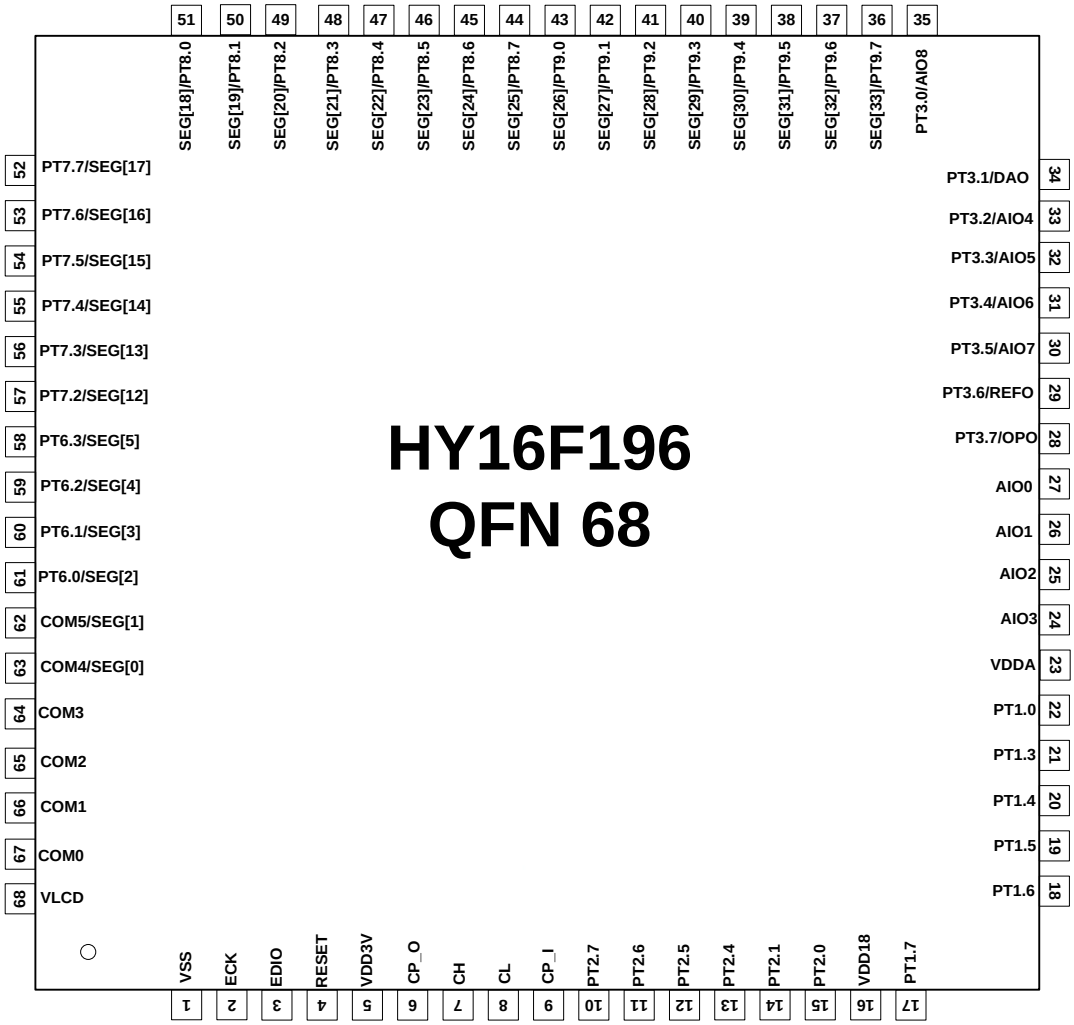


圖 2-3-2 HY16F196/HY16F196B QFN 68 管腳圖

2.4 引腳功能描述

2.4.1 HY16F19x 與 HY16F19xB 系列引腳定義

類型定義：I = 數字輸入;O = 數字輸出;OD = 開漏輸出;AI = 模擬輸入;AO = 模擬輸出;P = 電源連接端.

引腳	HY16F198-L100 HY16F198B-L100	HY16F197-L064 HY16F197B-L064	HY16F196-L064 HY16F196B-L064	類型	名稱	描述
ECK	1	64	64	DIO	ECK	開發調試通訊口(EDM)時鐘線引腳, 100K Resistance to VSS.
EDIO	2	1	1	DIO	EDIO	開發調試通訊口(EDM)數據線輸入/輸出引腳, 100K Resistance to VSS.
RESET	4	2	2	DI	RESET	復位引腳(低電位有效), 100K Resistance to VDD3V, 100nF Cap to VSS.
VDD3V	8	3	3	PI	VDD3V	晶片工作電源電壓輸入引腳, 10uF Cap to VSS.
CP_O	9	4	4	PO	CP_O	電荷泵升壓輸出引腳，輸出 3.3V, 10uF Cap to VSS.
CH	10	5	5	PIO	CH	電荷泵升壓電路輸入電容高電位接入引腳, 1uF Cap to CL
CL	11	6	6	PIO	CL	電荷泵升壓電路輸入電容低電位接入引腳, 1uF Cap to CH
CP_I	12	7	7	PI	CP_I	電荷泵升壓電路輸入電壓引腳, 10uF Cap to VSS.
PT2.7	15	8	8	IO XO I O O I I IO	PT2.7 HS_XOUT INT2.7 PWM3_4 MOSI_4 RX2_4 TCI2_8 SDA_8	通用數字輸入/輸出引腳 外部高速晶震 2~16MHZ 輸出引腳 外部中斷源 INT2.7 輸入引腳 TimerB2, PWM3_4 輸出引腳 SPI 通訊數據線引腳 MOSI_4(主機輸出，從機輸入) EUART2 通訊接收線引腳 RX2_4 捕捉比較器輸入源引腳 TCI2_8 I2C 通訊數據線引腳 SDA_8
PT2.6	16	9	9	IO XI	PT2.6 HS_XIN	通用數字輸入/輸出引腳 外部高速晶震 2~16MHZ 輸入引腳

引腳	HY16F198-L100 HY16F198B-L100	HY16F197-L064 HY16F197B-L064	HY16F196-L064 HY16F196B-L064	類型	名稱	描述
				I O I IO I IO	INT2.6 PWM2_4 MISO_4 TX2_4 TCI1_8 SCL_8	外部中斷源 INT2.6 輸入引腳 TimerB2, PWM2_4 輸出引腳 SPI 通訊數據線引腳 MISO_4(主機輸入，從機輸出) EUART2 通訊發送線引腳 TX2_4 捕捉比較器輸入源引腳 TCI1_8 I2C 通訊時鐘線引腳 SCL_8
PT2.5	17	10	10	IO XO I O I I I IO	PT2.5 LS_XIN INT2.5 PWM1_4 CK_4 RX_4 TCI2_7 SDA_7	通用數字輸入/輸出引腳 外部低速晶震 32768HZ 輸出引腳 外部中斷源 INT2.5 輸入引腳 TimerB, PWM1_4 輸出引腳 SPI 通訊時鐘線引腳 CK_4 EUART 通訊接收線引腳 RX_4 捕捉比較器輸入源引腳 TCI2_7 I2C 通訊數據線引腳 SDA_7
PT2.4	18	11	11	IO XI I O I IO I IO	PT2.4 LS_XOUT INT2.4 PWM0_4 CS_4 TX_4 TCI1_7 SCL_7	通用數字輸入/輸出引腳 外部低速晶震 32768HZ 輸入引腳 外部中斷源 INT2.4 輸入引腳 TimerB, PWM0_4 輸出引腳 SPI 通訊使能引腳 CS_4 EUART 通訊發送線引腳 TX_4 捕捉比較器輸入源引腳 TCI1_7 I2C 通訊時鐘線引腳 SCL_7
PT2.3	19	-	-	IO I O O I I IO AI	PT2.3 INT2.3 PWM3_3 MOSI_3 RX2_3 TCI2_6 SDA_6 CL8	通用數字輸入/輸出引腳 外部中斷源 INT2.3 輸入引腳 TimerB2, PWM3_3 輸出引腳 SPI 通訊數據線引腳 MOSI_3(主機輸出，從機輸入) EUART2 通訊接收線引腳 RX2_3 捕捉比較器輸入源引腳 TCI2_6 I2C 通訊數據線引腳 SDA_6 觸控按鍵輸入引腳 CL8
PT2.2	20	-	-	IO I O I	PT2.2 INT2.2 PWM2_3 MISO_3	通用數字輸入/輸出引腳 外部中斷源 INT2.2 輸入引腳 TimerB2, PWM2_3 輸出引腳 SPI 通訊數據線引腳 MISO_3(主機輸

引腳	HY16F198-L100 HY16F198B-L100	HY16F197-L064 HY16F197B-L064	HY16F196-L064 HY16F196B-L064	類型	名稱	描述
				IO I IO AI	TX2_3 TCI1_6 SCL_6 CL7	入，從機輸出) EUART2 通訊發送線引腳 TX2_3 捕捉比較器輸入源引腳 TCI1_6 I2C 通訊時鐘線引腳 SCL_6 觸控按鍵輸入引腳 CL7
PT2.1	21	12	12	IO I O I I I IO AI	PT2.1 INT2.1 PWM1_3 CK_3 RX_3 TCI2_5 SDA_5 CL6	通用數字輸入/輸出引腳 外部中斷源 INT2.1 輸入引腳 TimerB, PWM1_3 輸出引腳 SPI 通訊時鐘線引腳 CK_3 EUART 通訊接收線引腳 RX_3 捕捉比較器輸入源引腳 TCI2_5 I2C 通訊數據線引腳 SDA_5 觸控按鍵輸入引腳 CL6
PT2.0	22	13	13	IO I O I IO I IO AI	PT2.0 INT2.0 PWM0_3 CS_3 TX_3 TCI1_5 SCL_5 CL5	通用數字輸入/輸出引腳 外部中斷源 INT2.0 輸入引腳 TimerB, PWM0_3 輸出引腳 SPI 通訊使能引腳 CS_3 EUART 通訊發送線引腳 TX_3 捕捉比較器輸入源引腳 TCI1_5 I2C 通訊時鐘線引腳 SCL_5 觸控按鍵輸入引腳 CL5
VDD18	23	14	14	PI	VDD18	數字電源電壓引腳，輸出 1.8V, 1uF Cap to VSS
PT1.7	24	15	15	IO AO I O O I I IO	PT1.7 CMPO INT1.7 PWM3_2 MOSI_2 RX2_2 TCI2_4 SDA_4	通用數字輸入/輸出引腳 比較器比較結果輸出引腳(數位) 外部中斷源 INT1.7 輸入引腳 TimerB2, PWM3_2 輸出引腳 SPI 通訊數據線引腳 MOSI_2(主機輸出，從機輸入) EUART2 通訊接收線引腳 RX2_2 捕捉比較器輸入源引腳 TCI2_4 I2C 通訊數據線引腳 SDA_4
PT1.6	26	16	16	IO I O	PT1.6 INT1.6 PWM2_2	通用數字輸入/輸出引腳 外部中斷源 INT1.6 輸入引腳 TimerB2, PWM2_2 輸出引腳

引腳	HY16F198-L100 HY16F198B-L100	HY16F197-L064 HY16F197B-L064	HY16F196-L064 HY16F196B-L064	類型	名稱	描述
				I IO I IO AI	MISO_2 TX2_2 TCI1_4 SCL_4 CL4	SPI 通訊數據線引腳 MISO_2（主機輸入，從機輸出） EUART2 通訊發送線引腳 TX2_2 捕捉比較器輸入源引腳 TCI1_4 I2C 通訊時鐘線引腳 SCL_4 觸控按鍵輸入引腳 CL4
PT1.5	27	17	17	IO I O I I I IO AI	PT1.5 INT1.5 PWM1_2 CK_2 RX_2 TCI2_3 SDA_3 CL3	通用數字輸入/輸出引腳 外部中斷源 INT1.5 輸入引腳 TimerB, PWM1_2 輸出引腳 SPI 通訊時鐘線引腳 CK_2 EUART 通訊接收線引腳 RX_2 捕捉比較器輸入源引腳 TCI2_3 I2C 通訊數據線引腳 SDA_3 觸控按鍵輸入引腳 CL3
PT1.4	28	18	18	IO I O I IO I IO AI	PT1.4 INT1.4 PWM0_2 CS_2 TX_2 TCI1_3 SCL_3 CL2	通用數字輸入/輸出引腳 外部中斷源 INT1.4 輸入引腳 TimerB, PWM0_2 輸出引腳 SPI 通訊使能線引腳 CS_2 EUART 通訊發送線引腳 TX_2 捕捉比較器輸入源引腳 TCI1_3 I2C 通訊時鐘線引腳 SCL_3 觸控按鍵輸入引腳 CL2
PT1.3	29	19	19	IO I O O I I IO AI	PT1.3 INT1.3 PWM3_1 MOSI_1 RX2_1 TCI2_2 SDA_2 CL1	通用數字輸入/輸出引腳 外部中斷源 INT1.3 輸入引腳 TimerB2, PWM3_1 輸出引腳 SPI 通訊數據線引腳 MOSI_1(主機輸出，從機輸入) EUART2 通訊接收線引腳 RX2_1 捕捉比較器輸入源引腳 TCI2_2 I2C 通訊數據線引腳 SDA_2 觸控按鍵輸入引腳 CL1
PT1.2	30	20	-	IO I O I IO	PT1.2 INT1.2 PWM2_1 MISO_1 TX2_1	通用數字輸入/輸出引腳 外部中斷源 INT1.2 輸入引腳 TimerB2, PWM2_1 輸出引腳 SPI 通訊數據線引腳 MISO_1(主機輸入，從機輸出)

引腳	HY16F198-L100 HY16F198B-L100	HY16F197-L064 HY16F197B-L064	HY16F196-L064 HY16F196B-L064	類型	名稱	描述
				I IO AI	TCI1_2 SCL_2 CH3	EUART2 通訊發送線引腳 TX2_1 捕捉比較器輸入源引腳 TCI1_2 I2C 通訊時鐘線引腳 SCL_2 比較器模擬輸入引腳 CH3
PT1.1	31	21	-	IO I O I I I IO AI	PT1.1 INT1.1 PWM1_1 CK_1 RX_1 TCI2_1 SDA_1 CH2	通用數字輸入/輸出引腳 外部中斷源 INT1.1 輸入引腳 TimerB, PWM1_1 輸出引腳 SPI 通訊時鐘線引腳 CK_1 EUART 通訊接收線引腳 RX_1 捕捉比較器輸入源引腳 TCI2_1 I2C 通訊數據線引腳 SDA_1 比較器模擬輸入引腳 CH2
PT1.0	32	22	20	IO I O I IO I IO AI	PT1.0 INT1.0 PWM0_1 CS_1 TX_1 TCI1_1 SCL_1 CH1	通用數字輸入/輸出引腳 外部中斷源 INT1.0 輸入引腳 TimerB, PWM0_1 輸出引腳 SPI 通訊使能線引腳 CS_1 EUART 通訊發送線引腳 TX_1 捕捉比較器輸入源引腳 TCI1_1 I2C 通訊時鐘線引腳 SCL_1 比較器模擬輸入引腳 CH1
VDDA	38	23	21	PIO	VDDA	模擬電源電壓/LDO 穩壓輸出端/模擬電源電壓輸入端 1uF Cap to VSS.
AIO3	39	24	22	AI	AIO3	ADC 模擬輸入引腳 AIO3
AIO2	40	25	23	AI	AIO2	ADC 模擬輸入引腳 AIO2
AIO1	41	-	24	AI	AIO1	ADC 模擬輸入引腳 AIO1
AIO0	42	-	25	AI	AIO0	ADC 模擬輸入引腳 AIO0
PT3.7	43	26	26	IO AO	PT3.7 OPO	通用數字輸入/輸出引腳 運算放大器模擬輸出引腳 OPO
PT3.6	44	27	27	IO PIO	PT3.6 REFO	通用數字輸入/輸出引腳 模擬參考電壓 1.2V 輸出引腳, 0.1uF Cap to VSS.
PT3.5	45	28	28	IO AI	PT3.5 AIO7	通用數字輸入/輸出引腳 ADC 模擬輸入引腳 AIO7
PT3.4	46	-	29	IO AI	PT3.4 AIO6	通用數字輸入/輸出引腳 ADC 模擬輸入引腳 AIO6

引腳	HY16F198-L100 HY16F198B-L100	HY16F197-L064 HY16F197B-L064	HY16F196-L064 HY16F196B-L064	類型	名稱	描述
PT3.3	47	29	30	IO AI	PT3.3 AIO5	通用數字輸入/輸出引腳 ADC 模擬輸入引腳 AIO5
PT3.2	48	30	31	IO AI	PT3.2 AIO4	通用數字輸入/輸出引腳 ADC 模擬輸入引腳 AIO4
PT3.1	49	-	32	IO AO AO	PT3.1 OPO2 DAO	通用數字輸入/輸出引腳 運算放大器數字輸出引腳 OPO2 8-BIT Resistance Ladders.輸出引腳
PT3.0	50	31	33	IO AO AI	PT3.0 OPO1 AIO8	通用數字輸入/輸出引腳 運算放大器數字輸出引腳 OPO1 模擬輸入引腳 AIO8
SEG35	58	32	-	IO AO	PT10.1 SEG35	通用數字輸入/輸出引腳 LCD Segment 輸出
SEG34	59	33	-	IO AO	PT10.0 SEG34	通用數字輸入/輸出引腳 LCD Segment 輸出
SEG33	60	34	34	IO AO O O I	PT9.7 SEG33 PWM3_8 MOSI_8 RX2_8	通用數字輸入/輸出引腳 LCD Segment 輸出 TimerB2, PWM3_8 輸出引腳 SPI 通訊數據線引腳 MOSI_8(主機輸出，從機輸入) EUART2 通訊接收線引腳 RX2_8
SEG32	61	35	35	IO AO O O I	PT9.6 SEG32 PWM2_8 MISO_8 TX2_8	通用數字輸入/輸出引腳 LCD Segment 輸出 TimerB2, PWM2_8 輸出引腳 SPI 通訊數據線引腳 MISO_8(主機輸入，從機輸出) EUART2 通訊發送線引腳 TX2_8
SEG31	62	36	36	IO AO O O I	PT9.5 SEG31 PWM1_8 CK_8 RX_8	通用數字輸入/輸出引腳 LCD Segment 輸出 TimerB, PWM1_8 輸出引腳 SPI 通訊時鐘線引腳 CK_8 EUART 通訊接收線引腳 RX_8
SEG30	63	37	37	IO AO O O	PT9.4 SEG30 PWM0_8 CS_8	通用數字輸入/輸出引腳 LCD Segment 輸出 TimerB, PWM0_8 輸出引腳 SPI 通訊使能線引腳 CS_8

引腳	HY16F198-L100 HY16F198B-L100	HY16F197-L064 HY16F197B-L064	HY16F196-L064 HY16F196B-L064	類型	名稱	描述
				I	TX_8	EUART 通訊發送線引腳 TX_8
SEG29	64	38	38	IO AO O O I	PT9.3 SEG29 PWM3_7 MOSI_7 RX2_7	通用數字輸入/輸出引腳 LCD Segment 輸出 TimerB2, PWM3_7 輸出引腳 SPI 通訊數據線引腳 MOSI_7(主機輸出，從機輸入) EUART2 通訊接收線引腳 RX2_7
SEG28	65	39	39	IO AO O O I	PT9.2 SEG28 PWM2_7 MISO_7 TX2_7	通用數字輸入/輸出引腳 LCD Segment 輸出 TimerB2, PWM2_7 輸出引腳 SPI 通訊數據線引腳 MISO_7(主機輸入，從機輸出) EUART2 通訊發送線引腳 TX2_7
SEG27	66	40	40	IO AO O O I	PT9.1 SEG27 PWM1_7 CK_7 RX_7	通用數字輸入/輸出引腳 LCD Segment 輸出 TimerB, PWM1_7 輸出引腳 SPI 通訊時鐘線引腳 CK_7 EUART 通訊接收線引腳 RX_7
SEG26	67	41	41	IO AO O O I	PT9.0 SEG26 PWM0_7 CS_7 TX_7	通用數字輸入/輸出引腳 LCD Segment 輸出 TimerB, PWM0_7 輸出引腳 SPI 通訊使能線引腳 CS_7 EUART 通訊發送線引腳 TX_7
SEG25	68	42	42	IO AO O O I I	PT8.7 SEG25 PWM3_6 MOSI_6 RX2_6 TCI3_8	通用數字輸入/輸出引腳 LCD Segment 輸出 TimerB2, PWM3_6 輸出引腳 SPI 通訊數據線引腳 MOSI_6(主機輸出，從機輸入) EUART2 通訊接收線引腳 RX2_6 TimerB2 輸入源引腳 TCI3_8
SEG24	69	43	43	IO AO O O I	PT8.6 SEG24 PWM2_6 MISO_6 TX2_6	通用數字輸入/輸出引腳 LCD Segment 輸出 TimerB2, PWM2_6 輸出引腳 SPI 通訊數據線引腳 MISO_6(主機輸入，從機輸出)

引腳	HY16F198-L100 HY16F198B-L100	HY16F197-L064 HY16F197B-L064	HY16F196-L064 HY16F196B-L064	類型	名稱	描述
						EUART2 通訊發送線引腳 TX2_6
SEG23	70	44	44	IO AO O O I I	PT8.5 SEG23 PWM1_6 CK_6 RX_6 TCI3_7	通用數字輸入/輸出引腳 LCD Segment 輸出 TimerB, PWM1_6 輸出引腳 SPI 通訊時鐘線引腳 CK_6 EUART 通訊接收線引腳 RX_6 TimerB2 輸入源引腳 TCI3_7
SEG22	71	45	45	IO AO O O I	PT8.4 SEG22 PWM0_6 CS_6 TX_6	通用數字輸入/輸出引腳 LCD Segment 輸出 TimerB, PWM0_6 輸出引腳 SPI 通訊使能線引腳 CS_6 EUART 通訊發送線引腳 TX_6
SEG21	72	46	46	IO AO O O I I	PT8.3 SEG21 PWM3_5 MOSI_5 RX2_5 TCI3_6	通用數字輸入/輸出引腳 LCD Segment 輸出 TimerB2, PWM3_5 輸出引腳 SPI 通訊數據線引腳 MOSI_5(主機輸出，從機輸入) EUART2 通訊接收線引腳 RX2_5 TimerB2 輸入源引腳 TCI3_6
SEG20	73	47	47	IO AO O O I	PT8.2 SEG20 PWM2_5 MISO_5 TX2_5	通用數字輸入/輸出引腳 LCD Segment 輸出 TimerB2, PWM2_5 輸出引腳 SPI 通訊數據線引腳 MISO_5(主機輸入，從機輸出) EUART2 通訊發送線引腳 TX2_5
SEG19	74	48	48	IO AO O O I I	PT8.1 SEG19 PWM1_5 CK_5 RX_5 TCI3_5	通用數字輸入/輸出引腳 LCD Segment 輸出 TimerB, PWM1_5 輸出引腳 SPI 通訊時鐘線引腳 CK_5 EUART 通訊接收線引腳 RX_5 TimerB2 輸入源引腳 TCI3_5
VPP	75	-	-	PI	VPP	保留（不能連接到任何引腳）
SEG18	76	49	49	IO AO O	PT8.0 SEG18 PWM0_5	通用數字輸入/輸出引腳 LCD Segment 輸出 TimerB, PWM0_5 輸出引腳

引腳	HY16F198-L100 HY16F198B-L100	HY16F197-L064 HY16F197B-L064	HY16F196-L064 HY16F196B-L064	類型	名稱	描述
				O	CS_5	SPI 通訊使能線引腳 CS_5
				I	TX_5	EUART 通訊發送線引腳 TX_5
SEG17	77	50	50	IO	PT7.7	通用數字輸入/輸出引腳
				AO	SEG17	LCD Segment 輸出
				I	TCI3_4	TimerB2 輸入源引腳 TCI3_4
SEG16	78	51	51	IO	PT7.6	通用數字輸入/輸出引腳
				AO	SEG16	LCD Segment 輸出
SEG15	79	52	52	IO	PT7.5	通用數字輸入/輸出引腳
				AO	SEG15	LCD Segment 輸出
				I	TCI3_3	TimerB2 輸入源引腳 TCI3_3
SEG14	80	53	53	IO	PT7.4	通用數字輸入/輸出引腳
				AO	SEG14	LCD Segment 輸出
SEG13	81	54	54	IO	PT7.3	通用數字輸入/輸出引腳
				AO	SEG13	LCD Segment 輸出
				I	TCI3_2	TimerB2 輸入源引腳 TCI3_2
SEG12	82	55	55	IO	PT7.2	通用數字輸入/輸出引腳
				AO	SEG12	LCD Segment 輸出
SEG11	83	-	-	IO	PT7.1	通用數字輸入/輸出引腳
				AO	SEG11	LCD Segment 輸出
				I	TCI3_1	TimerB2 輸入源引腳 TCI3_1
SEG10	84	-	-	IO	PT7.0	通用數字輸入/輸出引腳
				AO	SEG10	LCD Segment 輸出
SEG9	85	-	-	IO	PT6.7	通用數字輸入/輸出引腳
				AO	SEG9	LCD Segment 輸出
SEG8	86	-	-	IO	PT6.6	通用數字輸入/輸出引腳
				AO	SEG8	LCD Segment 輸出
SEG7	87	-	-	IO	PT6.5	通用數字輸入/輸出引腳
				AO	SEG7	LCD Segment 輸出
SEG6	88	-	-	IO	PT6.4	通用數字輸入/輸出引腳
				AO	SEG6	LCD Segment 輸出
SEG5	89	-	-	IO	PT6.3	通用數字輸入/輸出引腳
				AO	SEG5	LCD Segment 輸出
SEG4	90	-	-	IO	PT6.2	通用數字輸入/輸出引腳
				AO	SEG4	LCD Segment 輸出
SEG3	91	-	-	IO	PT6.1	通用數字輸入/輸出引腳

引腳	HY16F198-L100 HY16F198B-L100	HY16F197-L064 HY16F197B-L064	HY16F196-L064 HY16F196B-L064	類型	名稱	描述
				AO	SEG3	LCD Segment 輸出
SEG2	92	-	-	IO AO	PT6.0 SEG2	通用數字輸入/輸出引腳 LCD Segment 輸出
SEG1	93	56	56	IO AO AO	PT10.3 SEG1 COM5	通用數字輸入/輸出引腳 LCD Segment 輸出 LCD Common 輸出
SEG0	94	57	57	IO AO AO	PT10.2 SEG0 COM4	通用數字輸入/輸出引腳 LCD Segment 輸出 LCD Common 輸出
COM3	95	58	58	AO	COM3	LCD Common 輸出
COM2	96	59	59	AO	COM2	LCD Common 輸出
COM1	97	60	60	AO	COM1	LCD Common 輸出
COM0	98	61	61	AO	COM0	LCD Common 輸出
VLCD	99	62	62	PIO	VLCD	LCD 穩壓電源輸出/LCD 電源輸入, 10uF Cap to VSS.
VSS	100	63	63	PI	VSS	接地端引腳
Others	-	-	-	-	NC	不連接

表2-1 HY16F198/198B/197/197B/196/196B 管腳定義及管腳功能描述

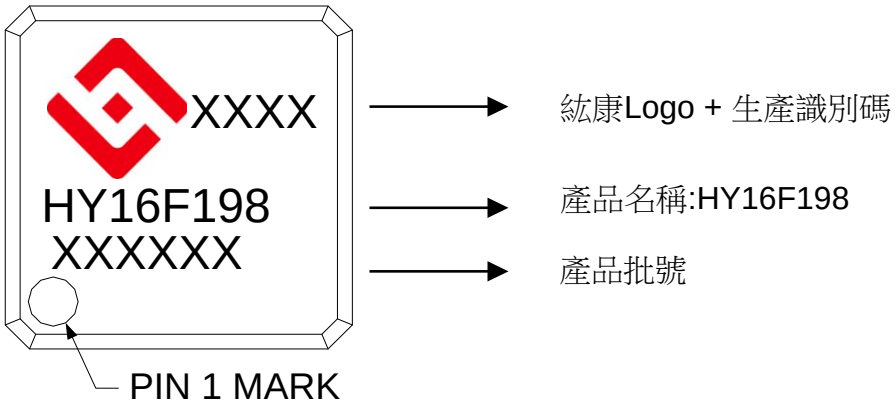
2.4.2 管腳複用功能及複用功能優先級

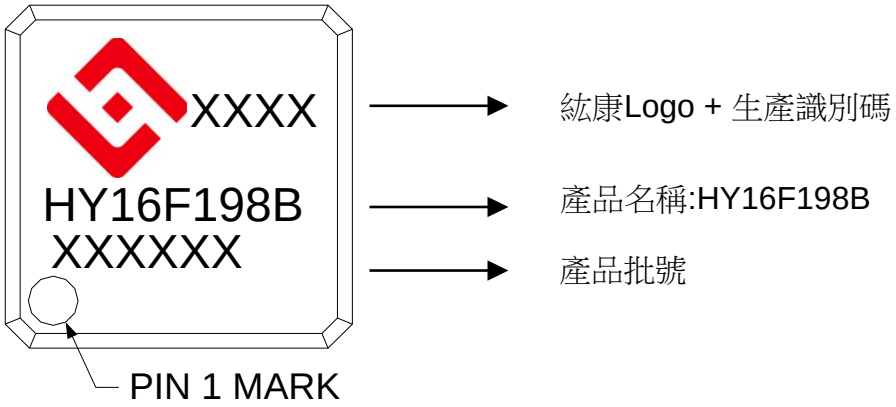
Function	INT	Timer C Capture	Special Function	SPI	I²C	UART	AIP	Analog	Timer B/B2 PWM
Output Priority	I/P	I/P	0	1	2	3	4	5	6
PT1.0	INT1.0	TCI1_1		CS_1	SCL_1	Tx_1		CH1	PWM0_1
PT1.1	INT1.1	TCI2_1		CK_1	SDA_1	Rx_1		CH2	PWM1_1
PT1.2	INT1.2	TCI1_2		MISO_1	SCL_2	Tx2_1		CH3	PWM2_1
PT1.3	INT1.3	TCI2_2		MOSI_1	SDA_2	Rx2_1		CL1	PWM3_1
PT1.4	INT1.4	TCI1_3		CS_2	SCL_3	Tx_2		CL2	PWM0_2
PT1.5	INT1.5	TCI2_3		CK_2	SDA_3	Rx_2		CL3	PWM1_2
PT1.6	INT1.6	TCI1_4		MISO_2	SCL_4	Tx2_2		CL4	PWM2_2
PT1.7	INT1.7	TCI2_4		MOSI_2	SDA_4	Rx2_2	CMPO		PWM3_2
PT2.0	INT2.0	TCI1_5		CS_3	SCL_5	Tx_3		CL5	PWM0_3
PT2.1	INT2.1	TCI2_5		CK_3	SDA_5	Rx_3		CL6	PWM1_3
PT2.2	INT2.2	TCI1_6		MISO_3	SCL_6	Tx2_3		CL7	PWM2_3
PT2.3	INT2.3	TCI2_6		MOSI_3	SDA_6	Rx2_3		CL8	PWM3_3
PT2.4	INT2.4	TCI1_7	LS_XOUT	CS_4	SCL_7	Tx_4			PWM0_4
PT2.5	INT2.5	TCI2_7	LS_XIN	CK_4	SDA_7	Rx_4			PWM1_4
PT2.6	INT2.6	TCI1_8	HS_XIN	MISO_4	SCL_8	Tx2_4			PWM2_4
PT2.7	INT2.7	TCI2_8	HS_XOUT	MOSI_4	SDA_8	Rx2_4			PWM3_4
PT3.0							OPO1	AIO8	
PT3.1							OPO2	DAO	
PT3.2								AIO4	
PT3.3								AIO5	
PT3.4								AIO6	
PT3.5								AIO7	
PT3.6								REFO	
PT3.7								OPO	
RESET	RESET								
AIO0								AIO0	
AIO1								AIO1	
AIO2								AIO2	
AIO3								AIO3	
COM0			COM 0						
COM1			COM 1						
COM2			COM 2						
COM3			COM 3						

PT10.2			COM 4/SEG 0						
PT10.3			COM 5/SEG 1						
PT6.0			SEG 2						
PT6.1			SEG 3						
PT6.2			SEG 4						
PT6.3			SEG 5						
PT6.4			SEG 6						
PT6.5			SEG 7						
PT6.6			SEG 8						
PT6.7			SEG 9						
PT7.0			SEG 10						
PT7.1		TCI3_1	SEG 11						
PT7.2			SEG 12						
PT7.3		TCI3_2	SEG 13						
PT7.4			SEG 14						
PT7.5		TCI3_3	SEG 15						
PT7.6			SEG 16						
PT7.7		TCI3_4	SEG 17						
PT8.0			SEG 18	CS_5		Tx_5			PWM0_5
PT8.1		TCI3_5	SEG 19	CK_5		Rx_5			PWM1_5
PT8.2			SEG 20	MISO_5		Tx2_5			PWM2_5
PT8.3		TCI3_6	SEG 21	MOSI_5		Rx2_5			PWM3_5
PT8.4			SEG 22	CS_6		Tx_6			PWM0_6
PT8.5		TCI3_7	SEG 23	CK_6		Rx_6			PWM1_6
PT8.6			SEG 24	MISO_6		Tx2_6			PWM2_6
PT8.7		TCI3_8	SEG 25	MOSI_6		Rx2_6			PWM3_6
PT9.0			SEG 26	CS_7		Tx_7			PWM0_7
PT9.1			SEG 27	CK_7		Rx_7			PWM1_7
PT9.2			SEG 28	MISO_7		Tx2_7			PWM2_7
PT9.3			SEG 29	MOSI_7		Rx2_7			PWM3_7
PT9.4			SEG 30	CS_8		Tx_8			PWM0_8
PT9.5			SEG 31	CK_8		Rx_8			PWM1_8
PT9.6			SEG 32	MISO_8		Tx2_8			PWM2_8
PT9.7			SEG 33	MOSI_8		Rx2_8			PWM3_8
PT10.0			SEG 34						
PT10.1			SEG 35						

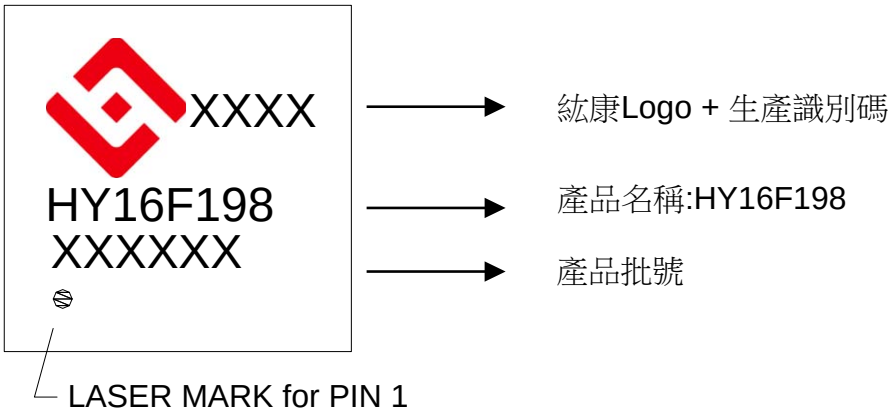
2.5 封裝片標記訊息

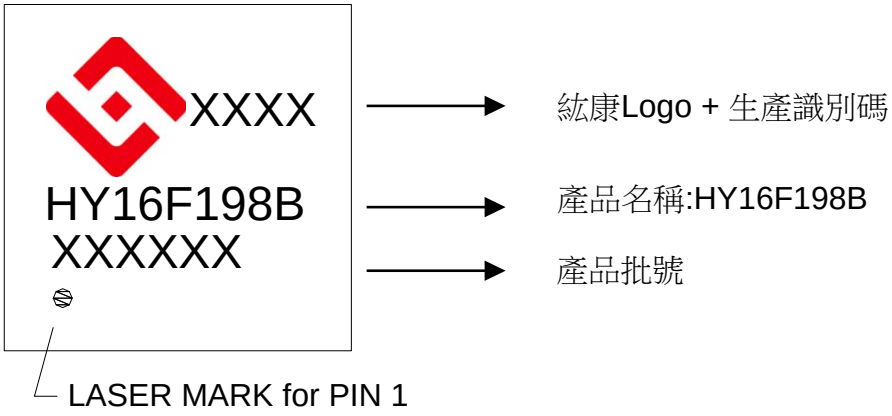
2.5.1 HY16F198/HY16F198B LQFP 封裝片標記訊息





2.5.2 HY16F198/HY16F198B QFN 封裝片標記訊息





3. 應用電路

3.1 橋式傳感器應用電路

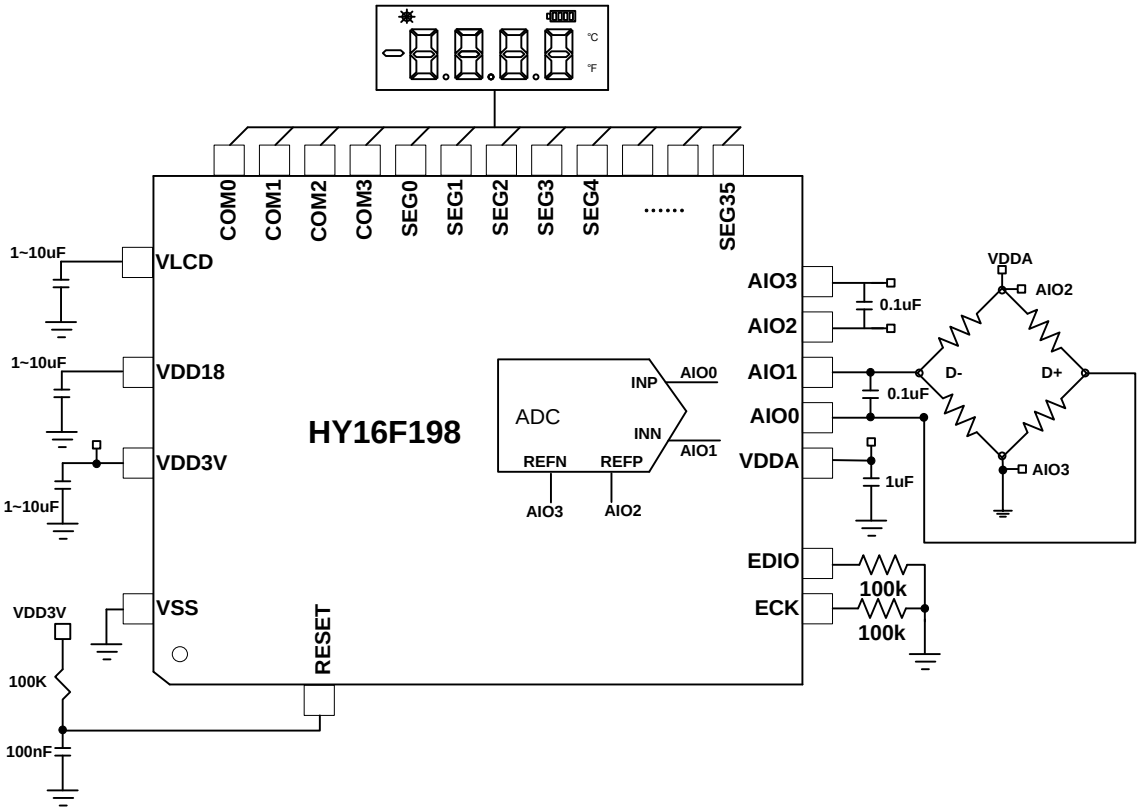


圖3-1 橋式傳感器應用電路

3.2 血壓傳感器應用電路

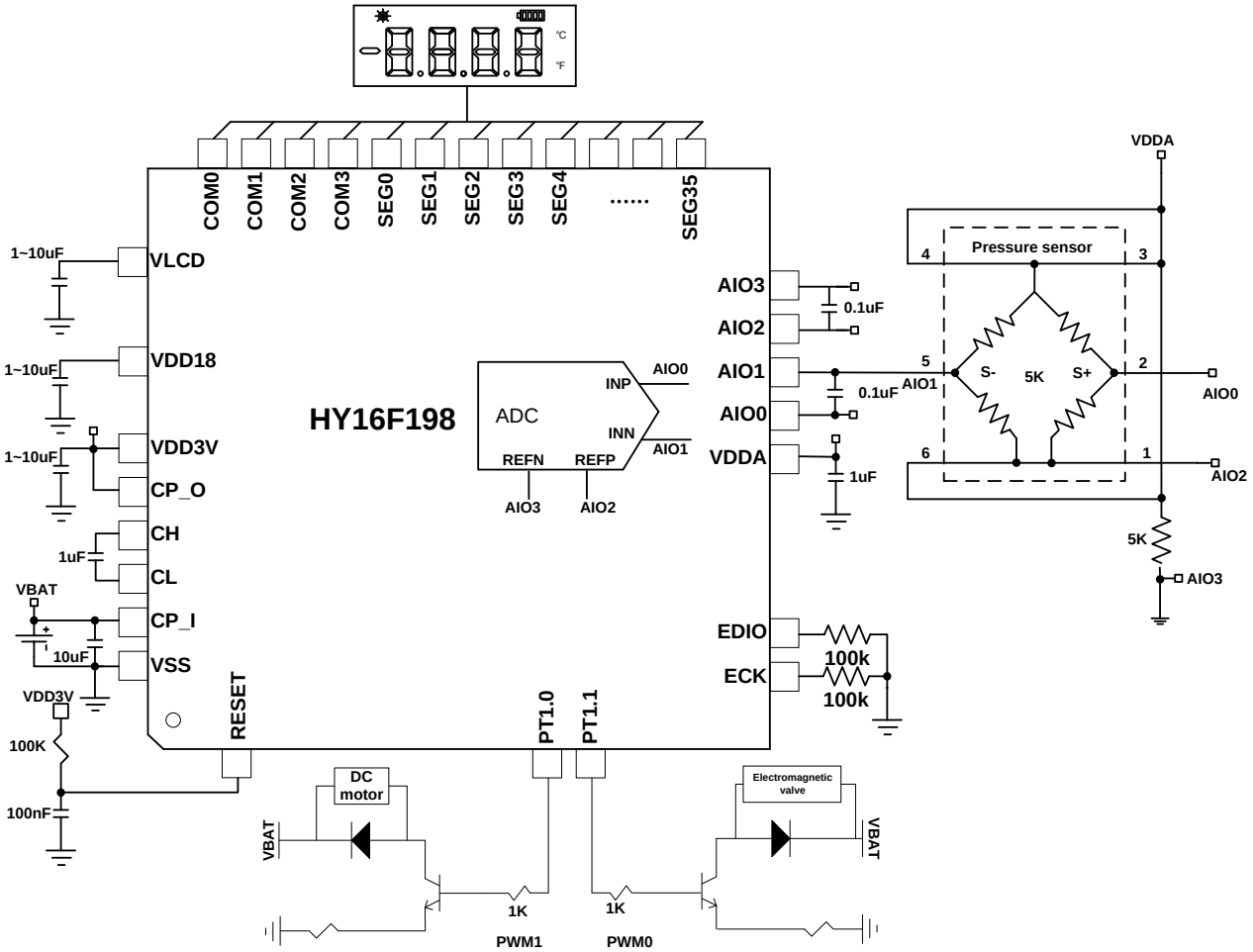


圖 3-2 血壓傳感器應用電路

3.3 電化學傳感器應用電路

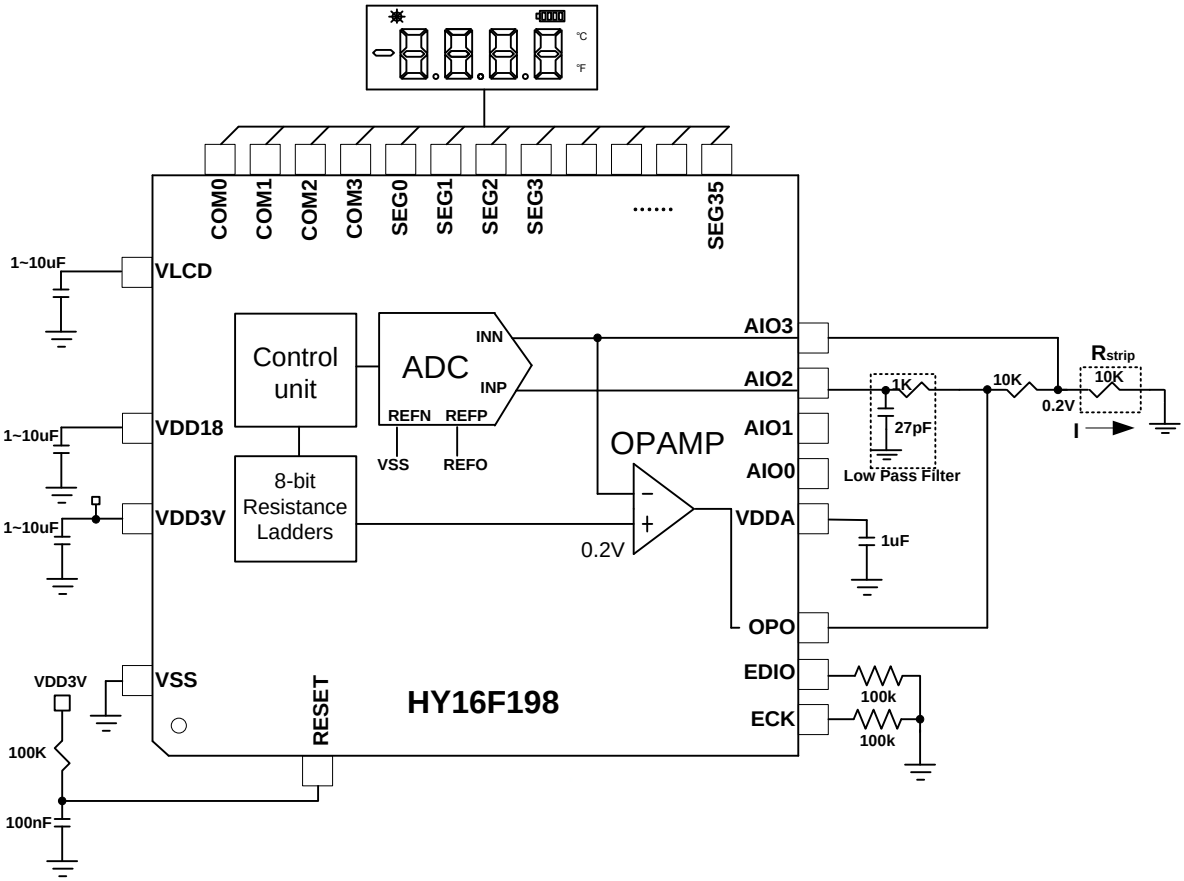


圖 3-3 電化學傳感器應用電路

3.4 觸控按鍵應用電路

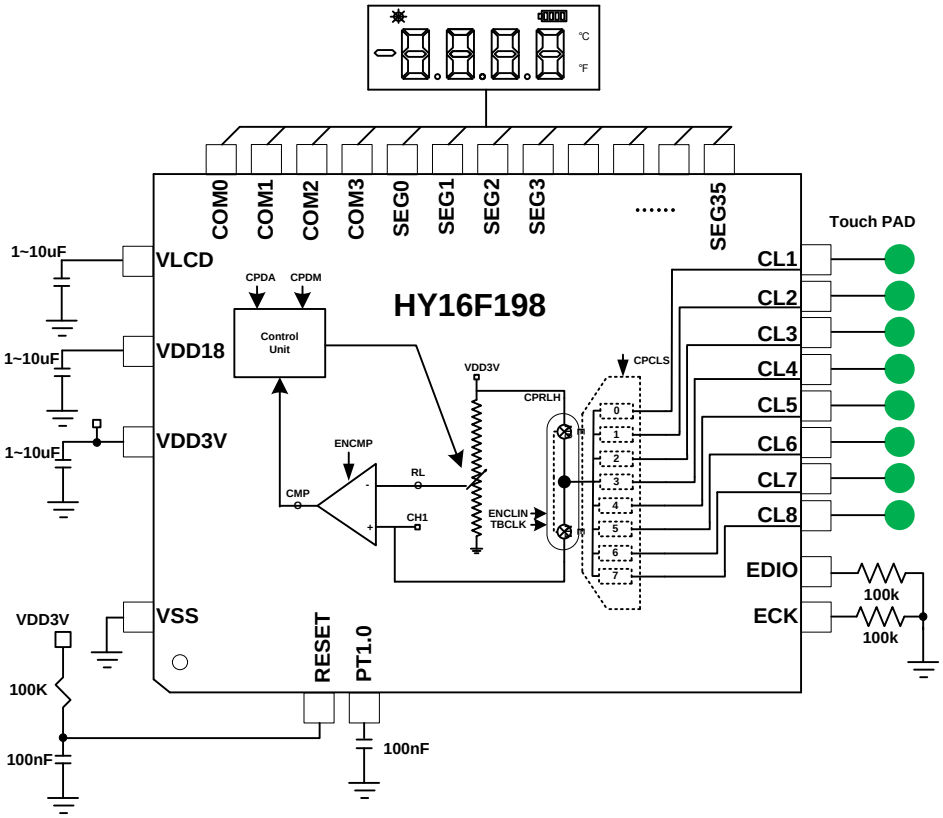


圖 3-4 觸控按鍵應用電路

3.5 三合一血糖計應用電路

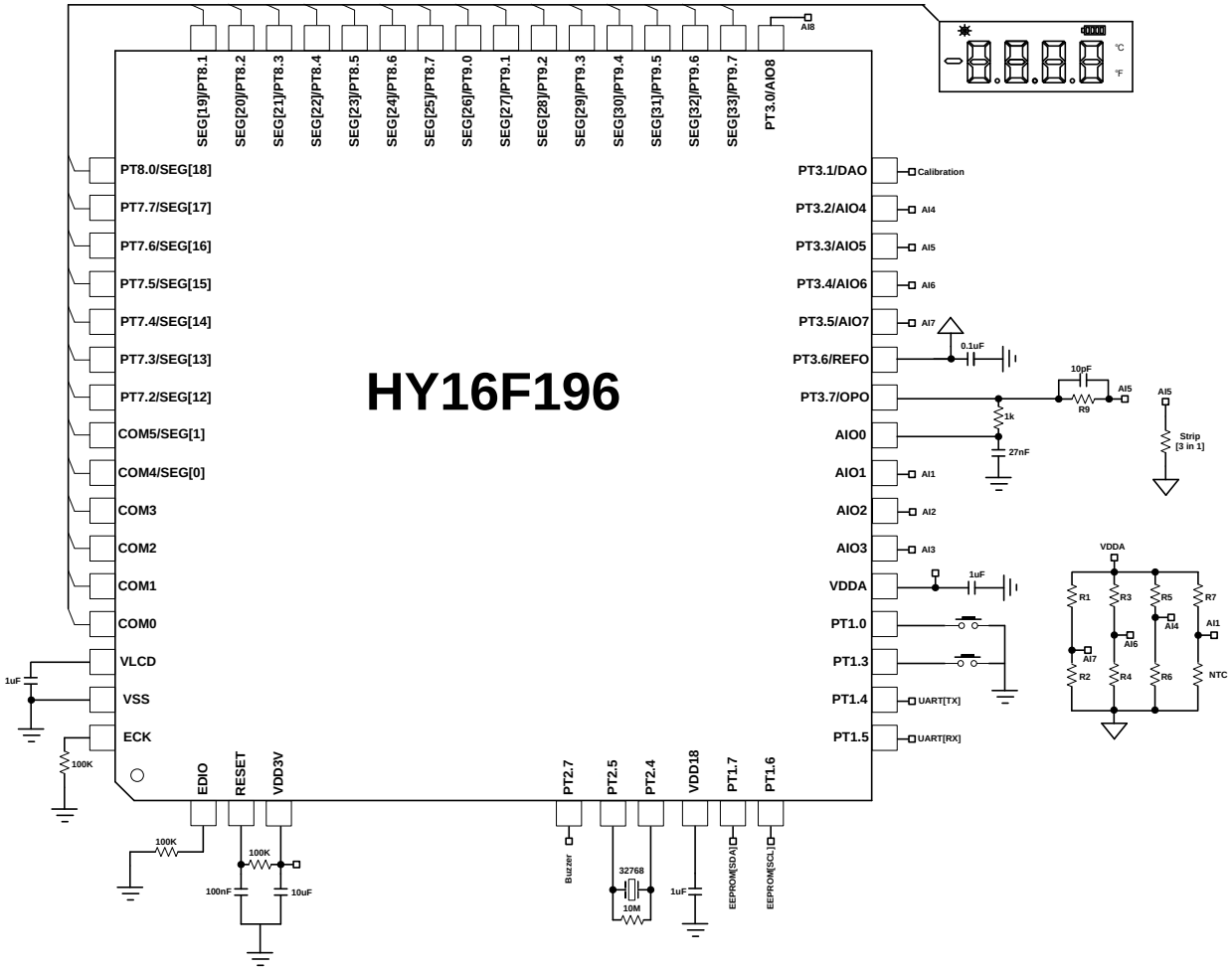


圖 3-5 三合一血糖計應用電路

4. 功能概述

4.1 內部框圖

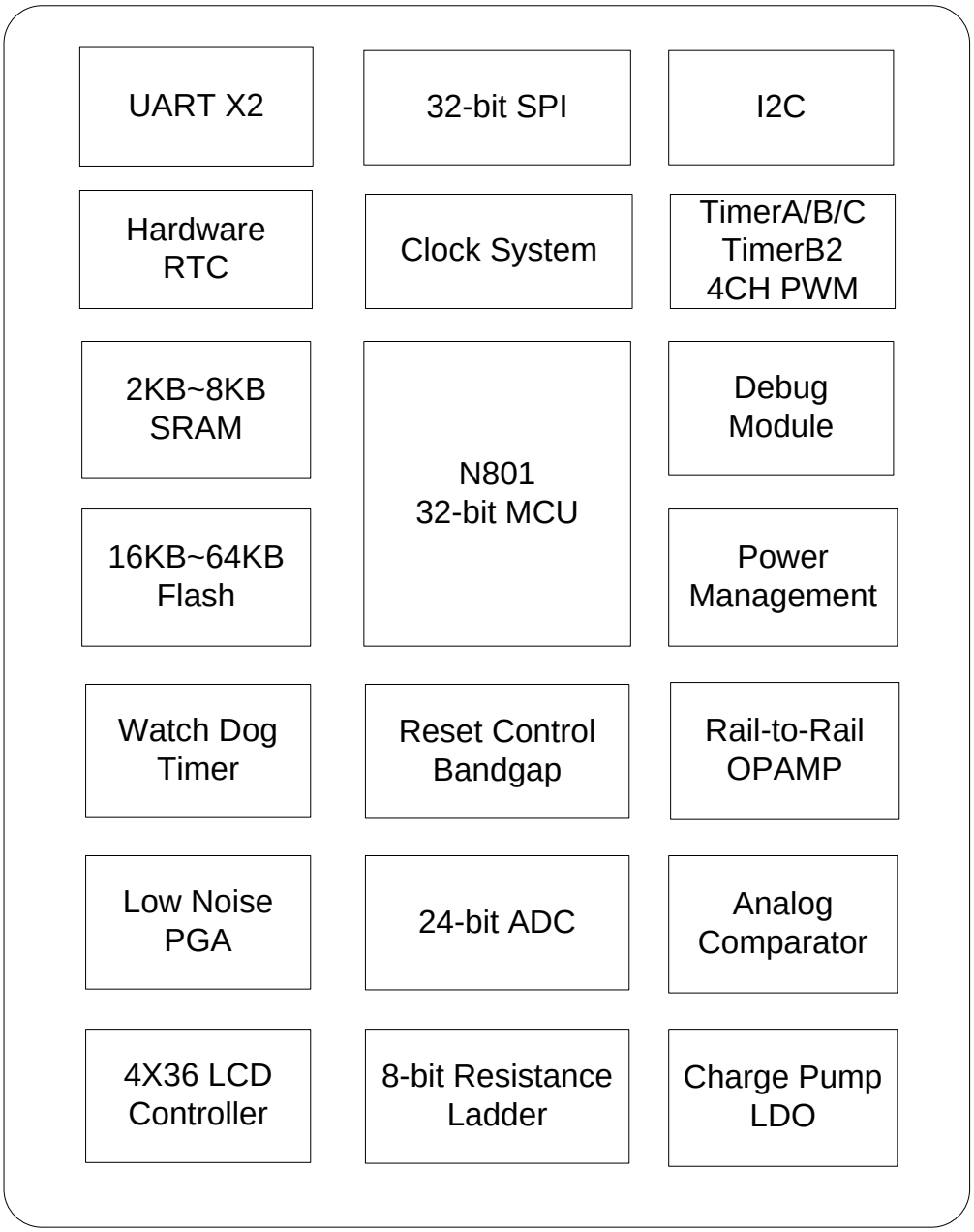


圖 4-1 HY16F198 內部框圖

4.2 中央處理器核心方框圖

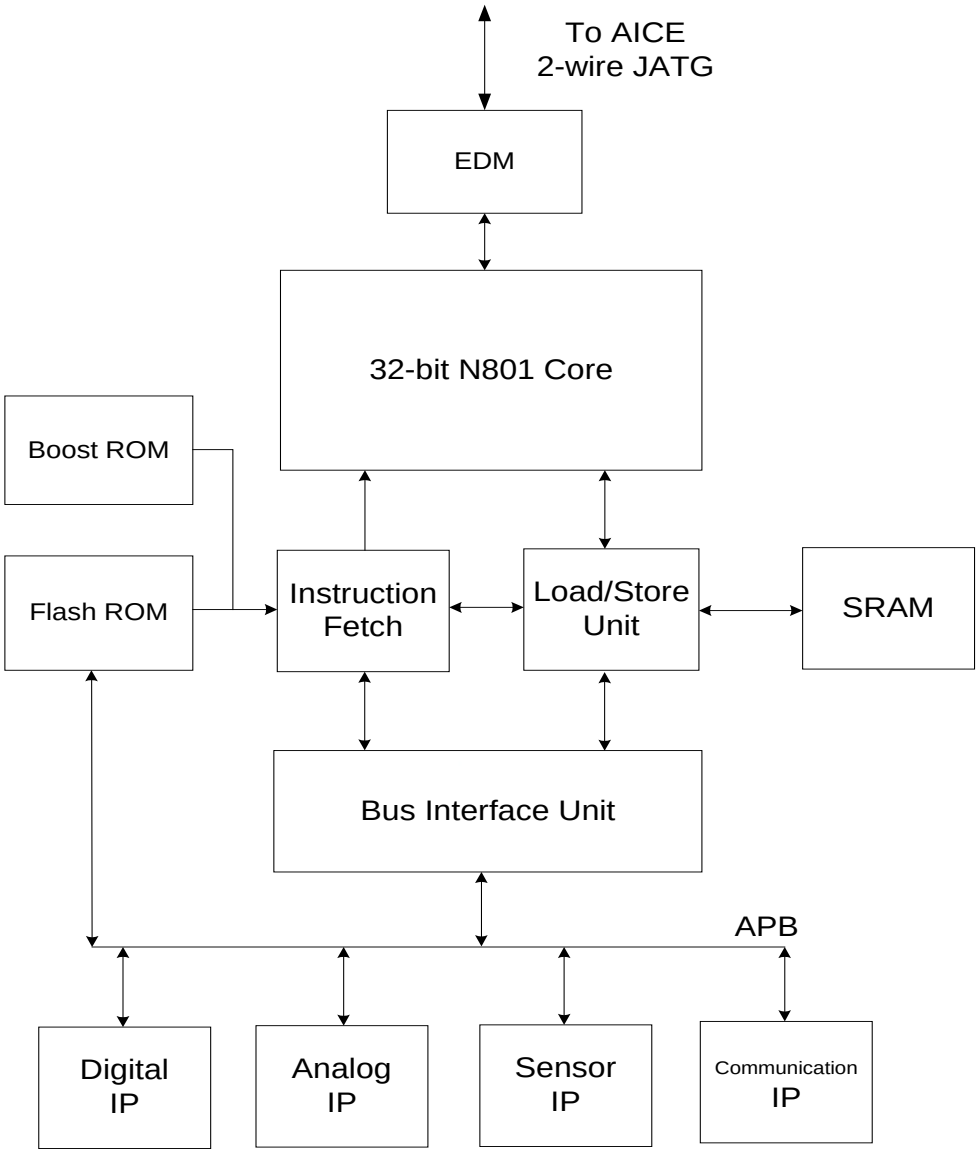
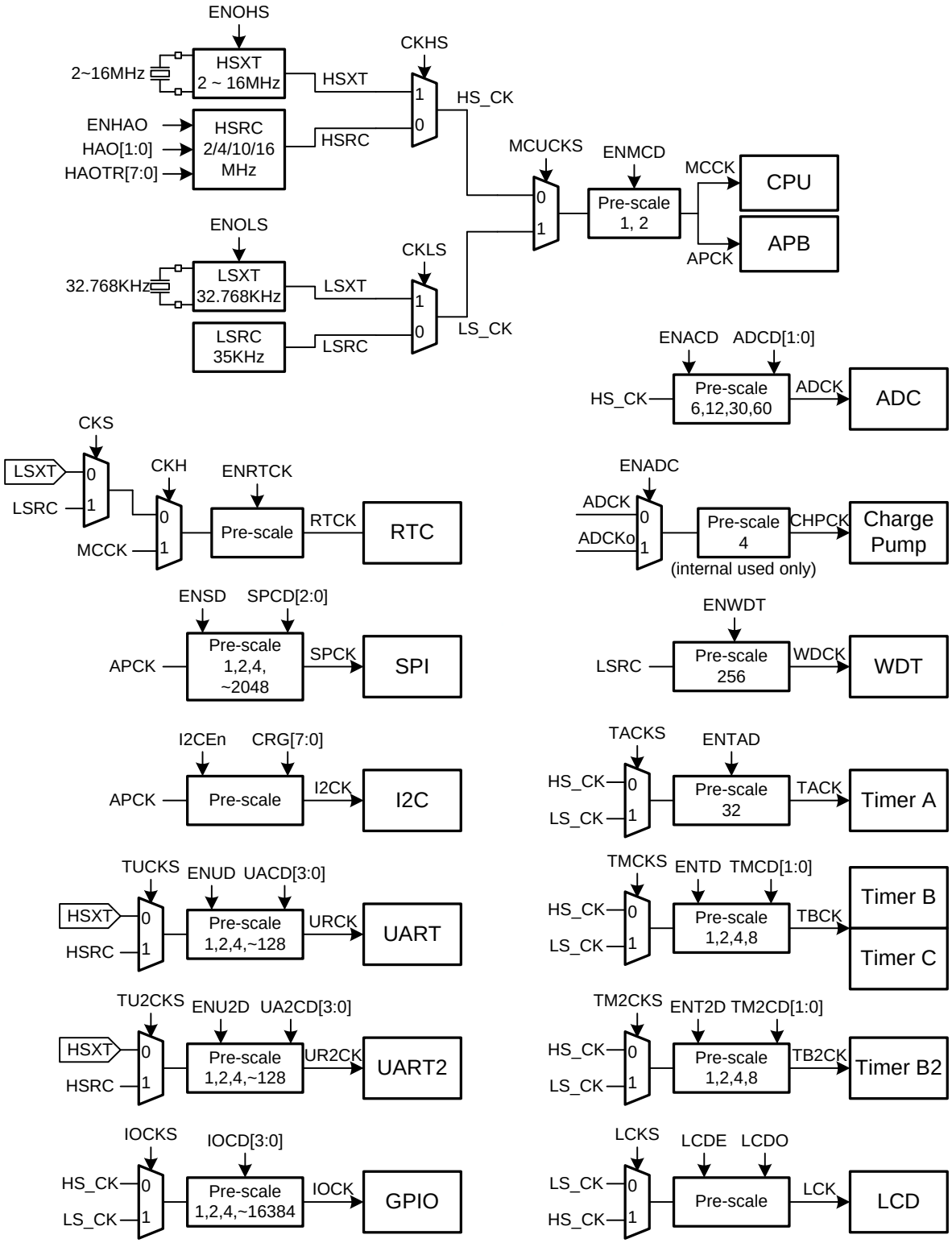


Figure 4-2 中央處理器核心方框圖

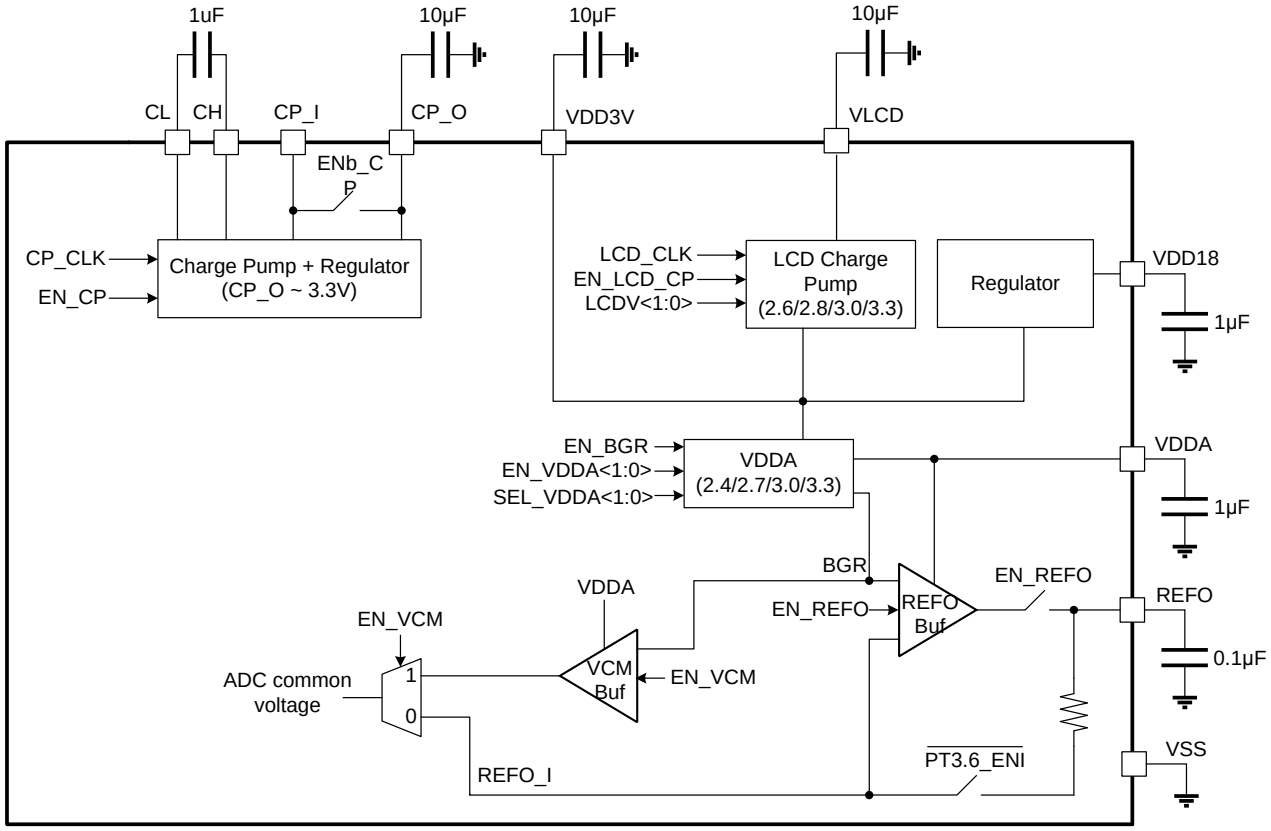
4.3 相關的支援文檔

檔案名稱	描述
UG-HY16F198	HY16F19 系列用戶手冊
APD-HY16IDE007	HY16F19X C 函數庫手冊
APD-HY16IDE005	HY16F19X C 函數庫編譯操作說明
APD-HY16IDE008	HY16F19X 各 IP 使用說明書
APD-HY16IDE001	HY16F 系列 IDE 軟體使用說明書/ HY16F Series Device 安裝程式
APD-HY16IDE009	HY16F 系列 ICE 硬體使用說明書
APD-HY16IDE006	HY16F 系列燒錄器使用說明書

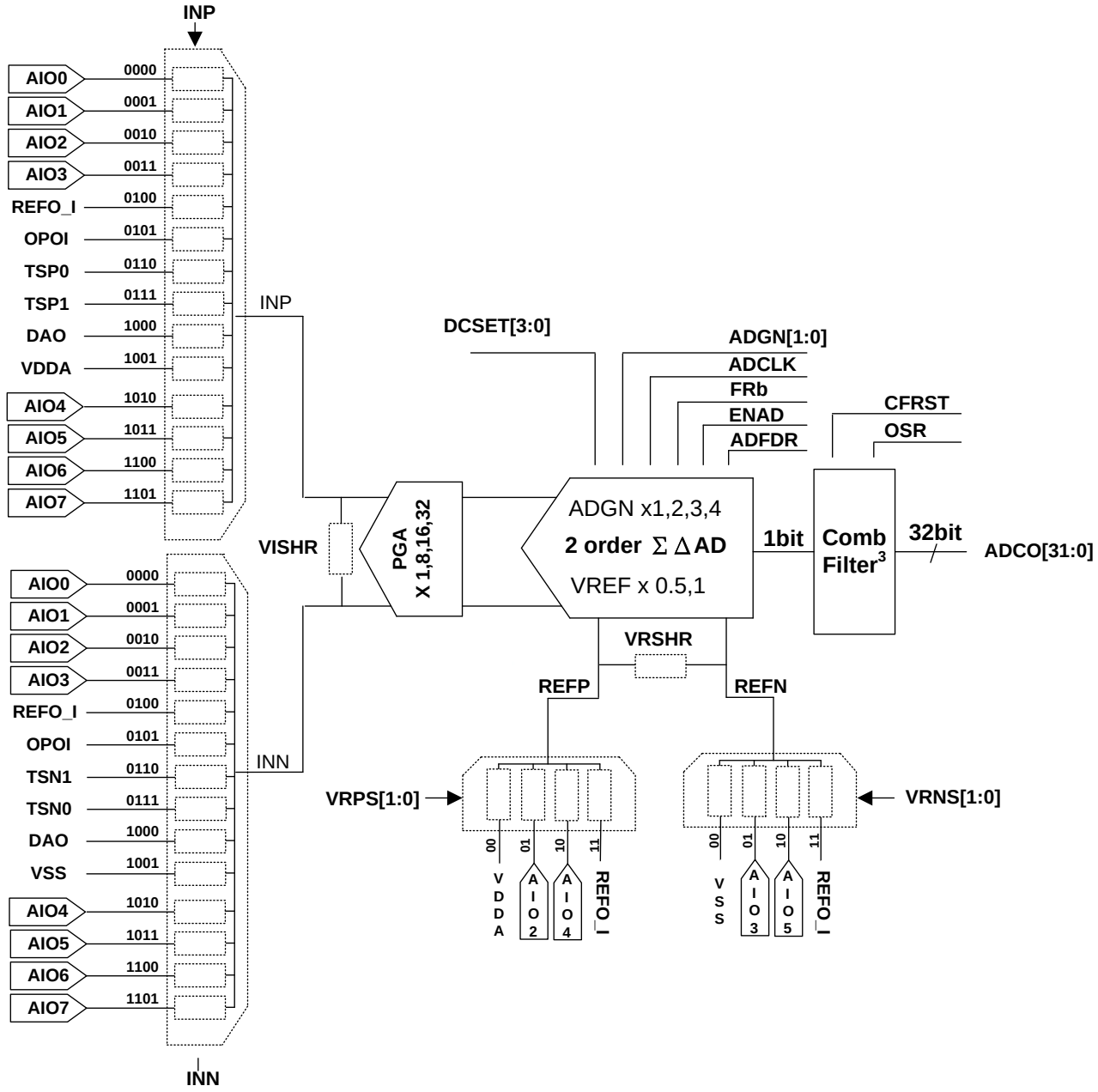
4.4 時鐘系統網絡


ENOHS
2~16MHz
HSXT
2 ~ 16MHz
HSXT
CKHS
HS_CK
ENHAO
HAO[1:0]
HAOTR[7:0]
HSRC
2/4/10/16
MHz
HSRC
MCUCKS
ENMCD
MCCK
CPU
Pre-scale
1, 2
APB
APCK
ENOLS
32.768KHz
LSXT
32.768KHz
LSXT
CKLS
LS_CK
LSRC
35KHz
LSRC
ENACD
ADCD[1:0]
HS_CK
Pre-scale
6,12,30,60
ADCK
ADC
CKS
LSXT
LSRC
CKH
ENRTCK
MCCK
Pre-scale
RTCK
RTC
ENADC
ADCK
ADCKo
Pre-scale
4
CHPCK
Charge
Pump
(internal used only)
ENSD
SPCD[2:0]
APCK
Pre-scale
1,2,4,
~2048
SPCK
SPI
ENWDT
LSRC
Pre-scale
256
WDCK
WDT
I2CEn
CRG[7:0]
APCK
Pre-scale
I2CK
I2C
TACKS
ENTAD
HS_CK
LS_CK
Pre-scale
32
TACK
Timer A
TUCKS
ENUD
UACD[3:0]
HSXT
HSRC
Pre-scale
1,2,4,~128
URCK
UART
TMCKS
ENTD
TMCD[1:0]
HS_CK
LS_CK
Pre-scale
1,2,4,8
TBCK
Timer B
Timer C
TU2CKS
ENU2D
UA2CD[3:0]
HSXT
HSRC
Pre-scale
1,2,4,~128
UR2CK
UART2
TM2CKS
ENT2D
TM2CD[1:0]
HS_CK
LS_CK
Pre-scale
1,2,4,8
TB2CK
Timer B2
IOCKS
IOCD[3:0]
HS_CK
LS_CK
Pre-scale
1,2,4,~16384
IOCK
GPIO
LCKS
LCDE
LCDO
LS_CK
HS_CK
Pre-scale
LCK
LCD

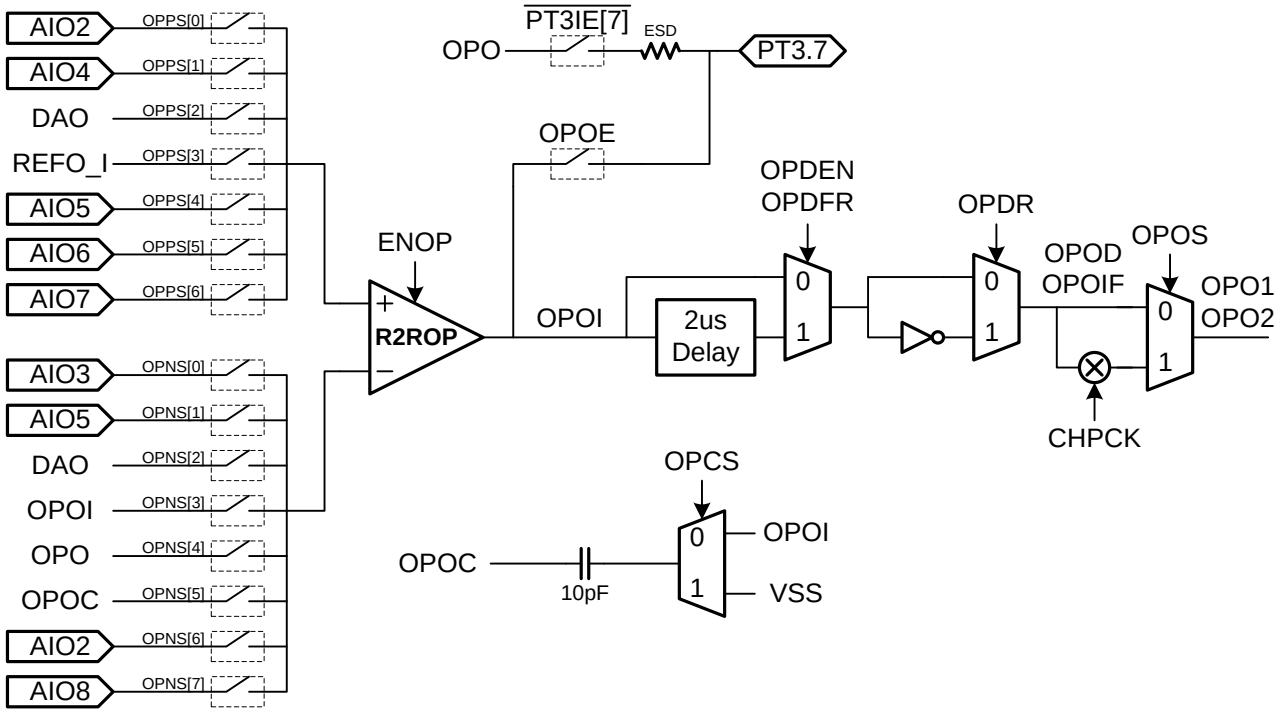
4.5 電源系統網絡


1uF
10μF
10μF
10μF
CL
CH
CP_I
CP_O
VDD3V
VLCD
ENb_CP
CP_CLK
EN_CP
Charge Pump + Regulator
(CP_O ~ 3.3V)
LCD_CLK
EN_LCD_CP
LCDV<1:0>
LCD Charge Pump
(2.6/2.8/3.0/3.3)
Regulator
VDD18
1μF
EN_BGR
EN_VDDA<1:0>
SEL_VDDA<1:0>
VDDA
(2.4/2.7/3.0/3.3)
VDDA
1μF
BGR
EN_REFO
REFO Buf
EN_REFO
REFO
VDDA
EN_VCM
ADC common voltage
1
0
VCM Buf
EN_VCM
0.1μF
PT3.6_ENI
VSS
REFO_I

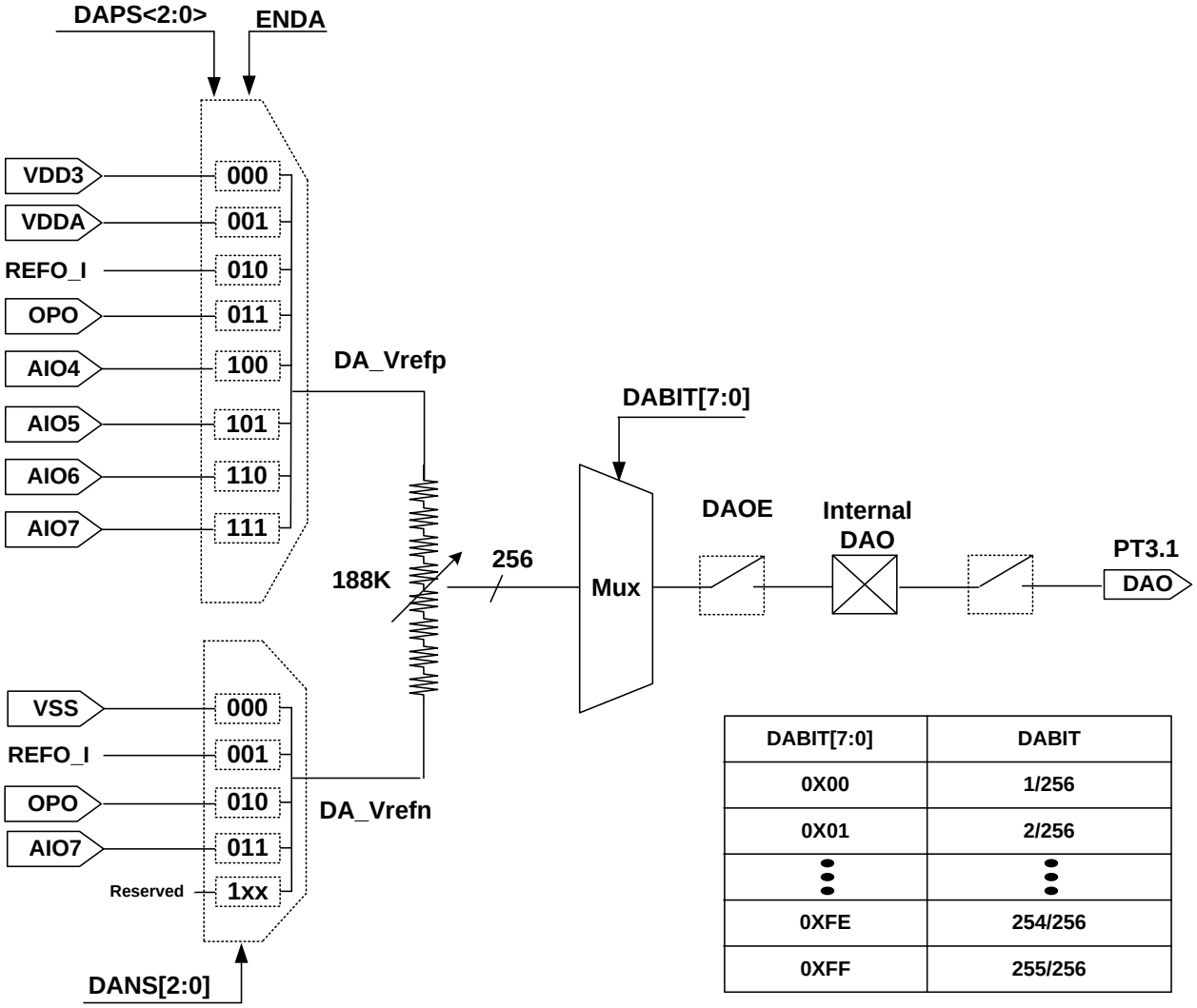
4.6 24-bit ΣΔADC 網絡



4.7 軌對軌運算放大器 OPAMP 網絡

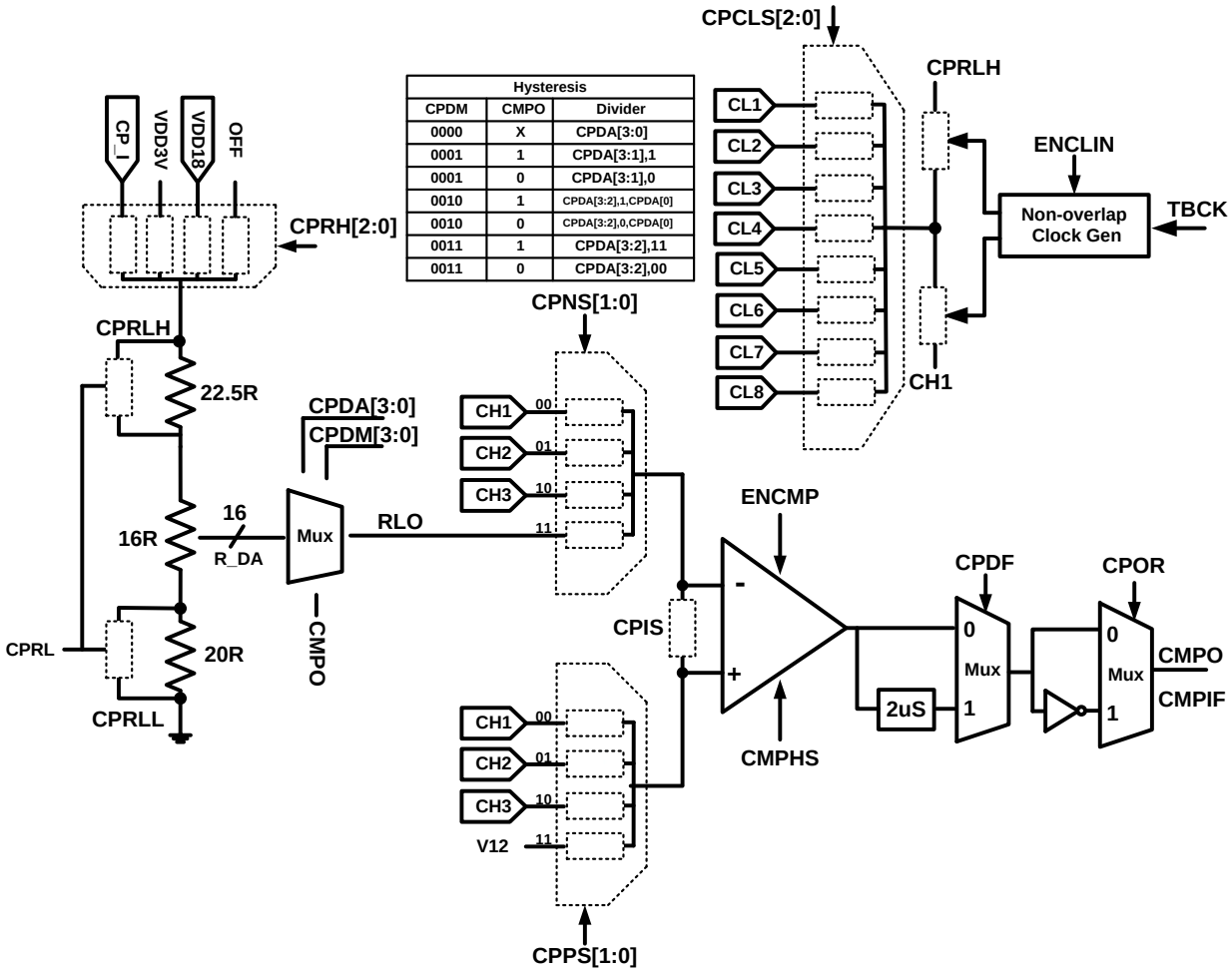


4.8 8-bit Resistance Ladder 網絡



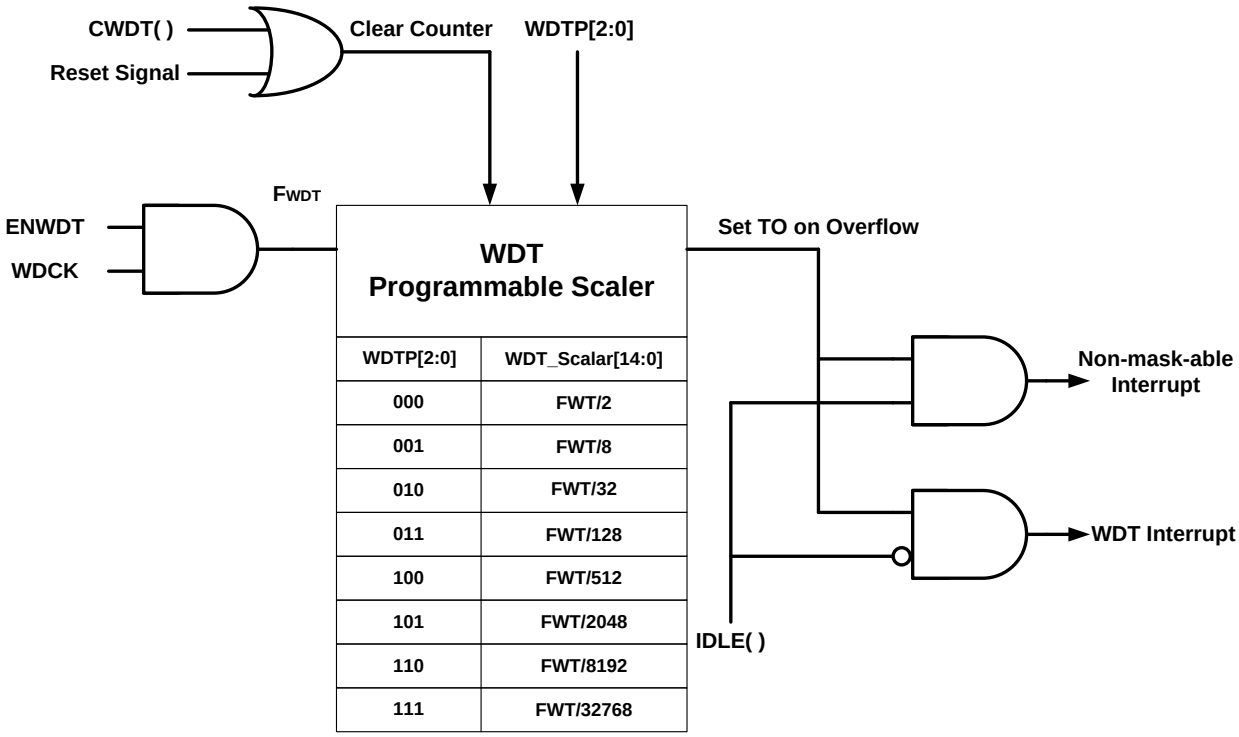
DABIT[7:0]	DABIT
0X00	1/256
0X01	2/256
⋮	⋮
0XFE	254/256
0XFF	255/256

4.9 多功能比較器 CMP 網絡



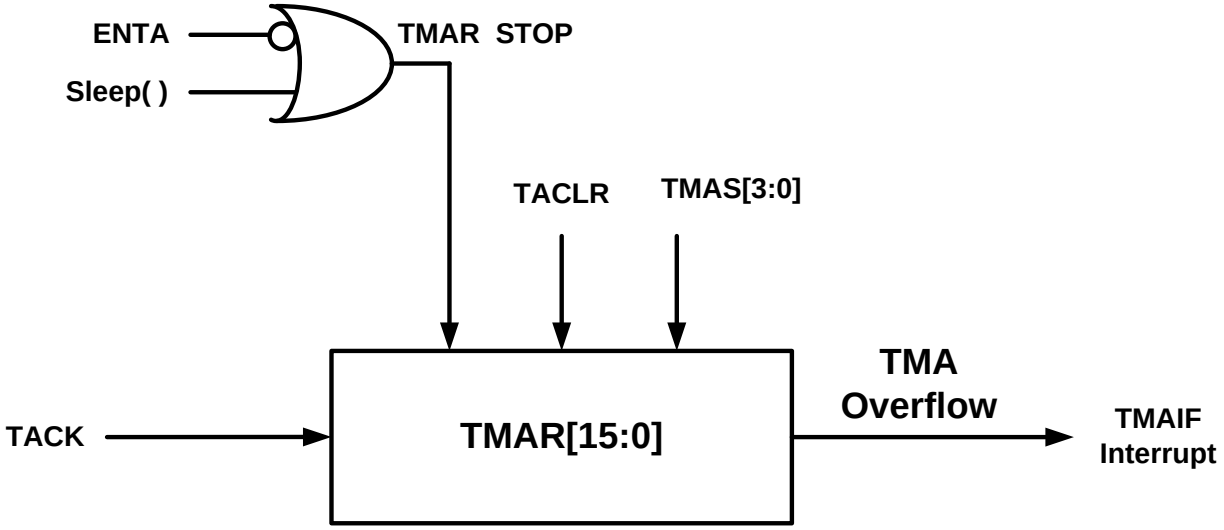
Hysteresis		
CPDM	CMPO	Divider
0000	X	CPDA[3:0]
0001	1	CPDA[3:1],1
0001	0	CPDA[3:1],0
0010	1	CPDA[3:2],1,CPDA[0]
0010	0	CPDA[3:2],0,CPDA[0]
0011	1	CPDA[3:2],11
0011	0	CPDA[3:2],00

4.10 看門狗(WDT)網絡



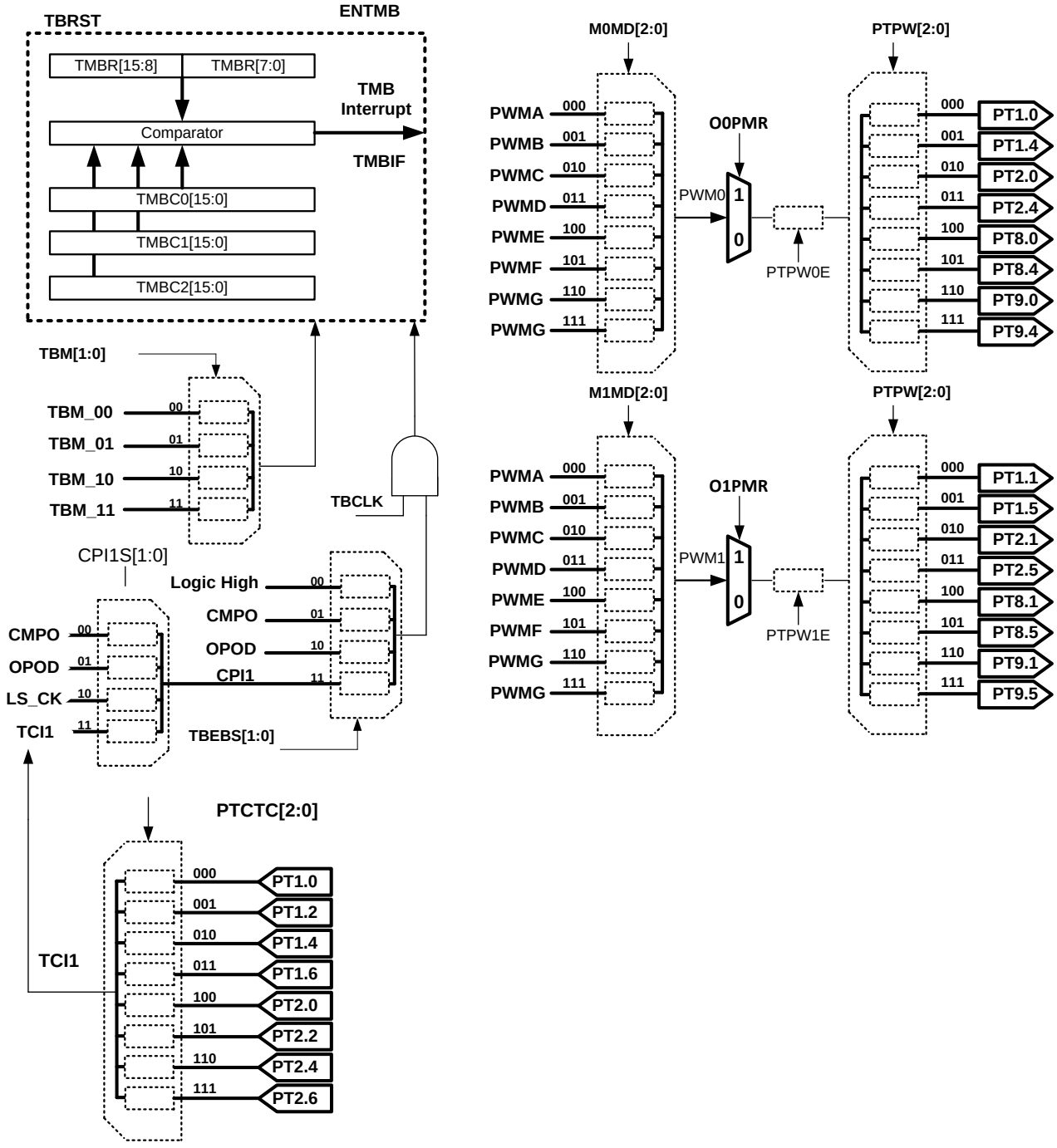
WDTP[2:0]	WDT_Scalar[14:0]
000	FWT/2
001	FWT/8
010	FWT/32
011	FWT/128
100	FWT/512
101	FWT/2048
110	FWT/8192
111	FWT/32768

4.11 定時計數器 A 網絡

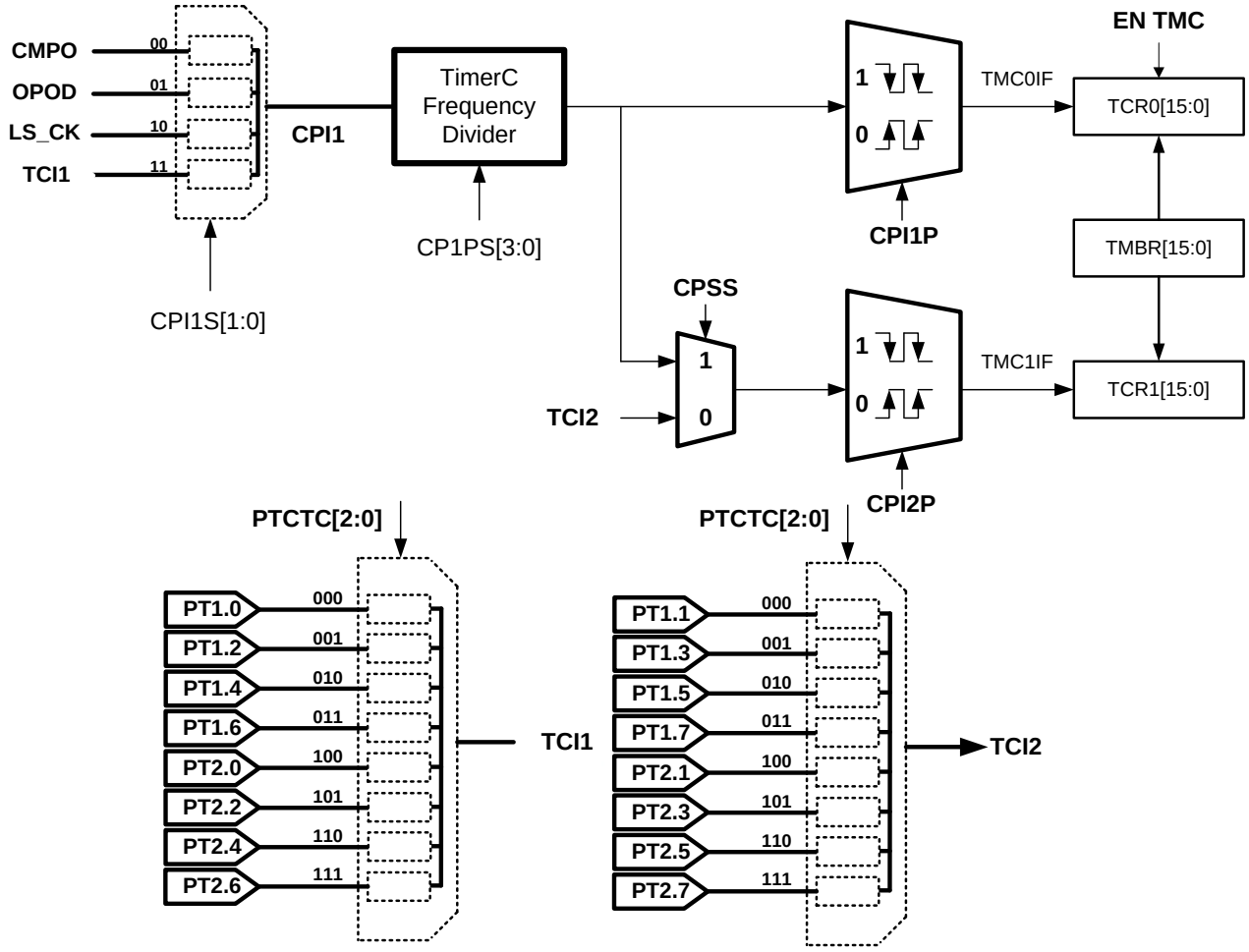


TMAS[3:0]	TMAR[15:0]	TMAS[3:0]	TMAR[15:0]
0000	TACK/2	1000	TACK/512
0001	TACK/4	1001	TACK/1024
0010	TACK/8	1010	TACK/2048
0011	TACK/16	1011	TACK/4096
0100	TACK/32	1100	TACK/8192
0101	TACK/64	1101	TACK/16384
0110	TACK/128	1110	TACK/32768
0111	TACK/256	1111	TACK/65536

4.12 定時計數器 B 網絡

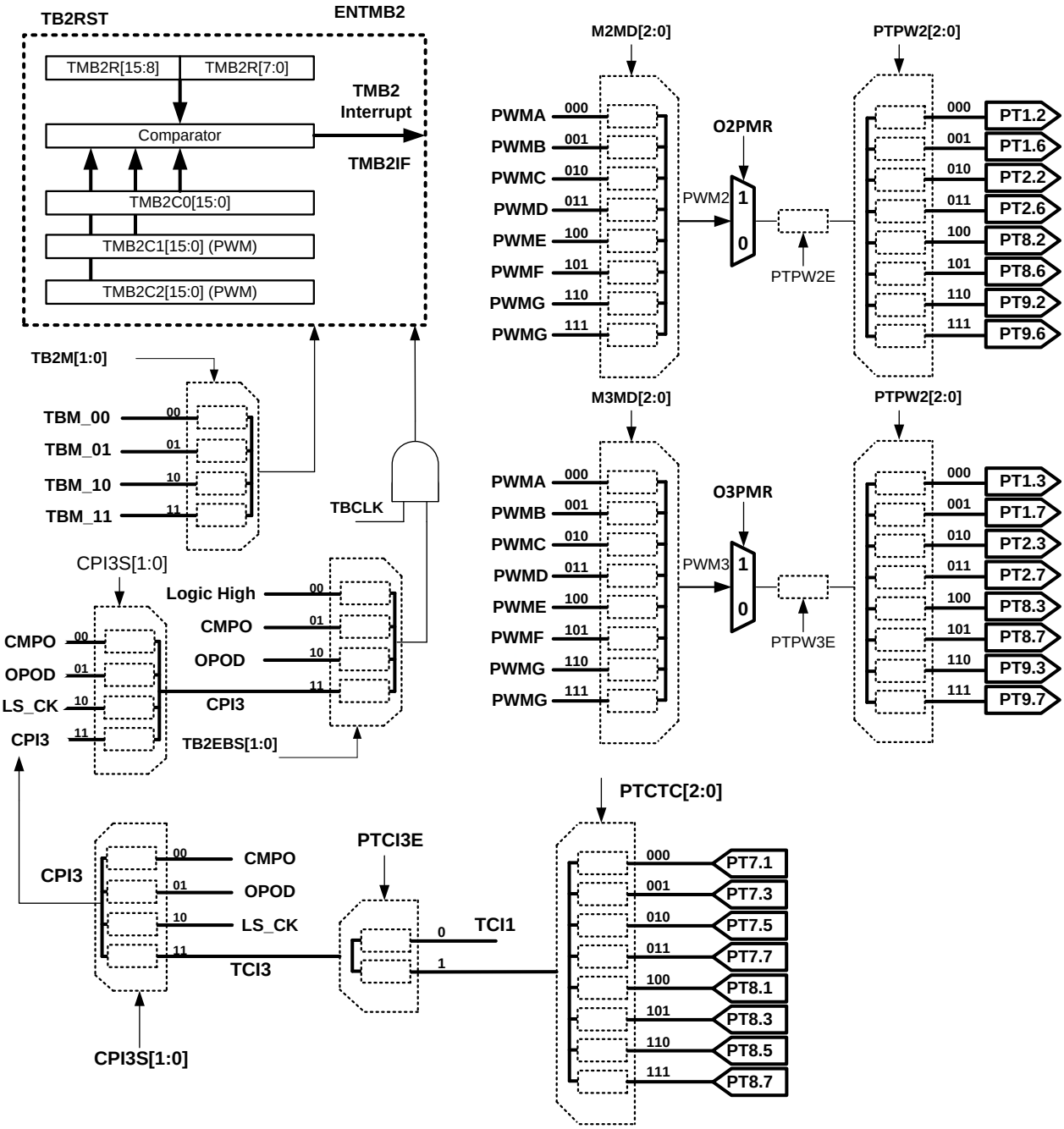


4.13 定時計數器 C 網絡

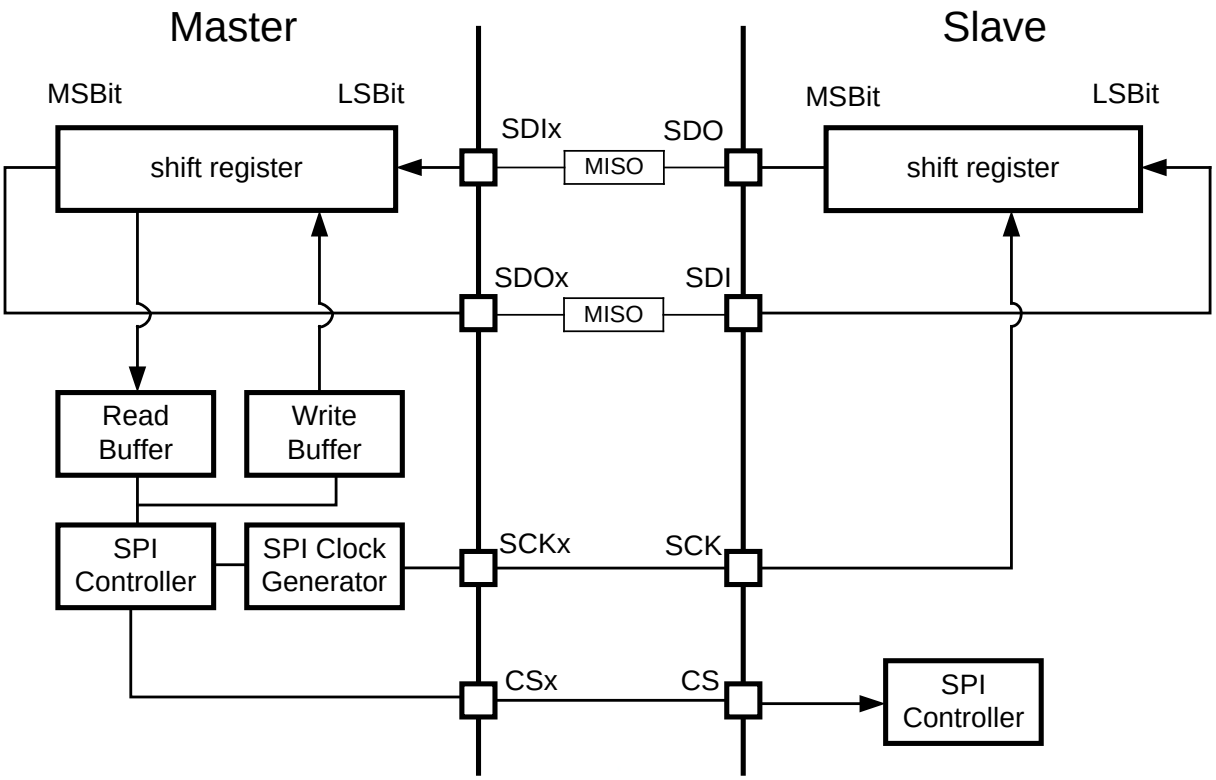


CP1PS[3:0]	CPI1 Divider	CP1PS[3:0]	CPI1 Divider
0000	CPI1/1	1000	CPI1/256
0001	CPI1/2	1001	CPI1/512
0010	CPI1/4	1010	CPI1/1024
0011	CPI1/8	1011	CPI1/2048
0100	CPI1/16	1100	CPI1/4096
0101	CPI1/32	1101	CPI1/8192
0110	CPI1/64	1110	CPI1/16384
0111	CPI1/128	1111	CPI1/32768

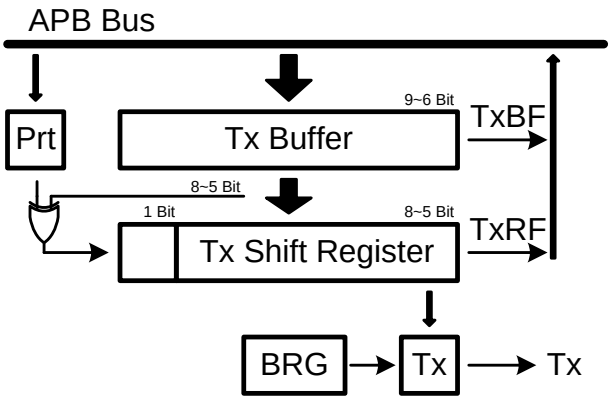
4.14 定時計數器 B2 網絡



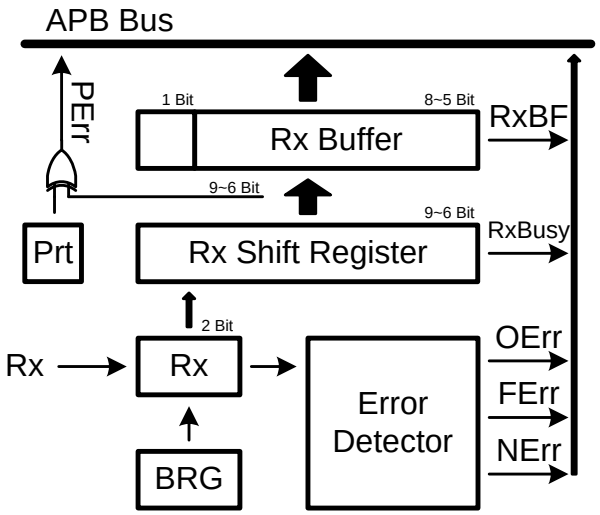
4.15 32-bit SPI 網絡



4.16 UART 網絡

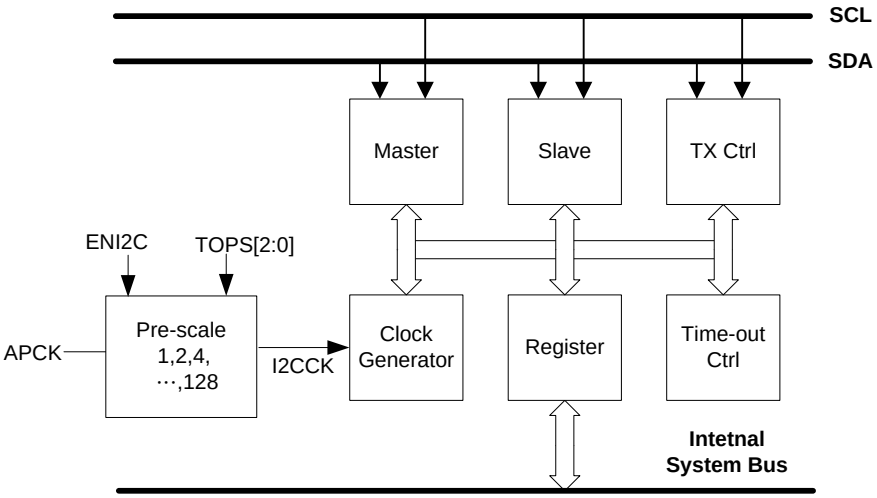


UART Transmit Block Diagram

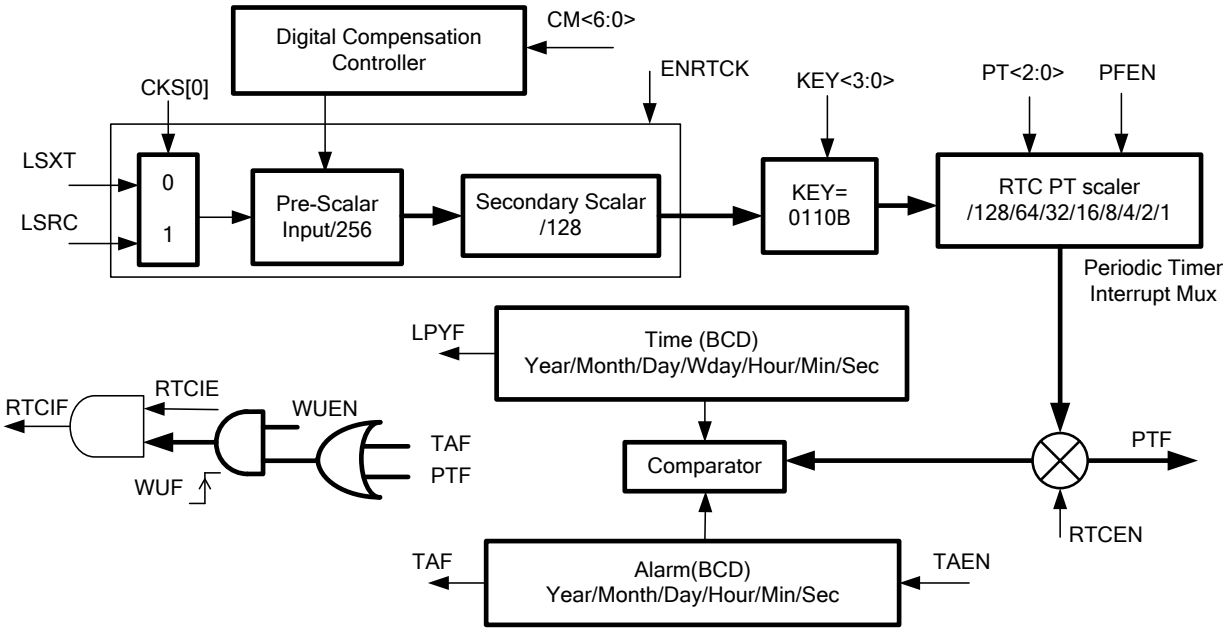


UART Receive Block Diagram

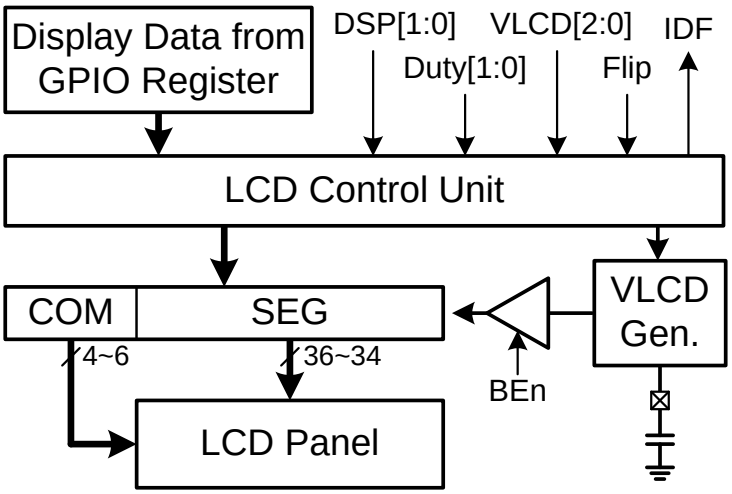
4.17 I2C 網絡



4.18 硬體時鐘 RTC 網絡



4.19 LCD 網路


Display Data from GPIO Register
DSP[1:0]
Duty[1:0]
VLCD[2:0]
Flip
IDF
LCD Control Unit
COM
SEG
4~6
36~34
BEn
VLCD Gen.
LCD Panel

5. Electrical Characteristics

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at VDD3V to VSS . . . . . −0.2 V to 4.0 V
Voltage applied to any pin . . . . . −0.2 V to VDD3V + 0.3 V
Diode current at any device terminal . . . . . ±2mA
Storage temperature, Tstg: (UN programmed device) . . . . . −55℃ to 150℃
(Programmed device) . . . . . −40℃ to 85℃
Soldering Temperature (10 Sec) . . . . . +260°C
Maximum output current sink by any PORT1 to PORT10 I/O PIN 10mA

5.1 Recommended Operating Conditions

VDD3V=2.2V to 3.6V.TA=-40℃~85℃,Unless Otherwise Noted

Parameter	Sym.	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	VDD3V	Digital Application	2.2	3.0	3.6	V
Supply Current	I_Sleep	Sleep Mode		2.5		uA
	I_Idle01	LSRC=34KHz+IDLE Mode		5.0		uA
	I_Idle02	HSRC=2MHz+IDLE Mode		50		uA
	I_Wait	LSRC=34KHz+Wait Mode		130		uA
	Free Run_01MHz	HSRC=2MHz@CPU_CK:2MHz/2		0.6		mA
	Free Run_02MHz	HSRC=2MHz@CPU_CK:2MHz		1.0		mA
	Free Run_04MHz	HSRC=4MHz@CPU_CK:4MHz		1.8		mA
	Free Run_10MHz	HSRC=10MHz@CPU_CK:10MHz		3.0		mA
	Free Run_16MHz	HSRC=16MHz@CPU_CK:16MHz		4.0		mA
Power Up Delay	$t_{PU,DLY}$	Wake Up From Sleep		64		ms

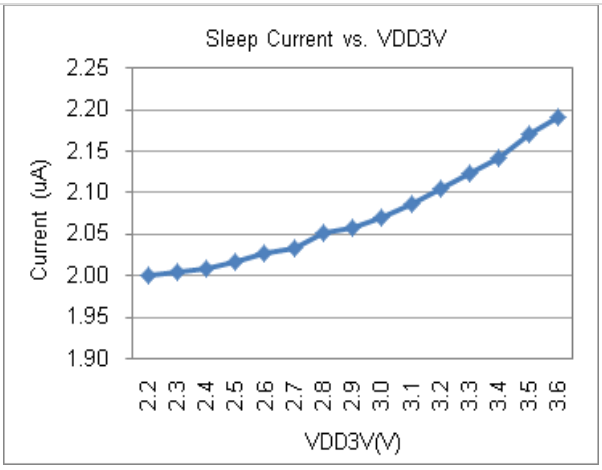


Figure5.1-1 Sleep Current vs. VDD3V

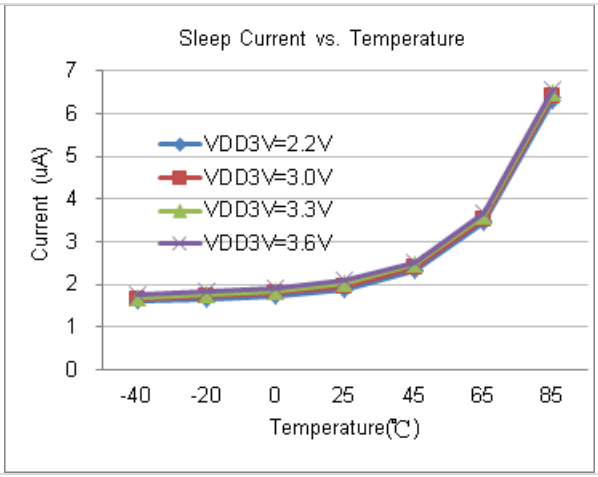


Figure5.1-2 Sleep Current vs. Temperature

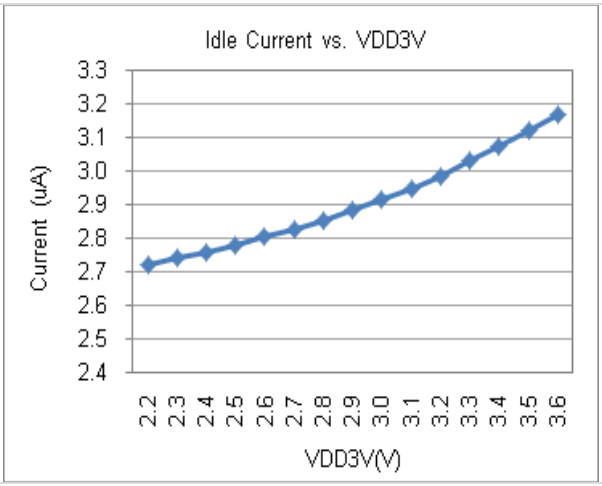


Figure5.1-3 Idle Current vs. VDD3V

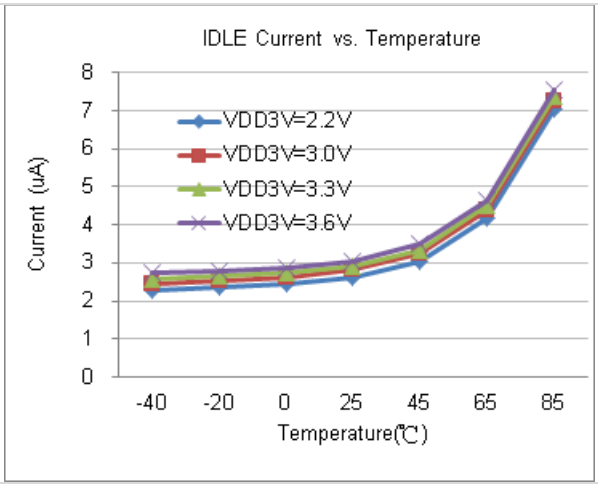


Figure5.1-4 Idle Current vs. Temperature

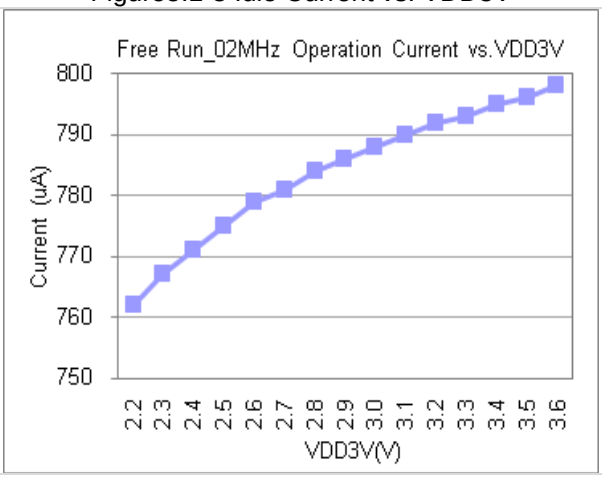


Figure5.1-5 Free Run_02MHz Operation Current vs. VDD3V

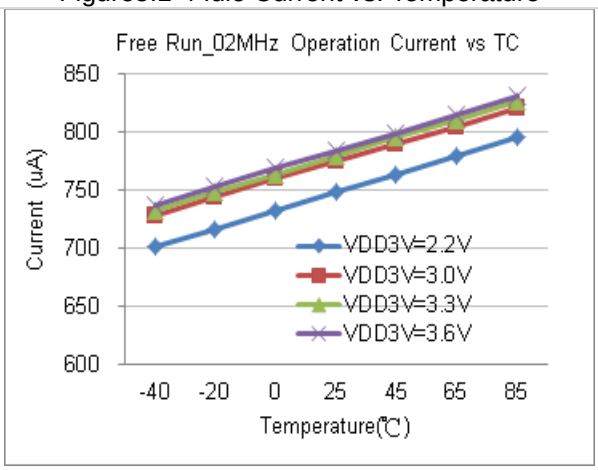


Figure5.1-6 Free Run_02MHz Current vs. Temperature

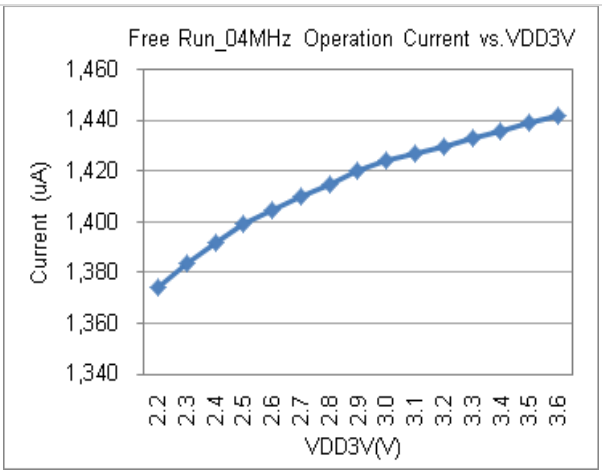


Figure5.1-7 Free Run_04MHz Operation Current vs. VDD3V

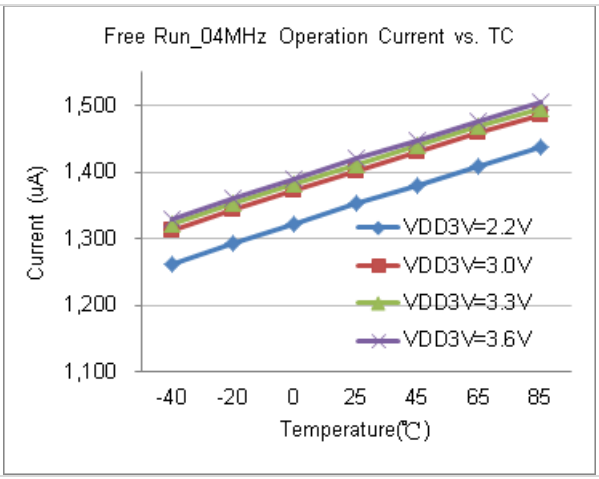


Figure5.1-8 Free Run_04MHz Current vs. Temperature

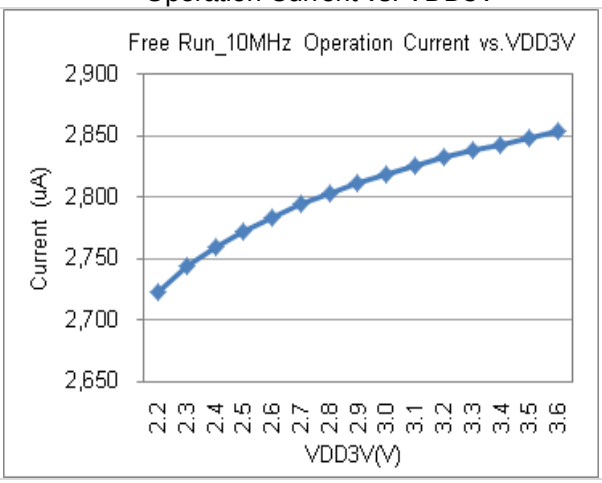


Figure5.1-9 Free Run_10MHz Operation Current vs. VDD3V

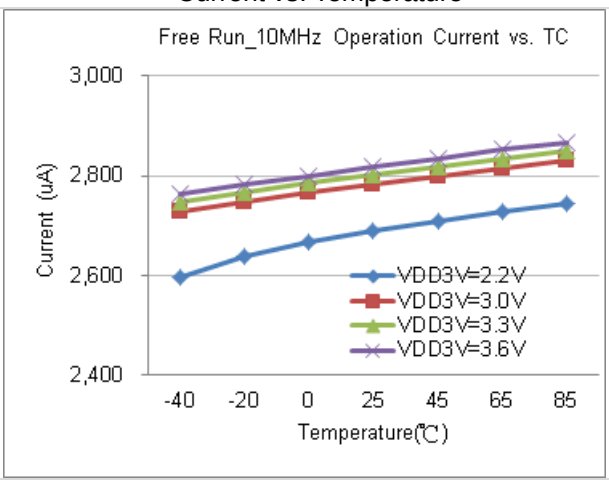


Figure5.1-10 Free Run_10MHz Current vs. Temperature

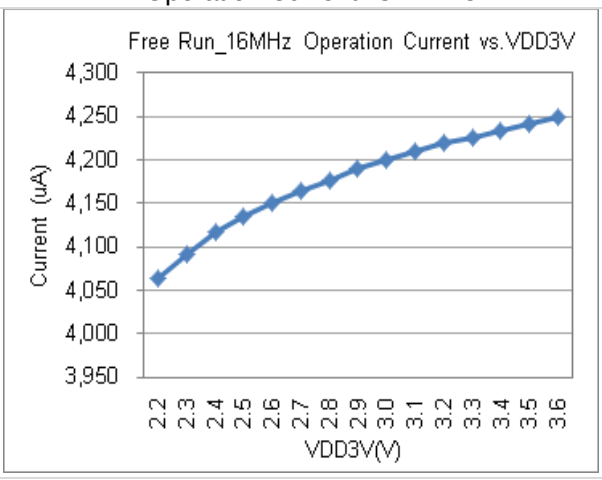


Figure5.1-11 Free Run_16MHz Operation Current vs. VDD3V

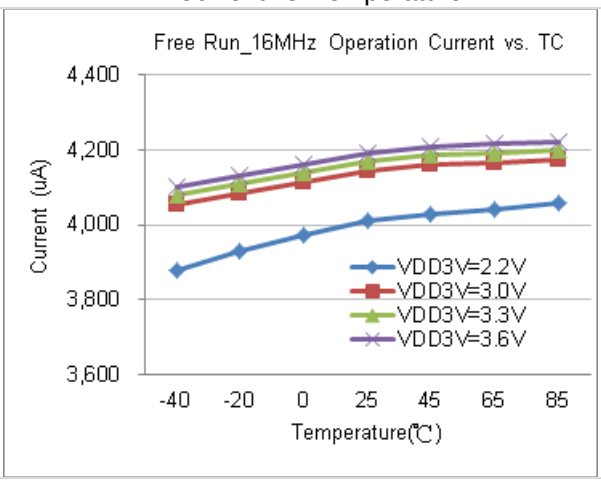


Figure5.1-12 Free Run_16MHz Current vs. Temperature

5.2 Clock System

Typical values are at T_A=25℃ and VDD3V = 3.0V.Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
External High Speed Oscillator						
VDD3V	Operation voltage		2.2		3.6	V
F_{XHS}	High speed oscillator frequency	VDD3V = 2.2V ~ 3.6V OHS_HS = 1b	4		16	MHz
		VDD3V = 2.2V ~ 3.6V OHS_HS = 0b	2		4	MHz
I_{XHS}	High speed oscillator current	F_{XHS} = 16MHz		100		uA
D_{XHS}	Duty of high oscillator		40		60	%
External Low Speed Oscillator						
F_{XLS}	Low speed oscillator frequency	VDD3V = 2.2V ~ 3.6V		32.768		KHz
I_{XLS}	Low speed oscillator current			2		uA
D_{XLS}	Duty of low speed oscillator		40		60	%
RTC	Normal Mode	VDD3V=3.3V @Flash Run		10		uA
Internal High Speed Oscillator						
F_{HAO}	Internal high speed oscillator frequency	F_{HAO} = 2MHz, after trim	-2%	1.843	+2%	MHz
		F_{HAO} = 4MHz, after trim	-2%	4.147	+2%	MHz
		F_{HAO} = 10MHz, after trim	-2%	9.216	+2%	MHz
		F_{HAO} = 16MHz, after trim	-2%	15.667	+2%	MHz
	Voltage coefficient	VDD3V = 2.2V ~ 3.6V	-0.2		+0.2	%
T_{HAO}	Temperature coefficient	-40~85℃	-1.5		+1.5	%
I_{HAO}	Internal high speed oscillator current	F_{HAO} = 2MHz		20		uA
		F_{HAO} = 16MHz		75		uA
D_{HAO}	Duty of oscillator		40		60	%
WT_{HAO}	Wake up time	F_{HAO} = 2MHz		30		us
Internal Low Speed Oscillator						
F_{LPO}	Internal low speed oscillator frequency	VDD3V = 3.3V	-10%	35	+10%	KHz
	Voltage coefficient	VDD3V = 2.2V ~ 3.6V	-2.5		+2.5	%
T_{LPO}	Temperature coefficient	-40~85℃	-2.5		+2.5	%
I_{LPO}	Internal low speed oscillator current			0.35	0.7	uA
D_{LPO}	Duty of low speed oscillator		40		60	%

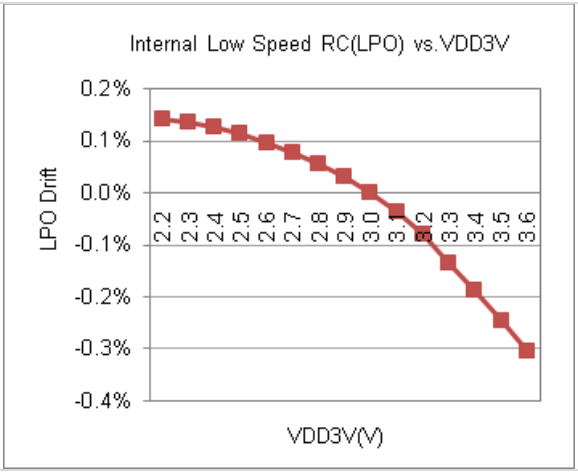


Figure5.2-1 LPO vs. VDD3V

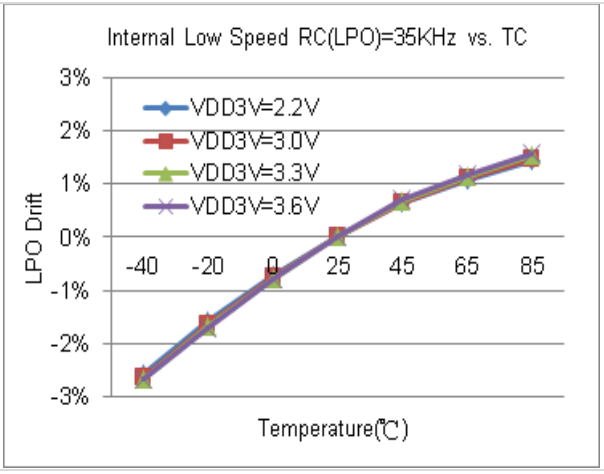


Figure5.2-2 LPO vs. Temperature

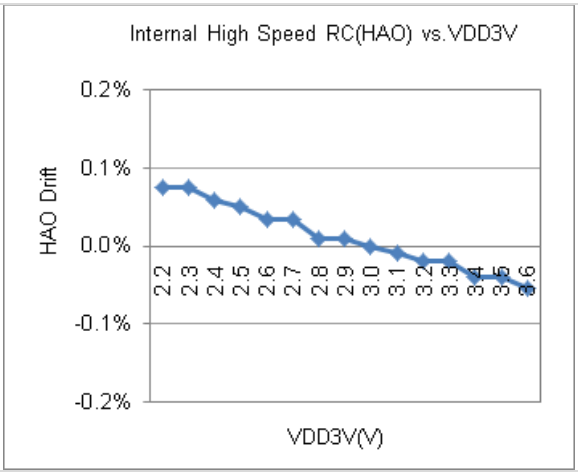


Figure5.2-3 HAO vs. VDD3V

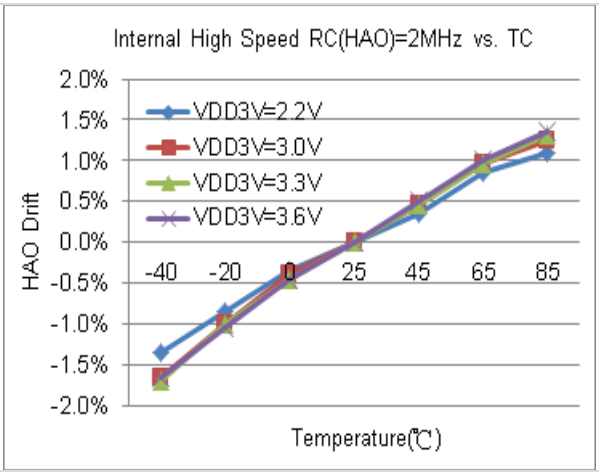


Figure5.2-4 HAO vs. VDD3V

5.3 Power Management System

Typical values are at T_A=25℃ and VDD3V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDDA LDO						
	Output voltage error		-5		5	%
	Capacitor loading		0.1	1	10	uF
	Settling time	Capacitor loading = 0.1uF, 99% of VDDA		50		us
	Operation current	Bias + Band gap + VDDA LDO		35	50	uA
	Dropout voltage	I_L=10mA		0.2		V
	Voltage coefficient	VDD3V = 2.5 ~ 3.6V		0.1		%/V
	VDDA voltage 1	I_L = 0.1mA		2.4		V
	VDDA voltage 2	I_L = 0.1mA		2.7		V
	VDDA voltage 3	I_L = 0.1mA		3.0		V
	VDDA voltage 4	I_L = 0.1mA		3.3		V
	Temperature coefficient	By using BRG VDDA=3.0V		100		ppm/°C
VDD18 LDO						
	Output voltage		1.7	1.8	1.9	V
	Capacitor loading		100	1000	10,000	nF
	Voltage coefficient	VDD3V= 2.2 ~ 3.6V		1		%/V
	Temperature coefficient			100		ppm/°C
	Load regulation	Load = 0.1~10mA		0.1		V/A
	Dropout voltage	Load = 10mA		0.2		V
REFO Buffer						
	Capacitor loading		22	100	1000	nF
	Operation current			15		uA
	Output current	1% change voltage	-1		1	mA
	Temperature coefficient	VDDA=3.0V		80		ppm/°C
	Offset voltage	REFO = 1.2V		±3	±12	mV
	Voltage coefficient	VDDA= 2.4V ~ 3.6V		0.1		%/V

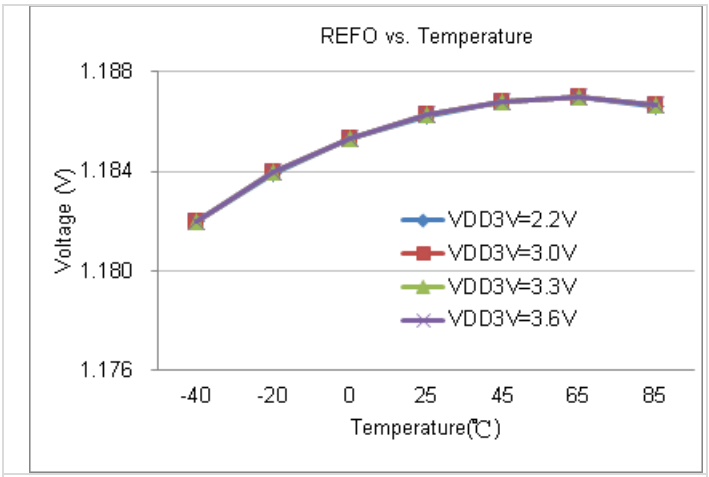


Figure5.3-1 REFO vs. Temperature

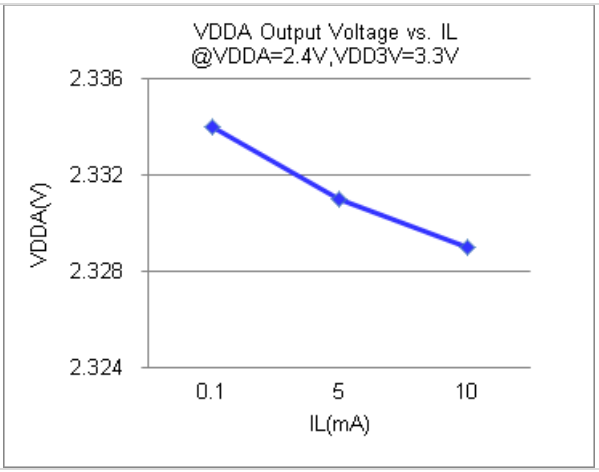


Figure5.3-2 VDDA vs. IL

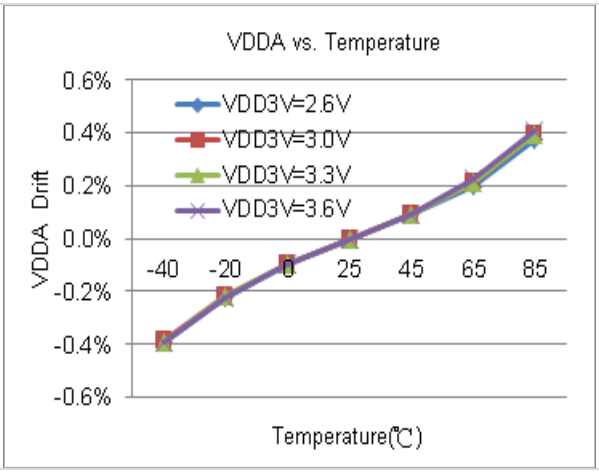


Figure5.3-3 VDDA vs. Temperature

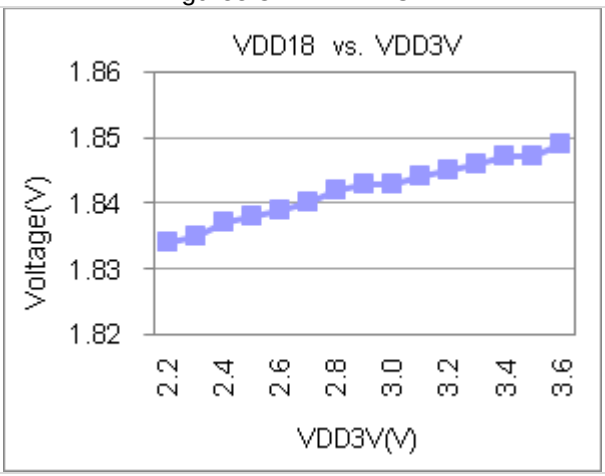


Figure5.3-4 VDD18 vs. VDD3V

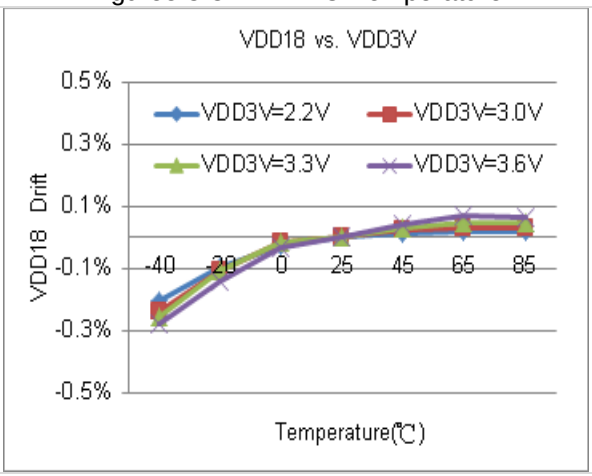


Figure5.3-5 VDD18 vs. Temperature

5.4 Charge Pump System

Typical values are at T_A=25℃, VDD3V = 3.0V, and C_{CP_O}:10uF. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CP_I	VDD supply voltage		2.4		3.6	V
CP_O	Backlight voltage	C_{CPO}:10uF, C_{HL}:1uF, VDD3V=3V, Loading≦15mA		3.3		V
I_{LED}	Driving current	VDD3V = 2.4V			15	mA

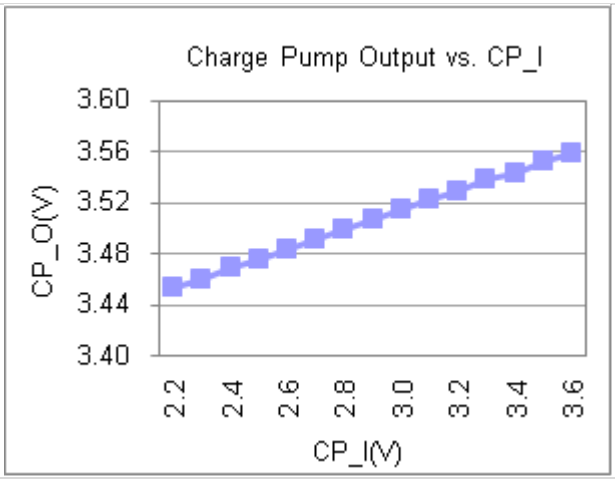


Figure5.4-1 CP_O vs. CP_I

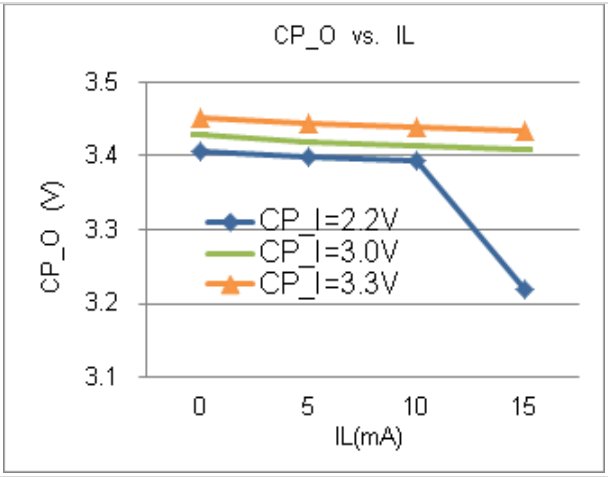


Figure5.4-2 CP_O vs. IL

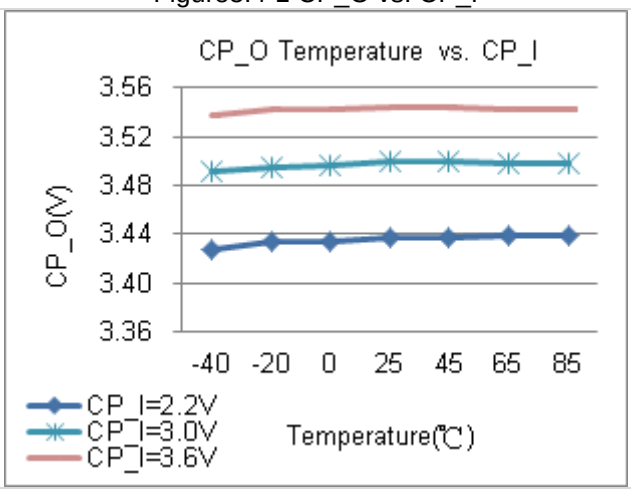


Figure5.4-3 CP_O vs. Temperature

5.5 Reset Management System

Reset Management System includes Brownout/External RST Pin/Low Voltage Detect.
Typical values are at T_A=25℃ and VDD3V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Min.	Typ.	Max.	Unit
BOR	Pulse length needed to accepted reset internally, $t_{d\text{-}LVR}$	2			us
	VDD Start Voltage to accepted reset internally (L→H),V_{LVR}	1.8	1.95	2.1	V
	Temperature drift, T_A=-40℃~85℃	-50		+50	mV
	Hysteresis, $V_{HYS\text{-}LVR}$		50		mV
POR	Operation Slew Rate			0.1	V/us
	Start Voltage to accepted reset	0.6			V

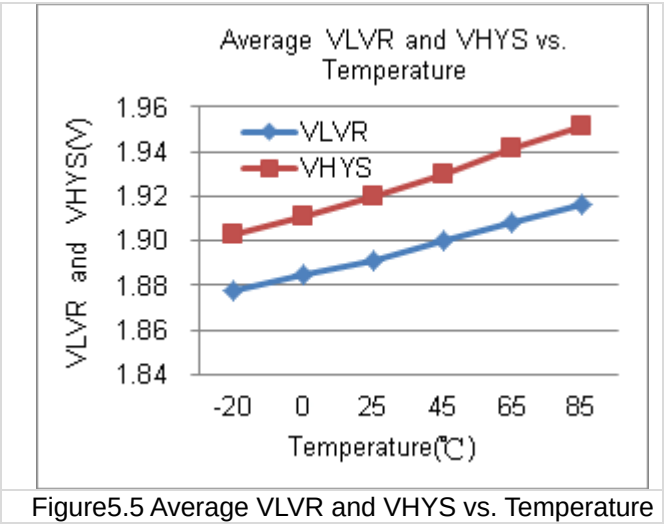


Figure5.5 Average VLVR and VHYS vs. Temperature

5.6 GPIO Port System

Typical values are at T_A=25℃ and VDD3V = 3.3V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PT 1.0 ~ 4.0 GPIO Port						
R_{PU}	Internal pull high resistor			75		kΩ
V_{IH}	Input high voltage		0.7*VDD3V			V
V_{IL}	Input low voltage				0.3*VDD3V	V
I_{OH}	Source current			10		mA
I_{OL}	Sink current			10		mA
PT 6.0 ~ 10.1 GPIO Port						
V_{IH}	Input high voltage		0.6*VDD3V			V
V_{IL}	Input low voltage				0.3*VDD3V	V
I_{OH}	Source current	VDD3V-0.3V		10		mA
I_{OL}	Sink current	VSS+0.3V		10		mA

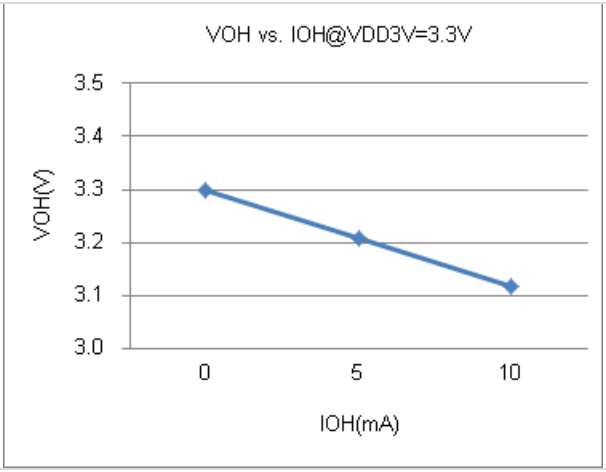


Figure5.6-1 VOH vs. IOH

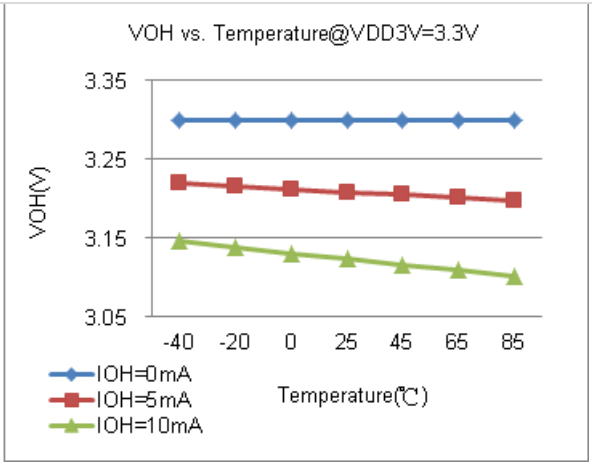


Figure5.6-2 VOH vs. Temperature

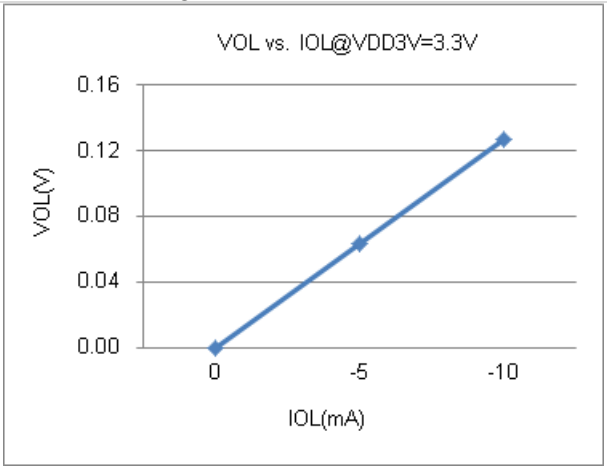


Figure5.6-3 VOL vs. IOL

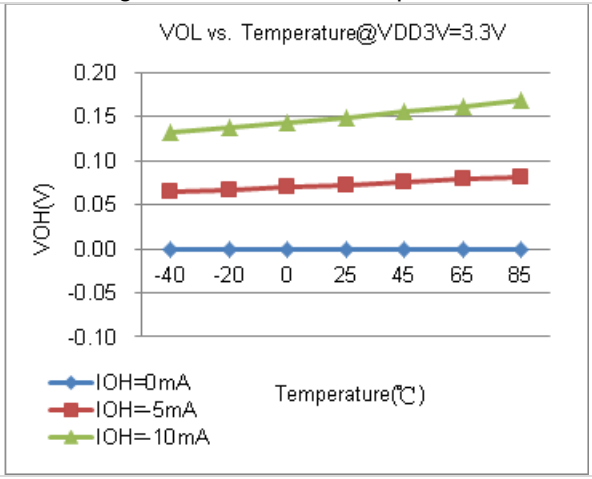


Figure5.6-4 VOL vs. Temperature

5.7 ΣΔADC ENOB and RMS Noise

Typical values are at TA=25℃ and VDD3V = 3.3V, VDDA=2.4V unless otherwise noted.

HY16F198 provides important input noise specification that aims at ΣΔADC. Table 5.6-1 and Table 5.7-2 lists out the relations of typical noise specification, Gain, Output rate, and maximum input voltage of single end. Test condition configuration and external input signal short, voltage reference: 1.2V and 1024 records were sampled.

ENOB(RMS) with OSR/GAIN at A/D Clock=333Khz, VDDA=2.4V, VREF=1.2V															
Max. Vin(mV) =0.9*VREF (1)	**OSR**					**32**	**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**	**8192**	**16384**	**32768**
	Output rate(HZ)					**10417**	**5208**	**2604**	**1302**	**651**	**326**	**163**	**81**	**41**	**20**	**10**
	Gain	**=**	**PGA**	**×**	**ADGN**											
±1080	**1**	**=**	**1**	**×**	**1**	12.3	14.2	16.3	16.8	17.4	17.9	18.3	18.8	19.4	19.9	20.3
±540	**2**	**=**	**1**	**×**	**2**	11.8	13.1	16.0	16.6	17.0	17.4	18.0	18.7	19.3	19.7	20.2
±135	**4**	**=**	**1**	**×**	**4**	11.1	14.6	16.0	16.5	16.9	17.3	17.9	18.6	19.1	19.5	20.1
±33.75	**32**	**=**	**8**	**×**	**4**	11.1	12.2	14.9	15.4	15.7	16.1	16.7	17.6	18.1	18.6	19.1
±16.875	**64**	**=**	**16**	**×**	**4**	11.1	12.7	14.6	15.1	15.4	15.9	16.4	17.1	17.6	18.1	18.6
±11.25	**96**	**=**	**24**	**×**	**4**	11.1	12.1	14.3	14.8	15.3	15.7	16.3	16.9	17.4	17.9	18.4
±8.435	**128**	**=**	**32**	**×**	**4**	11.1	13.4	14.1	14.6	15.1	15.5	16.1	16.7	17.1	17.6	18.2
(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).																

Table 5.7-1 ΣΔADC ENOB Table

RMS Noise(uV) with OSR/GAIN at A/D Clock=333Khz, VDDA=2.4V, VREF=1.2V															
Max. Vin(mV) =0.9*VREF	**OSR**					**32**	**64**	**128**	**256**	**512**	**1024**	**2048**	**4096**	**8192**	**16384**	**32768**
	Output rate(HZ)					**10417**	**5208**	**2604**	**1302**	**651**	**326**	**163**	**81**	**41**	**20**	**10**
	Gain	**=**	**PGA**	**×**	**ADGN**											
±1080	**1**	**=**	**1**	**×**	**1**	459	124	28.7	19.97	13.95	9.93	7.17	5.03	3.49	2.49	1.812
±540	**2**	**=**	**1**	**×**	**2**	323	136	17.6	11.62	9.08	6.97	4.60	2.78	1.88	1.39	0.966
±135	**4**	**=**	**1**	**×**	**4**	260	23.9	8.7	6.51	4.71	3.72	2.47	1.47	1.05	0.78	0.541
±33.75	**32**	**=**	**8**	**×**	**4**	33.1	15.9	2.4	1.69	1.38	1.09	0.70	0.38	0.26	0.19	0.132
±16.875	**64**	**=**	**16**	**×**	**4**	16.2	5.4	1.5	1.06	0.83	0.61	0.42	0.26	0.18	0.13	0.092
±11.25	**96**	**=**	**24**	**×**	**4**	11.3	5.5	1.2	0.85	0.60	0.45	0.30	0.20	0.14	0.10	0.071
±8.435	**128**	**=**	**32**	**×**	**4**	8.4	1.8	1.0	0.75	0.53	0.39	0.27	0.17	0.13	0.09	0.063

Table 5.7 -2 ΣΔADC RMS Table

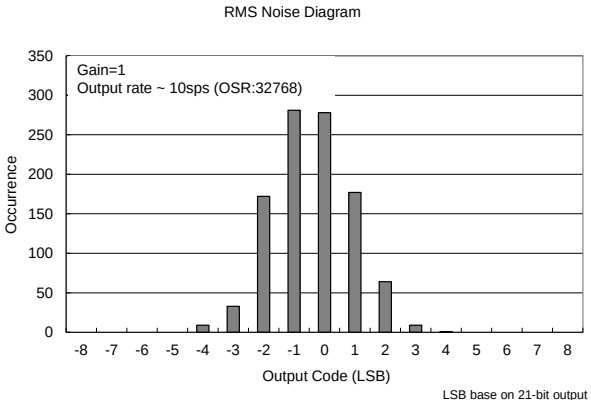


Figure5.7-1(a) RMS Noise Diagram

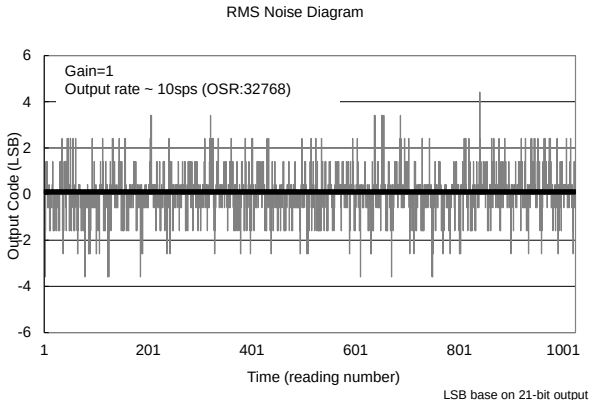


Figure5.7-1(b) Output Code Diagram

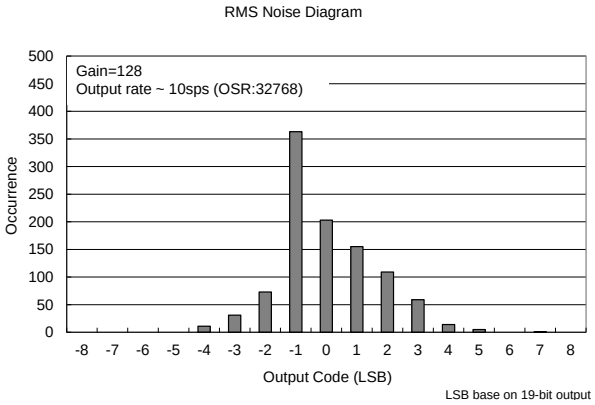


Figure5.7-2(a) RMS Noise Diagram

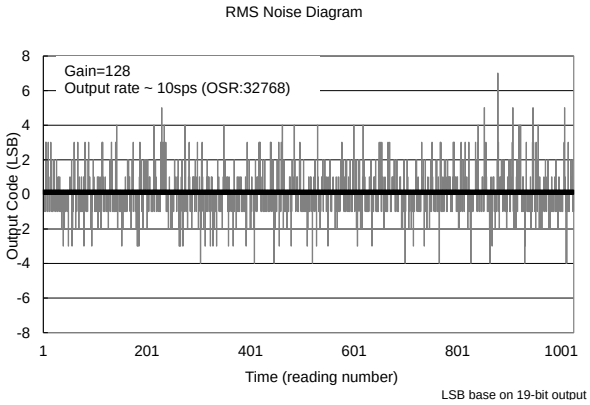


Figure5.7-2(b) Output Code Diagram

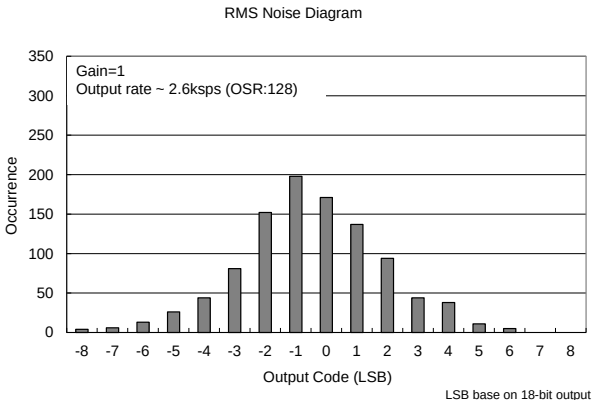


Figure5.7-3(a) RMS Noise Diagram

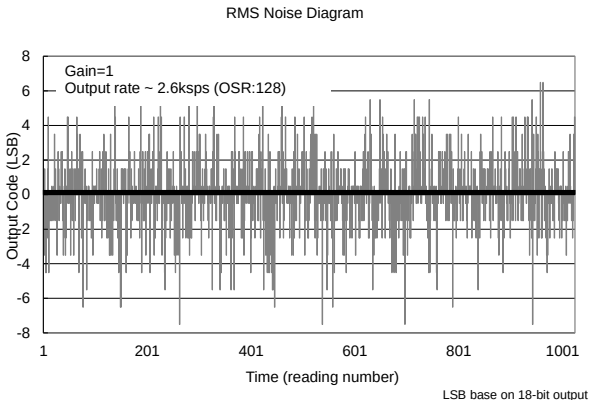


Figure5.7-3(b) Output Code Diagram

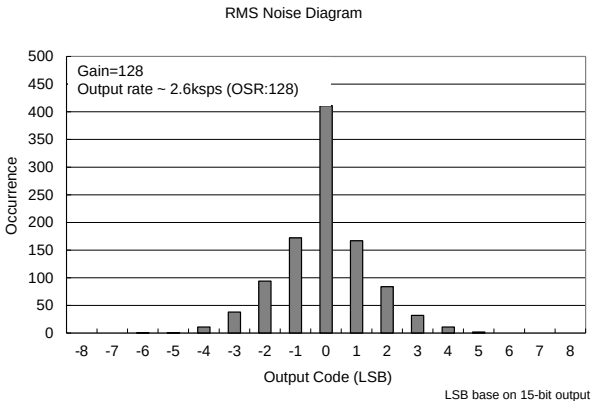


Figure5.7-4(a) RMS Noise Diagram

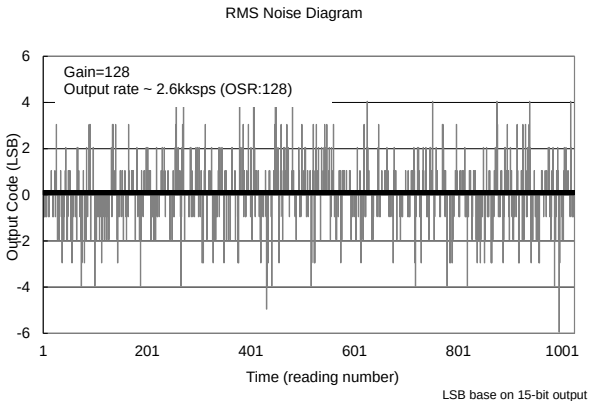


Figure5.7-4(b) Output Code Diagram

5.8 ADC Management System

All specifications at T_A=-40℃ to +85℃,
VDDA=REFP=3.0V, REFN=VSS, and Gain=128. Unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
Analog Inputs							
	Full-scale input voltage (VINP - AINN)				±0.5*VREF/Gain		V
	Common-mode input range	Gain = 1		VSS-0.2V		VDDA	V
System Performance							
	Resolution	No missing codes			24		Bits
	Data rate				ADC Clock /OSR		SPS
	Digital filter settling time	Full setting			3		Data
	Integral nonlinearity (INL)	Differential input End-point fit,OSR=32768			15		PPM
	Gain drift				5		ppm/℃
	Normal-mode rejection	f_{IN}=60Hz ±1Hz, Output rate = 10 SPS	Internal OSC		70		dB
			External OSC		80		dB
	Common-mode rejection	ΔVDDA = 0.1V @ DC			80		dB
	Input-referred noise	Output rate= 10 SPS			65		nV, rms
	Power-supply rejection	ΔVDDA = 0.1V @ DC			80		dB
Voltage Reference Input							
	Voltage reference input	VREF = REFP - REFN				VDDA	V
	Positive Reference Input	REFP		VDDA/2		VDDA+0.1	V
	Negative Reference Input	REFN		VSS-0.1V		VDDA/2	V
ADC Modulator Current							
ADC	ADC Modulator	VDD3V=3.3V,VDDA=2.4V			150		uA
PGA	ADC PGA	VDD3V=3.3V,VDDA=2.4V			625		uA

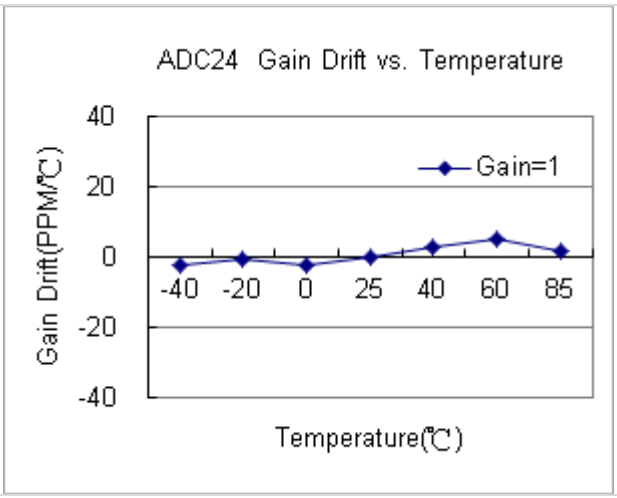


Figure5.8-1 ADC24 Gain Drift Gain=1
Vin=320mV SPS=10Hz
Delta VR=1V and VDDA=2.7V

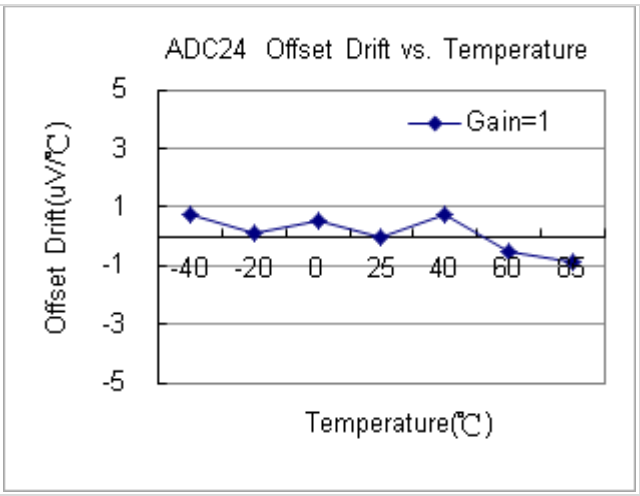


Figure5.8-5 ADC24 Offset Drift Gain=1
Vin=320mV SPS=10Hz
Delta VR=1V and VDDA=2.7V

5.9 Internal Temperature Sensor

Typical values are at T_A=25℃, VDD3V = 3.0V, and VDDA=2.4V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TC_S	Sensor temperature drift			173		uV/℃
KT	Absolute temperature scale 0°K			-288		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~85℃		±2		℃

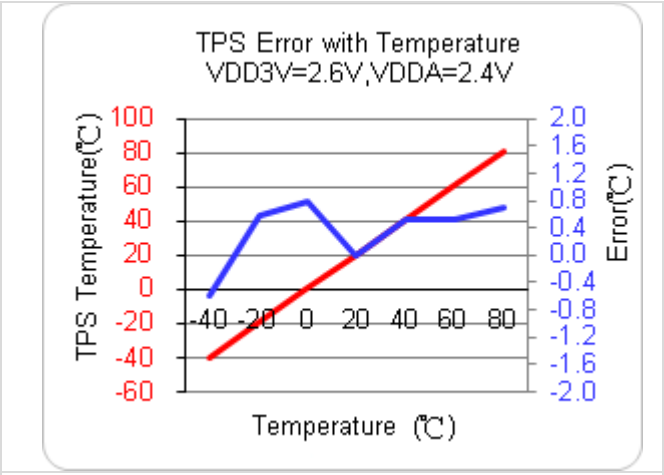


Figure5.9 TPS Performance

5.10 8-Bit Resistance Ladders

Typical values are at T_A=25℃ and VDD3V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Resolution		Monotonic		8		Bit
	Power Supply		2.4		VDD3V	V
V_{OUT}	Output range	DA output is between VR- and VR+	0		VDD3V	V
V_{REFP}	Positive reference voltage range	$V_{REFP} > V_{REFN}$	0		VDD3V	V
V_{REFN}	Negative reference voltage range		0		VDD3V	V
R_{ON}	8-Bit Resistance ladders. output switch	VDDA=2.4V 0.5V < DA_OP < VDD3V-0.5V			200	Ω
		VDDA=2.4V 0.5V > DA_OP, DA_OP > VDD3V-0.5V		10		Ω
R_{RSW}	Reference voltage switch	V_{REFP} = 2.2V, V_{REFN} = 0V, VDDA = 2.4V		15	30	Ω
R_{LADDER}	One LSB resistance ladder			600		Ω
INL	Integral linearity error	VR+ = 2.4V, VR- = 0V		±0.5	±1	LSB
DNL	Differential linearity error	VR+ = 2.4V, VR- = 0V		±0.5	±1	LSB
E_{OS}	Offset error	VR+ = 2.4V, VR- = 0V			1	LSB
8-Bit Resistance Ladders.	(Vin Floating)	VDD3V=3.3V,VDDA=2.4V		0.1		uA

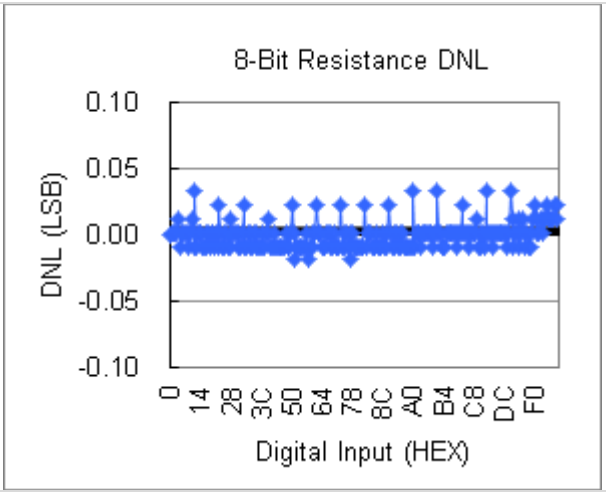


Figure5.10-1 8-Bit Resistance vs. DNL

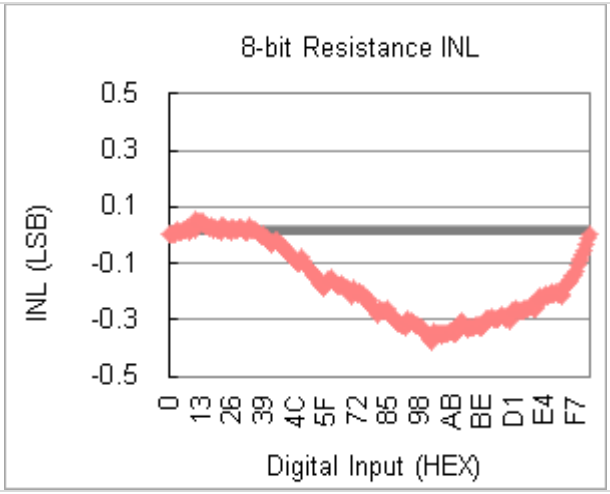


Figure5.10-2 8-Bit Resistance vs. INL

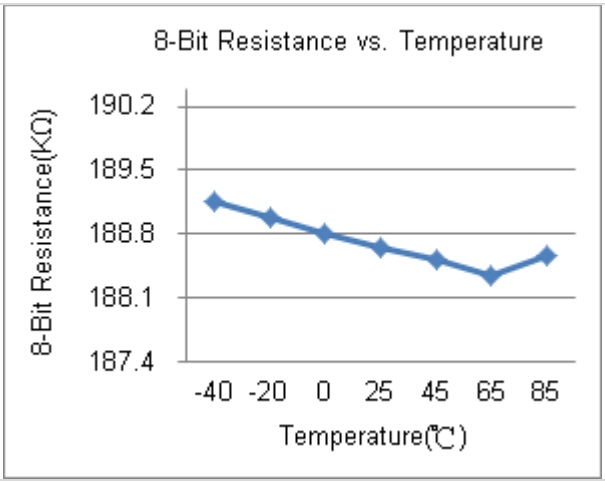


Figure5.10-3 8-bit Resistance vs. Temperature

5.11 OPAMP Management System

Typical values are at T_A=25℃, VDD3V = 3.0V, and C_{VLCD}=10uF. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDDA	Power supply		2.4		3.6	V
V_{OUT}	Output range		0		VDDA	V
V_{IN}	Input common range		0		VDDA	V
I_{OPA}	OPAMP current			120		uA
I_{OPA_LOAD}	Output current loading (push or pull)	VDDA = 3.0V, 0.3V< Output voltage <VDDA-0.3V			1	mA
		VDDA = 2.4V, 0.3V< Output voltage <VDDA-0.3V			0.5	mA
C_{LOAD}	Max output capacitor load				1	nF
SR	Slew rate	Loading R=10K, C=100pF, 0.3V → VDDA-0.3V		0.6		V/us
UGB	Unit gain bandwidth	Loading C=100pF		1000		KHz
V_{OS}	Offset error	Vin = 1.2V	-5		+5	mV
DFD	Digital filter delay	VDDA = 3.0V		2		us
C_{SA}	Sample capacitor			10		pF

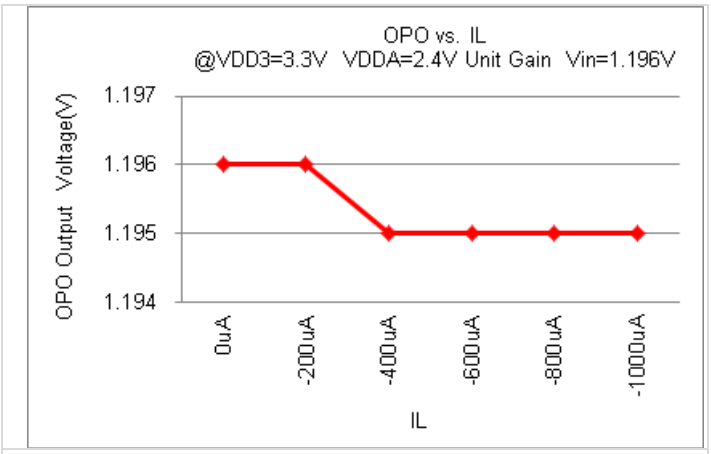


Figure5.11 OPO vs. IL

5.12 CMP Management System

Typical values are at T_A=25℃ and VDD3V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{MC}	Operation supply current	ENCMP[0]=1, CMPHS[0]=1b		10		uA
	Low Power Mode	ENCMP[0]=1, CMPHS[0]=0b		1		
V_{IC}	Common-mode input voltage		0		VDD3V-1	V
V_{OS}	Offset voltage		-5		5	mV
V_{hys}	Input hysteresis		0	0.7	1.5	mV
V_{REF}	Reference voltage	CPPS[1:0]=11b		1.2		V
	Temperature drift	CPPS[1:0]=11b		80		ppm/℃
I_R	Multi-node resistor current	CPRL[0]=0b		10		uA
		CPRL[0]=1b		30		

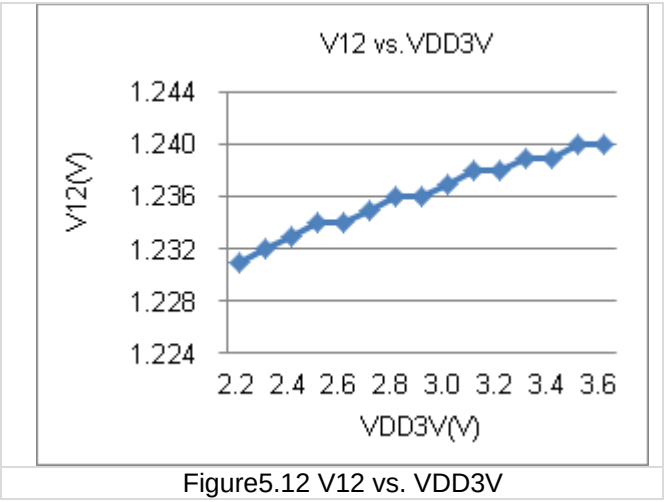


Figure5.12 V12 vs. VDD3V

5.13 LCD System

Typical values are at T_A=25℃, VDD3V = 3.3V, and C_{VLCD}=10uF. Unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{LCD}	Operation Current Charge Pump Mode	VDD3V=3.3V VLCD=3.0V (VLCD< VDD3V)	W/O Panel		10		uA
VLCD	Supply Voltage Range	VLCD	With Buffer	2.50		3.80	V
VLCD	Embedded Charge Pump Output Voltage @ VLCD Pin	VDD3V = 2.4V CVLCD = 10uF	Mode1: Data[1]=00_011B	3.26	3.43	3.60	V
			Mode2: Data[1]=00_100B	3.00	3.16	3.32	
			Mode3: Data[1]=00_101B	2.78	2.93	3.08	
			Mode4: Data[1]=11_101B	2.59	2.73	2.87	
			Mode5: Data[1]=01_101B	2.42	2.55	2.68	
Z_{LCD}	Output Impedance With LCD Buffer	FLCD = 128Hz, VLCD = 3.0V			10		KΩ

Data1 Bit: 0X41F24 [EN_Rshift1, EN_Rshift0], 0X41B00 [VLCD2, VLCD1, VLCD0]

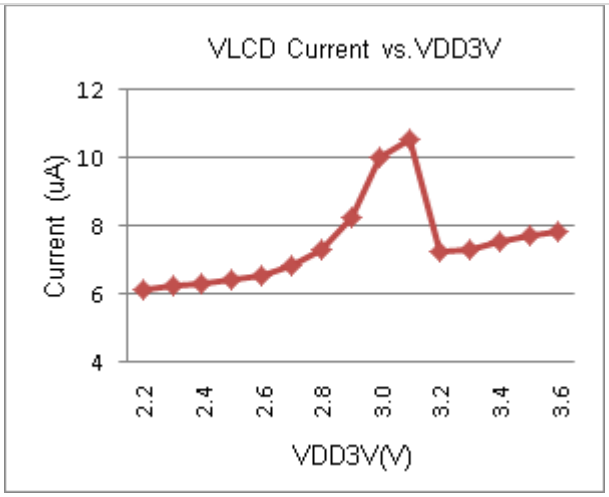


Figure5.13-1 VLCD Current vs. VDD3V @VLCD=3.16V (HY16F19x Only)

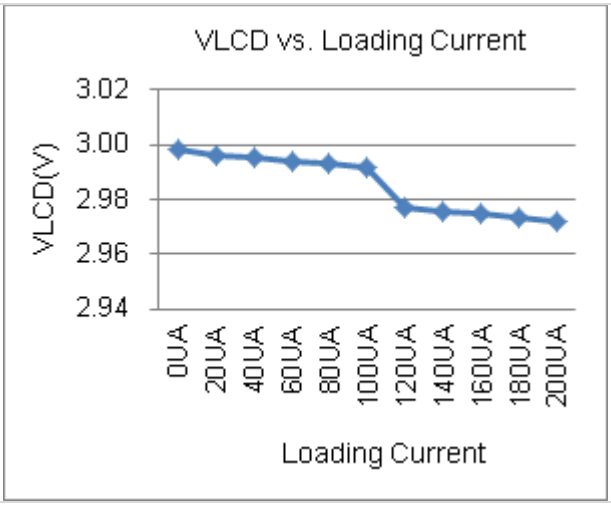


Figure5.13-2 VLCD With Load @VLCD=3.0V

6. 訂貨資訊

6.1 HY16F19x 系列選型編碼

下單品名[1]	封裝型式	引腳數	封裝型式描述方式		程式碼編號[2]	出貨包裝形式	個裝數量	材料組成	MSL[3]
HY16F198-D000	Die	-	D	000	-	-	100	Green[4]	-
HY16F198-N088	QFN	88	N	088	-	Tray	168	Green[4]	MSL-3
HY16F198-L100	LQFP	100	L	100	-	Tray	90	Green[4]	MSL-3
HY16F198-L064	LQFP	64	L	064	-	Tray	250	Green[4]	MSL-3
HY16F197-L064	LQFP	64	L	064	-	Tray	250	Green[4]	MSL-3
HY16F197-N068	QFN	68	N	068	-	Tray	348	Green[4]	MSL-3
HY16F196-L064	LQFP	64	L	064	-	Tray	250	Green[4]	MSL-3
HY16F196-N068	QFN	68	N	068	-	Tray	348	Green[4]	MSL-3

[1] 下單品名: 描述的內容為：晶片型號 – 晶片封裝形式

HY16F198-L100

IC型號　IC封裝類型

EX：你需求的是 LQFP 100 引腳封裝. 下單品名就是 HY16F198-L100.
當需要以 Tray 出貨，在下訂單時除下單品名外，請清楚指明出貨包裝形式為 Tray.

[3] MSL:
濕敏度等級符合 IPC/JEDEC J-STD-020 的行業分類工業標準.
產品的加工、包裝、運輸及使用都參考 IPC/JEDEC J-STD-033 行業標準.

[4] Green (RoHS & no Cl/Br):
HYCON 產品皆為 Green Product，符合 RoHS 指令以及無鹵素規定(Br<900ppm or Cl<900ppm or (Br+Cl)<1500ppm)

6.2 HY16F19xB 系列選型編碼

下單品名[1]	封裝型式	引腳數	封裝型式描述方式		程式碼編號[2]	出貨包裝形式	個裝數量	材料組成	MSL[3]
HY16F198B-D000	Die	-	D	000	-	-	100	Green[4]	-
HY16F198B-N088	QFN	88	N	088	-	Tray	168	Green[4]	MSL-3
HY16F198B-L100	LQFP	100	L	100	-	Tray	90	Green[4]	MSL-3
HY16F198B-L064	LQFP	64	L	064	-	Tray	250	Green[4]	MSL-3
HY16F197B-L064	LQFP	64	L	064	-	Tray	250	Green[4]	MSL-3
HY16F197B-N068	QFN	68	N	068	-	Tray	348	Green[4]	MSL-3

HY16F196B-L064	LQFP	64	L	064	-	Tray	250	Green[4]	MSL-3
HY16F196B-N068	QFN	68	N	068	-	Tray	348	Green[4]	MSL-3

[1] 下單品名: 描述的內容為：晶片型號 – 晶片封裝形式

HY16F198B-L100

IC型號　IC封裝類型

EX：你需求的是 LQFP 100 引腳封裝. 下單品名就是 HY16F198B-L100.
當需要以 Tray 出貨，在下訂單時除下單品名外，請清楚指明出貨包裝形式為 Tray.

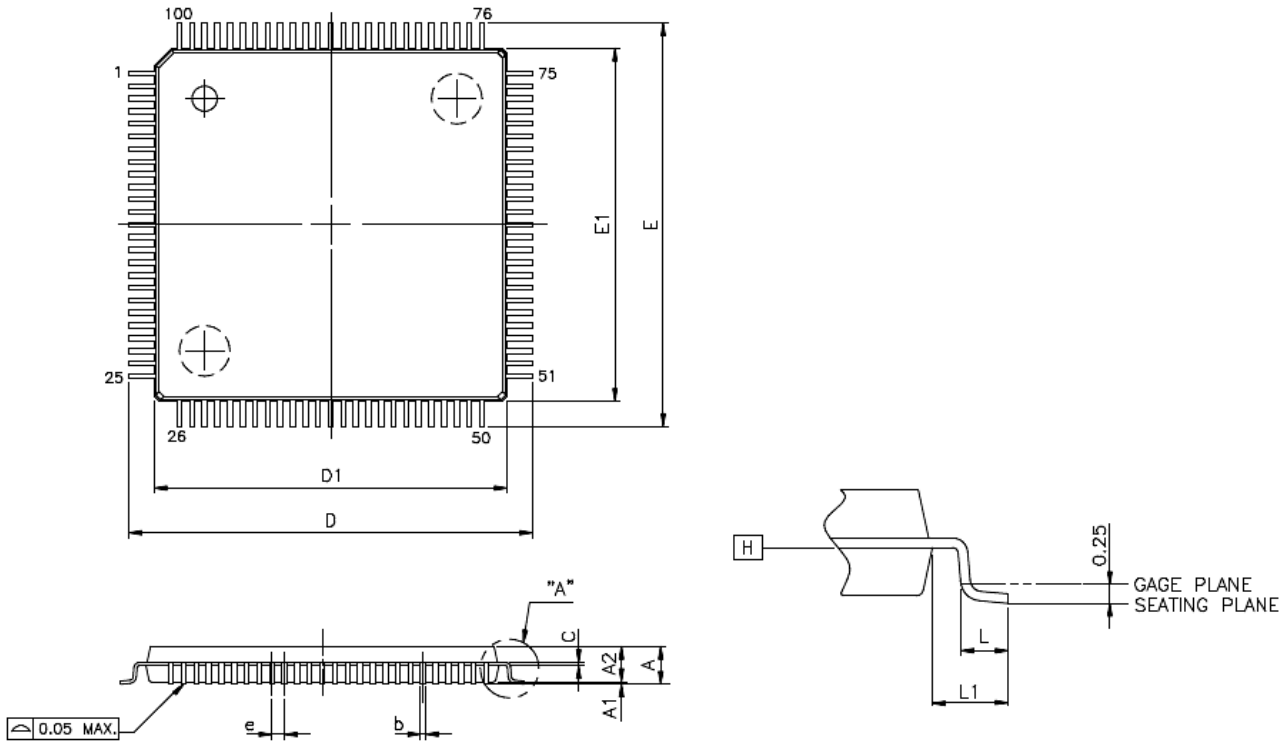
[3] MSL:
濕敏度等級符合 IPC/JEDEC J-STD-020 的行業分類工業標準.
產品的加工、包裝、運輸及使用都參考 IPC/JEDEC J-STD-033 行業標準.

[4] Green (RoHS & no Cl/Br):
HYCON 產品皆為 Green Product，符合 RoHS 指令以及無鹵素規定(Br<900ppm or Cl<900ppm or (Br+Cl)<1500ppm)

7. 封裝尺寸資訊

7.1 LQFP100 封裝圖

單位: mm



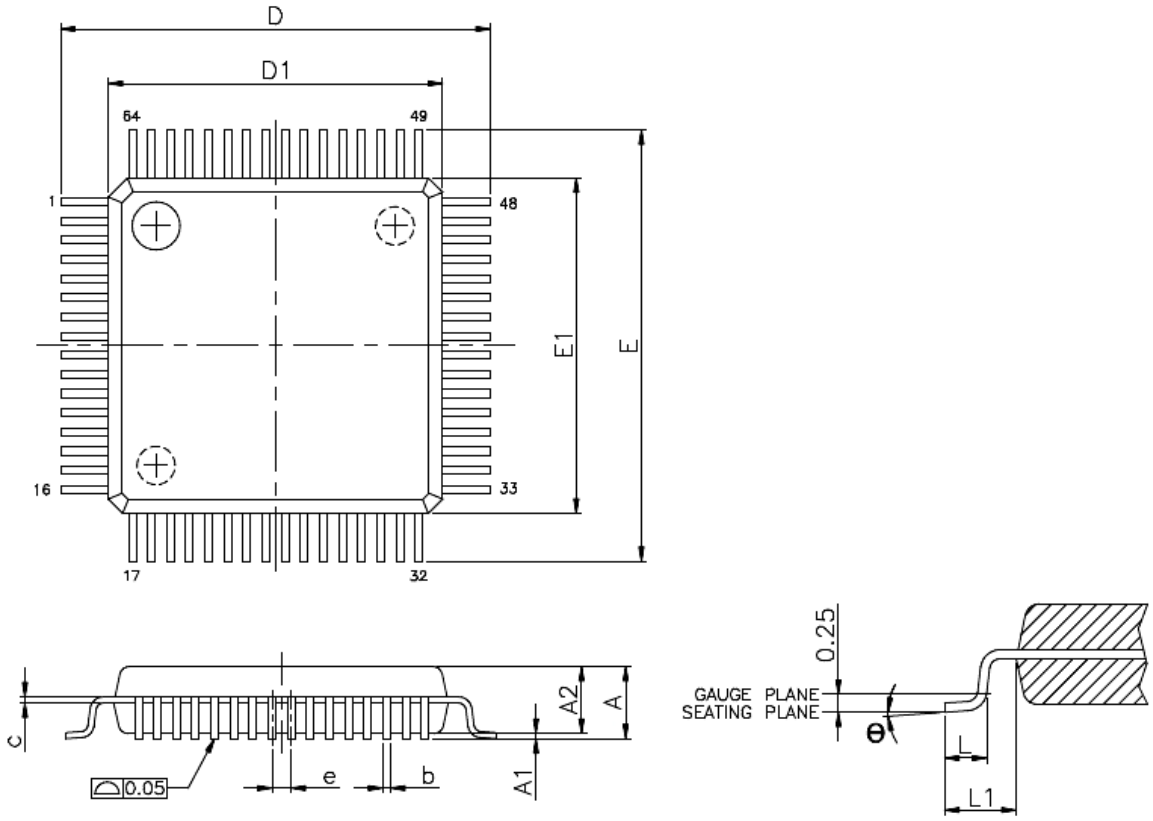
VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	0.127	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		

Note: JEDEC MS-026 compliant

7.2 LQFP64 封裝圖

單位: mm



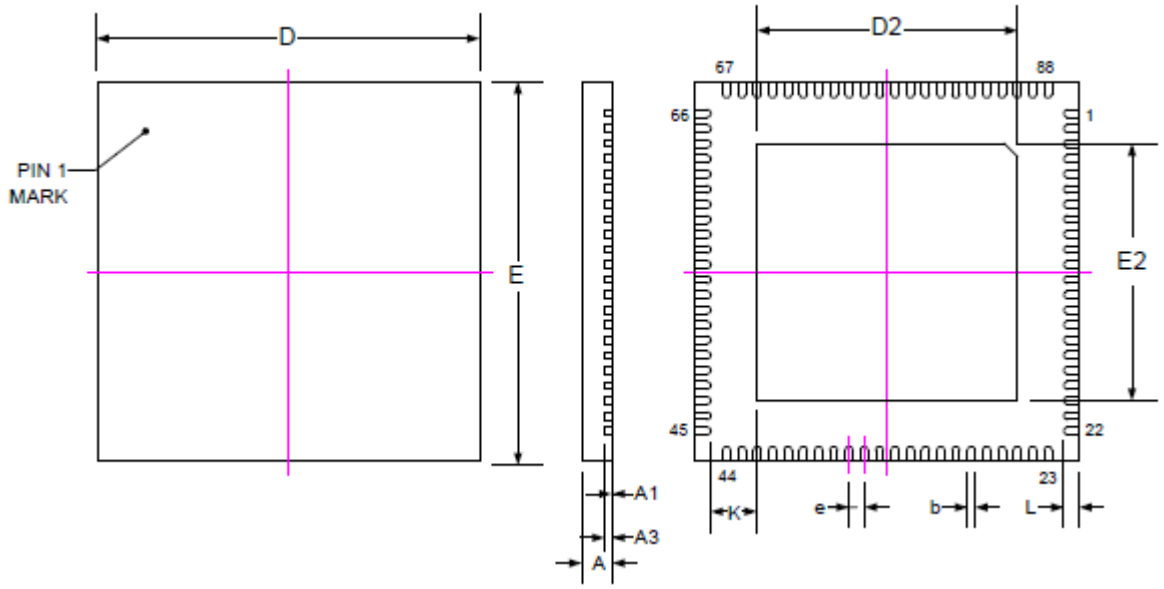
VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Note: JEDEC MS-026 compliant

7.3 QFN88 封裝圖

單位: mm



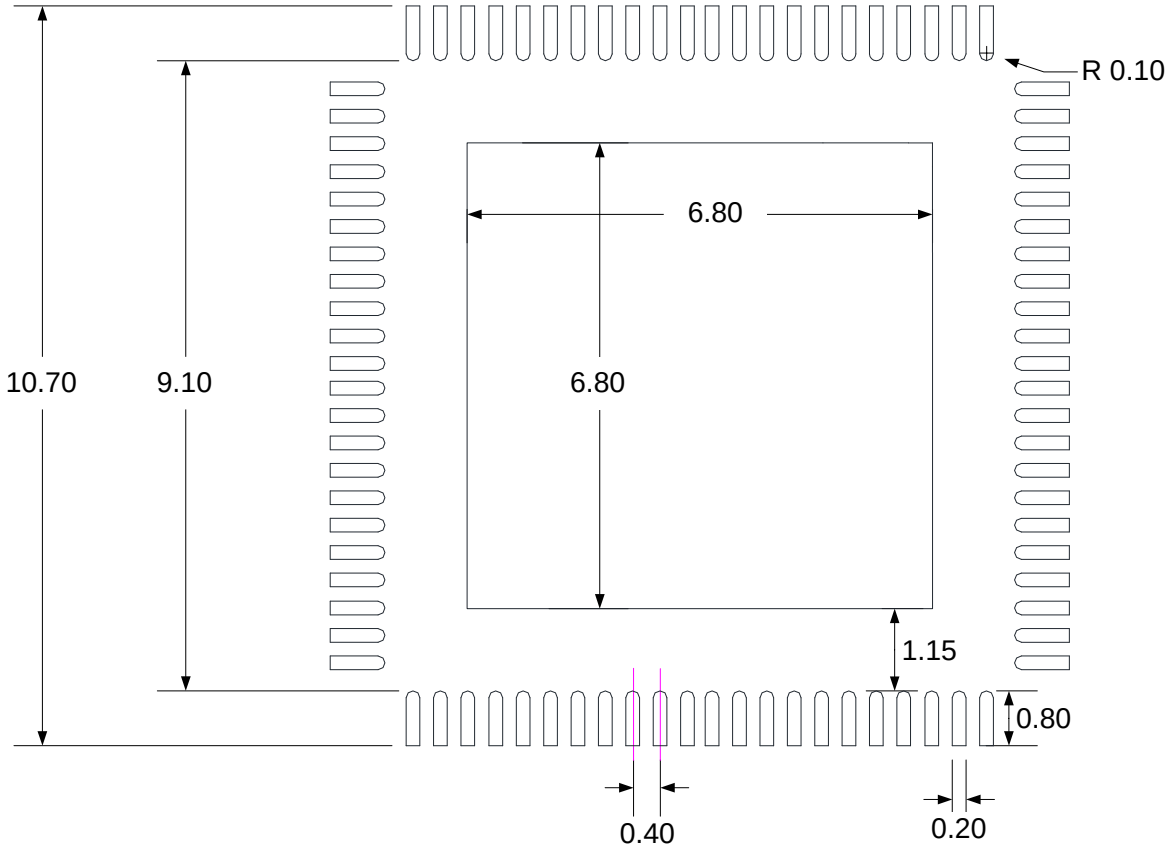
SYMBOLS	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.15	0.20	0.25
D		10.00 BSC	
E		10.00 BSC	
e		0.40 BSC	
D2	6.75	6.80	6.85
E2	6.75	6.80	6.85
L	0.30	0.40	0.50
K	1.08	1.20	1.33

Note: All dimensions refer to JEDEC OUTLINE MO-220.

Package Outline Drawing--- QFN 10x10 88

Land Pattern Design Recommendations

Unit : mm

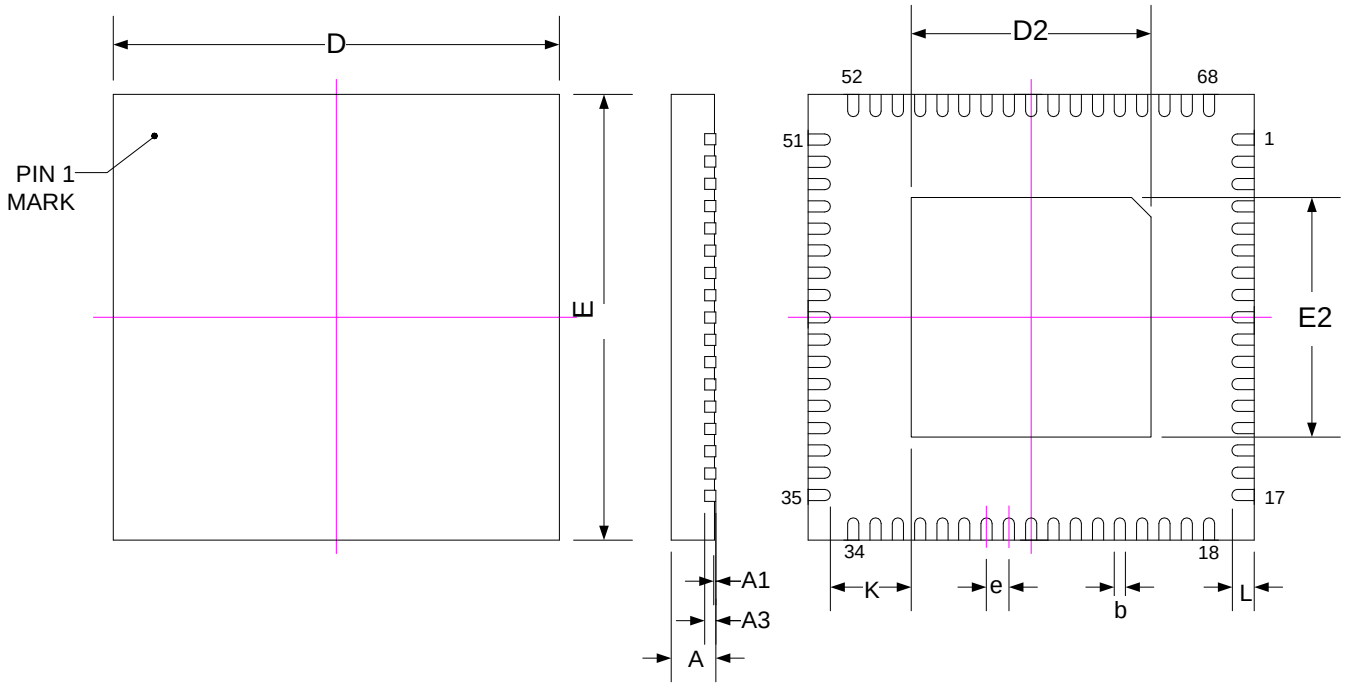


Note:

1. Publication IPC-7351 is recommended for alternate designs
2. Unit : mm
3. http://www.hycontek.com/attachments/MSP/OJTI-HM-2013-002.pdf

7.4 QFN68 封裝圖

單位: mm

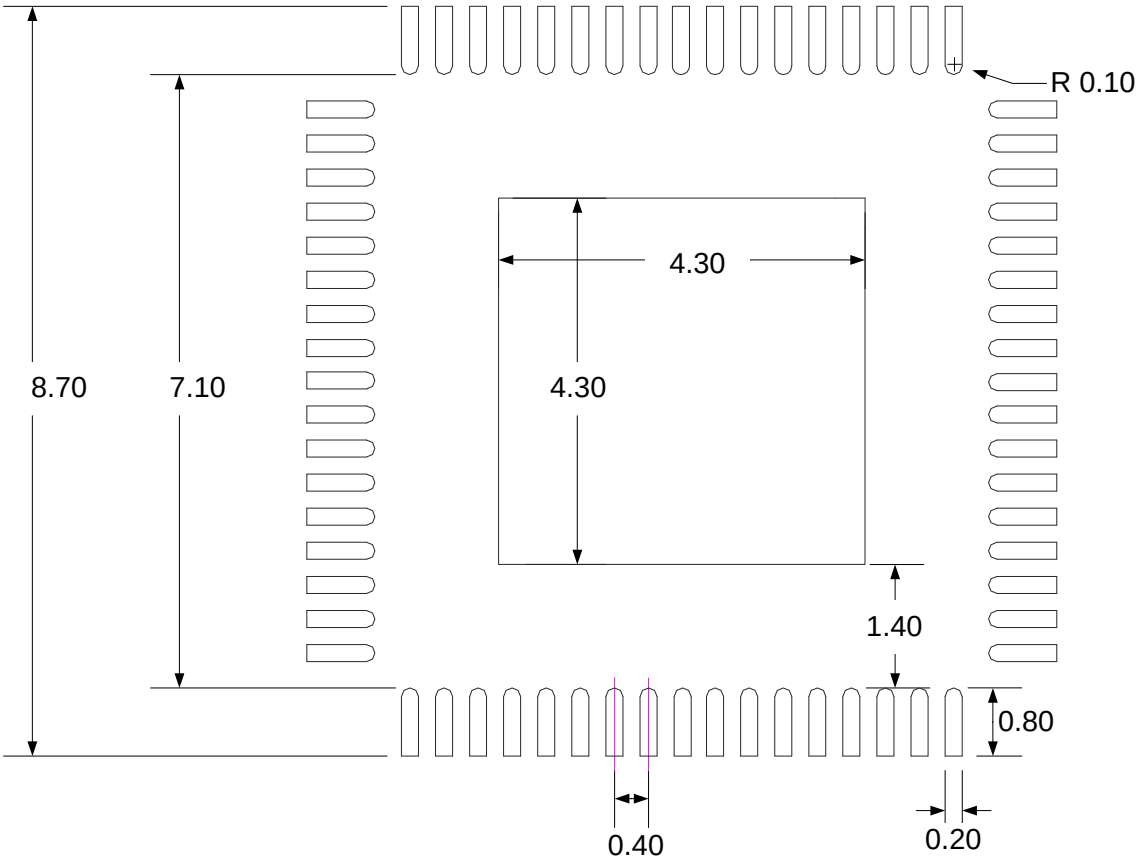


SYMBOLS	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.15	0.20	0.25
D		8.00 BSC	
E		8.00 BSC	
e		0.40 BSC	
D2	4.20	4.30	4.40
E2	4.20	4.30	4.40
L	0.35	0.40	0.45
K	1.35	1.45	1.55

Note: All dimensions refer to JEDEC OUTLINE MO-220.
Package Outline Drawing--- QFN 8x8 68

Land Pattern Design Recommendations

Unit : mm



Note:

1. Publication IPC-7351 is recommended for alternate designs
2. Unit : mm
3. http://www.hycontek.com/attachments/MSP/OJTI-HM-2013-002.pdf

8. HY16F19xB 性能升級說明

HY16F19xB 與 HY16F19x 為相同封裝腳位, HY16F19xB 為 HY16F19x 產品性能升級版本，除相容於既有功能之外，針對特定應用需求進行升級調整，以下為主要功能上的升級與說明.

1. SPI Function:

- 原 HY16F19x 產品不支援 SPI Slave mode,當晶片進入睡眠模式時(Sleep mode),達到喚醒晶片功能.
- HY16F19xB 開放支援在睡眠模式時(Sleep mode),可以透過 SPI CS 同步引腳,達到喚醒晶片功能.

2. VLCD 功耗降低:

- 原 HY16F19x 產品需要限制 VDD3V>VLCD 電源電壓下使用.
- HY16F19xB 改善晶片 VLCD 使用限制,不受 VDD3V 變化而增加系統電流.

3. Flash Erase 功能提升:

- 原 HY16F19x 產品透過燒錄器進行 Flash Erase 清除晶片程序時,需要輸入正確密碼才可以清空晶片.
- HY16F19xB 硬體已經支援 Flash Erase 動作時,不需要密碼也可以執行清空晶片.此調整可以解決客戶端,在量產時啓動晶片密碼保護功能後,之後卻忘記密碼時,仍可以支援對 Flash 進行 Erase 功能.

4. ISP Bootloader 功能支援:

- 原 HY16F19x 產品 Boot ROM Code 中並無支援 ISP Bootloader 功能.
- HY16F19xB 可以透過 Boot ROM Code，透過 UART 通訊界面，進行主程式段 Flash 資料更新.

5. Flash 自我燒錄函數功能增加:

- 原 HY16F19x 自我燒錄函數僅支援以下函數:
  - ROM_BurnWord,包含 Erase+ Word write 燒錄行為，約花費 30msec 燒錄時間.
  - ROM_BurnPage,包含 Erase+ Page write 燒錄行為，約花費 30msec 燒錄時間.
  - PageErase,包含 Page Erase 行為，約花費 25msec 燒錄時間.
  - SectorErase,包含 Sector Erase 行為，約花費 25msec 燒錄時間.
- HY16F19xB 則增加自我燒錄函數(不啓動 Erase),以縮短生產燒錄時間:
  - ROM_BurnWordonly,僅為 Word 燒錄行為，約花費 3msec 燒錄時間.
  - ROM_BurnPageWriteonly,僅為 Page 燒錄行為，約花費 3msec 燒錄時間.

6. HY16F19x 與 HY16F19xB 的燒錄檔無法相容

- 在 IDE 開發環境上,需要注意選擇型號為 HY16F19x 系列或是 HY16F19xB 系列,兩個版本的燒錄檔無法相容.
  - 原使用 HY16F19x 型號所開發專案,當要轉移到 HY16F19xB 型號時,需要透過 IDE 開發環境重新組譯程序後才可以燒錄到 HY16F19xB 產品上.轉換操作方式:需要重新建立 HY16F19xB 專案後,再將原本 HY16F19x 所開發 C Code 複製到新的專案上,重新調整程序後進行組譯程序即可.

9. 修改記錄

以下描述本文件差異較大的地方，而標點符號與字形的改變不在此描述範圍。

版本	頁數	變更摘要	修訂日期
V01	ALL	初版發行	2014/06/06
V02	P55/P52/P06	新增 QFN88 腳位圖資訊	2014/10/06
	P51	修改 LCD 電器規格說明	
V03	ALL	8-bit DAC 統一改為 8-bit 數位電阻器	2015/01/12
	CH5	新增電器特性曲線圖	
	CH7.4	新增 QFN68 腳位圖資訊	
V04	CH4.1	IC 內部框圖 8-bit DAC 改為 8-bit Resistance Ladder(數位電阻器)	2015/06/09
	CH4.6	ADC 網路輸入 OPO 更正為 OPOI, REFO 更正為 REFO_I	
	CH4.7	OPAMP 網路輸入 REFO 更正為 REFO_I	
	CH4.8	8-bit Resistance Ladder 網路輸入 REFO 更正為 REFO_I	
	CH5.3	REFO Buffer 的 Capacitor loading 單位原本為 pF 更正為 nF, 並且新增 Min 數值 22nF	
V05	CH1&2&CH6.2	新增 HY16F19xB 相關資訊	2015/8/6
	CH7.3&CH7.4	新增 QFN68 與 QFN88 Land Pattern design recommendations	
	CH8	新增章節 CH8, HY16F19xB 性能升級說明	
V06	P51	修改 HAO 2M/4M/8M/16M 中心頻率值	2016/3/4
	P67, P68	修正訂貨資訊 Green (RoHS & no Cl/Br)描述	
	CH2.5	新增章節封裝片正印說明訊息	