



HY13P56B

Datasheet

8-Bit RISC-like Mixed Signal Microcontroller

Embedded 24-Bit $\Sigma\Delta$ ADC

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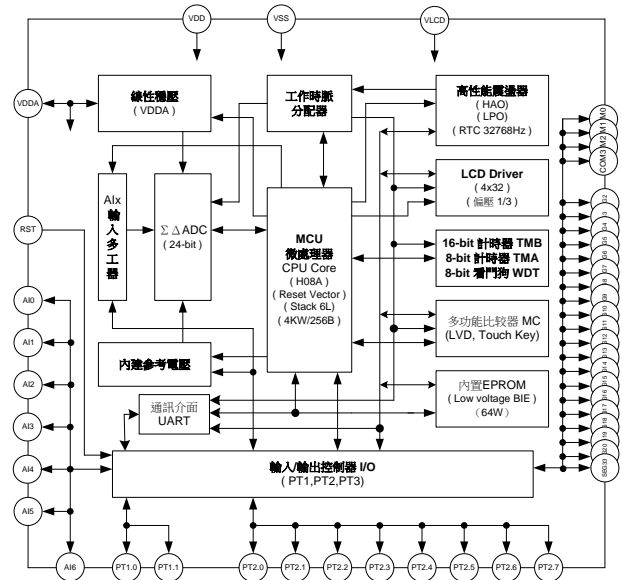
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1. 特點

- 8-Bit RISC-like 微控制器，具有 66 條高性能指令集 H08A
- 串列通訊 EUART 模組
- 24-Bit $\Sigma\Delta$ ADC 類比數位轉換器
 - 梳狀濾波器採三階設計，轉換頻率高達 31.25Ksps
 - 取樣頻率 125K/250K/500K/1MHz
 - 超取樣頻率設置 32~65535
 - 全差動輸入信號與測量範圍的零點調整
 - 信號放大 $x1, x2 \sim x128$
 - 測量信號輸入通道 7ch
 - 低溫飄係數與內置絕對溫度傳感器
- 內部電源系統
 - 內置 LDO 線性穩壓電源 VDDA
 - ◆ 內部類比電路或外部傳感器電壓源
 - ◆ 輸出可設置 2.4V/2.7V/3.0V/3.3V，可外灌輸入電壓
 - ◆ 低操作工耗與低溫飄係數
 - 內置參考電壓源 REFO
 - ◆ 類比電路參考電壓源
 - ◆ 輸出 1.2V，可外灌輸入電壓
 - ◆ 低操作工耗與低溫飄係數
- 多功能比較器
 - 輸出濾波與反相及低工耗設計
 - 中斷事件
 - 電壓檢測/電容測量等應用
- 計時器
 - Watch Dog
 - ◆ 復位事件與中斷事件
 - 8-bit Timer
 - ◆ 中斷事件
 - 16-bit Timer
 - ◆ 16-Bit PWM/PFD 輸出
 - ◆ 8+8 PWM 輸出
 - ◆ 兩個 8-Bit PWM 輸出
 - ◆ 中斷事件

- LCD 驅動顯示器
 - 支援 4x32 點，偏壓模式 1/3
 - 低功耗設計，操作電流 11uA



- 工作電壓與操作溫度範圍
 - 2.0V ~ 3.6V，-40°C ~ 85°C
- 工作頻率
 - 僅支援一組外接低速石英震盪器 32768Hz
 - 內建高精度 HAO 震盪器 2MHz/4MHz/7.6MHz
 - 內建低功耗 LPO 震盪器 11.5KHz
- 記憶體型式
 - 4KW OTP 程式記憶體
 - 256B 資料記憶體，6 層堆棧
 - Build-In EPROM
 - ◆ 工作電壓 2.75V
 - ◆ 64W EPROM 記憶體
- 引腳特色
 - 具 10mA 驅動能力
 - 自定義功能模組輸出引腳設計
- 復位機制
 - Power On Reset/Brown Out Reset
 - Watch Dog Reset/Reset PIN

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2. 引腳定義

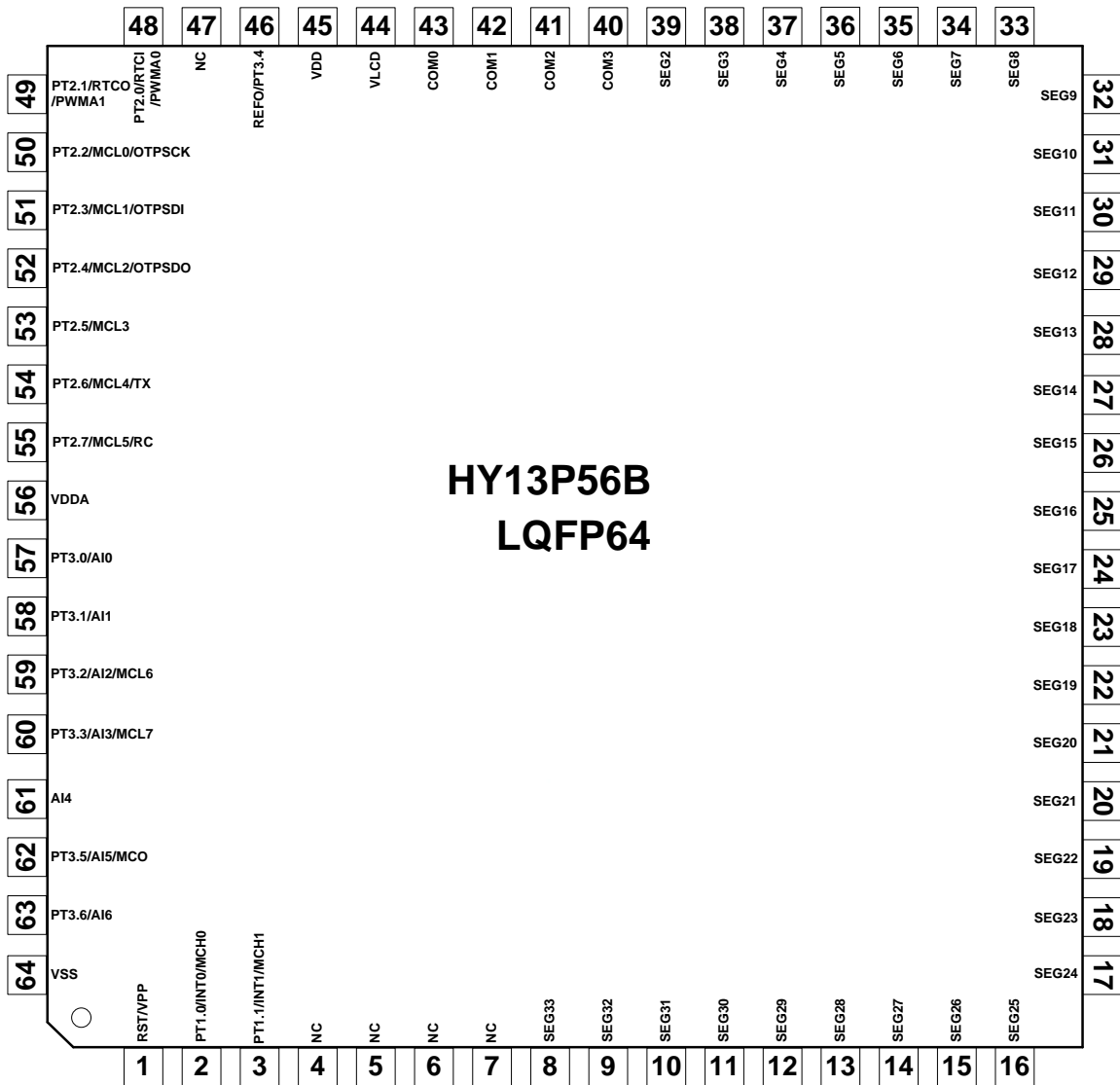


圖 2-1 HY13P56B LQFP64 引腳圖

2.1. LQFP64 引腳定義說明

“I”：輸入，“O”：輸出，“A”：類比，“S”：史密斯觸發，“C”：CMOS I/O，“*”：自定義，“/”：或，“X”：可忽略

引腳		設計		描述
編號	名稱/功能	型式	緩衝	
1	RST	I	S	復位引腳
	VPP	P	P	OTP 燒錄電壓引腳
2	PT1.0	I/O	S/C	數位輸入 / 輸出引腳
	INT0	I	S	外部中斷源
	MCH0	A	A	多功能比較器信號輸入引腳
3	PT1.1	I/O	S/C	數位輸入 / 輸出引腳
	INT1	I	S	外部中斷源
	MCH1	A	A	多功能比較器信號輸入引腳
8	SEG33	O	A	LCD 的 SEG.引腳
9	SEG32	O	A	LCD 的 SEG.引腳
10	SEG31	O	A	LCD 的 SEG.引腳
11	SEG30	O	A	LCD 的 SEG.引腳
12	SEG29	O	A	LCD 的 SEG.引腳
13	SEG28	O	A	LCD 的 SEG.引腳
14	SEG27	O	A	LCD 的 SEG.引腳
15	SEG26	O	A	LCD 的 SEG.引腳
16	SEG25	O	A	LCD 的 SEG.引腳
17	SEG24	O	A	LCD 的 SEG.引腳
18	SEG23	O	A	LCD 的 SEG.引腳
19	SEG22	O	A	LCD 的 SEG.引腳
20	SEG21	O	A	LCD 的 SEG.引腳
21	SEG20	O	A	LCD 的 SEG.引腳
22	SEG19	O	A	LCD 的 SEG.引腳
23	SEG18	O	A	LCD 的 SEG.引腳
24	SEG17	O	A	LCD 的 SEG.引腳
25	SEG16	O	A	LCD 的 SEG.引腳
26	SEG15	O	A	LCD 的 SEG.引腳
27	SEG14	O	A	LCD 的 SEG.引腳
28	SEG13	O	A	LCD 的 SEG.引腳
29	SEG12	O	A	LCD 的 SEG.引腳
30	SEG11	O	A	LCD 的 SEG.引腳
31	SEG10	O	A	LCD 的 SEG.引腳
32	SEG9	O	A	LCD 的 SEG.引腳

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33	SEG8	O	A	LCD 的 SEG.引腳	
34	SEG7	O	A	LCD 的 SEG.引腳	
35	SEG6	O	A	LCD 的 SEG.引腳	
36	SEG5	O	A	LCD 的 SEG.引腳	
37	SEG4	O	A	LCD 的 SEG.引腳	
38	SEG3	O	A	LCD 的 SEG.引腳	
39	SEG2	O	A	LCD 的 SEG.引腳	
40	COM3	O	A	LCD 的 COM 引腳	
41	COM2	O	A	LCD 的 COM 引腳	
42	COM1	O	A	LCD 的 COM 引腳	
43	COM0	O	A	LCD 的 COM 引腳	
44	VLCD	P	P	LCD 的電壓源接引腳	
45	VDD	P	P	晶片工作電壓源接引腳	
46	PT3.4	I/O	S/C	數位輸入 / 輸出引腳	
		REFO	P	P	參考電壓引腳
48	PT2.0	I/O	S/C	數位輸入 / 輸出引腳	
		PWMA0	O	C	TMB1 的 PWM0 輸出引腳
		RTCI	A	A	外接 RTC 震盪器引腳
49	PT2.1	I/O	S/C	數位輸入 / 輸出引腳	
		PWMA1	O	C	TMB1 的 PWM1 輸出引腳
		RTCO	A	A	外接 RTC 震盪器引腳
50	PT2.2	I/O	S/C	數位輸入 / 輸出引腳	
		MCL0	A	A	多功能比較器信號輸入引腳
51	PT2.3	I/O	S/C	數位輸入 / 輸出引腳	
		MCL1	A	A	多功能比較器信號輸入引腳
52	PT2.4	I/O	S/C	數位輸入 / 輸出引腳	
		MCL2	A	A	多功能比較器信號輸入引腳
53	PT2.5	I/O	S/C	數位輸入 / 輸出引腳	
		MCL3	A	A	多功能比較器信號輸入引腳
54	PT2.6	I/O	S/C	數位輸入 / 輸出引腳	
		MCL4	A	A	多功能比較器信號輸入引腳
55	PT2.7	I/O	S/C	數位輸入 / 輸出引腳	
		MCL5	A	A	多功能比較器信號輸入引腳

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	RC	I	S	EUART 通訊介面 RC 接口
56	VDDA	P	P	LDO 線性穩壓電源輸出引腳
57	PT3.0	I/O	S/C	數位輸入 / 輸出引腳
	A10	A	A	類比輸入通道
58	PT3.1	I/O	S/C	數位輸入 / 輸出引腳
	A11	A	A	類比輸入通道
59	PT3.2	I/O	S/C	數位輸入 / 輸出引腳
	A12	A	A	類比輸入通道
	MCL6	A	A	多功能比較器信號輸入引腳
60	PT3.3	I/O	S/C	數位輸入 / 輸出引腳
	A13	A	A	類比輸入通道
	MCL7	A	A	多功能比較器信號輸入引腳
61	A14	A	A	類比輸入通道
62	PT3.5	I/O	S/C	數位輸入 / 輸出引腳
	A15	A	A	類比輸入通道
	MCO*	I/O	S/C	多功能比較器信號輸出引腳
63	PT3.6	I/O	S/C	數位輸入 / 輸出引腳
	A16	A	A	類比輸入通道
64	VSS	P	P	晶片工作電壓源接地端引腳
Others	NC	--	-	未使用

表 2-1 HY13P56B LQFP64 引腳說明

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2.2. 管腳複用功能

Function control bit PIN	Multi-function Comparator				EUART		Timer B	
	No change		MCOO[0]		EUARTO[0]		PWMAO[0]	
			<0>	<1>	<0>	<1>	<0>	<1>
PT1.0		MCH0						
PT1.1		MCH1						
PT2.0							PWMA0	
PT2.1							PWMA1	
PT2.2	MCL0							
PT2.3	MCL1							
PT2.4	MCL2							
PT2.5	MCL3							
PT2.6	MCL4					TX		
PT2.7	MCL5					RC		
PT3.0								
PT3.1								
PT3.2	MCL6							
PT3.3	MCL7							
PT3.4								
PT3.5				MCO*				
PT3.6								

*** : Not default value;
Control bit default value: <0>

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3. 應用電路

3.1. 帶觸碰按鍵之橋式傳感器

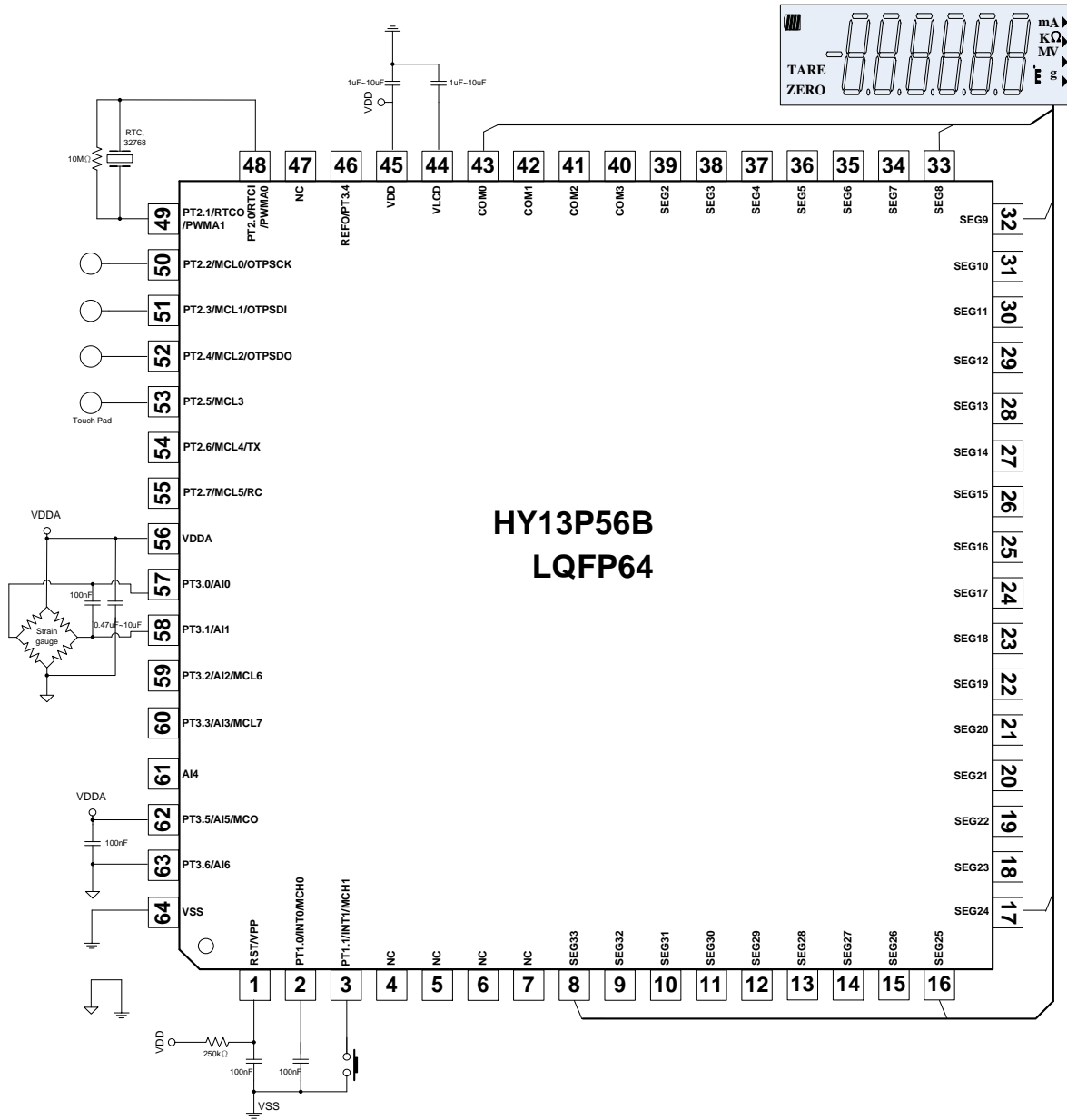


圖 3-1 帶觸碰按鍵橋式傳感器應用電路

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4. 功能概述

4.1. 内部方块图

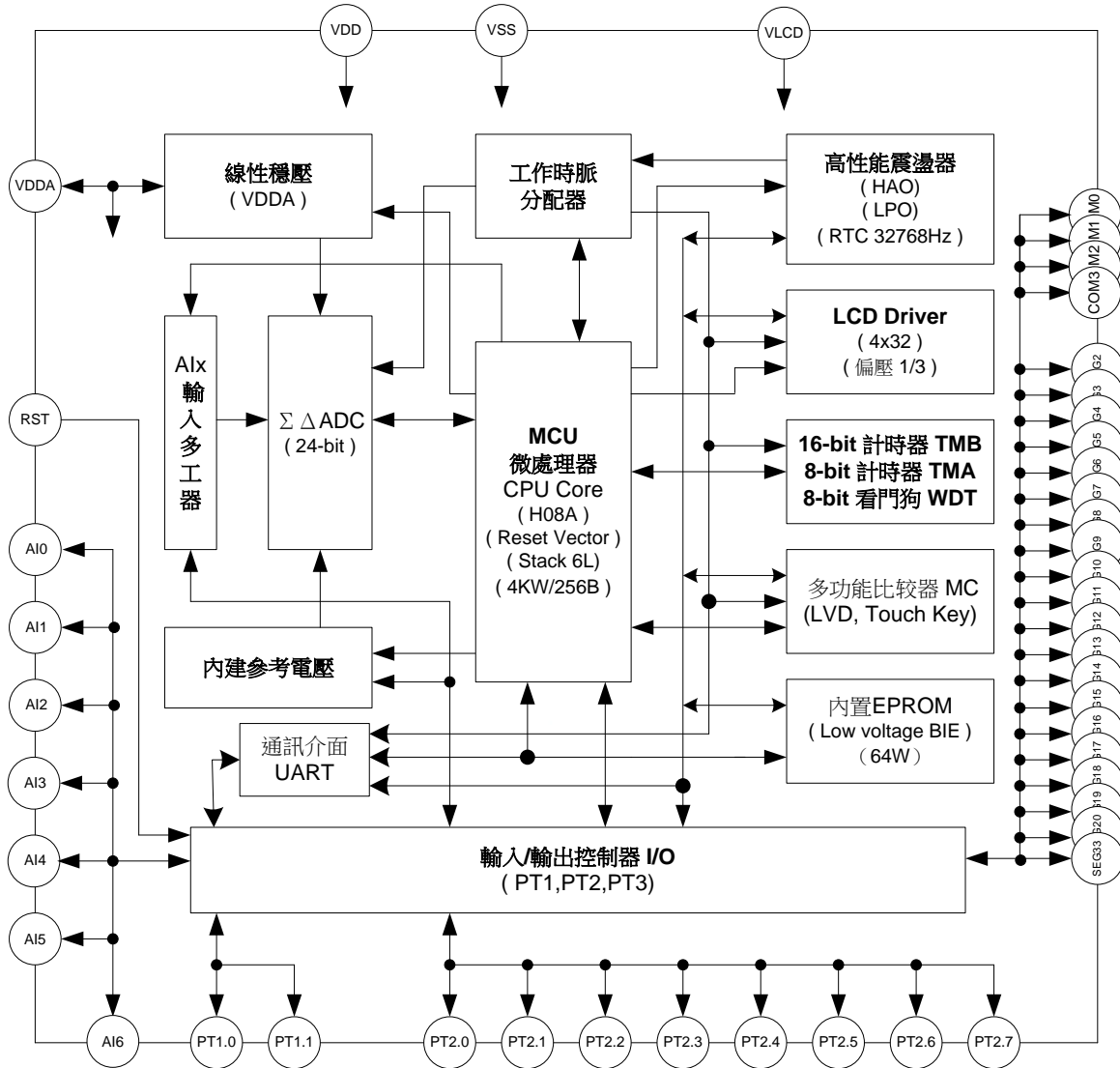


圖 4-1 HY13P56B 内部方块图

4.2. 相關說明與支援文件

晶片功能相關使用說明書

DS-HY13P56B

HY13P56B 說明書

UG-HY13S00

HY13Pxx 系列使用說明書

APD-CORE002

H08A 指令說明書

開發工具相關使用說明書

APD-HY13PIDE001

HY13Pxx 系列開發工具 ICE 硬體使用說明書

APD-HY13PIDE002

HY13Pxx 系列開發工具 IDE 軟體使用說明書

APD-OTP002

HY13Pxx 系列 OTP 產品燒錄引腳說明書

產品生產相關使用說明書

APD-HY13PIDE003

HY13Pxx 系列生產工具 HexLoader 軟體使用說明書

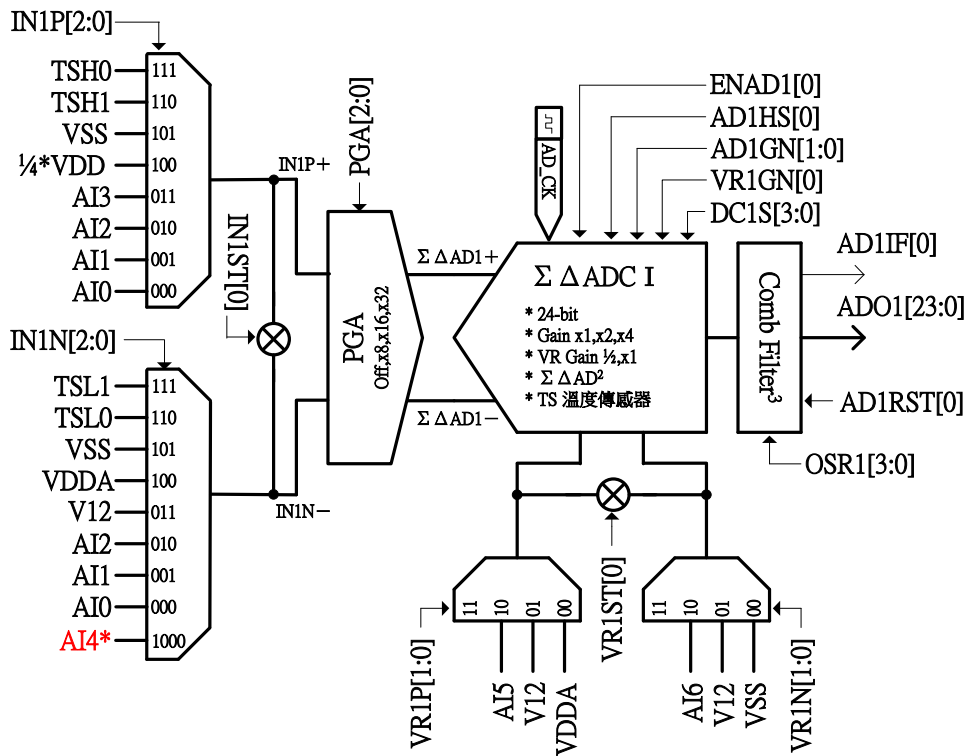
APD-HY13PIDE004

HY13Pxx 系列生產工具燒錄器硬體使用說明書

BDI-HY13P56B

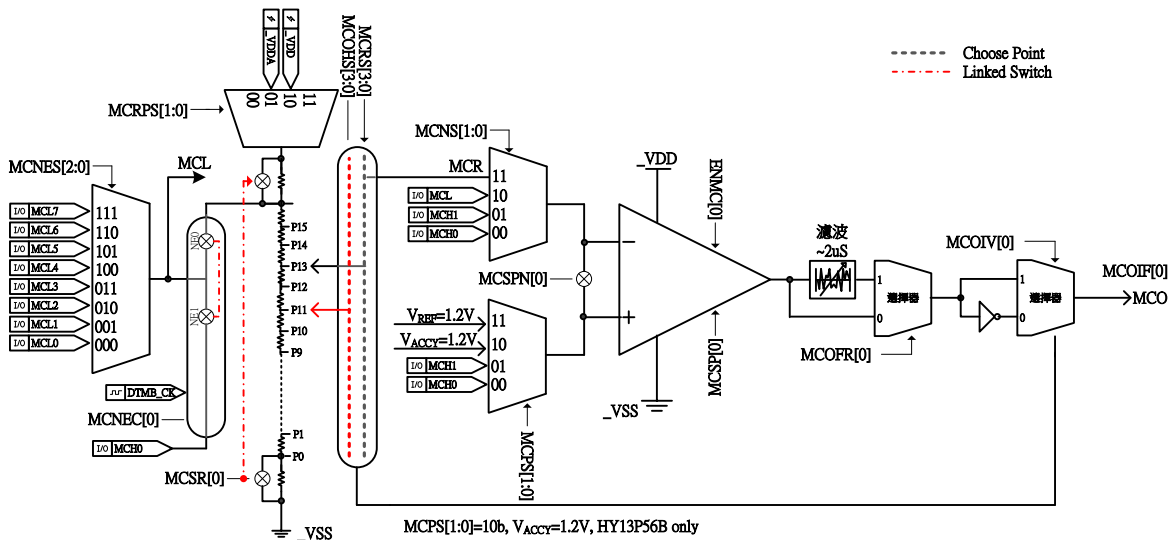
HY13P56B 個別產品的裸片打線資訊

4.3. $\Sigma\Delta$ ADC Network



*Note: [REFOO,IN1N[2:0]]=1000b=AI4 channel

4.4. Comparator Network



MCPSP[1:0]=10b, V_{ACCY}=1.2V, HY13P56B only

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4.5. $\Sigma\Delta$ ADC Performance

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{V}$, $V_{DDA} = 2.4\text{V}$, unless otherwise noted

HY13P56B 針對 $\Sigma\Delta$ ADC 提供了重要的輸入雜訊規格。下表列出典型的雜訊規格表與 Gain, Output rate, 及單端最大輸入電壓等關係。測試條件設定在外部輸入訊號短路，參考電壓為 1.2V，取樣 1024 筆資料。

ENOB(RMS) with OSR/GAIN at A/D Clock=1Mhz, VDDA=2.4V, VREF=1.2V																	
Max. Vin(mV) =0.9*VREF (1)	OSR				32	64	128	256	512	1024	2048	4096	8192	16384	32768	65536	
	Output rate(Hz)				31250	15625	7813	3906	1953	977	488	244	122	61	31	15	
	Gain	PGA	x	ADGN													
±1080	1	=	1	x	1	8.6	10.8	13.0	14.7	16.7	17.6	18.1	18.8	19.2	19.7	20.1	20.8
±540	2	=	1	x	2	8.6	10.9	12.8	14.7	16.5	17.5	18.2	18.6	19.0	19.6	20.0	20.6
±270	3	=	1	x	3	8.7	11.0	13.0	14.7	16.5	17.4	18.0	18.5	18.9	19.5	19.8	20.4
±135	4	=	1	x	4	8.6	11.1	12.9	14.7	16.5	17.4	17.9	18.4	18.9	19.3	19.9	20.3
±33.75	32	=	8	x	4	8.6	11.0	12.7	14.2	15.1	15.7	16.3	16.6	17.1	17.6	18.1	18.7
±16.875	64	=	16	x	4	8.6	10.9	12.7	13.9	14.6	15.2	15.7	16.2	16.7	17.3	17.6	18.2
±11.25	96	=	24	x	4	8.6	11.0	12.6	13.8	14.5	15.1	15.5	15.9	16.5	16.9	17.5	18.0
±8.435	128	=	32	x	4	8.6	10.9	12.5	13.6	14.2	14.9	15.2	15.8	16.3	16.9	17.3	17.7

(1) Max. Vin (mV) is the max. input voltage of single end to ground (VSS).

RMS Noise(uV) with OSR/GAIN at A/D Clock=1Mhz, VDDA=2.4V, VREF=1.2V																	
Max. Vin(mV) =0.9*VREF	OSR				32	64	128	256	512	1024	2048	4096	8192	16384	32768	65536	
	Output rate(Hz)				31250	15625	7813	3906	1953	977	488	244	122	61	31	15	
	Gain	PGA	x	ADGN													
±1080	1	=	1	x	1	6208	1317	301	89.6	22.9	12.3	8.34	5.30	4.01	2.91	2.09	1.35
±540	2	=	1	x	2	3067	612	165	45.7	12.6	6.41	4.08	3.01	2.29	1.53	1.11	0.78
±270	3	=	1	x	3	1937	388	99.9	30.3	8.50	4.59	3.13	2.23	1.60	1.07	0.88	0.56
±135	4	=	1	x	4	1508	279	77.3	22.9	6.42	3.57	2.44	1.78	1.27	0.93	0.62	0.47
±33.75	32	=	8	x	4	195	37.4	11.2	3.87	2.18	1.44	0.95	0.76	0.52	0.38	0.27	0.18
±16.875	64	=	16	x	4	97	19.8	5.8	2.49	1.51	0.99	0.71	0.52	0.36	0.23	0.19	0.13
±11.25	96	=	24	x	4	62	12.4	4.2	1.80	1.09	0.74	0.53	0.41	0.26	0.20	0.14	0.10
±8.435	128	=	32	x	4	48	9.6	3.2	1.50	0.99	0.62	0.48	0.32	0.24	0.16	0.12	0.09

ENOB(RMS) with OSR/GAIN at A/D Clock=0.25Mhz, VDDA=2.4V, VREF=1.2V																	
Max. Vin(mV) =0.9*VREF (1)	OSR				32	64	128	256	512	1024	2048	4096	8192	16384	32768	65536	
	Output rate(Hz)				7813	3906	1953	977	488	244	122	61	31	15	8	4	
	Gain	PGA	x	ADGN													
±1080	1	=	1	x	1	8.7	11.0	12.9	14.5	16.4	17.5	18.1	18.7	19.1	19.6	19.8	20.0
±540	2	=	1	x	2	8.7	10.9	13.0	14.7	16.5	17.3	17.9	18.4	19.1	19.5	20.0	20.2
±270	3	=	1	x	3	8.7	11.0	13.0	14.8	16.5	17.3	17.8	18.4	18.9	19.2	19.5	19.4
±135	4	=	1	x	4	8.7	11.1	13.0	14.6	16.4	17.3	17.6	18.3	18.7	19.3	19.7	19.9
±33.75	32	=	8	x	4	8.7	10.8	12.9	14.1	15.2	15.6	16.1	16.6	17.2	17.5	18.1	18.6
±16.875	64	=	16	x	4	8.7	11.0	12.7	13.9	14.8	15.1	15.7	16.1	16.7	17.2	17.8	18.0
±11.25	96	=	24	x	4	8.7	11.0	12.5	13.7	14.4	15.1	15.5	15.9	16.4	17.0	17.5	18.0
±8.435	128	=	32	x	4	8.7	10.9	12.6	13.7	14.3	14.7	15.3	15.8	16.2	16.9	17.2	17.8

RMS Noise(uV) with OSR/GAIN at A/D Clock=0.25Mhz, VDDA=2.4V, VREF=1.2V																	
Max. Vin(mV) =0.9*VREF	OSR				32	64	128	256	512	1024	2048	4096	8192	16384	32768	65536	
	Output rate(Hz)				7813	3906	1953	977	488	244	122	61	31	15	8	4	
	Gain	PGA	x	ADGN													
±1080	1	=	1	x	1	5709	1186	320	102.9	28.8	12.6	8.40	5.80	4.29	2.94	2.67	2.33
±540	2	=	1	x	2	2887	650	151	46.3	13.2	7.54	4.79	3.42	2.21	1.58	1.17	0.97
±270	3	=	1	x	3	1953	401	100.2	29.1	8.85	4.95	3.41	2.39	1.66	1.36	1.12	1.15
±135	4	=	1	x	4	1495	274	75.7	24.5	7.14	3.85	2.94	1.87	1.39	0.96	0.73	0.62
±33.75	32	=	8	x	4	175	41.9	10.1	4.34	2.07	1.48	1.06	0.77	0.48	0.40	0.27	0.19
±16.875	64	=	16	x	4	92	18.1	5.5	2.46	1.30	1.07	0.69	0.52	0.34	0.25	0.17	0.14
±11.25	96	=	24	x	4	59	12.4	4.4	1.90	1.15	0.73	0.53	0.42	0.28	0.19	0.13	0.10
±8.435	128	=	32	x	4	46	9.9	3.1	1.46	0.96	0.70	0.46	0.33	0.24	0.15	0.12	0.08

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The RMS noise are referred to the input. The Effective Number of Bits (ENOB(RMS)) is defined as:

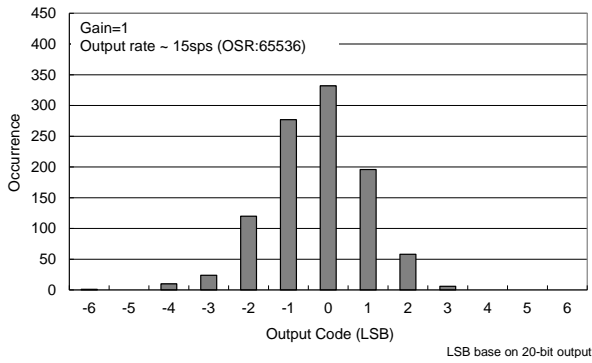
$$\text{ENOB(RMS)} = \frac{\ln\left(\frac{\text{FSR}}{\text{RMS Noise}}\right)}{\ln(2)}$$

$$\text{RMS Noise} = \frac{\left(2 \times \text{VREF} \times \sqrt{\sum_{k=1}^{1024} (\text{ADO}[k] - \text{Average})^2}\right)}{2^{24}}$$

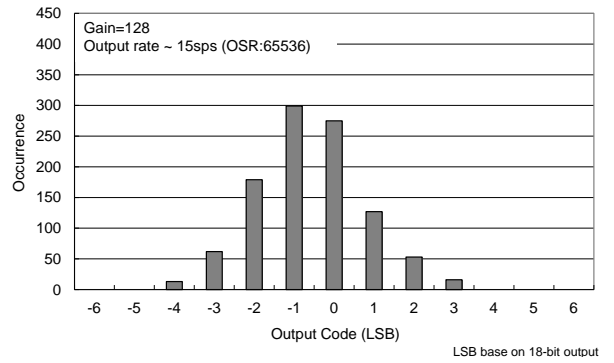
Where FSR (Full - Scale Range) = $2 \times \text{VREF}/\text{Gain}$.

$$\text{Average} = \frac{\sum_{k=1}^{1024} (\text{ADO}[k])}{1024}$$

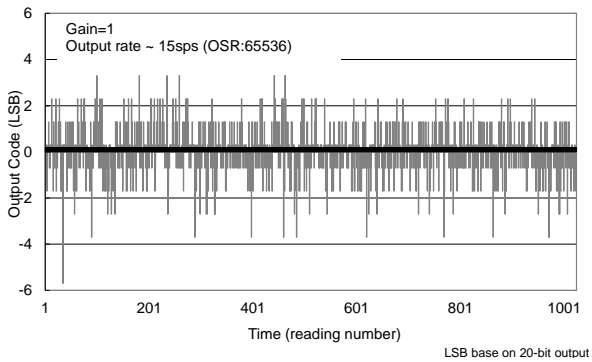
RMS Noise Diagram



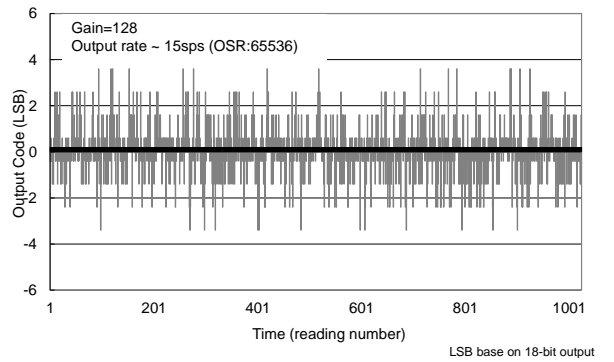
RMS Noise Diagram



RMS Noise Diagram



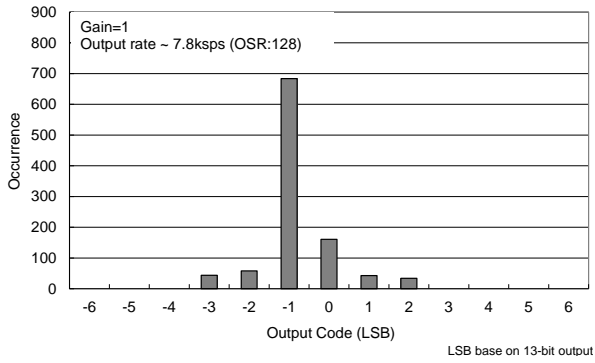
RMS Noise Diagram



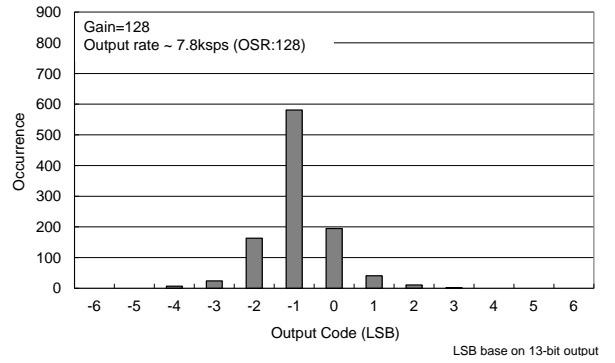
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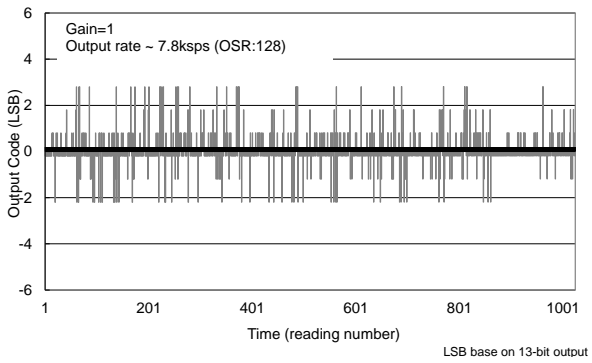
RMS Noise Diagram



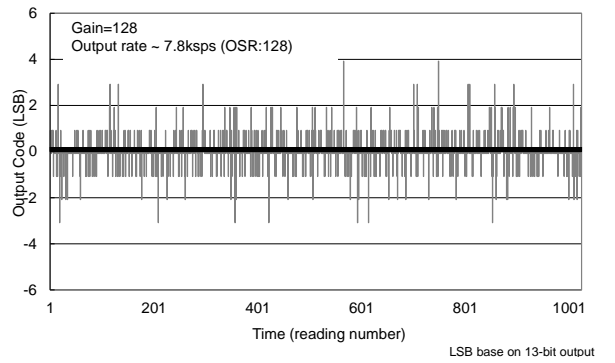
RMS Noise Diagram



RMS Noise Diagram



RMS Noise Diagram



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5. 暫存器列表

“.”no use,“r”read/write,“w”write,“r”read,“r0”only read 0,“r1”only read 1,“w0”only write 0,“w1”only write 1
 “\$”for event status,“.”unimplemented bit,“x”unknown,“u”unchanged,“d”depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	irst-wdt	irst-skerr	INT	R/W	
000h	INDF0	Contents of FSR0 to address data memoryvalue of FSR0 not changed									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
001h	POINC0	Contents of FSR0 to address data memoryvalue of FSR0 post-incremented									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
002h	PODEC0	Contents of FSR0 to address data memoryvalue of FSR0 post-decremented									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
003h	PRINC0	Contents of FSR0 to address data memoryvalue of FSR0 pre-incremented									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
004h	PLUSW0	Contents of FSR0 to address data memoryvalue of FSR0 offset by W									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
005h	INDF1	Contents of FSR1 to address data memoryvalue of FSR0 not changed									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
006h	POINC1	Contents of FSR1 to address data memoryvalue of FSR0 post-incremented									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
007h	PODEC1	Contents of FSR1 to address data memoryvalue of FSR0 post-decremented									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
008h	PRINC1	Contents of FSR1 to address data memoryvalue of FSR1 pre-incremented									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
009h	PLUSW1	Contents of FSR1 to address data memoryvalue of FSR0 offset by W									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
00Fh	FSR0H	-	-	-	-	-	-	-	-	FSR0[8]xuuuu	rw, rw0, rw1
010h	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte, FSR0[7:0]									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
011h	FSR1H	-	-	-	-	-	-	-	-	FSR1[8]xuuuu	rw, rw0, rw1
012h	FSR1L	Indirect Data Memory Address Pointer 0 Low Byte, FSR0[7:0]									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
016h	TOSH	-	-	-	-	TOS[11]	TOS[10]	TOS[9]	TOS[8]xxxxuuuuuuuuuuuu\$\$\$\$	rw, rw0, rw1	
017h	TOSL	Top-of-Stack Low Byte (TOS<7:0>)									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	\$\$\$\$ \$\$\$\$	rw, rw0, rw1
018h	SKCN	SKFL	SKUN	SKOV						SKPRT[2:0]	000..000	u\$\$..\$\$\$	uuu..000	u\$\$..000	uu\$. \$\$\$	rw0, rw0, rw0, rw1
01Ah	PCLATH	-	-	-	-	PC[11]	PC[10]	PC[9]	PC[8]000000000000000000000000	rw, rw0, rw1
01Bh	PCLATL	PC Low Byte for PC<7:0>									0000 0000	0000 0000	0000 0000	0000 0000	0000 0100	rw, rw0, rw1
01Dh	TBLPTRH	-	-	-	-	TBLPTR[11]	TBLPTR[10]	TBLPTR[9]	TBLPTR[8]xxxxuuuuuuuuuuuuuuuuuuuu	rw, rw0, rw1
01Eh	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
01Fh	TBLDH	Program Memory Table Latch High Byte									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
020h	TBLDL	Program Memory Table Latch Low Byte									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
021h	PRODH	Product Register of Multiply High Byte									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
022h	PRODL	Product Register of Multiply Low Byte									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
023h	INTE0	GIE		MCOIE	WDTIE	TB1IE	TMAIE	E1IE	E0IE	0.00 0000	0.uu uuuu	0.uu uuuu	0.uu uuuu	0.uu uuuu	0.uu uuuu	rw, rw0, rw1
024h	INTE1		AD1IE							.0.u.u.u.u.u.	rw, rw0, rw1
026h	INTF0			MCOIF	WDTIF	TB1IF	TMAIF	E1IF	E0IF	..00 0000	..uu uuuu	..uu uuuu	..uu uuuu	..uu uuuu	..\$\$ \$\$\$\$	rw, rw0, rw1
027h	INTF1		AD1IF							.0.u.u.u.u.	\$.	rw, rw0, rw1
029h	WREG	Working Register									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
02Ah	BSRCN	-	-	-	C	DC	N	OV	Zxuuuuu	rw, rw0, rw1
02Bh	MSTAT	-	-	-	C	DC	N	OV	Zxuuuuu	rw, rw0, rw1
02Ch	PSTAT	POR	PD	TO	IDL	RST	SKERR	MCO		\$000 \$00.	uu\$u u\$u.	uu1u uu.	uuu\$ uu\$.	uuu\$ uu\$.	uuu\$ uu\$.	rw0, rw0, rw0, rw0, rw0, rw0, rw1
02Eh	BIECN					VPPHV	BIELV	BIEWR	BIERD	1...\$000	1...\$uuu	1...\$uuu	1...\$uuu	1...\$uuu	1...\$uuu	rw, rw0, rw1
02Fh	BIEARH	ENBIE				12-bit look-up Table as BIEAH[3:0]				0...xxxx	u...uuuu	u...uuuu	u...uuuu	u...uuuu	u...uuuu	rw, rw0, rw1
030h	BIEARL	BIE Address Register as BIEAL[5:0] or 12-bit look-up Table as BIEA[7:0]									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
031h	BIEDRH	BIE High Byte Data Register									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
032h	BIEDRL	BIE Low Byte Data Register									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
033h	PWRCN	ENLDO[1:0]		VDDAX[1:0]		ENREFO		AD1RST	CSFON	0000 0.00	uuuu u.0u	uuuu u.0u	uuuu u.0u	uuuu u.0u	uuuu u.0u	rw, rw0, rw1
034h	OSCCN0	OSCS[1:0]		DHS[1:0]		DMS[2:0]			CUPS	0000 0000	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
035h	OSCCN1	LCPS[1:0]		DADC[1:0]		DTMB[1:0]		TMBS		0000 0000	uuuu uu.	uuuu uu.	uuuu uu.	uuuu uu.	uuuu uu.	rw, rw0, rw1
036h	OSCCN2	ENRTC		XTS[1:0]		HAOM[1:0]		ENHAO	LPO	0000 0011	uuuu uu11	uuuu uu11	uuuu uu11	uuuu uu11	uuuu uu11	rw, rw0, rw1
037h	WDTCN	ENBZ	BZS	BZ[1:0]		ENWDT		DWDT[2:0]		0000 0000	uuuu \$000	uuuu 1000	uuuu uuuu	uuuu uuuu	rw1, rw1, rw1	
038h	TMACN	ENTMA	TMACL	TMAS		DTMA[2:0]				0000 00..	u0uu uu..	u0uu uu..	u0uu uu..	u0uu uu..	rw1, rw1, rw1	
039h	TMAR	TMA counter Register									0000 0000	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw0, rw0, rw0, rw0, rw0, rw0, rw1
03Ah	AD1CN0		ENAD1	AD1HS	IN1ST	VR1ST	AGND1S	CHOP1		..00 0000	..uu uuuu	..uu uuuu	..uu uuuu	..uu uuuu	..uu uuuu	rw, rw0, rw1
03Bh	AD1CN1	IN1P[2:0]			IN1N[2:0]			AD1GN[1:0]		0000 0000	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
03Ch	AD1CN2	DC1S[3:0]			VR1P[1:0]			VR1N[1:0]		0000 0000	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
03Dh	AD1CN3	OSR1[3:0]			PGA[2:0]			VR1GN		000. 0000	uu. uuuu	uu. uuuu	uu. uuuu	uu. uuuu	uu. uuuu	rw, rw0, rw1
03Eh	AD1H	ADC1 conversion high byte data register									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
03Fh	AD1M	ADC1 conversion middle byte data register									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
040h	AD1L	ADC1 conversion low byte data register									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
041h	CSFCN0	SKRST	REFOO			HAOTR[5:0]				0010 0000	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
042h	CSFCN1					PWMAO	MCOO		00..uu..uu..uu..uu..uu..	rw, rw0, rw1
04Bh	MCCN0	ENMC	MCLP	MCSR	MCSPN	MCPS[1:0]			MCNS[1:0]	0000 0000	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
04Ch	MCCN1	MCNES[2:0]			MCRPS[1:0]			MCNEC	MCOFR	MCOIV	0000 0000	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
04Dh	MCCN2	MCRS[3:0]			MCOHS[3:0]					0000 0000	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
04Eh	TB1Flag		PWM6A	PWM5A	PWM4A	PWM3A	PWM2A	PWM1A		..00 0000	..uu uuuu	..uu uuuu	..uu uuuu	..uu uuuu	..uu uuuu	rw, rw0, rw1
04Fh	TB1CN0	ENTB1	TB1M[1:0]	TB1RT[1:0]	TB1CL					0000 00..	uuuu u0..	uuuu u0..	uuuu u0..	uuuu u0..	uuuu u0..	rw1, rw1, rw1
050h	TB1CN1	PA11V	PWMA1[2:0]			PA0IV	PWMA0[2:0]			0000 0000	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
051h	TB1RH	TimerB1 counter Register [15:8]									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
052h	TB1RL	TimerB1 counter Register [7:0]									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
053h	TB1C0H	TimerB1 counter Condition Register [15:8]									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
054h	TB1C0L	TimerB1 counter Condition Register [7:0]									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
055h	TB1C1H	TimerB1 counter Condition Register [15:8]									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
056h	TB1C1L	TimerB1 counter Condition Register [7:0]									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
057h	TB1C2H	TimerB1 counter Condition Register [15:8]									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1
058h	TB1C2L	TimerB1 counter Condition Register [7:0]									xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	rw, rw0, rw1

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Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	irst-wdt	irst-skerr	INT	R/W		
059h	UR0CN	ENSP	ENTX	TX9	TX9D	PARITY			WUE	0000 0.0	uuuu u..u	uuuu u..u	uuuu u..u	uuuu uuuu	r.....rw0		
05Ah	UR0STA		RC9D	PERR	FERR	OERR	RCIDL	TRMT	ABDOVF	.000 0010	.uuu uuuu	.uuu uuuu	.uuu uuuu	uuuu u\$Su	-r.r.r.r.r.r.r.r		
05Bh	BA0CN					ENCR	RC9	ENADD	ENABD 0000 uuuu uuuu uuuu	uuuu uuuu	r.....r		
05Ch	BG0RH	Baud Rate Generator Register High Byte								...x xxxx	...u uuuu	...u uuuu	...u uuuu	...u uuuu	r.....r		
05Dh	BG0RL	Baud Rate Generator Register Low Byte								xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r		
05Eh	TXOR	UART Transmit Register								xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r		
05Fh	RCREG	UART Receive Register								xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r		
070h	PT1							PT11	PT10xxxxxxxx\$\$	r.....r		
071h	TRISC1							TC11	TC1000uuuuuuuu	r.....r		
072h	PT1DA					FMCO		DA11	DA10 0.00 u.uu u.uu u.uu u.uu	r.....r		
073h	PT1PU							PU11	PU1000uuuuuuuu	r.....r		
074h	PT1EG					E1EG[1:0]		E0EG[1:0]	 0000 uuuu uuuu uuuu uuuu	r.....r		
075h	PT2	PT27	PT26	PT25	PT24	PT23	PT22	PT21	PT20	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	r.....r		
076h	TRISC2	TC27	TC26	TC25	TC24	TC23	TC22	TC21	TC20	0000 0000	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r		
077h	PT2DA	DA27	DA26	DA25	DA24	DA23	DA22	FPWMA1	FPWMA0	0000 0000	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r		
078h	PT2PU	PU27	PU26	PU25	PU24	PU23	PU22	PU21	PU20	0000 0000	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r		
079h	PT3	PT37	PT36	PT35	PT34	PT33	PT32	PT31	PT30	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	r.....r		
07Ah	TRISC3		TC36	TC35	TC34	TC33	TC32	TC31	TC30	.000 0000	.uuu uuuu	.uuu uuuu	.uuu uuuu	.uuu uuuu	-r.....r		
07Bh	PT3DA		DA36	DA35	DA34	DA33	DA32	DA31	DA30	.000 0000	.uuu uuuu	.uuu uuuu	.uuu uuuu	.uuu uuuu	-r.....r		
07Ch	PT3PU		PU36	PU35	PU34	PU33	PU32	PU31	PU30	.000 0000	.uuu uuuu	.uuu uuuu	.uuu uuuu	.uuu uuuu	-r.....r		
080h - 017Fh	General Purpose Register as 256Byte										uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r	
180h	LCDCN1	ENLCD	LC DPR	VLCD[1:0]			LCDBF				0000 00..	uuuu uu..	uuuu uu..	uuuu uu..	uuuu uu..	r.....r	
181h	LCDCN2	LCDBL	LCDMX[1:0]			LCDS	DLCD[1:0]				0000 00..	uuuu uu..	uuuu uu..	uuuu uu..	uuuu uu..	r.....r	
182h	LCD0	Segment SEG2@[3:0] and SEG3@[7:4] data register of LCD										xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r
183h	LCD1	Segment SEG4@[3:0] and SEG5@[7:4] data register of LCD										xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r
184h	LCD2	Segment SEG6@[3:0] and SEG7@[7:4] data register of LCD										xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r
185h	LCD3	Segment SEG8@[3:0] and SEG9@[7:4] data register of LCD										xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r
186h	LCD4	Segment SEG10@[3:0] and SEG11@[7:4] data register of LCD										xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r
187h	LCD5	Segment SEG12@[3:0] and SEG13@[7:4] data register of LCD										xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r
188h	LCD6	Segment SEG14@[3:0] and SEG15@[7:4] data register of LCD										xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r
189h	LCD7	Segment SEG16@[3:0] and SEG17@[7:4] data register of LCD										xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r
18Ah	LCD8	Segment SEG18@[3:0] and SEG19@[7:4] data register of LCD										xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r
18Bh	LCD9	Segment SEG20@[3:0] and SEG21@[7:4] data register of LCD										xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r
18Ch	LCD10	Segment SEG22@[3:0] and SEG23@[7:4] data register of LCD										xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r
18Dh	LCD11	Segment SEG24@[3:0] and SEG25@[7:4] data register of LCD										xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r
18Eh	LCD12	Segment SEG26@[3:0] and SEG27@[7:4] data register of LCD										xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r
18Fh	LCD13	Segment SEG28@[3:0] and SEG29@[7:4] data register of LCD										xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r
190h	LCD14	Segment SEG30@[3:0] and SEG31@[7:4] data register of LCD										xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r
191h	LCD15	Segment SEG32@[3:0] and SEG33@[7:4] data register of LCD										xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	r.....r

6. 訂貨資訊

下單品名 ¹	封裝型式	引腳數	封裝型式		程式碼	出貨包裝 形式	個裝 數量	材料 組成	MSL ³
			描述方式	編號 ²					
HY13P56B-D000	Die	-	D	000	000	-	200	Green ⁴	-
HY13P56B-L064	LQFP	64	L	064	000	Tray	250	Green ⁴	MSL-3

¹ 產品名稱 – 封裝型式描述方式 – 程式碼編號 (空白片 / 標準品 / 代客燒錄碼)

例如：您的需求是不帶程式碼的空白片且需要的產品是裸片出貨，晶片型號為 HY13P56B。則下單品名為 HY13P56B-D000

例如：您的代客燒錄服務申請的程式碼編號為 008，晶片型號為 HY13P56B，且需要的產品是裸片出貨。則下單品名為 HY13P56B-D000-008

例如：您的需求是晶片型號為 HY13P56B，不帶程式碼的空白片且需要的產品是封裝片 LQFP64 出貨，則下單品名為 HY13P56B-L064，且需以 Tray 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tray

例如：您的需求是晶片型號為 HY13P56B，代客燒錄服務申請的程式碼編號為 009，而需求的產品是封裝片 LQFP64 出貨，則下單品名為 HY13P56B-L064-009，且需以 Tray 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tray

² 程式碼編號

“001”~“999” 為標準品或代客燒錄申請的程式碼編號，而空白晶片不帶此碼。

³ MSL:

濕度敏感性等級係依據 IPC/JEDEC J-STD-020 的規範加以試驗分級，並參考 IPC/JEDEC J-STD-033 的標準處理、包裝、運輸與使用。

⁴ Green (RoHS & no Cl/Br):

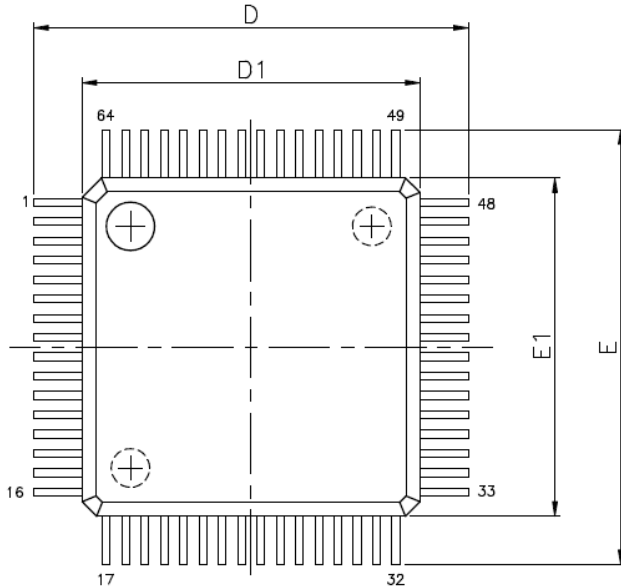
HYCON 產品皆為 Green Product，符合 RoHS 指令以及無鹵素規定(Br/Cl<0.1%)

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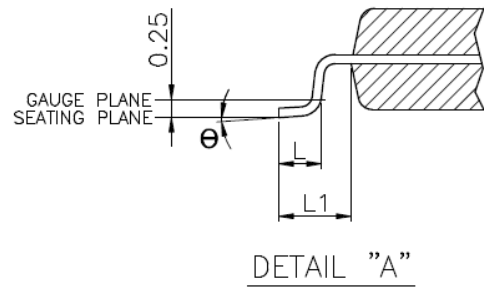
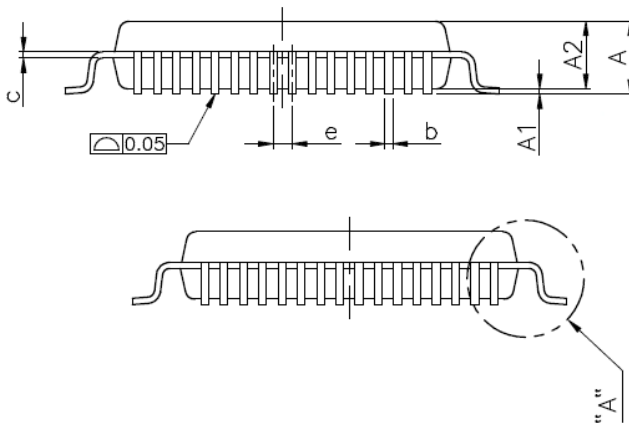
7. 封裝型式資訊

7.1. LQFP64(L064)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°



JEDEC MS-026 compliant

HY13P56B

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8. 電器特性

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at V_{DD} to V_{SS}	-0.2 V to 4.0 V
Voltage applied to any pin (see Note 1)	-0.2 V to $V_{DD} + 0.3$ V
Voltage applied to RST/VPP pin	-0.2 V to 6.9 V
Voltage applied to TST pin (see Note 1)	-0.2 V to $V_{DD} + 1V$
Diode current at any device terminal	± 2 mA
Storage temperature, Tstg: (unprogrammed device)	-55°C to 150°C
(programmed device)	-40°C to 85°C
Total power dissipation	0.5w
Maximum output current sink by any PORT1 to PORT3 I/O pin25mA

8.1. Recommended operating conditions

$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{DD}	Supply Voltage	All digital peripherals and CPU	2.2		3.6	V
		Analog peripherals	2.4		3.6	
V_{SS}	Supply Voltage		0		0	
RTC	External Oscillator Frequency	$V_{DD} = 2.2V, ENRTC[0]=1$		32.768K		HZ

8.2. Internal RC Oscillator

$T_A = 25^\circ\text{C}, V_{DD} = 3.0V$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
IRCH	High Speed Oscillator frequency	ENHAO[0]=1, HAOM[1:0]=00b		2.0		MHz
		ENHAO[0]=1, HAOM[1:0]=01b		4.0		MHz
		ENHAO[0]=1, HAOM[1:0]=11b		7.6		MHz
IRCL	Low Power Oscillator frequency			11.5		KHz

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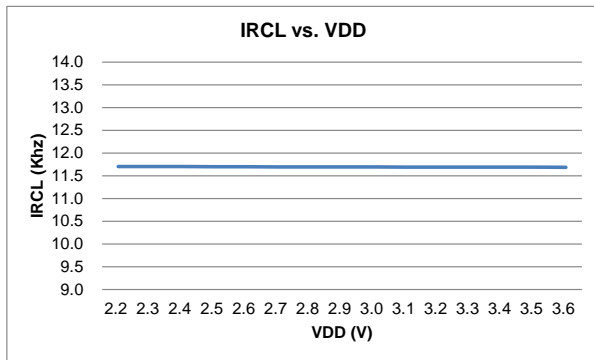


Figure IRCL vs. VDD

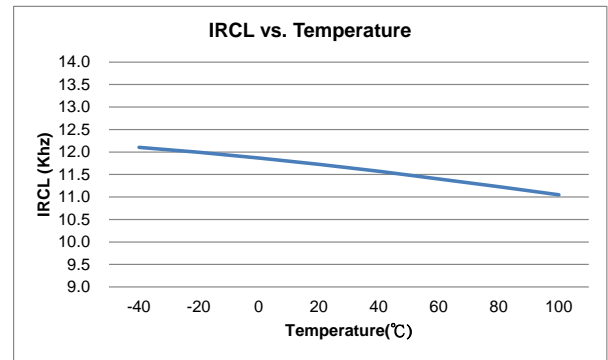


Figure IRCL vs. Temperature

8.3. Supply current into VDD excluding peripherals current

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, \text{OSC_LPO} = 11\text{KHz}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM1}	Active mode 1	OSC_CY = off, OSC_HAO = 6.8MHz, CPU_CK = 6.8MHz		0.9	2	mA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO = 3.7MHz, CPU_CK = 3.7MHz		0.5	1	mA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 2MHz		0.27	0.5	mA
I_{AM4}	Active mode 4	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 1MHz		0.15	0.3	mA
I_{LP1}	Low Power 1	OSC_CY = 32768Hz, OSC_HAO = off, CPU_CK = 32768Hz		7	12	uA
I_{LP2}	Low Power 2	OSC_CY = 32768Hz, OSC_HAO = off, CPU_CK = 16384Hz		5	10	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		2	4	uA
I_{LP4}	Low Power 4	Sleep state		0.7	1.2	uA

OSC_CY : External Oscillator frequency.

OSC_HAO : Internal High Accuracy Oscillator frequency.

CPU_CK : CPU core work frequency.

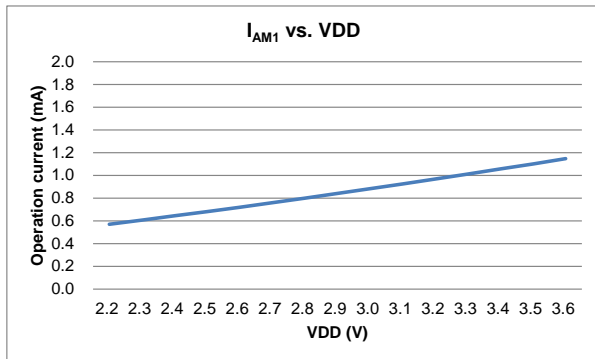


Figure I_{AM1} vs. VDD

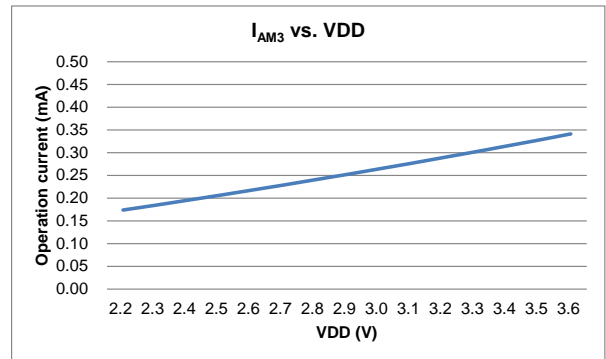


Figure I_{AM3} vs. VDD

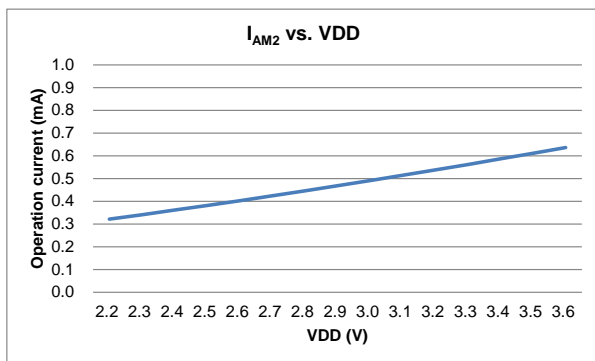


Figure I_{AM2} vs. VDD

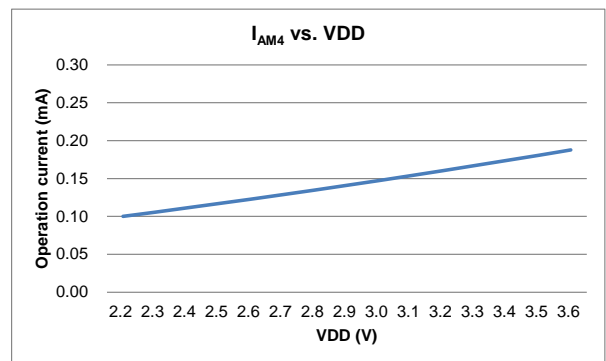


Figure I_{AM4} vs. VDD

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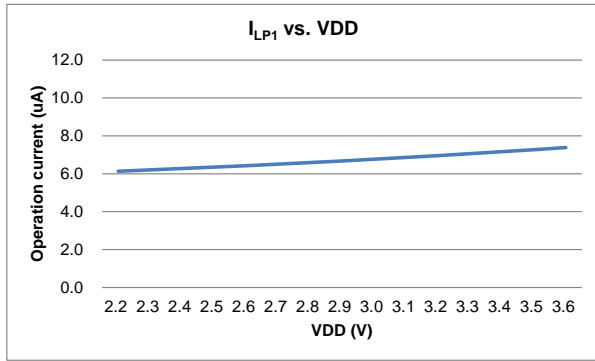


Figure I_{LP1} vs. VDD

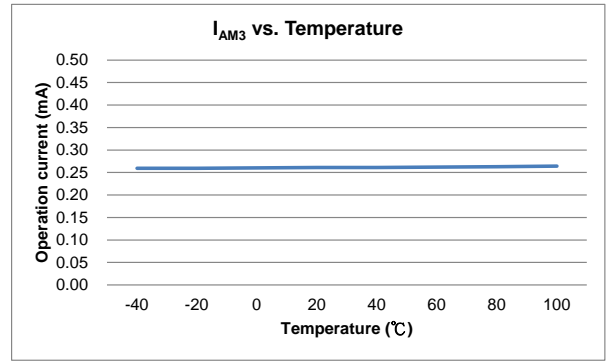


Figure I_{AM3} vs. Temperature

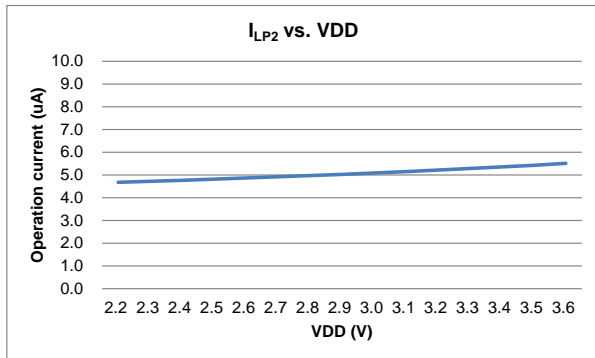


Figure I_{LP2} vs. VDD

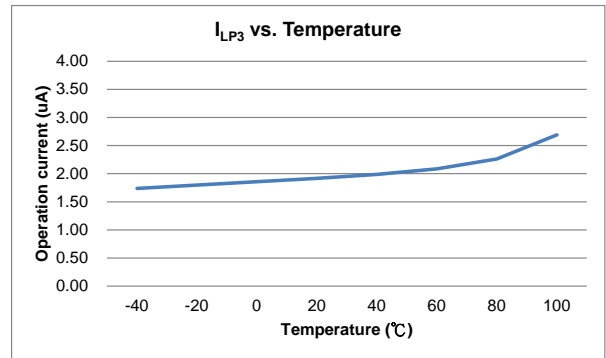


Figure I_{LP3} vs. Temperature

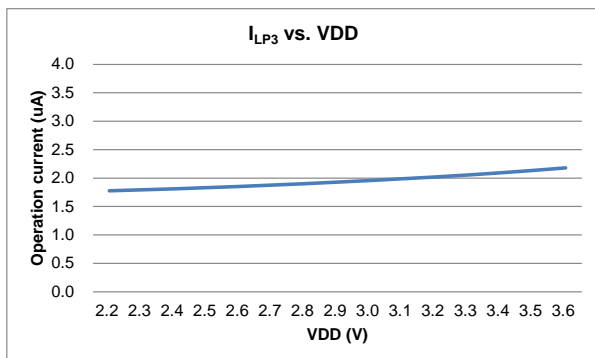


Figure I_{LP3} vs. VDD

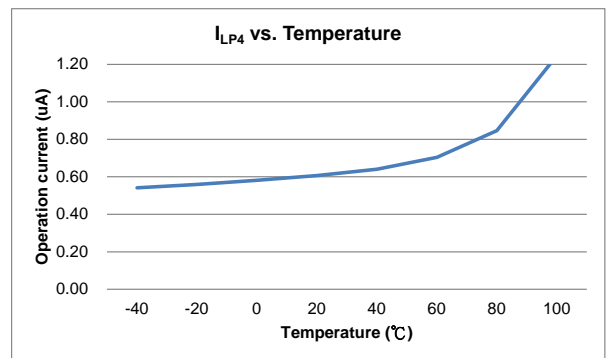


Figure I_{LP4} vs. Temperature

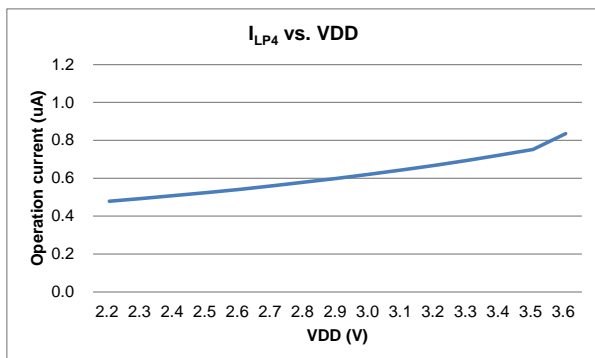


Figure I_{LP4} vs. VDD

8.4. Port1~3

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				2.1	V
V_{IL}	Low-Level input voltage		0.9			
V_{hys}	Input Voltage hysteresis($V_{IH} - V_{IL}$)			0.8		V
I_{LKG}	Leakage Current				0.1	μA
R_{PU}	Port pull high resistance			200		$\text{k}\Omega$
Output voltage and current and frequency						
V_{OH}	High-level output voltage	$I_{OH}=10\text{mA}$	$V_{DD} - 0.3$			V
V_{OL}	Low-level output voltage	$I_{OL}=-10\text{mA}$			$V_{SS} + 0.3$	

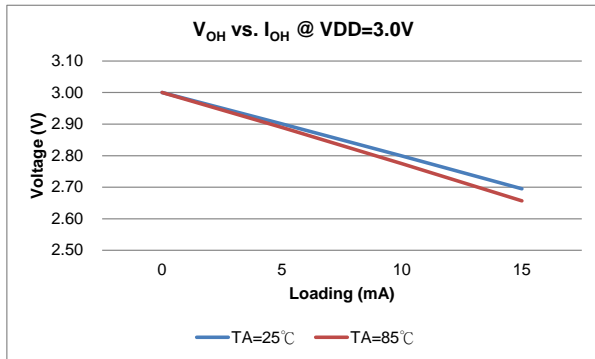


Figure V_{OH} vs. I_{OH} @ $V_{DD}=3.0\text{V}$

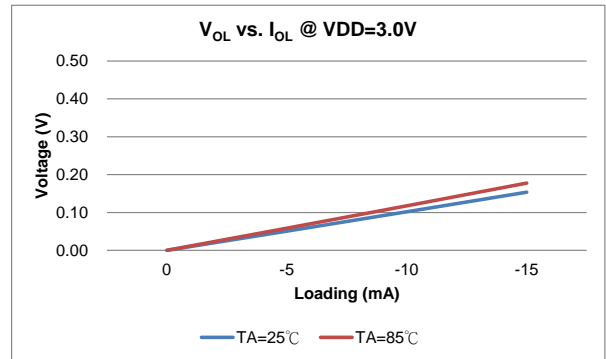


Figure V_{OL} vs. I_{OL} @ $V_{DD}=3.0\text{V}$

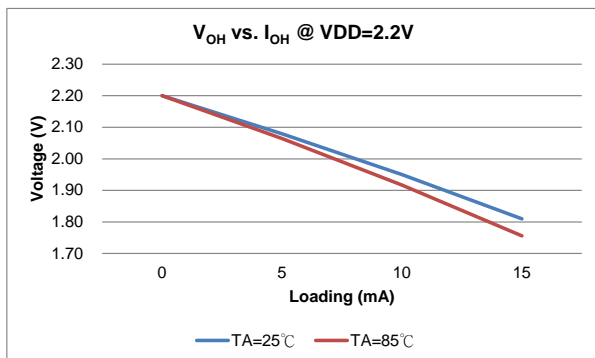


Figure V_{OH} vs. I_{OH} @ $V_{DD}=2.2\text{V}$

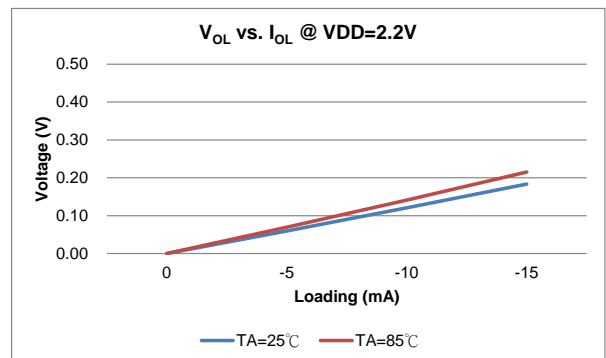


Figure V_{OL} vs. I_{OL} @ $V_{DD}=2.2\text{V}$

8.5. Reset(Brownout, External RST pin, Low Voltage Detect)

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
BOR	Pulse length needed to accepted reset internally, t_{d-LVR}		2			us
	V_{DD} Start Voltage to accepted reset internally (L \rightarrow H), V_{LVR}		1.8	1.9	2.0	V
	Hysteresis, $V_{HYS-LVR}$			35		mV
RST	Pulse length needed as RST/VPP pin to accepted reset internally, t_{d-RST}		2			us
	Input Voltage to accepted reset internally		0.9			V
	Hysteresis, $V_{HYS-RST}$			0.8		V

BOR : Brownout Reset. LVD : Low Voltage Detect. LVR : Low Voltage Reset of BOR. RST : External Reset pin

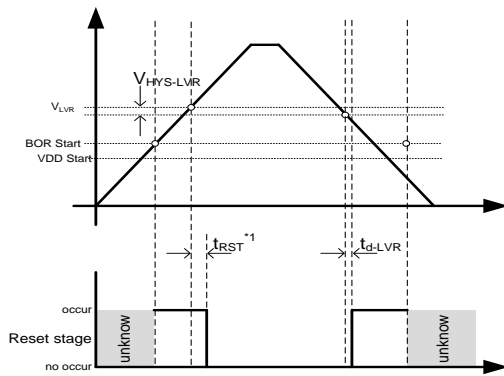


Figure BOR reset diagram

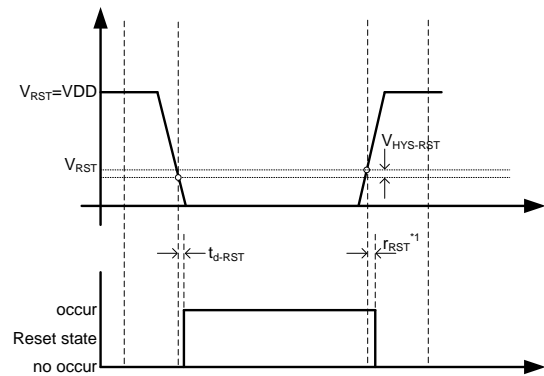


Figure RST reset diagram

8.6. Power System

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
VDDA	VDDA operation current, I_{VDDA}	$I_L = 0\text{mA}$	ENLDO[1:0]=11b		11		μA
	Select VDDA output voltage	$I_L = 0.1\text{mA}$, $V_{DD} \geq V_{VDDA} + 0.2\text{V}$	VDDAX[1:0]=00b		2.4		V
			VDDAX[1:0]=01b		2.7		V
			VDDAX[1:0]=10b		3.0		V
			VDDAX[1:0]=11b		3.3		V
	Dropout voltage	$I_L = 10\text{mA}$	VDDAX[2:0]=00b		120		mV
			VDDAX[2:0]=01b		130		mV
			VDDAX[2:0]=10b		140		mV
			VDDAX[2:0]=11b		160		mV
	Temperature drift	VDDX[1:0]=11b	$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$		50		ppm/ $^\circ\text{C}$
V_{DD} Voltage drift	$I_L = 0.1\text{mA}$	$V_{DD} = 2.5\text{V} \sim 3.6\text{V}$		± 0.2		%/V	
REFO	REFO operation current, I_{REFO}	$I_L = 0\text{mA}$			20		μA
	Output voltage, V_{REFO}	ENREFO[0]=1	$I_L = 0\mu\text{A}$		1.2		V
	Output voltage with Load		$I_L = \pm 200\mu\text{A}$	0.98		1.02	V_{ACM}
	Temperature drift	ENREFO[0]=1,	$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$		50		ppm/ $^\circ\text{C}$
	VDDA Voltage drift	$I_L = 10\mu\text{A}$			150		$\mu\text{V}/\text{V}$
VDDA : Adjust Voltage Regulator							
REFO : Reference Voltage							

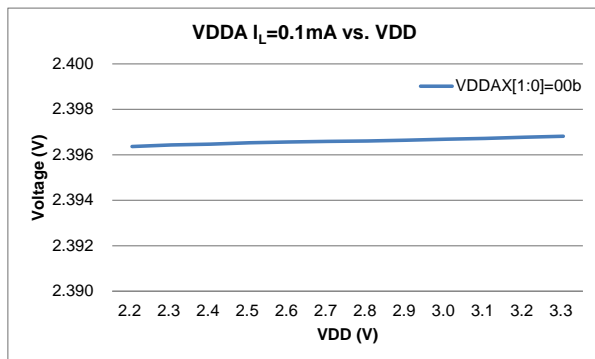


Figure VDDA vs. VDD

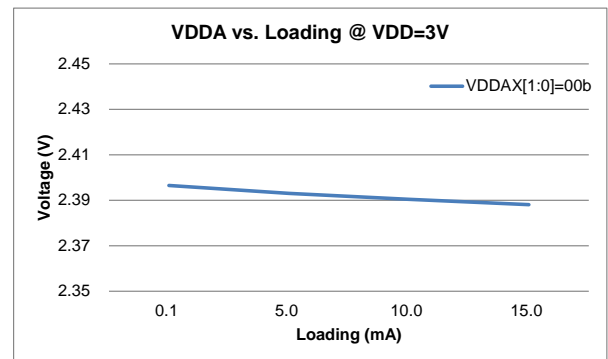


Figure VDDA vs. Loading

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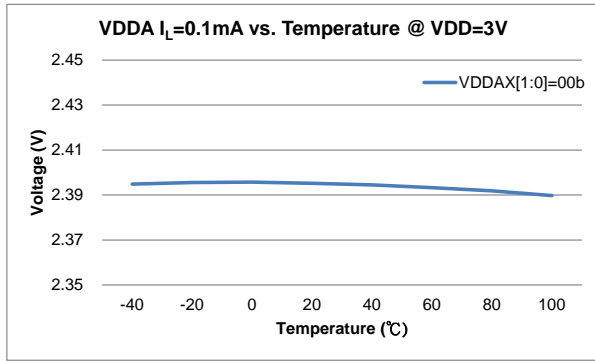


Figure VDDA vs. Temperature

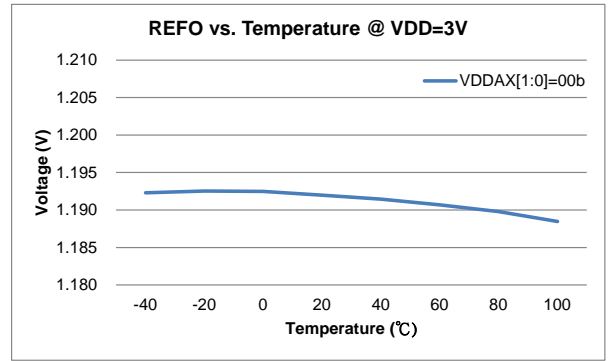


Figure REFO vs. Temperature

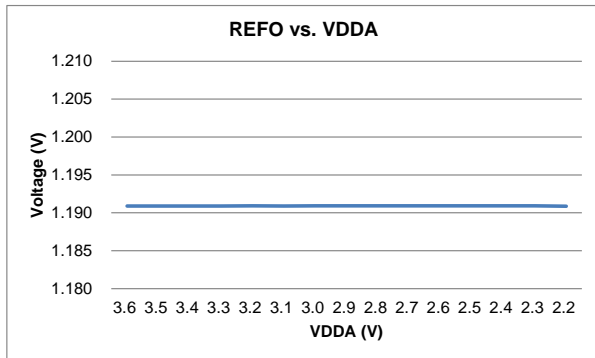


Figure REFO vs. VDDA

8.7. LCD

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{V}$, $C_{VLCD} = 1\mu\text{F}$, unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
I_{LCD}	Operation supply current without output buffer.	LCDPR[0]=1	$V_{DD} = 2.2\text{V}$	11			uA
			$V_{DD} = 3.0\text{V}$				
VLCD	Supply Voltage at VLCD pin	LCDPR[0]=0		2.2		3.6	V
	Embedded Charge Pump output voltage at VLCD pin	$V_{DD} = 2.2\text{V}$, LCDPR[0]=1, $C_{VLCD} = 1\mu\text{F}$	VLCDX[1:0]=11b	-10%	2.55	+10%	V
			VLCDX[1:0]=10b	-10%	2.75	+10%	
			VLCDX[1:0]=01b	-10%	2.95	+10%	
VLCDX[1:0]=00b	-10%	3.25	+10%				
Z_{LCD}	Output impedance with LCD buffer	$f_{LCD} = 178\text{Hz}$, VLCD=2.9V		10			k Ω

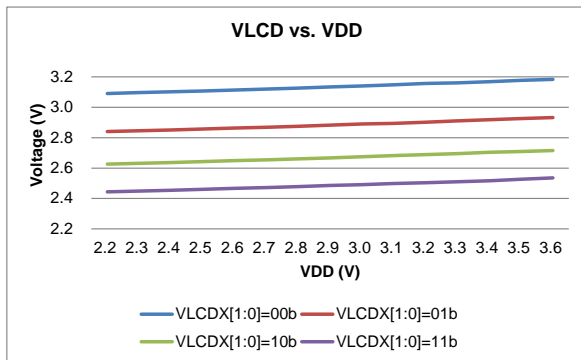


Figure VLCD vs. VDD

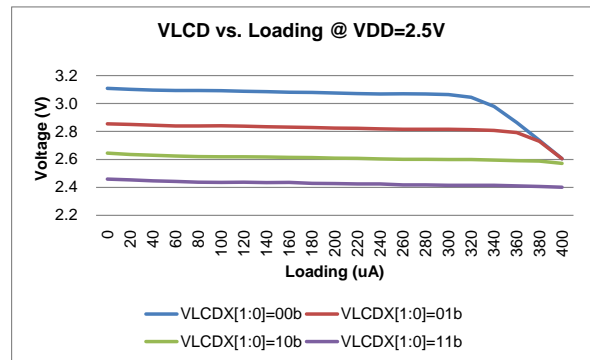


Figure VLCD vs. Loading

8.8. Multi-Comparator

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{MC}	Operation supply current	ENMC[0]=1, MCLP[0]=1b	5			uA
	Low Power Mode	ENMC[0]=1, MCLP[0]=0b	1			
V_{IC}	Common-mode input voltage		0		$V_{DD}-1$	V
V_{OS}	Offset voltage		-5		5	mV
V_{hys}	Input hysteresis		0	0.7	1.5	mV
V_{REF}	Reference Voltage	MCPS[1:0]=11b	1.1	1.2	1.3	V
	Temperature Drift	MCPS[1:0]=11b	50			ppm/ $^\circ\text{C}$
	VDD Voltage drift	MCPS[1:0]=11b	± 2			%/V
V_{ACCY}	Reference Voltage	ENLDO[1:0]=11b, MCPS[1:0]=10b	1.15	1.2	1.25	V
	Temperature Drift	ENLDO[1:0]=11b, MCPS[1:0]=10b	50			ppm/ $^\circ\text{C}$
	VDD Voltage drift	ENLDO[1:0]=11b, MCPS[1:0]=10b	± 0.2			%/V
I_R	Multi-node resistor current	MCSR[0]=0b	10			uA
		MCSR[0]=1b	30			
LVD	ENLDO[1:0]=11b, MCPS[1:0]=11b, MCSR[0]=0b, MCRS[3:0]=0011b		-0.1	3.2	+0.1	V
	ENLDO[1:0]=11b, MCPS[1:0]=11b, MCSR[0]=0b, MCRS[3:0]=0100b		-0.1	3.0	+0.1	
	ENLDO[1:0]=11b, MCPS[1:0]=11b, MCSR[0]=0b, MCRS[3:0]=0101b		-0.1	2.9	+0.1	
	ENLDO[1:0]=11b, MCPS[1:0]=11b, MCSR[0]=0b, MCRS[3:0]=0110b		-0.1	2.7	+0.1	
	ENLDO[1:0]=11b, MCPS[1:0]=11b, MCSR[0]=0b, MCRS[3:0]=0111b		-0.1	2.6	+0.1	
	ENLDO[1:0]=11b, MCPS[1:0]=11b, MCSR[0]=0b, MCRS[3:0]=1000b		-0.1	2.5	+0.1	
	ENLDO[1:0]=11b, MCPS[1:0]=11b, MCSR[0]=0b, MCRS[3:0]=1001b		-0.1	2.4	+0.1	
	ENLDO[1:0]=11b, MCPS[1:0]=11b, MCSR[0]=0b, MCRS[3:0]=1010b		-0.1	2.3	+0.1	
	ENLDO[1:0]=11b, MCPS[1:0]=11b, MCSR[0]=0b, MCRS[3:0]=1011b		-0.1	2.2	+0.1	
	ENLDO[1:0]=11b, MCPS[1:0]=11b, MCSR[0]=0b, MCRS[3:0]=1100b		-0.1	2.1	+0.1	
	ENLDO[1:0]=11b, MCPS[1:0]=11b, MCSR[0]=0b, MCRS[3:0]=1101b		-0.1	2.0	+0.1	
	MCRS[3:0]=0000b~0010b, and 1110b~1111b (reserved)		-			

LVD : Low Voltage Detect.

Note : 當 MCPS[1:0]= 11b 的時候, 代表選擇到 VREF, 則 LVD 上下限規格為 0.1V. 而當 MCPS[1:0]= 10b 的時候, 代表選擇到 VACCY, 則 LVD 上下限規格為 0.05V

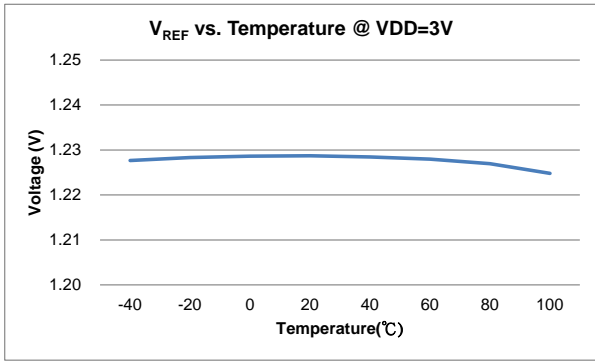


Figure V_{REF} vs. Temperature

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8.9. $\Sigma\Delta$ ADC, Power Supply and Recommended operating conditions

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA}=2.4\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{SD18}	Supply Voltage at VDDA		2.4		3.6	V
f_{SD18}	Modulator sample frequency, ADC_CK		125	250	1000	KHz
	Over Sample Ratio, OSR		32		65536	
f_{ADC_CK}	High Power mode	AD1HS[0]=1b	0.5		1.0	MHz
	Low Power mode	AD1HS[0]=0b	0.125		0.5	MHz

8.9.1. Operating Current

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA}=2.4\text{V}$, unless otherwise noted

Parameter	Test Conditions	Min.	Typ.	Max.	unit
Analog Supply Current I, ADC_CK= 1000KHz, OSR=65536, AD1HS[0]=1b, $f_{DATA} = 15\text{SPS}$	VDDA=2.4V, Gain=1		250		μA
	VDDA=2.4V, Gain=128@PGA=x32		850		μA
Analog Supply Current II, ADC_CK= 250KHz, OSR=65536, AD1HS[0]=0b, $f_{DATA} = 4\text{SPS}$	VDDA=2.4V, Gain=1		120		μA
	VDDA=2.4V, Gain=128@PGA=x32		550		μA

8.9.2. Analog Inputs

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA}=2.4\text{V}, \text{PGA}*\text{Gain}=128$, unless otherwise noted

Parameter	Test Conditions	Min.	Typ.	Max.	unit
Full-Scale Input Voltage(VINP – VINN)	$V_{REF} = V_{DDA}$,		$\pm 0.5 * V_{REF} / (\text{Gain} * \text{PGA})$		V
Full-Scale Input Voltage(VINP – VINN)	$V_{REF} = 1\text{V}$,		$\pm 0.9 * V_{REF} / (\text{Gain} * \text{PGA})$		V
Negative Signal Input (VINN)		VSSA-0.2		VDDA+0.2	V
Positive Signal Input (VINP)		VSSA-0.2		VDDA+0.2	V
Common-Mode Input Range		VSSA-0.2		VDDA+0.2	V

8.9.3. Performance

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA}=2.4\text{V}, \text{PGA}*\text{Gain}=128$, unless otherwise noted

Parameter	Test Conditions	Min.	Typ.	Max.	unit
Data Rate	ADC_CK=1000KHz, OSR=32, AD1HS [0]=1b		31,250		SPS
	ADC_CK=1000KHz, OSR=65536, AD1HS [0]=1b		15		SPS
	ADC_CK=500KHz, OSR=32, AD1HS [0]=1b		15,625		SPS
	ADC_CK=500KHz, OSR=65536, AD1HS [0]=1b		7.5		SPS

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	ADC_CK=250KHz, OSR=32, AD1HS [0]=0b	7,812	SPS
	ADC_CK=250KHz, OSR=65536, AD1HS [0]=0b	3.8	SPS
Digital Filter Settling Time	Full Settling	3	Conversions
Integral Nonlinearity (INL)	Differential Input, End-Point Fit, G = 1, VIN=0.9*VR, delta VR~1.2V	± 30 ± 100	ppm
Input Offset Error	Gain=1,	± 50	ppm of FS
	Gain=128,	± 5	ppm of FS
Input Offset Drift	Gain=1	2	$\mu\text{V}/^\circ\text{C}$
	Gain=128	4	$\text{nV}/^\circ\text{C}$
Gain Drift	Input common voltage=VDDA	5	ppm/ $^\circ\text{C}$
	Input common voltage=VDDA/2	5	ppm/ $^\circ\text{C}$
AC power supply rejection ratio	VDD=3V \pm 100mV, Gain = 1, f _{VDD} =50Hz,60Hz \pm 1Hz	>80	dB
		Gain = 128	>70
Common-Mode Rejection	at DC, Input Voltage=VDDA/2 \pm 0.1V	>75	dB
Power-Supply Rejection	at DC, VDDA=3V \pm 100mV, Gain=1	60	dB
	at DC, VDDA=3V \pm 100mV, Gain=128	95	dB

8.9.4. Voltage Reference

T_A = -40°C to +85°C, V_{DD} = 3.0V, VDDA=2.4V, PGA*Gain=128, unless otherwise noted

Parameter	Test Conditions	Min.	Typ.	Max.	unit
Voltage Reference Input (VREF)	VREF = REFP – REFN			VDDA	V
Negative Reference Input (REFN)		VSS-0.1		VDDA/2	V
Positive Reference Input (REFP)		VDDA/2		VDDA+0.1	V
Reference Voltage (V12)	IN1N[2:0]=011b, or VR1P[1:0]=01b, or VR1N[1:0]=01b		1.2		V
V12 Temperature drift	T _A =-40°C ~85°C		50		ppm/ $^\circ\text{C}$
V12 Voltage drift (VDDA)			150		$\mu\text{V}/\text{V}$

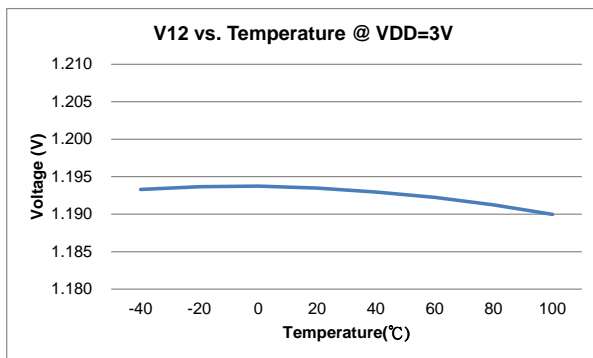


Figure V12 vs. Temperature

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8.9.5. Temperature sensor

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA} = 3.3\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
TC_{Sensor}	Sensor temperature drift			178		$\mu\text{V}/^\circ\text{C}$
KT	Absolute Temperature Scale 0°K	Gain = 1, $V_{\text{REF}} = V_{\text{DDA}}/2$		-289		$^\circ\text{C}$
TC_{ERR}	One point calibrate error temperature	Calibration at 25°C of $-40^\circ\text{C} \sim 85^\circ\text{C}$		± 2		$^\circ\text{C}$

8.10. Build-In EPROM(BIE)

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
T_O	Operation temperature range		0	25	40	$^\circ\text{C}$
$V_{\text{VPP-BIE}}$	Supply Voltage	ENBIE[0]=1, BIELV[0]=0		6.0	6.5	V
	Low Supply Voltage	ENBIE[0]=1, BIELV[0]=1	2.75			V
I_{BIE}	Operation supply current			5		mA
V_{SS}	Supply Voltage			0		V

當使用外部 V_{BIE} 電源燒錄BIE區塊時，可以透過指令一次燒錄一個字節(word)資料於BIE區塊內; BIELV[0]=0

當使用 2.75V 低壓燒錄控制電路時，則不需外接 V_{BIE} 電源仍可燒錄 BIE 區塊。

9. 修訂記錄

以下描述本文件差異較大的地方，而標點符號與字形的改變不在此描述範圍。

版本	頁次	變更摘要
V01	all	初版文件;
V02	18	移除 VLCD 暫存器 LCDCN1 的控制位元 LCDTE
	28	修正 VLCD 規格描述
	29	新增 LVD 上下限規格描述