HY13P52
Datasheet

8-Bit RISC-like Mixed Signal Microcontroller

Embedded 24-Bit ΣΔADC

目錄

注意：

1、 本說明書中的內容，隨著產品的改進，有可能不經過預告而更改。請客戶及時到本公司網站下載更新 http://www.hycontek.com。

2、 本規格書中的圖形、應用電路等，因第三方工業所有權引發的問題，本公司不承擔其責任。

3、 本產品在單獨應用的情況下，本公司保證它的性能、典型應用和功能符合說明書中的條件。當使用在客戶的產品或設備中，以上條件我們不作保證，建議客戶做充分的評估和測試。

4、 請注意輸入電壓、輸出電壓、負載電流的使用條件，使 IC 內的功耗不超過封裝的容許功耗。對於客戶在超出說明書中規定額定值使用產品，即使是瞬間的使用，由此所造成的損失，本公司不承擔任何責任。

5、 本產品雖內置防靜電保護電路，但請不要施加超過保護電路性能的過大靜電。

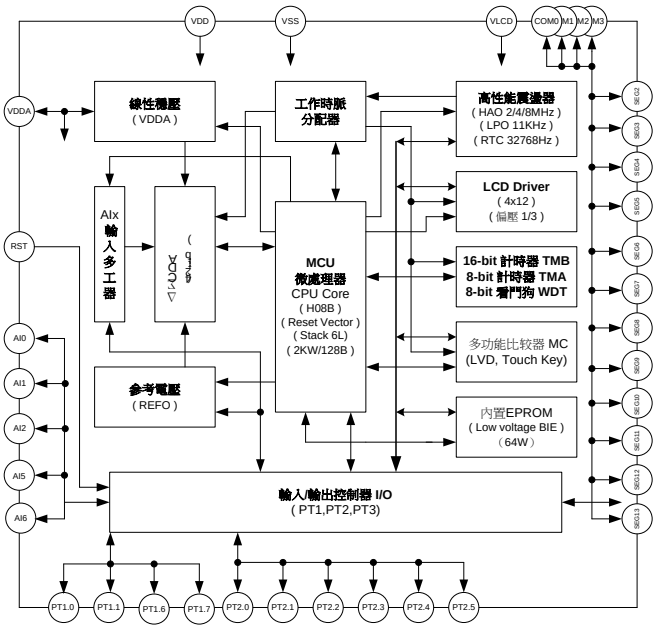
6、 本規格書中的產品，未經書面許可，不可使用在要求高可靠性的電路中。例如健康醫療器械、防災器械、車輛器械、車載器械及航空器械等對人體產生影響的器械或裝置，不得作為其部件使用。

7、 本公司一直致力於提高產品的品質和可靠度，但所有的半導體產品都有一定的失效概率，這些失效概率可能會導致一些人身事故、火災事故等。當設計產品時，請充分留意冗餘設計並採用安全指標，這樣可以避免事故的發生。

8、 本規格書中內容，未經本公司許可，嚴禁用於其他目的之轉載或複製。

1. 特點

- 8-Bit RISC-like 微控制器，具有 46 條高性能指令集 H08B
- 24-Bit ΣΔADC 類比數位轉換器
  - 梳狀濾波器採三階設計，轉換頻率高達 31.25Ksps
  - 取樣頻率 125K/250K/500K/1MHz
  - 超取樣頻率設置 32～65535
  - 全差動輸入信號與測量範圍的零點調整
  - 信號放大 x1,x2 ~ x128
  - 測量信號輸入通道 4ch
  - 低溫飄係數與內置絕對溫度傳感器
- 內部電源系統
  - 內置 LDO 線性穩壓電源 VDDA
    - 內部類比電路或外部傳感器電壓源
    - 輸出可設置 2.4V/2.7V/3.0V/3.3V，可外灌輸入電壓
    - 低操作功耗與低溫飄係數
  - 內置參考電壓源 REFO
    - 內置參考電壓源 1.2V 僅供 ADC 輸入使用
    - 低操作功耗與低溫飄係數
- 多功能比較器
  - 輸出濾波與反相及低功耗設計
  - 中斷事件
  - 電壓檢測/電容測量等應用
- 計時器
  - Watch Dog
    - 復位事件與中斷事件
  - 8-bit Timer
    - 中斷事件
  - 16-bit Timer
    - 16-Bit PWM/PFD 輸出
    - 8+8 PWM 輸出
    - 兩個 8-Bit PWM 輸出
    - 中斷事件
- LCD 驅動顯示器
  - 支援 4x12 點，偏壓模式 1/3
  - 低功耗設計，操作電流 10uA



- 工作電壓與操作溫度範圍
  - 2.2V ～ 3.6V，- 40°C ～ 85°C
- 工作頻率
  - 僅支援一組外接低速石英震盪器 32768Hz
  - 內建高精度 HAO 震盪器 2MHz/4MHz/8MHz
  - 內建低功耗 LPO 震盪器 11KHz
- 記憶體型式
  - 2KW OTP 程式記憶體
  - 128B 資料記憶體，6 層堆棧
  - Build-In EPROEM
    - 工作電壓 2.75V
    - 64W EPROM 記憶體
- 引腳特色
  - 具 10mA 驅動能力
- 復位機制
  - Power On Reset/Brown Out Reset
  - Watch Dog Reset/Reset PIN

2. 引腳定義

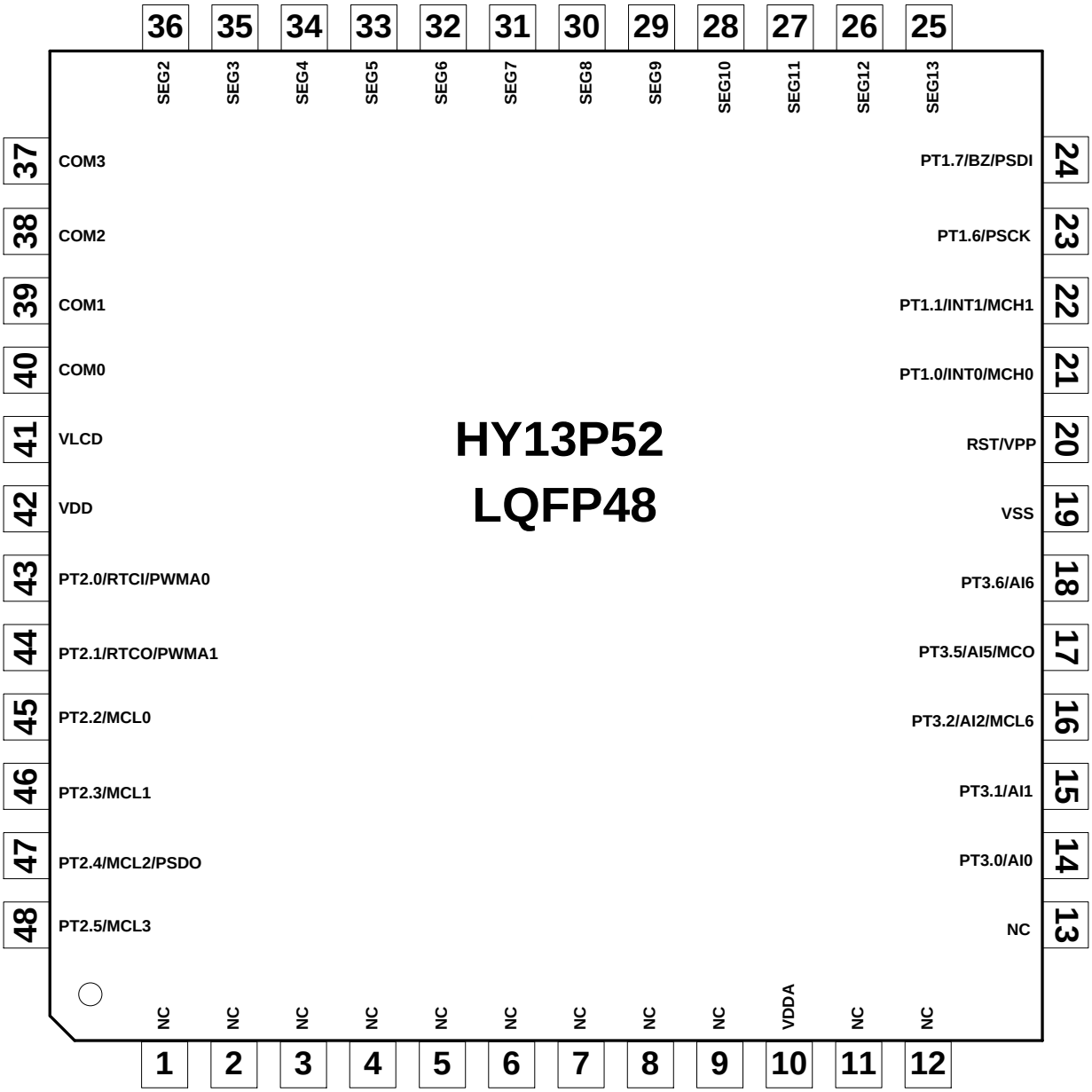


圖 2-1 HY13P52 LQFP48 引腳圖

2.1. LQFP48 引腳定義說明

"I"：輸入,"O"：輸出,"A"：類比, "S"：史密斯觸發, "C"：CMOS I/O,"*"：自定義,"/"：或,"X"：可忽略

引腳		設計		描述
編號	名稱/功能	型式	緩衝	
1	NC	--	-	未使用
2	NC	--	-	未使用
3	NC	--	-	未使用
4	NC	--	-	未使用
5	NC	--	-	未使用
6	NC	--	-	未使用
7	NC	--	-	未使用
8	NC	--	-	未使用
9	NC	--	-	未使用
10	VDDA	P	P	LDO 線性穩壓電源輸出引腳
11	NC	--	-	未使用
12	NC	--	-	未使用
13	NC	--	-	未使用
14	PT3.0 AI0	I/O A	S/C A	數位輸入 / 輸出引腳 類比輸入通道
15	PT3.1 AI1	I/O A	S/C A	數位輸入 / 輸出引腳 類比輸入通道
16	PT3.2 AI2 MCL6	I/O A A	S/C A A	數位輸入 / 輸出引腳 類比輸入通道 多功能比較器信號輸入引腳
17	PT3.5 AI5 MCO	I/O A I/O	S/C A S/C	數位輸入 / 輸出引腳 類比輸入通道 多功能比較器信號輸出引腳
18	PT3.6 AI6	I/O A	S/C A	數位輸入 / 輸出引腳 類比輸入通道
19	VSS	P	P	晶片工作電壓源接地端引腳
20	RST VPP	I P	S P	復位引腳 OTP 燒錄電壓引腳
21	PT1.0 INT0 MCH0	I/O I A	S/C S A	數位輸入 / 輸出引腳 外部中斷源 多功能比較器信號輸入引腳

22	PT1.1	I/O	S/C	數位輸入 / 輸出引腳
	INT1	I	S	外部中斷源
	MCH1	A	A	多功能比較器信號輸入引腳
23	PT1.6	I/O	S	數位輸入 / 輸出引腳
	PSCK	I	S	OTP 讀/寫介面 PSCK 接口
24	PT1.7	I/O	S/C	數位輸入 / 輸出引腳
	BZ	O	S	蜂鳴器輸出
	PSDI	I	S	OTP 讀/寫介面 PSDI 接口
25	SEG13	O	A	LCD 的 SEG 引腳
26	SEG12	O	A	LCD 的 SEG 引腳
27	SEG11	O	A	LCD 的 SEG 引腳
28	SEG10	O	A	LCD 的 SEG 引腳
29	SEG9	O	A	LCD 的 SEG 引腳
30	SEG8	O	A	LCD 的 SEG 引腳
31	SEG7	O	A	LCD 的 SEG 引腳
32	SEG6	O	A	LCD 的 SEG 引腳
33	SEG5	O	A	LCD 的 SEG 引腳
34	SEG4	O	A	LCD 的 SEG 引腳
35	SEG3	O	A	LCD 的 SEG 引腳
36	SEG2	O	A	LCD 的 SEG 引腳
37	COM3	O	A	LCD 的 COM 引腳
38	COM2	O	A	LCD 的 COM 引腳
39	COM1	O	A	LCD 的 COM 引腳
40	COM0	O	A	LCD 的 COM 引腳
41	VLCD	P	P	LCD 的電壓源接引腳
42	VDD	P	P	晶片工作電壓源接引腳
43	PT2.0	I/O	S/C	數位輸入 / 輸出引腳
	PWMA0	O	C	TMB1 的 PWM0 輸出引腳
	RTCI	A	A	外接 RTC 震盪器引腳
44	PT2.1	I/O	S/C	數位輸入 / 輸出引腳
	PWMA1	O	C	TMB1 的 PWM1 輸出引腳
	RTCO	A	A	外接 RTC 震盪器引腳
45	PT2.2	I/O	S/C	數位輸入 / 輸出引腳
	MCL0	A	A	多功能比較器信號輸入引腳
46	PT2.3	I/O	S/C	數位輸入 / 輸出引腳
	MCL1	A	A	多功能比較器信號輸入引腳

47	PT2.4	I/O	S/C	數位輸入 / 輸出引腳
	MCL2	A	A	多功能比較器信號輸入引腳
	PSDO	O	C	OTP 讀/寫介面 PSDO 接口
48	PT2.5	I/O	S/C	數位輸入 / 輸出引腳
	MCL3	A	A	多功能比較器信號輸入引腳

表 2-1 HY13P52 LQFP48 引腳說明

3. 功能概述

3.1. 內部方塊圖

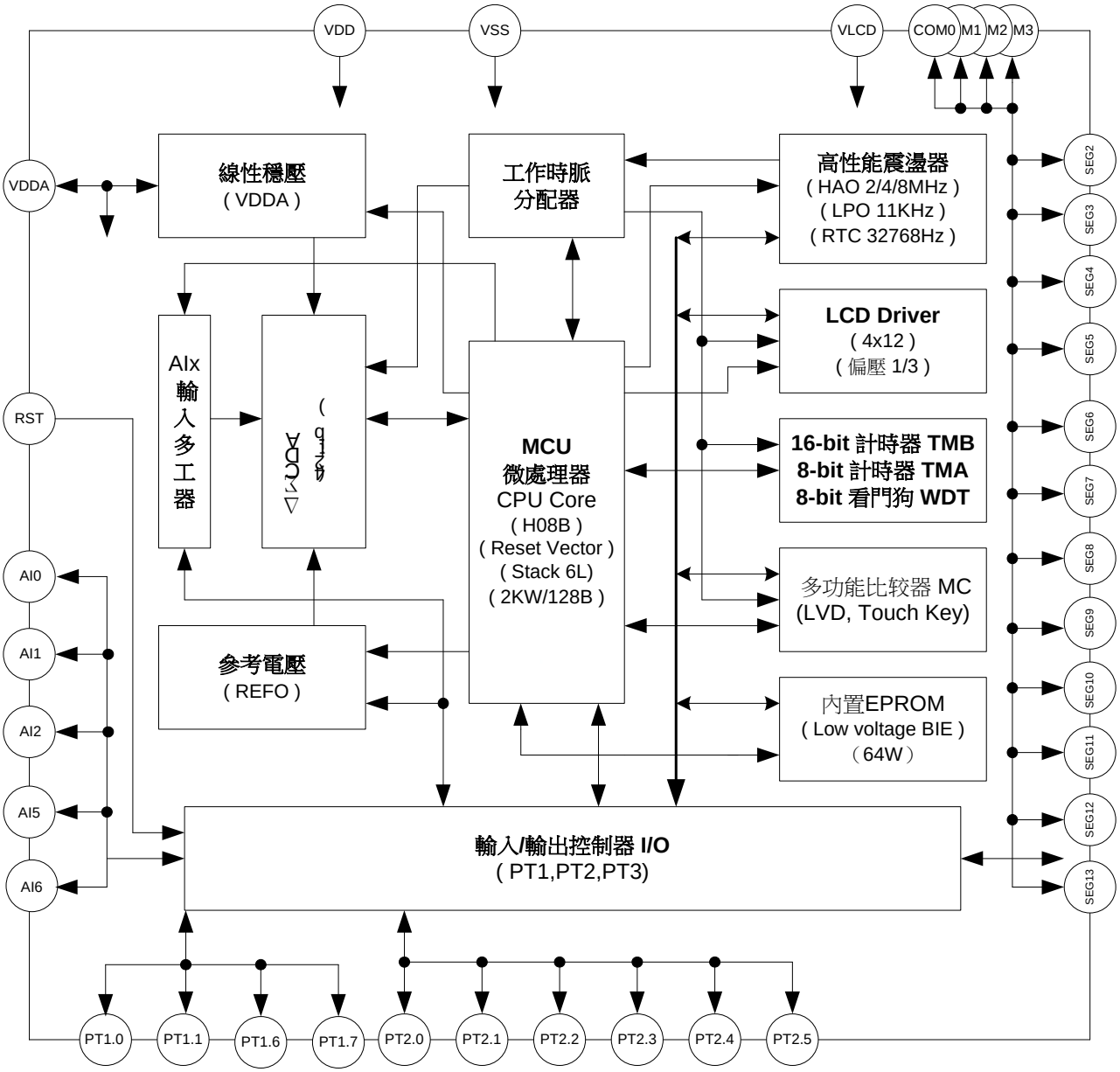
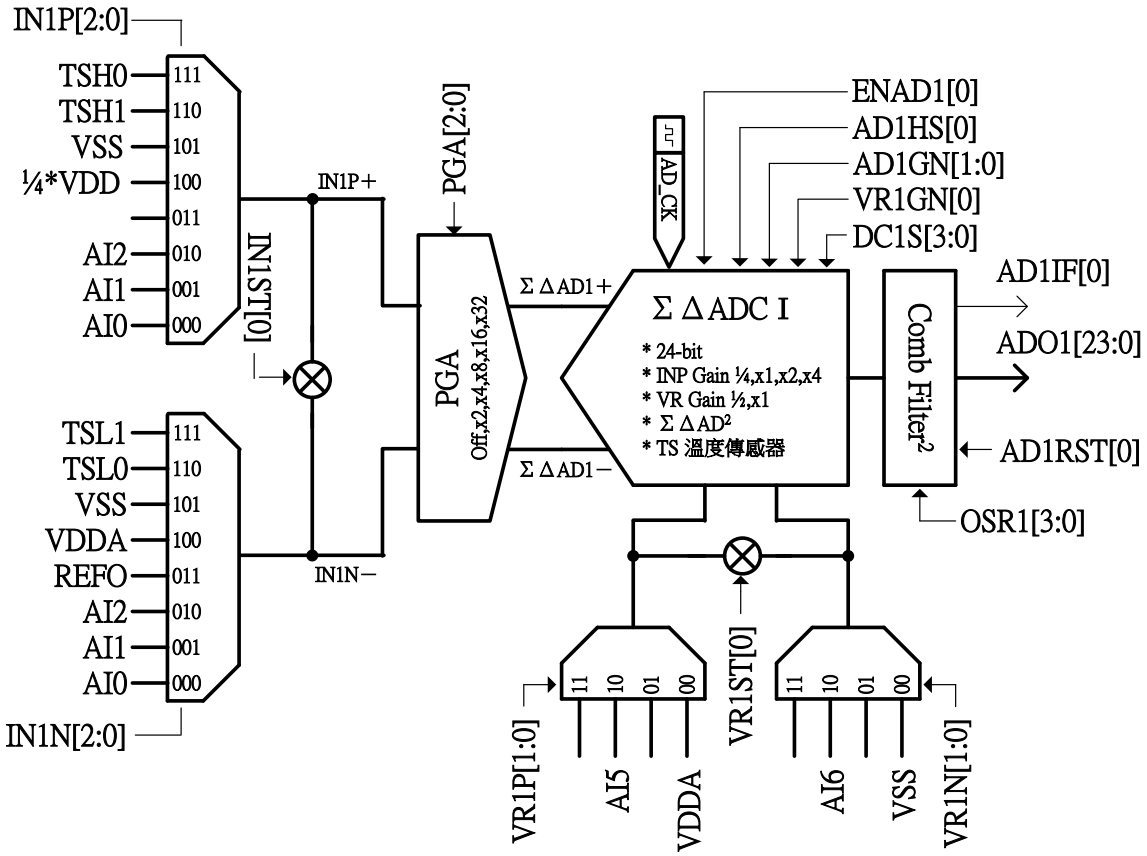


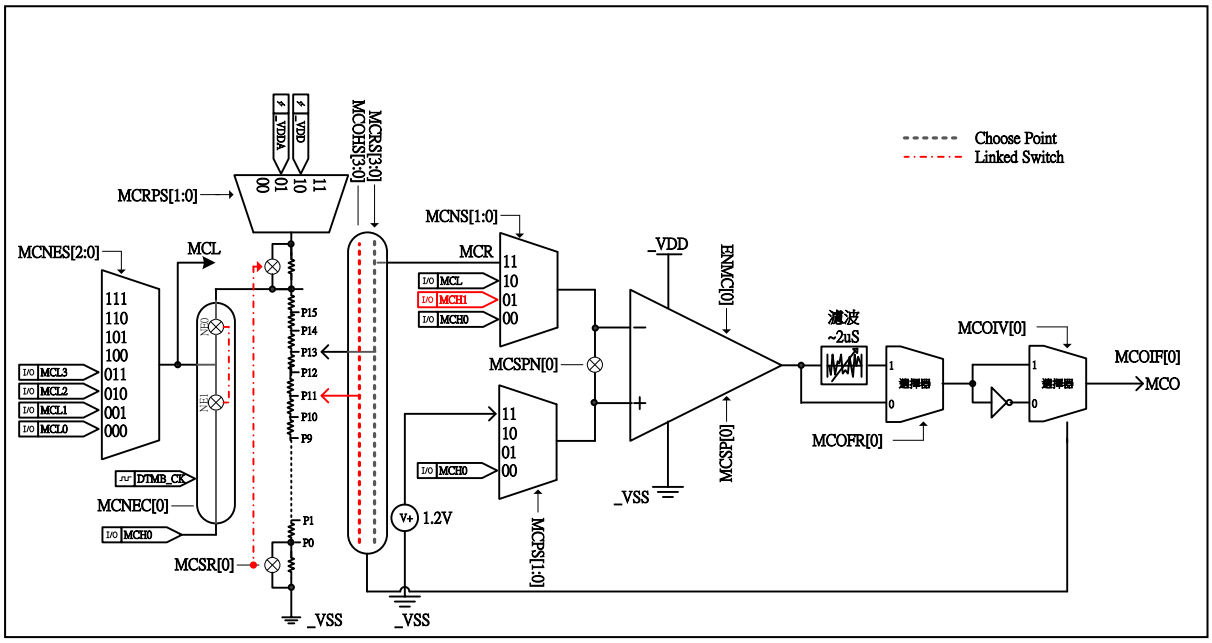
圖 4-1 HY13P52 內部方塊圖

3.2. ΣΔADC Network



※REFO : Internal Reference Voltage

3.3. Comparator Network



4. ΣΔADC Performance

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

HY13P52 針對 ΣΔADC 提供了重要的輸入雜訊規格。下表列出典型的雜訊規格表與 Gain, Output rate, 及單端最大輸入電壓等關係。測試條件設定在外部輸入訊號短路，參考電壓為 1.2V，取樣 1024 筆資料。

ENOB(RMS) with OSR/GAIN at A/D Clock=1Mhz, VDDA=2.4V, VREF=1.2V

Max. Vin(mV) =0.9*VREF (1)	OSR					32	64	128	256	512	1024	2048	4096	8192	16384	32768	65536
	Output rate(HZ)					31250	15625	7813	3906	1953	977	488	244	122	61	31	15
	Gain	=	PGA	×	ADGN												
±1080	1	=	1	×	1	8.6	10.8	13.0	14.7	16.7	17.6	18.1	18.8	19.2	19.7	20.1	20.8
±540	2	=	1	×	2	8.6	10.9	12.8	14.7	16.5	17.5	18.2	18.6	19.0	19.6	20.0	20.6
±270	3	=	1	×	3	8.7	11.0	13.0	14.7	16.5	17.4	18.0	18.5	18.9	19.5	19.8	20.4
±135	4	=	1	×	4	8.6	11.1	12.9	14.7	16.5	17.4	17.9	18.4	18.9	19.3	19.9	20.3
±33.75	32	=	8	×	4	8.6	11.0	12.7	14.2	15.1	15.7	16.3	16.6	17.1	17.6	18.1	18.7
±16.875	64	=	16	×	4	8.6	10.9	12.7	13.9	14.6	15.2	15.7	16.2	16.7	17.3	17.6	18.2
±11.25	96	=	24	×	4	8.6	11.0	12.6	13.8	14.5	15.1	15.5	15.9	16.5	16.9	17.5	18.0
±8.435	128	=	32	×	4	8.6	10.9	12.5	13.6	14.2	14.9	15.2	15.8	16.3	16.9	17.3	17.7

(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).

RMS Noise(uV) with OSR/GAIN at A/D Clock=1Mhz, VDDA=2.4V, VREF=1.2V

Max. Vin(mV) =0.9*VREF	OSR					32	64	128	256	512	1024	2048	4096	8192	16384	32768	65536
	Output rate(HZ)					31250	15625	7813	3906	1953	977	488	244	122	61	31	15
	Gain	=	PGA	×	ADGN												
±1080	1	=	1	×	1	6208	1317	301	89.6	22.9	12.3	8.34	5.30	4.01	2.91	2.09	1.35
±540	2	=	1	×	2	3067	612	165	45.7	12.6	6.41	4.08	3.01	2.29	1.53	1.11	0.78
±270	3	=	1	×	3	1937	388	99.9	30.3	8.50	4.59	3.13	2.23	1.60	1.07	0.88	0.56
±135	4	=	1	×	4	1508	279	77.3	22.9	6.42	3.57	2.44	1.78	1.27	0.93	0.62	0.47
±33.75	32	=	8	×	4	195	37.4	11.2	3.87	2.18	1.44	0.95	0.76	0.52	0.38	0.27	0.18
±16.875	64	=	16	×	4	97	19.8	5.8	2.49	1.51	0.99	0.71	0.52	0.36	0.23	0.19	0.13
±11.25	96	=	24	×	4	62	12.4	4.2	1.80	1.09	0.74	0.53	0.41	0.26	0.20	0.14	0.10
±8.435	128	=	32	×	4	48	9.6	3.2	1.50	0.99	0.62	0.48	0.32	0.24	0.16	0.12	0.09

ENOB(RMS) with OSR/GAIN at A/D Clock=0.25Mhz, VDDA=2.4V, VREF=1.2V

Max. Vin(mV) =0.9*VREF (1)	OSR					32	64	128	256	512	1024	2048	4096	8192	16384	32768	65536
	Output rate(HZ)					7813	3906	1953	977	488	244	122	61	31	15	8	4
	Gain	=	PGA	×	ADGN												
±1080	1	=	1	×	1	8.7	11.0	12.9	14.5	16.4	17.5	18.1	18.7	19.1	19.6	19.8	20.0
±540	2	=	1	×	2	8.7	10.9	13.0	14.7	16.5	17.3	17.9	18.4	19.1	19.5	20.0	20.2
±270	3	=	1	×	3	8.7	11.0	13.0	14.8	16.5	17.3	17.8	18.4	18.9	19.2	19.5	19.4
±135	4	=	1	×	4	8.7	11.1	13.0	14.6	16.4	17.3	17.6	18.3	18.7	19.3	19.7	19.9
±33.75	32	=	8	×	4	8.7	10.8	12.9	14.1	15.2	15.6	16.1	16.6	17.2	17.5	18.1	18.6
±16.875	64	=	16	×	4	8.7	11.0	12.7	13.9	14.8	15.1	15.7	16.1	16.7	17.2	17.8	18.0
±11.25	96	=	24	×	4	8.7	11.0	12.5	13.7	14.4	15.1	15.5	15.9	16.4	17.0	17.5	18.0
±8.435	128	=	32	×	4	8.7	10.9	12.6	13.7	14.3	14.7	15.3	15.8	16.2	16.9	17.2	17.8

RMS Noise(uV) with OSR/GAIN at A/D Clock=0.25Mhz, VDDA=2.4V, VREF=1.2V

Max. Vin(mV) =0.9*VREF	OSR					32	64	128	256	512	1024	2048	4096	8192	16384	32768	65536
	Output rate(HZ)					7813	3906	1953	977	488	244	122	61	31	15	8	4
	Gain	=	PGA	×	ADGN												
±1080	1	=	1	×	1	5709	1186	320	102.9	28.8	12.6	8.40	5.80	4.29	2.94	2.67	2.33
±540	2	=	1	×	2	2887	650	151	46.3	13.2	7.54	4.79	3.42	2.21	1.58	1.17	0.97
±270	3	=	1	×	3	1953	401	100.2	29.1	8.85	4.95	3.41	2.39	1.66	1.36	1.12	1.15
±135	4	=	1	×	4	1495	274	75.7	24.5	7.14	3.85	2.94	1.87	1.39	0.96	0.73	0.62
±33.75	32	=	8	×	4	175	41.9	10.1	4.34	2.07	1.48	1.06	0.77	0.48	0.40	0.27	0.19
±16.875	64	=	16	×	4	92	18.1	5.5	2.46	1.30	1.07	0.69	0.52	0.34	0.25	0.17	0.14
±11.25	96	=	24	×	4	59	12.4	4.4	1.90	1.15	0.73	0.53	0.42	0.28	0.19	0.13	0.10
±8.435	128	=	32	×	4	46	9.9	3.1	1.46	0.96	0.70	0.46	0.33	0.24	0.15	0.12	0.08

The RMS noise are referred to the input. The Effective Number of Bits (ENOB(RMS)) is defined as:

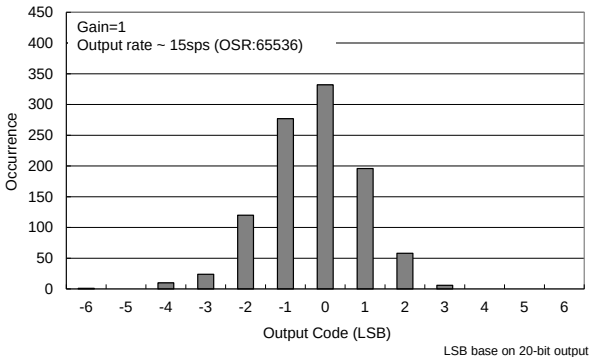
$$\text{ENOB(RMS)} = \ln\left(\frac{\text{FSR}}{\text{RMS Noise}}\right) \Big/ \ln(2)$$

$$\text{RMS Noise} = \left(2 \times \text{VREF} \times \sqrt{\sum_{k=1}^{1024}\left(\text{ADO}[k] - \text{Average}\right)^2}\right) \Big/ 2^{24}$$

$$\text{Where FSR (Full - Scale Range)} = 2 \times \text{VREF/Gain.}$$

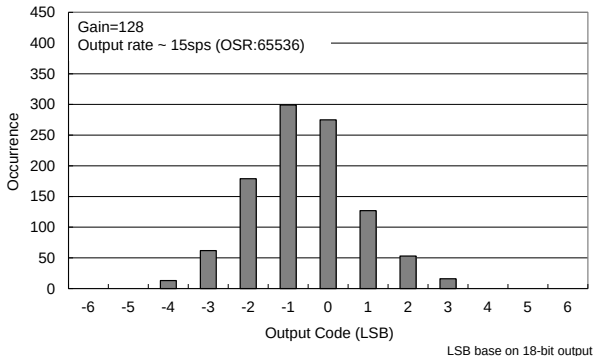
$$\text{Average} = \frac{\sum_{k=1}^{1024}(\text{ADO}[k])}{1024}$$

RMS Noise Diagram



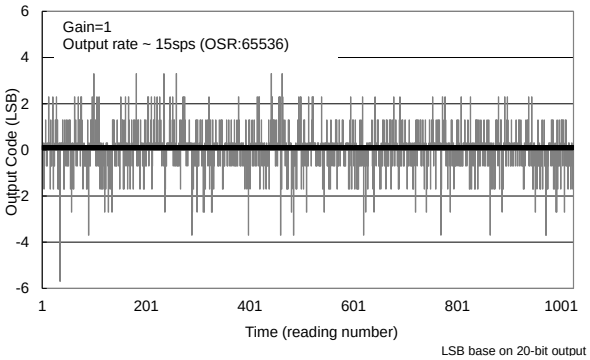
LSB base on 20-bit output

RMS Noise Diagram



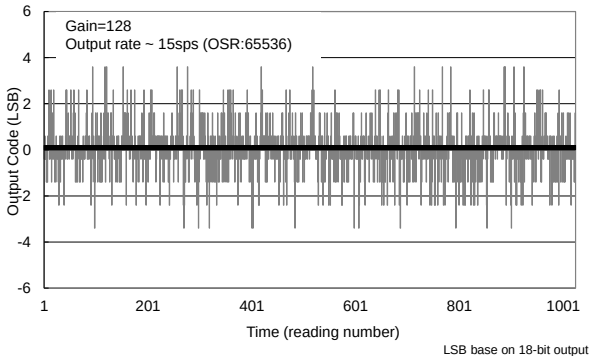
LSB base on 18-bit output

RMS Noise Diagram



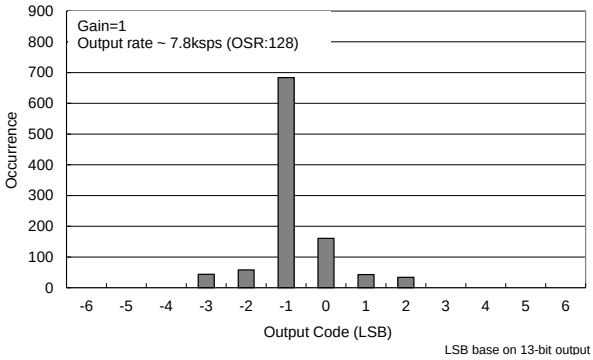
LSB base on 20-bit output

RMS Noise Diagram



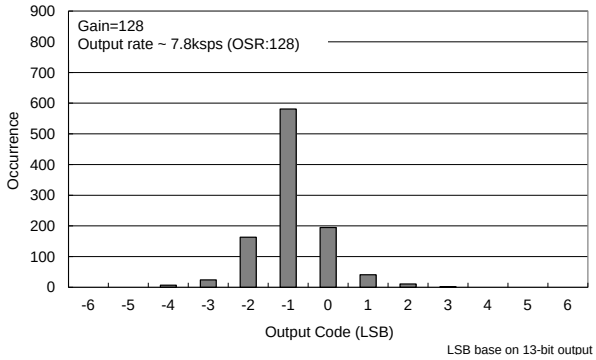
LSB base on 18-bit output

RMS Noise Diagram



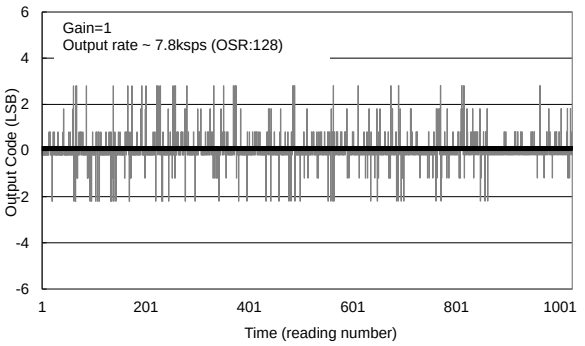
LSB base on 13-bit output

RMS Noise Diagram



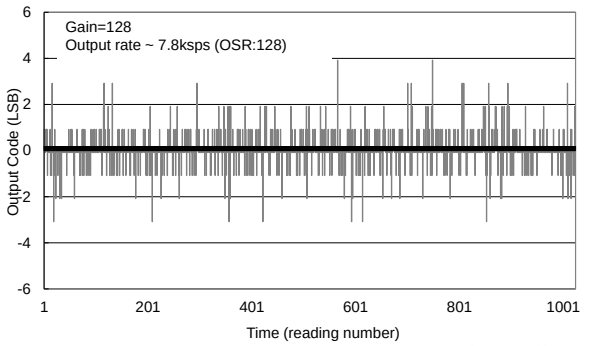
LSB base on 13-bit output

RMS Noise Diagram



LSB base on 13-bit output

RMS Noise Diagram



LSB base on 13-bit output

5. 暫存器列表

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
000h	INDF0	Contents of FSR0 to address data memory - value of FSR0 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
001h	POINC0	Contents of FSR0 to address data memory - value of FSR0 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
002h	PODEC0	Contents of FSR0 to address data memory - value of FSR0 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
003h	PRINC0	Contents of FSR0 to address data memory - value of FSR0 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
004h	PLUSW0	Contents of FSR0 to address data memory - value of FSR0 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
010h	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
011h	FSR0H	Indirect Data Memory Address Pointer 0 High Byte,FSR0[8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
018h	SKCN	SKFL	SKUN	SKOV	-	-	SKPRT[2:0]			000. .000	u$$. .$$$	rw 0,rw 0,rw 0,- -,*,*
01Ah	PCLATH	-	-	-	-	PC[11]	PC[10]	PC[9]	PC[8]	.... .0000	 0000	-,-,-,- *,*,*
01Bh	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	*,*,*,*,*,*,*,*
023h	INTE0	GIE	-	MCOIE	WDTIE	TB1IE	TMAIE	E1IE	E0IE	0000 0000	0uuu uuuu	*,*,*,*,*,*,*,*
024h	INTE1	-	AD1IE	-	-	-	-	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
026h	INTF0	-	-	MCOIF	WDTIF	TB1IF	TMAIF	E1IF	E0IF	.000 0000	.uuu uuuu	*,*,*,*,*,*,*,*
027h	INTF1	-	AD1IF	-	-	-	-	-	-	0000 0000	uuuu uuuu	*,*,*,* r,r,*,*
029h	WREG	Working Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
02Bh	MSTAT	-	-	-	C	DC	N	OV	Z	...x xxxx	...u uuuu	-,-,-,-,*,*,*,*
02Ch	PSTAT	POR	PD	TO	IDL	RST	SKERR	MCO	-	$000 $00.	uu$u u$u.	rw 0,rw 0,rw 0,rw 0 rw 0,rw 0,rw 0,-
02Eh	BIECN	-	-	-	-	VPPHV	-	BIEWR	BIERD	1... $.00	1... $.uu	r1,-,-,- r,-,*,*
02Fh	BIEARH	ENBIE	-	-	-	12-bit look-up Table as BIEAH[3:0]				0... xxxx	u... uuuu	*,-,-,- *,*,*,*
030h	BIEARL	BIE Address Register as BIEAL[5:0] or 12-bit look-up Table as BIEA[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
031h	BIEDRH	BIE High Byte Data Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
032h	BIEDRL	BIE Low Byte Data Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
033h	PWRCN	ENLDO[1:0]		VDDAX[1:0]		ENREFO	-	AD1RST	CSFON	0000 0000	uuuu u00u	*,*,*,* *,w r0,w r0,*
034h	OSCCN0	OSCS[1:0]		DHS[1:0]		DMS[2:0]			CUPS	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
035h	OSCCN1	LCPS[1:0]		DADC[1:0]		DTMB[1:0]		TMBS	-	0000 0000	uuuu uuu.	*,*,*,*,*,*,*,-
036h	OSCCN2	RTC_EN	-	-	-	HAOM[1:0]		ENHAO	LPO	.000 0011	.uuu uu11	.,*,*,*,*,*,*,r
037h	WDTCN	ENBZ	BZS	BZ[1:0]		ENWDT	DWDT[2:0]			0000 0000	uuuu $000	-,*,*,* rw 1,*,*,*
038h	TMACN	ENTMA	TMACL	TMAS	DTMA[2:0]			-	-	0000 00..	u0uu uu..	*,rw 1,*,*,*,-,-
039h	TMAR	TMA counter Register								0000 0000	uuuu uuuu	rw 0,rw 0,rw 0,rw 0 rw 0,rw 0,rw 0,rw 0
03Ah	AD1CN0	-	-	ENAD1	AD1HS	IN1ST	VR1ST	AGND1S	CHOP1	..00 0000	..uu uuuu	-,-,*,*,*,*,*,*
03Bh	AD1CN1	IN1P[2:0]			IN1N[2:0]			AD1GN[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
03Ch	AD1CN2	DC1S[3:0]				VR1P[1:0]		VR1N[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
03Dh	AD1CN3	OSR1[3:0]				PGA[2:0]			VR1GN	000. 0000	uuu. uuuu	*,*,*,- *,*,*,*
03Eh	AD1H	ADC1 conversion high byte data register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
03Fh	AD1M	ADC1 conversion middle byte data register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
040h	AD1L	ADC1 conversion low byte data register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
041h	CSFCN0	SKRST		HAOTR[5:0]						0.10 0000	u.uu uuuu	*,-,*,*,*,*,*,*
042h	CSFCN1					PWMAO	MCOO	I2CO	BZO	 0000	.... uuuu	-,-,-,- *,*,*,*
04Bh	MCCN0	ENMC	MCLP	MCSR	MCSPN	MCPS[1:0]		MCNS[1:0]		0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
04Ch	MCCN1	MCNES[2:0]			MCRPS[1:0]		MCNEC	MCOFR	MCOIV	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
04Dh	MCCN2	MCRS[3:0]				MCRS[3:0]				0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
04Eh	TB1Flag			PWM6A	PWM5A	PWM4A	PWM3A	PWM2A	PWM1A	..00 0000	..uu uuuu	-,-,r,r r,r,r,r
04Fh	TB1CN0	ENTB1	TB1M[1:0]		TB1RT[1:0]		TB1CL	TC2ED	TC1ED	0000 0000	uuuu u0uu	*,*,*,*,*,rw 1,*,*
050h	TB1CN1	PA1IV	PWMA1[2:0]			PA0IV	PWMA0[2:0]			0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
051h	TB1RH	TimerB1 counter Register [15:8]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
052h	TB1RL	TimerB1 counter Register [7:0]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
053h	TB1C0H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
054h	TB1C0L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
055h	TB1C1H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
056h	TB1C1L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
057h	TB1C2H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
058h	TB1C2L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W
070h	PT1	PT17	PT16	-	-	-	-	PT11	PT10	xx.. ..xx	xx.. ..xx	*,*,-,- -,-,*,*
071h	TRISC1	TC17	TC16	-	-	-	-	TC11	TC10	0000 0000	uuuu uuuu	*,*,-,- -,-,*,*
072h	PT1DA	-	-	-	-	-	-	DA11	DA10	0000 0000	uuuu uuuu	-,-,-,- *,-,*,*
073h	PT1PU	PU17	PU16	-	-	-	-	PU11	PU10	0000 0000	uuuu uuuu	*,*,-,- -,-,*,*
074h	PT1EG	-	-	-	-	E1EG[1:0]		E0EG[1:0]		 0000	.... uuuu	-,-,-,- *,*,*,*
075h	PT2	-	-	PT25	PT24	PT23	PT22	PT21	PT20	xx	xx	-,-,-,- -,-,*,*
076h	TRISC2	-	-	TC25	TC24	TC23	TC22	TC21	TC20	00	.... ..uu	-,-,-,- -,-,*,*
077h	PT2DA	-	-	DA25	DA24	DA23	DA22	FPWMA1	FPWMA0	00	.... ..uu	-,-,-,- -,-,*,*
078h	PT2PU	-	-	PU25	PU24	PU23	PU22	PU21	PU20	00	.... ..uu	-,-,-,- -,-,*,*
079h	PT3	-	-	PT35	PT34	PT33	PT32	PT31	PT30	..xx xxxx	..xx xxxx	-,-,*,*,*,*,*,*
07Ah	TRISC3	-	TC36	TC35	-	-	TC32	TC31	TC30	..00 0000	..uu uuuu	-,-,*,*,*,*,*,*
07Bh	PT3DA	-	DA36	DA35	-	-	DA32	DA31	DA30	..00 0000	..uu uuuu	-,-,*,*,*,*,*,*
07Ch	PT3PU	-	PU36	PU35	-	-	PU32	PU31	PU30	..00 0000	..uu uuuu	-,-,*,*,*,*,*,*
080h ~ 017Fh		General Purpose Register as 256Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*
180h	LCDCN1	ENLCD	LCDPR	VLCD[1:0]		LCDBF	-	-	-	0000 00..	uuuu uu..	*,*,*,*,*,*,-,-
181h	LCDCN2	LCDBL	LCDMX[1:0]		LCDS	DLCD[1:0]		-	-	0000 00..	uuuu uu..	*,*,*,*,*,*,-,-
182h	LCD0	Segment SEG2@[3:0] and SEG3@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
183h	LCD1	Segment SEG4@[3:0] and SEG5@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
184h	LCD2	Segment SEG6@[3:0] and SEG7@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
185h	LCD3	Segment SEG8@[3:0] and SEG9@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
186h	LCD4	Segment SEG10@[3:0] and SEG11@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
187h	LCD5	Segment SEG12@[3:0] and SEG13@[7:4] data register of LCD								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*

6. 電器特性

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at V_{DD} to V_{SS} . . . . . −0.2 V to 4.0 V

Voltage applied to any pin (see Note 1) . . . . . −0.2 V to V_{DD} + 0.3 V

Voltage applied to RST/VPP pin . . . . . −0.2 V to 6.9 V

Voltage applied to TST pin (see Note 1) . . . . . −0.2 V to VDD + 1V

Diode current at any device terminal . . . . . ±2 mA

Storage temperature, Tstg: (unprogrammed device) . . . . . −55℃ to 150℃

(programmed device) . . . . . −40℃ to 85℃

Total power dissipation 0.5w

Maximum output current sink by any PORT1 to PORT3 I/O pin. 25mA

6.1. Recommended operating conditions

T_A = -40℃ ~ 85℃,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{DD}	Supply Voltage	All digital peripherals and CPU	2.2		3.6	V
		Analog peripherals	2.4		3.6	
V_{SS}	Supply Voltage		0		0	
RTC	External Oscillator Frequency	V_{DD} = 2.2V,ENRTC[0]=1		32.768K		HZ

.

6.2. Internal RC Oscillator

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
IRCH	High Speed Oscillator frequency	ENHAO[0]=1, HAOM[1:0]=00b		2.0		MHz
		ENHAO[0]=1, HAOM[1:0]=01b		3.7		MHz
		ENHAO[0]=1, HAOM[1:0]=11b		6.8		MHz
IRCL	Low Power Oscillator frequency			11.5		KHz

6.3. Supply current into VDD excluding peripherals current

T_A = 25℃,V_{DD} = 3.0V,OSC_LPO = 11KHz,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM1}	Active mode 1	OSC_CY =off, OSC_HAO = 8MHz, CPU_CK = 8MHz		0.9	2	mA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO = 4MHz, CPU_CK = 4MHz		0.5	1	mA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 2MHz		0.27	0.5	mA
I_{AM4}	Active mode 4	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 1MHz		0.15	0.3	mA
I_{LP1}	Low Power 1	OSC_CY = 32768Hz, OSC_HAO = off, CPU_CK = 32768Hz		7	12	uA
I_{LP2}	Low Power 2	OSC_CY = 32768Hz, OSC_HAO = off, CPU_CK = 16384Hz		5	10	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		2	4	uA
I_{LP4}	Low Power 4	Sleep state		0.7	1.2	uA

OSC_CY：External Oscillator frequency.

OSC_HAO：Internal High Accuracy Oscillator frequency.

CPU_CK：CPU core work frequency.

6.4. Port1~3

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				2.1	V
V_{IL}	Low-Level input voltage		0.9			
V_{hys}	Input Voltage hysteresis(VIH - VIL)			0.8		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance			200		kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	I_{OH}=10mA	V_{DD} -0.3			V
V_{OL}	Low-level output voltage	I_{OL}=-10mA			VSS +0.3	

6.5. Reset(Brownout, External RST pin, Low Voltage Detect)

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
BOR	Pulse length needed to accepted reset internally, t_{d-LVR}		2			us
	V_{DD} Start Voltage to accepted reset internally (L➔H),V_{LVR}		1.8	1.9	2.0	V
	Hysteresis, $V_{HYS-LVR}$			35		mV
RST	Pulse length needed as RST/VPP pin to accepted reset internally, t_{d-RST}		2			us
	Input Voltage to accepted reset internally		0.9			V
	Hysteresis, $V_{HYS-RST}$			0.8		V

BOR：Brownout Reset. LVD：Low Voltage Detect. LVR：Low Voltage Reset of BOR. RST：External Reset pin

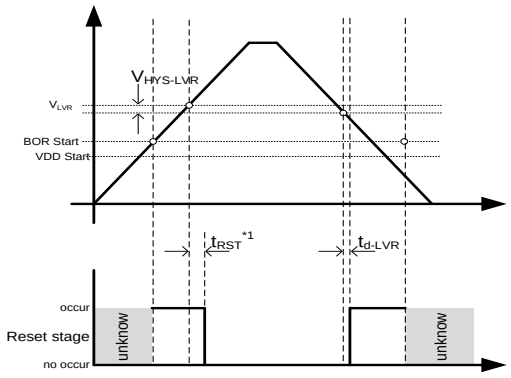


Figure BOR reset diagram

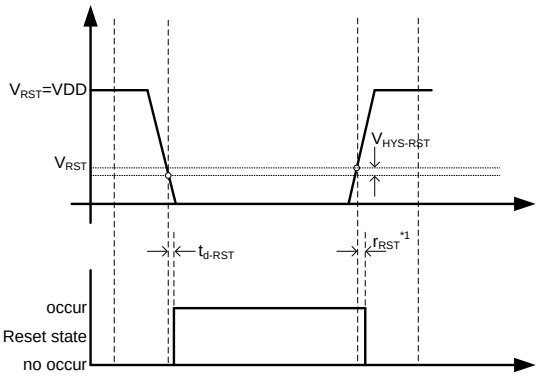


Figure RST reset diagram

6.6. Power System

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
VDDA	VDDA operation current, I_{VDDA}	I_L = 0mA	ENLDO[1:0]=11b		11		uA
	Select VDDA output voltage	I_L = 0.1mA, VDD≧VDDA+0.2V	VDDAX[1:0]=00b		2.4		V
			VDDAX[1:0]=01b		2.7		V
			VDDAX[1:0]=10b		3.0		V
			VDDAX[1:0]=11b		3.3		V
	Dropout voltage	I_L = 10mA	VDDAX[2:0]=00b		120		mV
			VDDAX[2:0]=01b		130		mV
			VDDAX[2:0]=10b		140		mV
			VDDAX[2:0]=11b		160		mV
	Temperature drift	VDDX[1:0]=11b	T_A=-40℃~85℃		50		ppm/℃
	V_{DD} Voltage drift	I_L = 0.1mA	V_{DD}=2.5V~3.6V		±0.2		%/V
REFO	REFO operation current, I_{REFO}	I_L = 0mA			20		uA
	Internal REFO voltage ,V_{REFO}	ENREFO[0]=1	I_L = 0uA		1.2		V
	Temperature drift	ENREFO[0]=1, I_L = 10uA	T_A=-40℃~85℃		50		ppm/℃
	VDDA Voltage drift				150		uV/V

VDDA：Adjust Voltage Regulator

REFO：Internal Reference Voltage

6.7. LCD

T_A = 25℃,V_{DD} = 3.0V, C_{VLCD} =1uF,unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
I_{LCD}	Operation supply current without output buffer.	LCDPR[0]=1	V_{DD} = 2.2V		11		uA
			V_{DD} = 3.0V				
VLCD	Supply Voltage at VLCD pin	LCDPR[0]=0		2.2		3.6	V
	Embedded Charge Pump output voltage at VLCD pin	V_{DD} = 2.2V, LCDPR[0]=1, C_{VLCD} =1uF	VLCDX[1:0]=11b	-10%	2.55	+10%	V
			VLCDX[1:0]=10b	-10%	2.75	+10%	
			VLCDX[1:0]=01b	-10%	2.95	+10%	
			VLCDX[1:0]=00b	-10%	3.25	+10%	
Z_{LCD}	Output impedance with LCD buffer	f_{LCD} =178Hz,VLCD=2.9V			10		kΩ

6.8. Multi-Comparator

T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{MC}	Operation supply current	ENMC[0]=1, MCLP[0]=1b		5		uA
	Low Power Mode	ENMC[0]=1, MCLP[0]=0b		1		
V_{IC}	Common-mode input voltage		0		V_{DD}-1	V
V_{OS}	Offset voltage		-5		5	mV
V_{hys}	Input hysteresis		0	0.7	1.5	mV
V_{REF}	Reference Voltage	MCPS[1:0]=11b	1.1	1.2	1.3	V
	Temperature Drift	MCPS[1:0]=11b		50		ppm/℃
	VDD Voltage drift	MCPS[1:0]=11b		±2		%/V
I_R	Multi-node resistor current	MCSR[0]=0b		10		uA
		MCSR[0]=1b		30		
LVD	ENLDO[1:0]=11b,MCPS[1:0]=11b,MCSR[0]=0b,MCRS[3:0]=0011b		-0.1	3.2	+0.1	V
	ENLDO[1:0]=11b,MCPS[1:0]=11b,MCSR[0]=0b,MCRS[3:0]=0100b		-0.1	3.0	+0.1	
	ENLDO[1:0]=11b,MCPS[1:0]=11b,MCSR[0]=0b,MCRS[3:0]=0101b		-0.1	2.9	+0.1	
	ENLDO[1:0]=11b,MCPS[1:0]=11b,MCSR[0]=0b,MCRS[3:0]=0110b		-0.1	2.7	+0.1	
	ENLDO[1:0]=11b,MCPS[1:0]=11b,MCSR[0]=0b,MCRS[3:0]=0111b		-0.1	2.6	+0.1	
	ENLDO[1:0]=11b,MCPS[1:0]=11b,MCSR[0]=0b,MCRS[3:0]=1000b		-0.1	2.5	+0.1	
	ENLDO[1:0]=11b,MCPS[1:0]=11b,MCSR[0]=0b,MCRS[3:0]=1001b		-0.1	2.4	+0.1	
	ENLDO[1:0]=11b,MCPS[1:0]=11b,MCSR[0]=0b,MCRS[3:0]=1010b		-0.1	2.3	+0.1	
	ENLDO[1:0]=11b,MCPS[1:0]=11b,MCSR[0]=0b,MCRS[3:0]=1011b		-0.1	2.2	+0.1	
	ENLDO[1:0]=11b,MCPS[1:0]=11b,MCSR[0]=0b,MCRS[3:0]=1100b		-0.1	2.1	+0.1	
	ENLDO[1:0]=11b,MCPS[1:0]=11b,MCSR[0]=0b,MCRS[3:0]=1101b		-0.1	2.0	+0.1	
	MCRS[3:0]=0000b~0010b, and 1110b~1111b (reserved)			-		

LVD：Low Voltage Detect.　Note：當 MCPS[1:0]=11b 的時候，代表選擇到 VREF，則 LVD 上下限規格為 0.1V

6.9. ΣΔADC, Power Supply and Recommended operating conditions

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{SD18}	Supply Voltage at VDDA		2.4		3.6	V
f_{SD18}	Modulator sample frequency, ADC_CK		125	250	1000	KHz
	Over Sample Ratio, OSR		32		65536	
f_{ADC_CK}	High Power mode	AD1HS[0]=1b	0.5		1.0	MHz
	Low Power mode	AD1HS[0]=0b	0.125		0.5	MHz

6.9.1. Operating Current

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

Parameter	Test Conditions	Min.	Typ.	Max.	unit
Analog Supply Current I, ADC_CK= 1000KHz,OSR=65536, AD1HS[0]=1b, f_{DATA} = 15SPS	VDDA=2.4V, Gain=1		250		μA
	VDDA=2.4V, Gain=128@PGA=x32		850		μA
Analog Supply Current II, ADC_CK= 250KHz,OSR=65536, AD1HS[0]=0b, f_{DATA} = 4SPS	VDDA=2.4V, Gain=1		120		μA
	VDDA=2.4V, Gain=128@PGA=x32		550		μA

6.9.2. Analog Inputs

T_A = –40°C to +85°C,V_{DD} = 3.0V, VDDA=2.4V, PGA*Gain=128,unless otherwise noted

Parameter	Test Conditions	Min.	Typ.	Max.	unit
Full-Scale Input Voltage(VINP – VINN)	VREF =VDDA,		±0.5*VREF/(Gain*PGA)		V
Full-Scale Input Voltage(VINP – VINN)	VREF =1V,		±0.9*VREF/(Gain*PGA)		V
Negative Signal Input (VINN)		VSSA-0.2		VDDA+0.2	V
Positive Signal Input (VINP)		VSSA-0.2		VDDA+0.2	V
Common-Mode Input Range		VSSA-0.2		VDDA+0.2	V

6.9.3. Performance

T_A = –40°C to +85°C,V_{DD} = 3.0V, VDDA=2.4V, PGA*Gain=128,unless otherwise noted

Parameter	Test Conditions	Min.	Typ.	Max.	unit
Data Rate	ADC_CK=1000KHz, OSR=32, AD1HS [0]=1b		31,250		SPS
	ADC_CK=1000KHz, OSR=65536, AD1HS [0]=1b		15		SPS
	ADC_CK=500KHz, OSR=32, AD1HS [0]=1b		15,625		SPS
	ADC_CK=500KHz, OSR=65536, AD1HS [0]=1b		7.5		SPS

	ADC_CK=250KHz, OSR=32, AD1HS [0]=0b		7,812		SPS
	ADC_CK=250KHz, OSR=65536, AD1HS [0]=0b		3.8		SPS
Digital Filter Settling Time	Full Settling		3		Conversions
Integral Nonlinearity (INL)	Differential Input, End-Point Fit, G = 1,VIN=0.9*VR, delta VR~1.2V		±30	±100	ppm
Input Offset Error	Gain=1,		±50		ppm of FS
	Gain=128,		±5		ppm of FS
Input Offset Drift	Gain=1		2		uV/°C
	Gain=128		4		nV/°C
Gain Drift	Input common voltage=VDDA		5		ppm/°C
	Input common voltage=VDDA/2		5		ppm/°C
AC power supply rejection ratio	VDD=3V±100mV,	Gain = 1,	>80		dB
	f_{VDD}=50Hz,60Hz ± 1Hz	Gain = 128	>70		dB
Common-Mode Rejection	at DC, Input Voltage=VDDA/2± 0.1V		>75		dB
Power-Supply Rejection	at DC,VDDA=3V±100mV, Gain=1		60		dB
	at DC,VDDA=3V±100mV, Gain=128		95		dB

6.9.4. Voltage Reference

T_A = –40°C to +85°C,V_{DD} = 3.0V, VDDA=2.4V, PGA*Gain=128,unless otherwise noted

Parameter	Test Conditions	Min.	Typ.	Max.	unit
Voltage Reference Input (VREF)	VREF = REFP – REFN			VDDA	V
Negative Reference Input (REFN)		VSS-0.1		VDDA/2	V
Positive Reference Input (REFP)		VDDA/2		VDDA+0.1	V
Reference Voltage (V12)	IN1N[2:0]=011b, or VR1P[1:0]=01b, or VR1N[1:0]=01b		1.2		V

6.9.5. Temperature sensor

T_A = 25℃,V_{DD} = 3.0V, VDDA=3.3V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
TC_{Sensor}	Sensor temperature drift			178		uV/℃
KT	Absolute Temperature Scale 0°K	Gain = 1,VREF=VDDA/2		-289		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~85℃		±2		℃

6.10. Build-In EPROM(BIE)

T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
T_O	Operation temperature range		0	25	40	℃
$V_{VPP-BIE}$	Supply Voltage	ENBIE[0]=1,BIELV[0]=0		6.0	6.5	V
	Low Supply Voltage	ENBIE[0]=1,BIELV[0]=1	2.75			V
I_{BIE}	Operation supply current			5		mA
V_{SS}	Supply Voltage			0		V

當使用外部V_{BIE}電源燒錄BIE區塊時，可以透過指令一次燒錄一個字節(word)資料於BIE區塊內; BIELV[0]=0

當使用 2.75V 低壓燒錄控制電路時，則不需外接 VBIE 電源仍可燒錄 BIE 區塊.

7. 修訂記錄

以下描述本文件差異較大的地方，而標點符號與字形的改變不在此描述範圍。

版本	頁次	變更摘要
V01	All	初版文件;
V02	All	REFO 敘述修正
	14~15	更新暫存器列表
V03	5~7	OTP 燒錄腳位描述 PSDI 與 PSCK 分別從 Pin22 與 Pin21 更正為 Pin24 與 Pin23
V04	15	移除 VLCD 暫存器 LCDCN1 的控制位元 LCDTE
	19	移除 LVD 描述
	21	修正 VLCD 規格描述
	22	新增 LVD 描述與上下限規格