



HY12P63
Datasheet
DMM Specialized IC
Embedded Digital T-RMS

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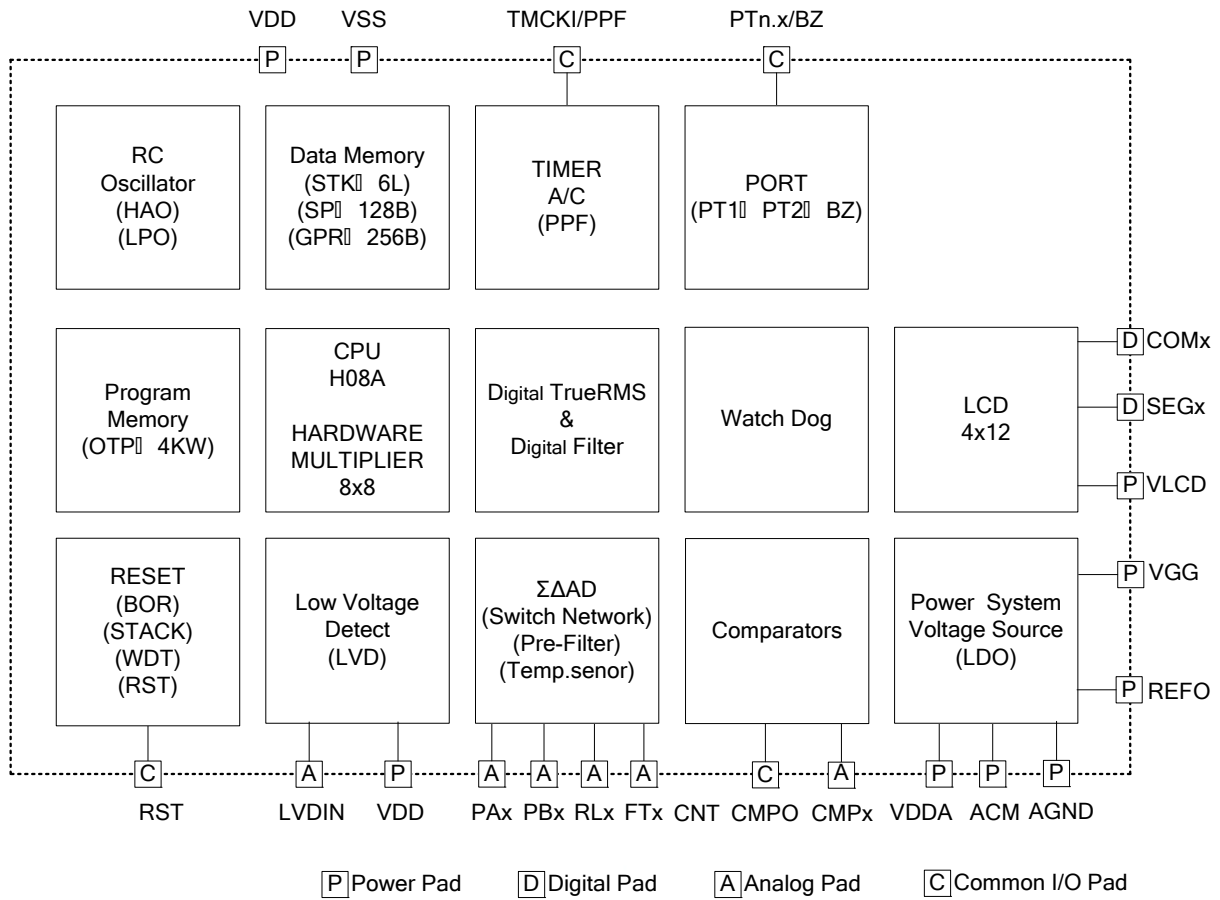
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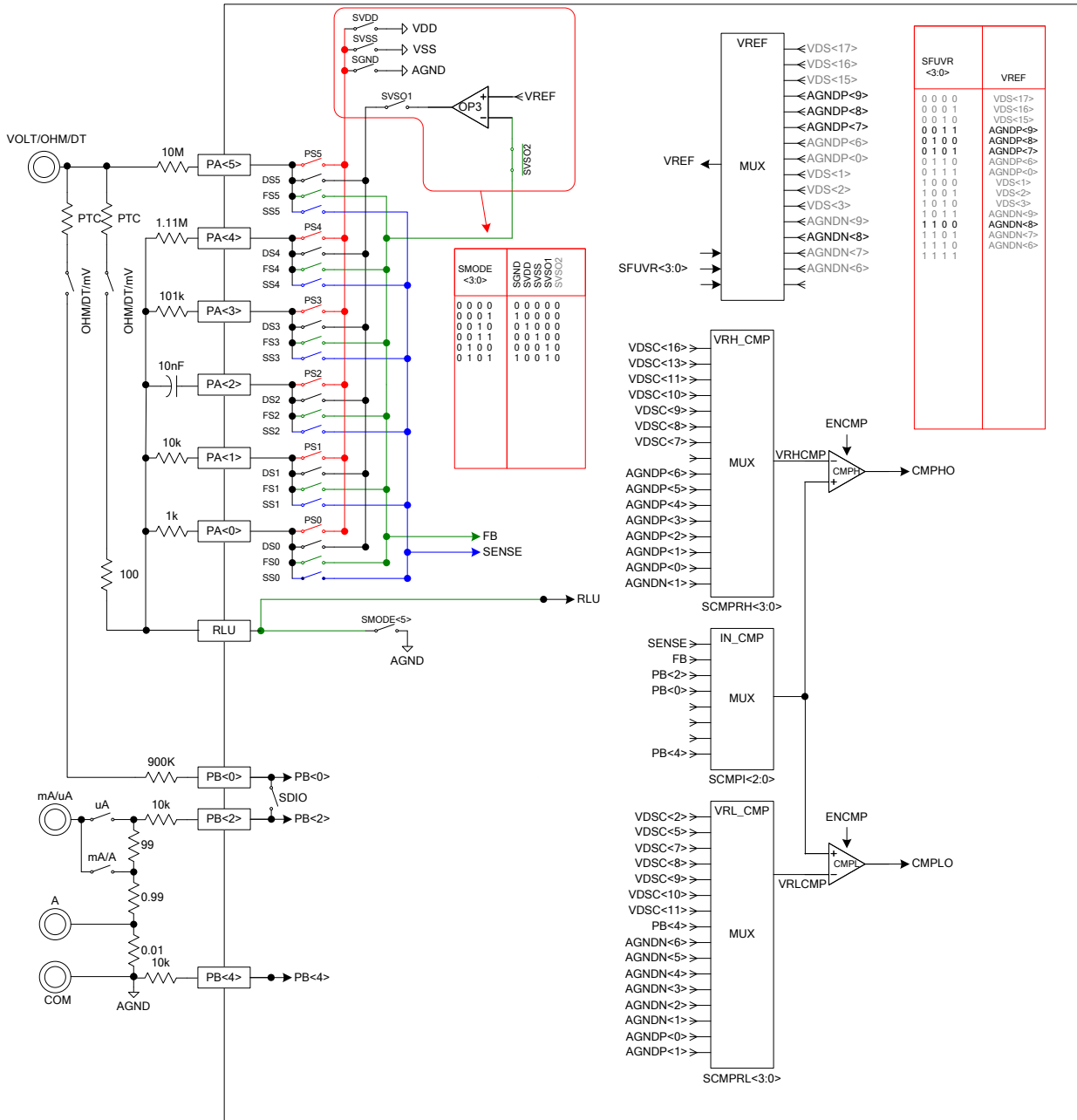
1. Features

- 2.5V~3.6V工作電壓
- 4KWord OTP (One Time Programmable) 程式記憶體，256Byte 資料記憶體
- 內建Brownout與Watch dog timer，可防止CPU進入死機模式
- 內建高精度RC震盪器
 - 操作模式:4MHz
 - 待機模式:32KHz
- 可程式化多功能網路
 - 電壓/電阻/電容換檔量測
 - 定電壓輸出
 - 元件可自我校正
 - 元件正負極性判別
- 多功能比較器
 - 具有遲滯與latch功能，可降低glitch
 - 可程式化設定比較電壓
 - 可做為短路測試量測
- 高解析度 $\Sigma\Delta$ ADC
 - 零輸入電壓，零輸出電壓
 - 高輸入阻抗 (內置輸入緩衝器)
 - 內置絕對溫度感測器
- 1.2V的內部類比電路共地電壓源
- LVD 低電壓檢測功能具 14 段檢測電壓設置與外部輸入電壓檢測功能
- 4x12 LCD 液晶驅動器
 - 內建Charge Pump穩壓線路，可提供 4 種LCD偏壓
 - Static、1/2、1/3、1/4 Duty及 1/3 Bias 軟體選擇
- 8-bit Timer A
- 8-bit Timer C模組具PWM波形產生功能
- Support 6 stack level.

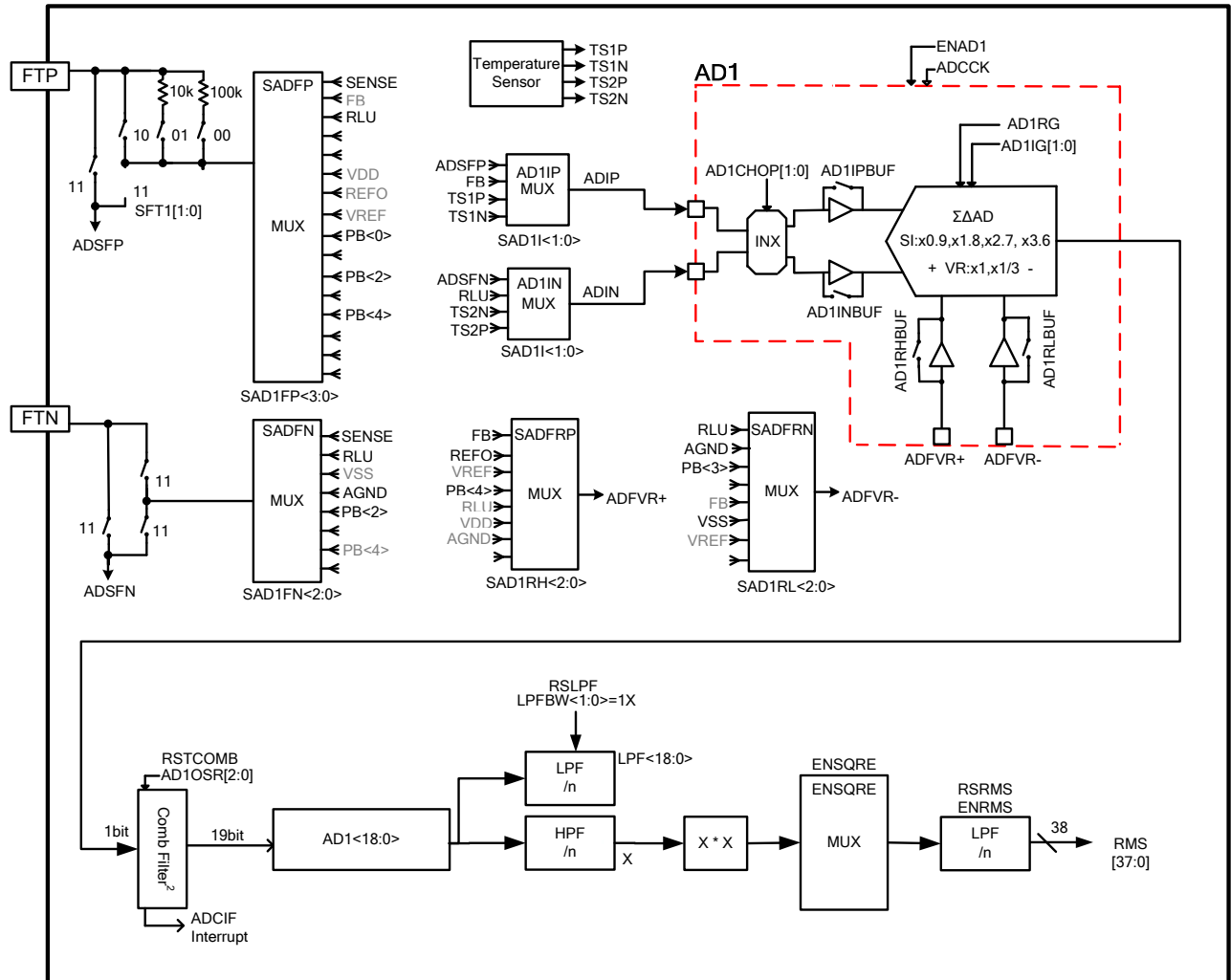
2. Block Diagram



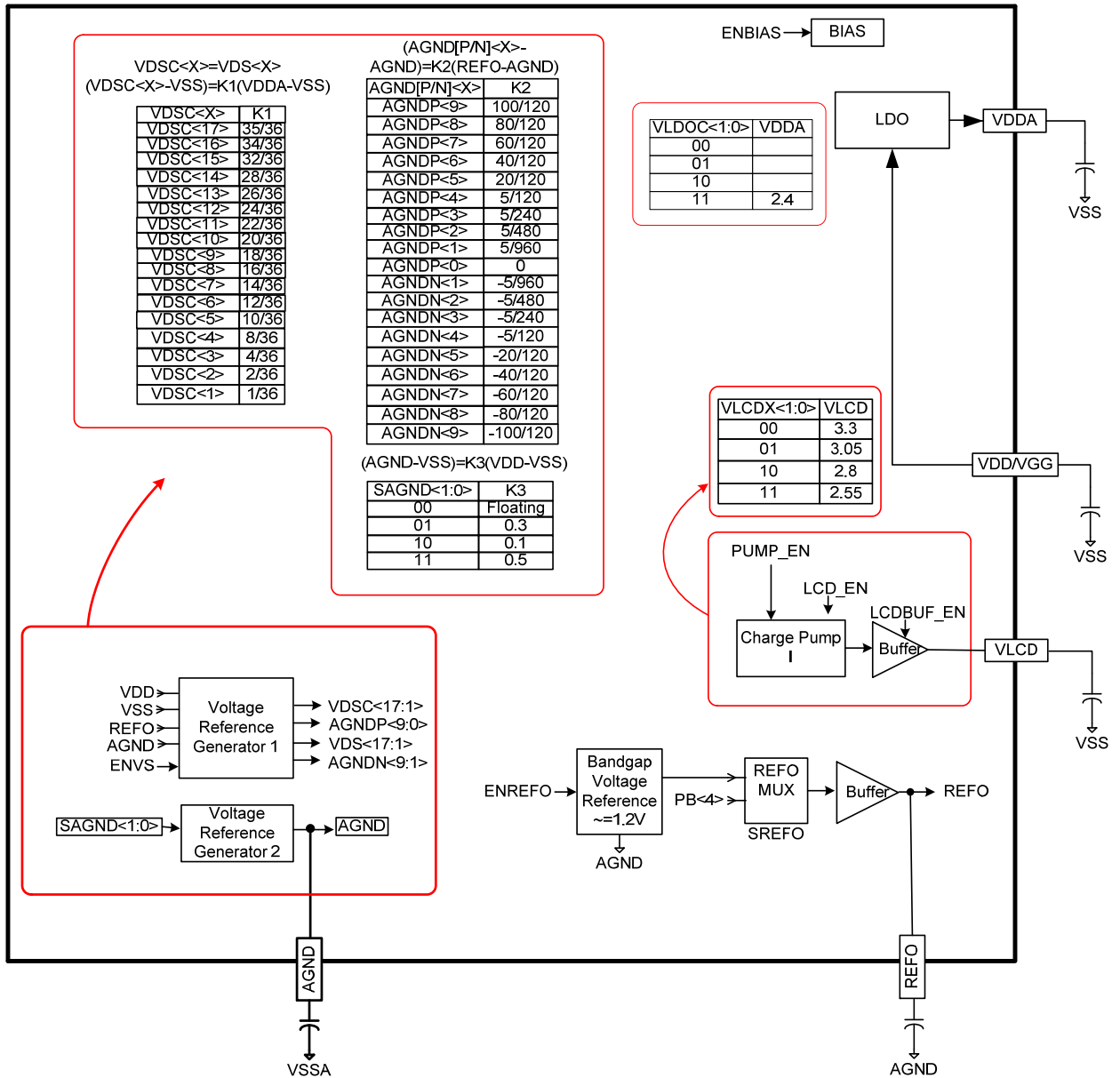
2.1. Multi-Function Block



2.2. ADC

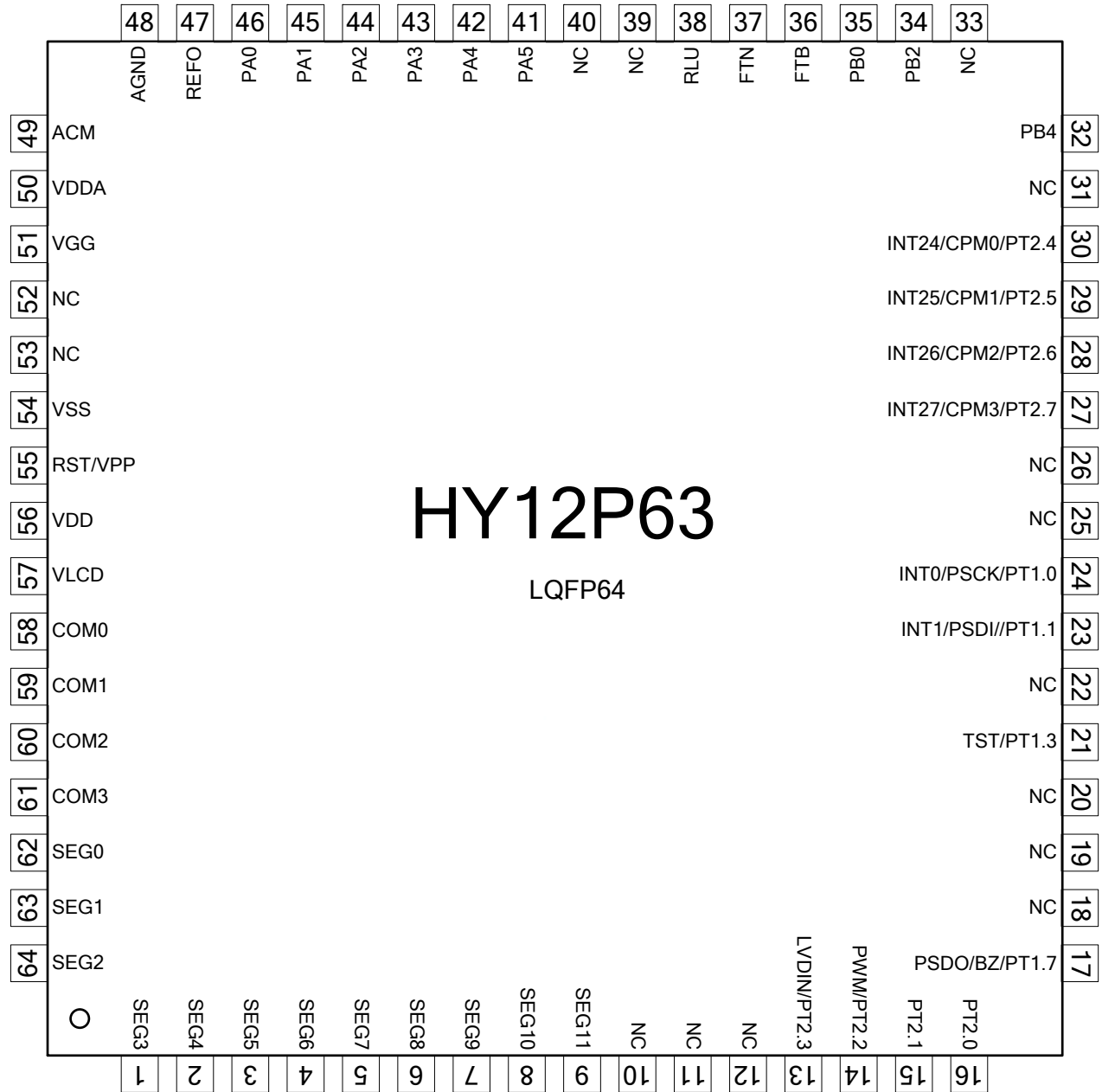


2.3. Power



3. Package And Pin

3.1. 64PIN Diagram LQFP64



3.2. Pin Description

"I/O" Input/Output, "I" Input, "O" Output, "S" Schmitt Trigger, "C" CMOS, "P" Power, "A" Analog

Pin		Characteristic		Description	
No.	Name	I/O	Type		
1	SEG3	O	A	Segment output of LCD	
2	SEG4	O	A	Segment output of LCD	
3	SEG5	O	A	Segment output of LCD	
4	SEG6	O	A	Segment output of LCD	
5	SEG7	O	A	Segment output of LCD	
6	SEG8	O	A	Segment output of LCD	
7	SEG9	O	A	Segment output of LCD	
8	SEG10	O	A	Segment output of LCD	
9	SEG11	O	A	Segment output of LCD	
10	NC			No Connect	
11	NC			No Connect	
12	NC			No Connect	
13	PT2.3/LVDIN	PT2.3	I/O	S	Digital input/output
		LVDIN	I	A	LVD external signal input port
14	PT2.2/PWM	PT2.2	I/O	C	Digital input/output
		PWM	O	C	PWM output port
15	PT2.1	PT2.1	I/O	S	Digital input/output
16	PT2.0	PT2.0	I/O	S	Digital input/output
17	PT1.7/BZ/PSDO	PT1.7	I/O	S	Digital input/output
		BZ	O	C	Buzzer output port
		PSDO	O	C	PSDO port of OTP read/write interface
18	NC			No Connect	
19	NC			No Connect	
20	NC			No Connect	
21	PT1.3/TST	PT1.3	II	S	Digital input
		TST	I	S	Enable input of test mode (invalid)
22	NC			No Connect	

23	PT1.1/PSDI/INT1	PT1.1	I/O	S	Digital input
		PSDI	I	S	PSDI of OTP read/write interface
		INT1	I	S	Interrupt source, INT1
24	PT1.0/PSCK/INT0	PT1.0	I/O	S	Digital input
		PSCK	I	S	PSCK of OTP read/write interface
		INT0	I	S	Interrupt source, INT0
25	NC				No Connect
26	NC				No Connect
27	PT2.7/CMP3/INT27	PT2.7	I/O	C	Digital input/output
		CMP3	I	A	Input port of comparator
		INT27	I	C	Interrupt source, E27IF
28	PT2.6/CMP2/INT26	PT2.6	I/O	S	Digital input/output
		CMP2	I	A	Input port of comparator
		INT26	I	S	Interrupt source, E26IF
29	PT2.5/CMP1/INT25	PT2.5	I/O	S	Digital input/output
		CMP1	I	A	Input port of comparator
		INT25	I	S	Interrupt source, E25IF
30	PT2.4/CMP0/INT24	PT2.4	I/O	S	Digital input/output
		CMP0	I	A	Input port of comparator
		INT24	I	S	Interrupt source, E24IF
31	NC				No Connect
32	PB4		I	A	Analog input channel
33	NC				No Connect
34	PB2		I	A	Analog input channel
35	PB0		I	A	Analog input channel
36	FTP		I/O	A	Capacitor connect port of pre-filter
37	FTN		I/O	A	Capacitor connect port of pre-filter
38	RLU		I/O	A	Switch of analog network
39	NC				No Connect
40	NC				No Connect
41	PA5		I/O	A	Switch of analog network
42	PA4		I/O	A	Switch of analog network

43	PA3		I/O	A	Switch of analog network
44	PA2		I/O	A	Switch of analog network
45	PA1		I/O	A	Switch of analog network
46	PA0		I/O	A	Switch of analog network
47	REFO		I/O	P	Voltage reference port
48	AGND		I/O	P	Analog power ground end
49	ACM		I/O	P	Voltage reference port
50	VDDA		I/O	P	Analog circuit voltage source
51	VGG		I	P	Low Dropout Regulator Input
52	NC				No Connect
53	NC				No Connect
54	VSS		P	P	Ground end of IC operation voltage source
55	RST/VPP	RST VPP	I P	S P	Reset IC (Low active) EPROM read/write voltage source
56	VDD		P	P	Voltage source of IC operation
57	VLCD		I/O	P	Voltage source of LCD
58	COM0		O	A	COM output of LCD
59	COM1		O	A	COM output of LCD
60	COM2		O	A	COM output of LCD
61	COM3		O	A	COM output of LCD
62	SEG0		O	A	Segment output of LCD
63	SEG1		O	A	Segment output of LCD
64	SEG2		O	A	Segment output of LCD

4. Register list

"r"no use,"w"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1													
"u"unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition													
Address	File Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A-RESET	i-RESET	R/W	
00H	INDF0	Contents of FSR0 to address data memory value of FSR0 not changed									N/A	N/A	*****
01H	POINC0	Contents of FSR0 to address data memory value of FSR0 post-incremented									N/A	N/A	*****
02H	PODEC0	Contents of FSR0 to address data memory value of FSR0 post-decremented									N/A	N/A	*****
03H	PRINC0	Contents of FSR0 to address data memory value of FSR0 pre-incremented									N/A	N/A	*****
04H	PLUSW0	Contents of FSR0 to address data memory value of FSR0 offset by W									N/A	N/A	*****
05H	INDF1	Contents of FSR1 to address data memory value of FSR0 not changed									N/A	N/A	*****
06H	POINC1	Contents of FSR1 to address data memory value of FSR0 post-incremented									N/A	N/A	*****
07H	PODEC1	Contents of FSR1 to address data memory value of FSR0 post-decremented									N/A	N/A	*****
08H	PRINC1	Contents of FSR1 to address data memory value of FSR0 pre-incremented									N/A	N/A	*****
09H	PLUSW1	Contents of FSR1 to address data memory value of FSR0 offset by W									N/A	N/A	*****
0FH	FSR0H									xu	-----
10H	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]									xxxx xxxx	uuuu uuuu	*****
11H	FSR1H									xu	-----
12H	FSR1L	Indirect Data Memory Address Pointer 1 Low Byte,FSR1[7:0]									xxxx xxxx	uuuu uuuu	*****
16H	TOSH										...0 0000	...0 0000	-----
17H	TOSL	Top-of-Stack Low Byte (TOS<7:0>)									0000 0000	0000 0000	*****
18H	STKPTR	STKFL	STKUN	STKOV				STKPRT[2]	STKPRT[1]	STKPRT[0]	000..000	000..000	r,rw0,rw0,-,r,r,r
1AH	PCLATH										...0 0000	...0 0000	-----
1BH	PCLATL	PC Low Byte for PC<7:0>									0000 0000	0000 0000	*****
1DH	TBLPTRH										...0 0000	...0 0000	-----
1EH	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)									0000 0000	0000 0000	*****
1FH	TBLDH	Program Memory Table Latch High Byte									0000 0000	0000 0000	*****
20H	TBLDL	Program Memory Table Latch Low Byte									0000 0000	0000 0000	*****
21H	PRODH	Product Register of Multiply High Byte									xxxx xxxx	uuuu uuuu	r,r,r,r,r,r,r,r
22H	PRODL	Product Register of Multiply Low Byte									xxxx xxxx	uuuu uuuu	r,r,r,r,r,r,r,r
23H	INTE1	GIE	TMCIE		TMAIE		WDTIE	E1IE	E0IE	0.0.0000	0.0.0000	*****	
24H	INTE2	RMSIE		LPFIE	AD1IE		CTIE		0000 000.	0000 000.	*****		
25H	INTE3	E24IE	E25IE	E26IE	E27IE			0000		0000	*****		
26H	INTF1	TMCIF		TMAIF		WDTIF	E1IF	E0IF	...0 0000	...0 0000	*****		
27H	INTF2	RMSIF		LPFIF	AD1IF		CTIF		0000 000.	0000 000.	*****		
28H	INTF3	E24IF	E25IF	E26IF	E27IF			0000		0000	*****		
29H	WREG	Working Register									xxxx xxxx	uuuu uuuu	*****
2AH	BSRCN									 0000 0000	-----
2BH	STATUS										...x xxxx	...u uuuu	-----
2CH	SPSTATUS	PD	TO	IDLEB	BOR	SKERR				000d 0..	u0uu d..	rw0,rw0,rw0,rw0,-,rw0,-,-	
2DH	LVDCN1	ENLVD	LVD	VJ1	VJ2	VLDX[3:0]							
2EH	LVDCN2	VSL	SVIN[2:0]			SVIP[3:0]							
2FH	SBMSET1	SKRST	HAOTR[5:0]										
30H	MCKCN1	CPUCK[1:0]		HSS[1:0]		HSKC	ENHAO		x.xx xxxx	u.uu uuuu	*****		
31H	MCKCN2	LCDS[2:0]		ADCCK	PERCK	BZS[2:0]			0000 0000	0000 0000	*****		
32H	TMACN	ENTMA	TMACK	TMAS[1:0]		ENWDT	WDT[2:0]		0000 0000	0000 0000	***** w1,***		
33H	TMAR	TimerA data register									xxxx xxxx	uuuu uuuu	r,r,r,r,r,r,r,r
34H	TMCN	ENTMC	TMCC[1:0]		TMCS[2:0]		TMCS0[1:0]		0000 0000	0000 0000	*****		
35H	PRC	TimerC programmable register									1111 1111	1111 1111	*****
36H	TMCR	TimerC register									0000 0000	0000 0000	r,r,r,r,r,r,r,r
37H	PWMCN	ENPWM	PWMRL[1:0]						0000 0000	0000 0000	*****		
38H	PWMR	PWM MSB Byte register									xxxx xxxx	uuuu uuuu	*****
39H	LCDCN1	ENLCD	LC DPR	VLCDX[1:0]		LCDBF	LCDB[1:0]		0000 000.	0000 000.	*****		
3AH	LCDCN2	LCDBL	LC DMX[1:0]						000.	000.	*****		
3BH	LCD0	Segment SEG1@[7:4] and SEG0@[3:0] data register of LCD									xxxx xxxx	uuuu uuuu	*****
3CH	LCD1	Segment SEG3@[7:4] and SEG2@[3:0] data register of LCD									xxxx xxxx	uuuu uuuu	*****
3DH	LCD2	Segment SEG5@[7:4] and SEG4@[3:0] data register of LCD									xxxx xxxx	uuuu uuuu	*****
3EH	LCD3	Segment SEG7@[7:4]and SEG6@[3:0] data register of LCD									xxxx xxxx	uuuu uuuu	*****
3FH	LCD4	Segment SEG9@[7:4] and SEG8@[3:0] data register of LCD									xxxx xxxx	uuuu uuuu	*****
40H	LCD5	Segment SEG11@[7:4] and SEG10@[3:0] data register of LCD									xxxx xxxx	uuuu uuuu	*****
41H	LCD6	Segment SEG13@[7:4] and SEG12@[3:0] data register of LCD									xxxx xxxx	uuuu uuuu	*****
42H	LCD7	Segment SEG14@[3:0] data register of LCD								 xxxx uuuu	-----
46H											0000 0..	0000 0..	*****
47H											..00 0110	..00 0110	~r,r,r,r,r,r,rw0
48H										 0000 0000	-----
49H											...x xxxx	...u uuuu	-----
4AH											xxxx xxxx	uuuu uuuu	*****
4BH											xxxx xxxx	uuuu uuuu	*****
4CH											xxxx xxxx	uuuu uuuu	r,r,r,r,r,r,r,r

“-”no use, “*”read/write, “w”write, “r”read, “r0”only read 0, “r1”only read 1, “w0”only write 0, “w1”only write 1
 “.”unimplemented bit, “x”unknown, “u”unchanged, “d”depends on condition

Address	File Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A-RESET	i-RESET	R/W	
4DH	PT1	PT1.7				PT1.3		PT1.1	PT1.0	xxxx xxxx	uuuu uuuu	r,r,r,r	
4EH	TRISC1	TC1.7				TC1.3		TC1.1	TC1.0	0000 0000	0000 0000	r,r,r,r	
4FH	PT1PU	PU1.7				PU1.3		PU1.1	PU1.0	0000 0000	0000 0000	r,r,r,r	
50H	PT1M1	PM1.7				INTEG1[1:0]		INTEG0[1:0]		0000 0000	0000 0000	r,r,r,r	
51H	PT2	PT2.7	PT2.6	PT2.5	PT2.4	PT2.3	PT2.2	PT2.1	PT2.0	xxxx xxxx	uuuu uuuu	r,r,r,r	
52H	TRISC2	TC2.7	TC2.6	TC2.5	TC2.4	TC2.3	TC2.2	TC2.1	TC2.0	0000 0000	0000 0000	r,r,r,r	
53H	PT2DA	DA2.7	DA2.6	DA2.5	DA2.4	DA2.3		PM2.2[1:0]		0000 0.00	0000 0.00	r,r,r,r	
54H	PT2PU	PU2.7	PU2.6	PU2.5	PU2.4	PU2.3	PU2.2	PU2.1	PU2.0	0000 0000	0000 0000	r,r,r,r	
55H										xxx. 000.	uuu. 000.	r,r,r,r	
56H										000. 0.0.	000. 0.0.	r,r,r,r	
57H	PAX6												
58H	PA54	PS5	DS5	FS5	SS5	PS4	DS4	FS4	SS4				
59H	PA32	PS3	DS3	FS3	SS3	PS2	DS2	FS2	SS2				
5AH	PA10	PS1	DS1	FS1	SS1	PS0	DS0	FS0	SS0				
5BH	PWRCN	DMMBIAS	SAGND[1:0]	ENVS	ENREFO	ENLDO	LDOC[1:0]=11						
5CH	PWRCN2	MCUBIAS	ENCMP		RSTCOMB	RSLPF	RSRMS						
5DH	ADCN1	SDIO	SREFO	SFT1<1:0>	SFUVR<3:0>								
5EH	ADCN2		SMODE<7:0>										
5FH	ADCN3		SCMPRH<3:0>		SCMPRL<3:0>								
60H	ADCN4		SCMPI<2:0>	AD1CHOP<1:0>	AD1OSR<2:0>								
61H	ADCN5		SAD1FP<3:0>	HSAD	SAD1FN<2:0>								
62H	ADCN6		SAD1RH<2:0>	SAD1RL<2:0>	SAD1I<1:0>								
63H	ADCN7	ENAD1	AD1IG<1:0>	AD1RG	AD1RHBUF	AD1RLBUF	AD1IPBUF	AD1INBUF					
64H	RMSCN	ENRMS	ENLPF	ENSQRE=1	LFPBW<1>=	LFPBW<0>							
65H													
66H													
67H													
68H													
69H													
6AH													
6BH													
6CH													
6DH													
6EH	CTSTA		CMPHO	CMPLO									
6FH													
70H													
71H													
72H													
73H													
74H													
75H	RMSDATA4	RMS<37:30>								xxxx xxxx	uuuu uuuu	r,r,r,r	
76H	RMSDATA3	RMS<29:22>								xxxx xxxx	uuuu uuuu	r,r,r,r	
77H	RMSDATA2	RMS<21:14>								xxxx xxxx	uuuu uuuu	r,r,r,r	
78H	RMSDATA1	RMS<13:6>								xxxx xxxx	uuuu uuuu	r,r,r,r	
79H	RMSDATA0	RMS<5:0>								xxxx xxxx	uuuu uuuu	r,r,r,r	
7AH	LPFDATAU	LPF<18:11>								xxxx xxxx	uuuu uuuu	r,r,r,r	
7BH	LPFDATAH	LPF<10:3>								xxxx xxxx	uuuu uuuu	r,r,r,r	
7CH	LPFDATAI	LPF<2:0>								xxxx xxxx	uuuu uuuu	r,r,r,r	
7DH	AD1DATAU	AD1<18:11>								xxxx xxxx	uuuu uuuu	r,r,r,r	
7EH	AD1DATAH	AD1<10:3>								xxxx xxxx	uuuu uuuu	r,r,r,r	
7FH	AD1DATAI	AD1<2:0>								xxxx xxxx	uuuu uuuu	r,r,r,r	
80H ~ FFH	GPR0	General Purpose Register as 128Byte									xxxx xxxx	uuuu uuuu	r,r,r,r
100H~17FH	GPR1	General Purpose Register as 128Byte									xxxx xxxx	uuuu uuuu	r,r,r,r

5. Absolute Maximum Ratings

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at VDD(VDDA) to VSS(VSSA)	-0.2 V to 4.0 V
Voltage applied to any pin	-0.2 V to V _{DD} + 0.3 V
Diode current at any device terminal	±2 mA
Storage temperature range, Tstg	-55°C to 150°C
Total power dissipation	0.5w
Lead temperature (soldering, 10s)	300°C

5.1. Recommended Operating Conditions

T_A = -40°C ~ 85°C, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V _{DD}	Supply Voltage	All digital peripherals and CPU	2.2		3.6	V
		Analog peripherals	2.5		3.6	
V _{SS}	Supply Voltage		0		0	

5.2. Internal RC Oscillator

T_A = 25°C, V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1		4		MHz
LPO	Low Power Oscillator frequency	V _{DD} supply voltage be enable LPO		32		KHz

5.3. Supply Current into VDD Excluding Peripherals Current

T_A = 25°C, V_{DD} = 3.0V, OSC_LPO = 32KHz, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I _{AM1}	Active mode 1	OSC_HAO = 4MHz, CPU_CK = 4MHz		0.36	0.55	mA
I _{AM2}	Active mode 2	OSC_HAO = 4MHz, CPU_CK = 2MHz		0.2	0.3	mA
I _{LP3}	Low Power 3	OSC_HAO = off, CPU_CK = off, Sleep state		0.65	1.2	uA

OSC_HAO : Internal High Accuracy Oscillator frequency.

CPU_CK : CPU core work frequency.

5.4. Port 1~2

$T_A = 25^{\circ}\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				2.1	V
V_{IL}	Low-Level input voltage		0.9			
V_{hys}	Input Voltage hysteresis($V_{IH} - V_{IL}$)			0.8		V
I_{LKG}	Leakage Current				0.1	μA
R_{PU}	Port pull high resistance			180		$\text{k}\Omega$
Output voltage and current and frequency						
V_{OH}	High-level output voltage	$I_{OH}=10\text{mA}$			$V_{DD} - 0.3$	V
V_{OL}	Low-level output voltage	$I_{OL}=-10\text{mA}$			$V_{SS} + 0.3$	

5.5. Reset(Brownout, External RST pin, Low Voltage Detect)

$T_A = 25^{\circ}\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
BOR	Pulse length needed to accepted reset internally, t_{d-LVR}		2			us
	V_{DD} Start Voltage to accepted reset internally (L→H), V_{LVR}		1.6	1.85	2.1	V
	Hysteresis, $V_{HYS-LVR}$		70			mV
RST	Pulse length needed as RST/VPP pin to accepted reset internally, t_{d-RST}		2			us
	Input Voltage to accepted reset internally		0.9			V
	Hysteresis, $V_{HYS-RST}$		0.8			V
LVD Compare Mode	Operation current, I_{LVD}			10	15	uA
	External input voltage to compare reference voltage			1.2		V
	Compare reference voltage temperature drift	$T_A = -40^{\circ}\text{C} \sim 85^{\circ}\text{C}$		100		ppm/ $^{\circ}\text{C}$
	Detect V_{DD} voltage rang by user option, V_{SVS} $VLDx[3:0]=1110b$			3.3		V
	Detect V_{DD} voltage rang by user option, V_{SVS} $VLDx[3:0]=1101b$			3.2		
	Detect V_{DD} voltage rang by user option, V_{SVS} $VLDx[3:0]=1100b$			3.1		
	Detect V_{DD} voltage rang by user option, V_{SVS} $VLDx[3:0]=1011b$			3.0		
	Detect V_{DD} voltage rang by user option, V_{SVS} $VLDx[3:0]=1010b$			2.9		
	Detect V_{DD} voltage rang by user option, V_{SVS} $VLDx[3:0]=1001b$			2.8		
	Detect V_{DD} voltage rang by user option, V_{SVS} $VLDx[3:0]=1000b$			2.7		
	Detect V_{DD} voltage rang by user option, V_{SVS} $VLDx[3:0]=0111b$			2.6		
	Detect V_{DD} voltage rang by user option, V_{SVS} $VLDx[3:0]=0110b$			2.5		
	Detect V_{DD} voltage rang by user option, V_{SVS} $VLDx[3:0]=0101b$			2.4		
	Detect V_{DD} voltage rang by user option, V_{SVS} $VLDx[3:0]=0100b$			2.3		
	Detect V_{DD} voltage rang by user option, V_{SVS} $VLDx[3:0]=0011b$			2.2		
	Detect V_{DD} voltage rang by user option, V_{SVS} $VLDx[3:0]=0010b$			2.1		
	Detect V_{DD} voltage rang by user option, V_{SVS} $VLDx[3:0]=0001b$			2.0		
VDD Ratio	Comparator Offset Error		-150		150	mV
Compare Mode	VDD Ratio Error		-5		5	%
BOR : Brownout Reset LVR : Low Voltage Reset of BOR LVD : Low Voltage Detect RST : External Reset pin						

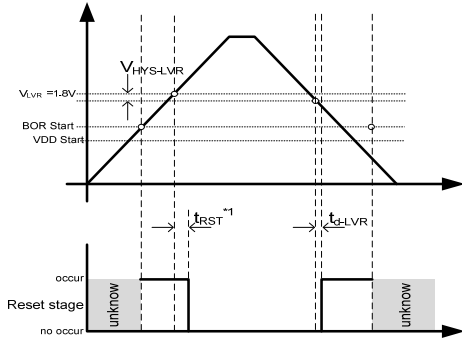


Figure 6.5-1 BOR reset diagram

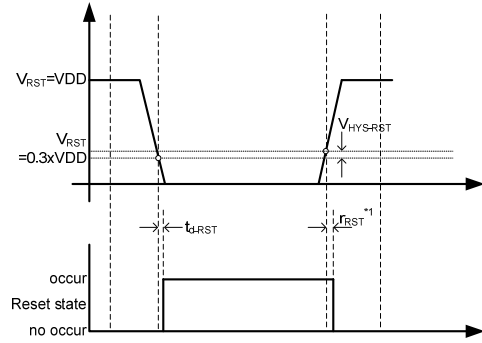


Figure 6.5-2 RST reset diagram

*1 t_{RST} : Please see BOR Introduce of HY12Pxx series User's Guide (UG-HY12S65-Vxx).

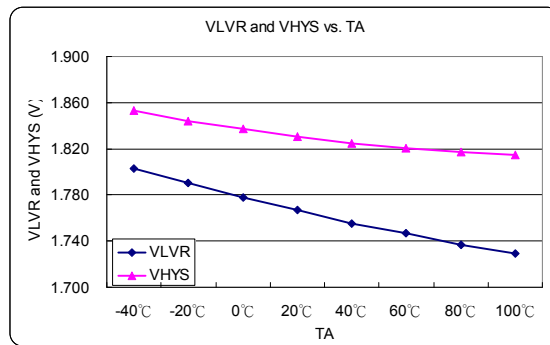


Figure 6.5-3 VLVR and VHYS vs. Temperature

5.6. Power System

$T_A = 25^{\circ}\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
VDDA	VDDA operation current, I_{VDDA}	$I_L = 0\text{mA}$	LDOC[1:0]=11b	22			μA
	Select VDDA output voltage	$I_L = 0.1\text{mA}$, $V_{DD}=3\text{V}$	LDOC[1:0]=11b	3.6			V
	Load Regulation	$V_{DD}=2.5\text{V}$ $I_L = 1\sim 5\text{mA}$	LDOC[1:0]=11b	10			mV
	Line Regulation	$V_{DD}=2.5\text{V}\sim 3.6\text{V}$ $I_L = 1\text{mA}$	LDOC[1:0]=11b	40			mV
	Temperature drift	LDOC[1:0]=11b	$T_A = -40^{\circ}\text{C}\sim 85^{\circ}\text{C}$	100			ppm/ $^{\circ}\text{C}$
	V_{DD} Voltage drift	$I_L = 0.1\text{mA}$	$V_{DD}=2.5\text{V}\sim 3.6\text{V}$	± 0.2			%/V
AGND	AGND operation current, I_{Agnd}	SAGND#00b	$I_L = 0\text{mA}$	20			μA
	Output voltage, V_{Agnd}		$I_L = 0\mu\text{A}$	1.0			V
	Output voltage with Load		$I_L = \pm 200\mu\text{A}$	0.98	1.02		V_{AGND}
REFO	V(REFO,AGND)	ENLDO=1b,	$I_L = 0\mu\text{A}$	1.2			V
	Temperature drift	SAGND#00b	$T_A = -40^{\circ}\text{C}\sim 85^{\circ}\text{C}$	100			ppm/ $^{\circ}\text{C}$
	RMS Noise			60			μVrms

5.7. LCD

$T_A = 25^{\circ}\text{C}, V_{DD} = 3.0\text{V}, C_{VLCD} = 4.7\mu\text{F}$, unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
I_{LCD}	Operation supply current without output buffer.(all segment turn on)	LCDPR[0]=1	$V_{DD} = 2.2\text{V}$	20			μA
			$V_{DD} = 3.0\text{V}$				
VLCD	Supply Voltage at VLCD pin	LCDPR[0]=0		2.2	3.6		V
	Embedded Charge Pump output voltage at VLCD pin	$V_{DD} = 2.2\text{V}$, LCDPR[0]=1, $C_{VLCD} = 4.7\mu\text{F}$	VLCDX[1:0]=11b	2.295	2.55	2.805	V
			VLCDX[1:0]=10b	2.52	2.8	3.08	
			VLCDX[1:0]=01b	2.745	3.05	3.355	
VLCDX[1:0]=00b	2.97	3.3	3.63				
Z_{LCD}	Output impedance with LCD buffer	$f_{LCD} = 128\text{Hz}, VLCD=3.05\text{V}$		10			k Ω

5.8. Σ ADC, Power Supply and Recommended Operating Conditions

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{V}$, $V_{DDA}=2.4\text{V}$, $V_R=1.2\text{V}$, $AGND=0.5V_{DD}$, $ADC\ Clock=400\text{kHz}$ Input buffer on unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
$f_{\Sigma\text{ADC}}$	Modulator sample frequency, ADC_CK			400			KHz
$I_{\Sigma\text{ADC}}$	Operation supply current	Input gain =0.9, input buffer on ADC_CK=400KHz		550			uA
$D_{\Sigma\text{ADC}}$	Maximum ADC Output Code (ADC Gain Factor)	OSR=2500~20000		17D79		d	
		OSR=64~256		3FFFF			
		OSR=32		3FD7C			
Eos	Input offset voltage	Chopper on OSR=20000	Input gain=0.9, reference gain=1	20	100	uV	
			Input gain=3.6, reference gain=0.33	5	10		
Rev	Roll-over error voltage	Chopper on OSR=20000	Input gain=0.9, reference gain=1	200	600	uV	
			Input gain=3.6, reference gain=0.33	10	30		
Vrms	Input RMS Noise	Chopper on, OSR=20000, input gain=0.9 reference gain=1		10		uV	
		Chopper on, OSR=20000, input gain=3.6 reference gain=0.33		2			
		Chopper off, OSR=32, input gain=0.9 reference gain=1		400			
		Chopper off, OSR=32, input gain=3.6 reference gain=0.33		80			
NM	Normal Rejection ratio	Chopper On OSR=20000 ADCLK=1	Input gain=0.9, reference gain=1. Vin=200mVrms 50/60Hz	60		dB	
			Input gain=3.6, reference gain=0.33. Vin=20mVrms 50/60Hz				
AC_{bw}	AC Measurement	OSR=32, LPFBW=1024	0.5% error	20	350	Hz	
	Bandwidth (Sine wave only)		3dB	TBD			

5.9. ΣΔADC, Temperature Sensor

$T_A = 25^{\circ}\text{C}, V_{DD} = 3.0\text{V}, V_{DDA}=2.4\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
TC_S	Sensor temperature drift			65		$\mu\text{V}/^{\circ}\text{C}$
KT	Absolute Temperature Scale 0°K	ADC Gain=0.9, OSR=20000, Input buffer Off, VR:REFO-AGND AGND=0.3VDDA		-277		$^{\circ}\text{C}$
TC_{ERR}	One point calibrate error temperature	Calibration at 25°C of $-40^{\circ}\text{C} \sim 85^{\circ}\text{C}$		± 2		$^{\circ}\text{C}$

5.10. Analog Input and Switch Performance

$T_A = 25^{\circ}\text{C}, V_{DD} = 3.0\text{V}, V_{DDA}=3.6\text{V}$ AGND=0.3VDDA, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AL}	Analog Input Leakage Current	AGND=0.3VDDA		10	100	pA
		AGND=0.1VDDA		100	500	
		AGND=0.1VDDA		100	500	
Rsw	Switch Turn On Resistance	PS0,PS1		20		Ohm
		DS0,DS1		40		
		DS2~DS5, PS2~PS5		80		
		SS0~SS5,FS0~FS5		400		

5.11. DMM Comparator

$T_A = 25^{\circ}\text{C}, V_{DD} = 3.0\text{V}, V_{DDA}=2.4\text{V}$ AGND=0.5VDDA, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{CMP}	Comparator Supply Current					μA
V_I	Comparator Input Range	CMPL	0		$V_{DDA}-0.7$	V
		CMPH	0.4		V_{DDA}	
Vos	Comparator Input Offset Voltage	CMPL , VRLCMP=AGND		5		mV
		CMPH , VRHCMP=AGND		5		
Vn	Comparator Input peak to peak noise	CMPL		5		mV
		CMPH		5		
		CMPH&CMPL		10		
CMP_{BW}	Comparator Bandwidth	VRHCMP=AGNDP<2>, VRLCMP=AGNDN<2> VIN=100mVrms		1		MHz

6. Ordering Information

下單品名 ¹	封裝型式	引腳數	封裝型式 描述方式		程式碼 編號 ²	出貨包裝 形式	個裝 數量	材料 組成	MSL ³
			L	064					
HY12P63-L064	LQFP	64	L	064	000	Tray	250	Green ⁴	MSL-3

¹ 產品名稱 – 封裝型式描述方式 – 程式碼編號（空白片 / 標準品 / 代客燒錄碼）

例如：您的需求是不帶程式碼的空白片且需要的產品是封裝片 LQFP64 出貨。
則下單品名為 HY12P63-L064，且需以 Tray 出貨，則除下單品名外，請特別著名出貨包裝形式為 Tray

例如：您的代客燒錄服務申請的程式碼編號為 008，且需要的產品是封裝片 LQFP64 出貨。則下單品名為 HY12P63-L064-008，且需以 Tray 出貨，則除下單品名外，請特別著名出貨包裝形式為 Tray

² 程式碼編號

“001”~“999” 為標準品或代客燒錄申請的程式碼編號，而空白晶片不帶此碼。

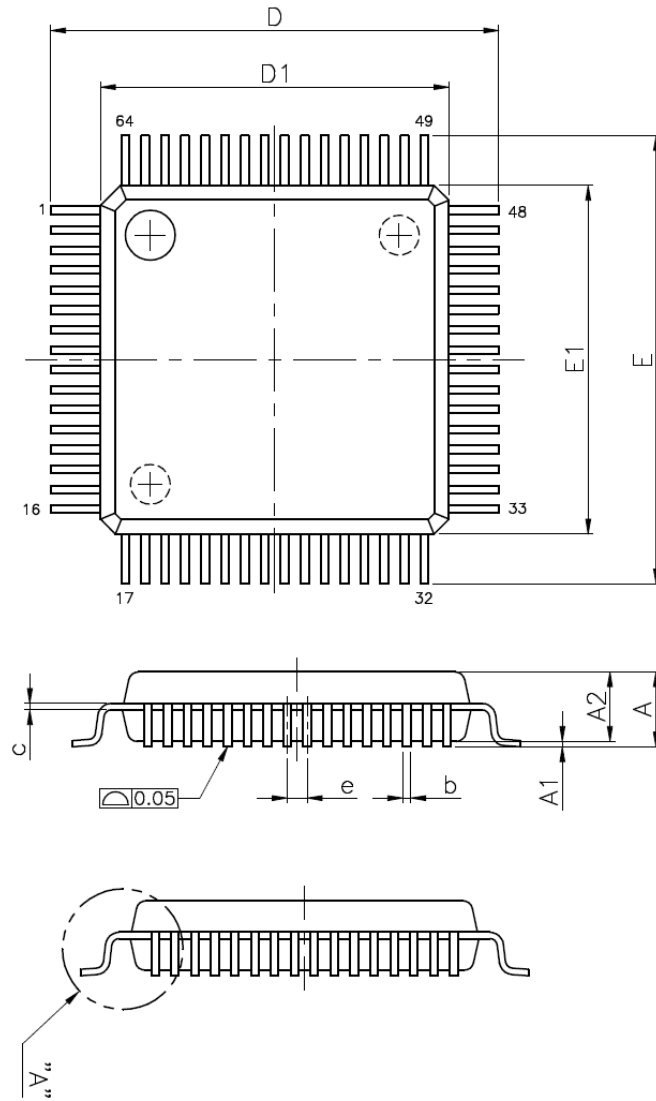
³ MSL:

濕度敏感性等級係依據 IPC/JEDEC J-STD-020 的規範加以試驗分級，並參考 IPC/JEDEC J-STD-033 的標準處理、包裝、運輸與使用。

⁴ Green (RoHS & no Cl/Br):

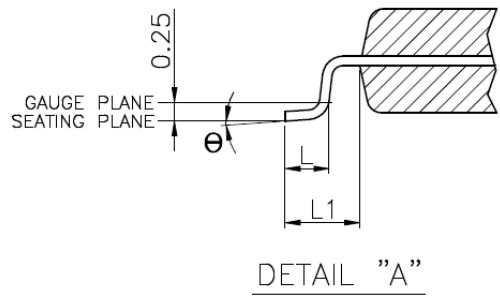
HYCON 產品皆為 Green Product，符合 RoHS 指令以及無鹵素規定(Br/Cl<0.1%)

7. Packaging Information



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°



JEDEC MS-026 Compliant

8. Revision Record

Major differences are stated thereafter :

Version	Page	Revision Summary
V01	All	New release