



HY11P12
Datasheet
8-Bit RISC-like Mixed Signal Microcontroller
Embedded 4x12 LCD Driver
18-Bit Σ ADC

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1. 特點

- 8 位元精簡指令集，共有 46 個指令
- 2.2V to 3.6V工作電壓範圍，
-40~85°C工作溫度範圍.
- 外部石英震盪器及內部高精度RC震盪器，6 種CPU工作時脈切換選擇，可讓使用者達到最佳省電規劃。
 - 運行模式 300uA @ 2MHz
 - 待機模式 3uA @ 28KHz
 - 休眠模式 1uA
- 2KWord OTP (One Time Programmable) Type程式記憶體，128Byte資料記憶體
- Brownout detector及Watch dog Timer，可防止CPU進入死機模式.
- 18bit 全差動輸入 $\Sigma\Delta$ ADC 類比數位轉換器
 - 內置PGA (Programmable Gain Amplifier) 及可有 1/4、1/2、1、.....128 倍 10 種輸入信號放大倍率選擇
 - 內置輸入零點調整，可針對不同應用增加其量測範圍
- 內置高阻抗輸入緩衝器(4 以上輸入倍率不適用)
- 內置絕對溫度感測器
- 1.0V的內部類比電路共地電壓源，具有Push-Pull 驅動能力，可提供傳感器驅動電壓
- LVD低電壓檢測功能具 14 段檢測電壓設置 與外部輸入電壓 檢測功能
- 類比電壓源VDDA可選擇 4 種不同輸出電壓，具 10mA穩壓電壓源輸出能力
- 4x12 LCD 液晶驅動器
 - Static、1/2、1/3、1/4 Duty及 1/3 Bias 軟體選擇
 - 內建Charge Pump穩壓線路，可提供 4 種LCD偏壓
- 8-bit Timer A
- Support 6 stack level

2. 引腳定義

2.1 LQFP44 引腳圖

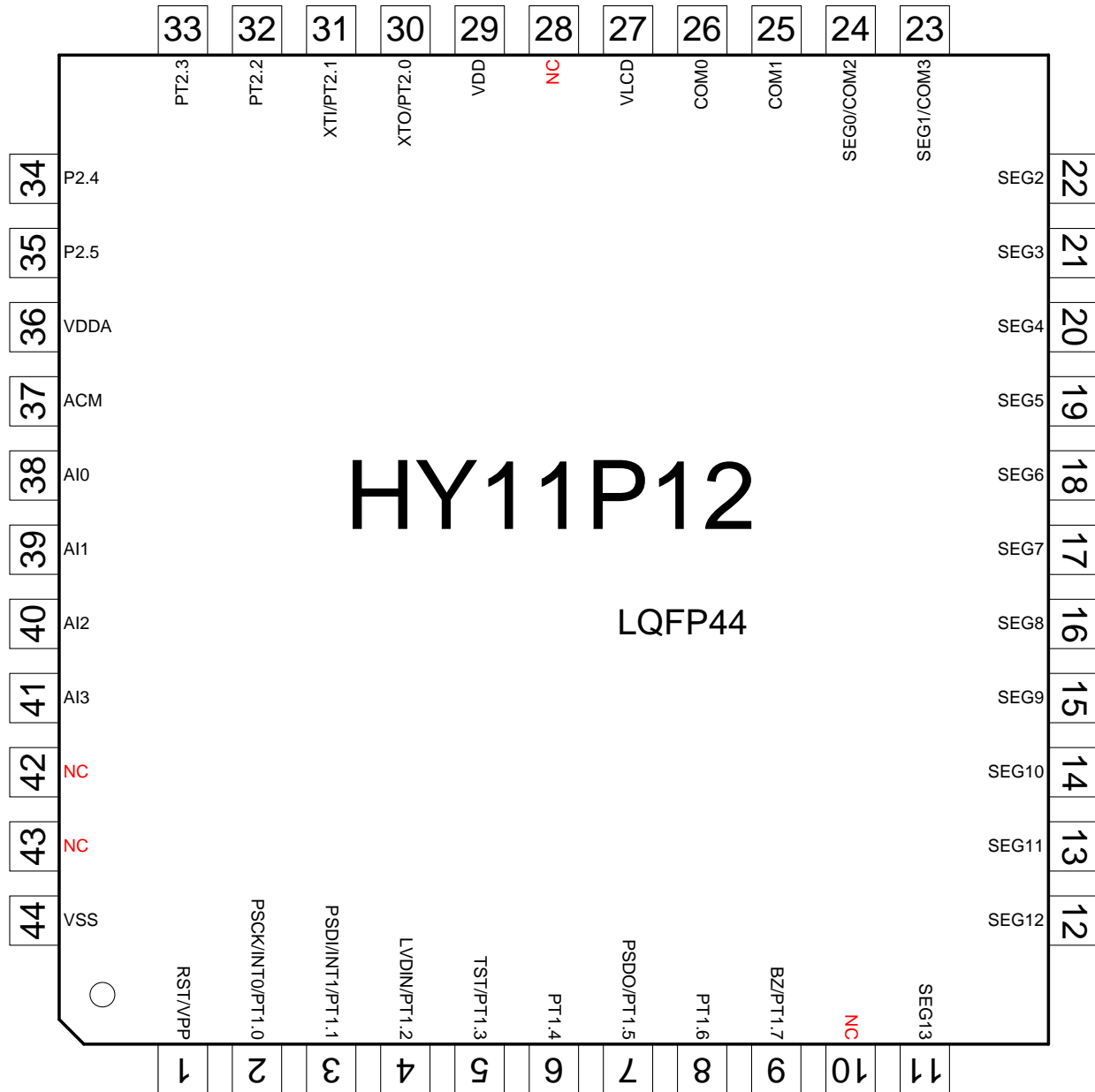


圖 2-1 HY11P12 LQFP44 引腳圖

註 1：VPP與RST復用同一接口，非燒錄EPROM時禁止輸入電壓超過 5.8V

註 2：TST與PT1.3 復用同一接口，操作時禁止輸入電壓超過Vdd+0.3V

註 3：若不將 PT1.3 設定成外部引腳按鍵，可以提升抗干擾能力

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2.2 LQFP48 引腳圖

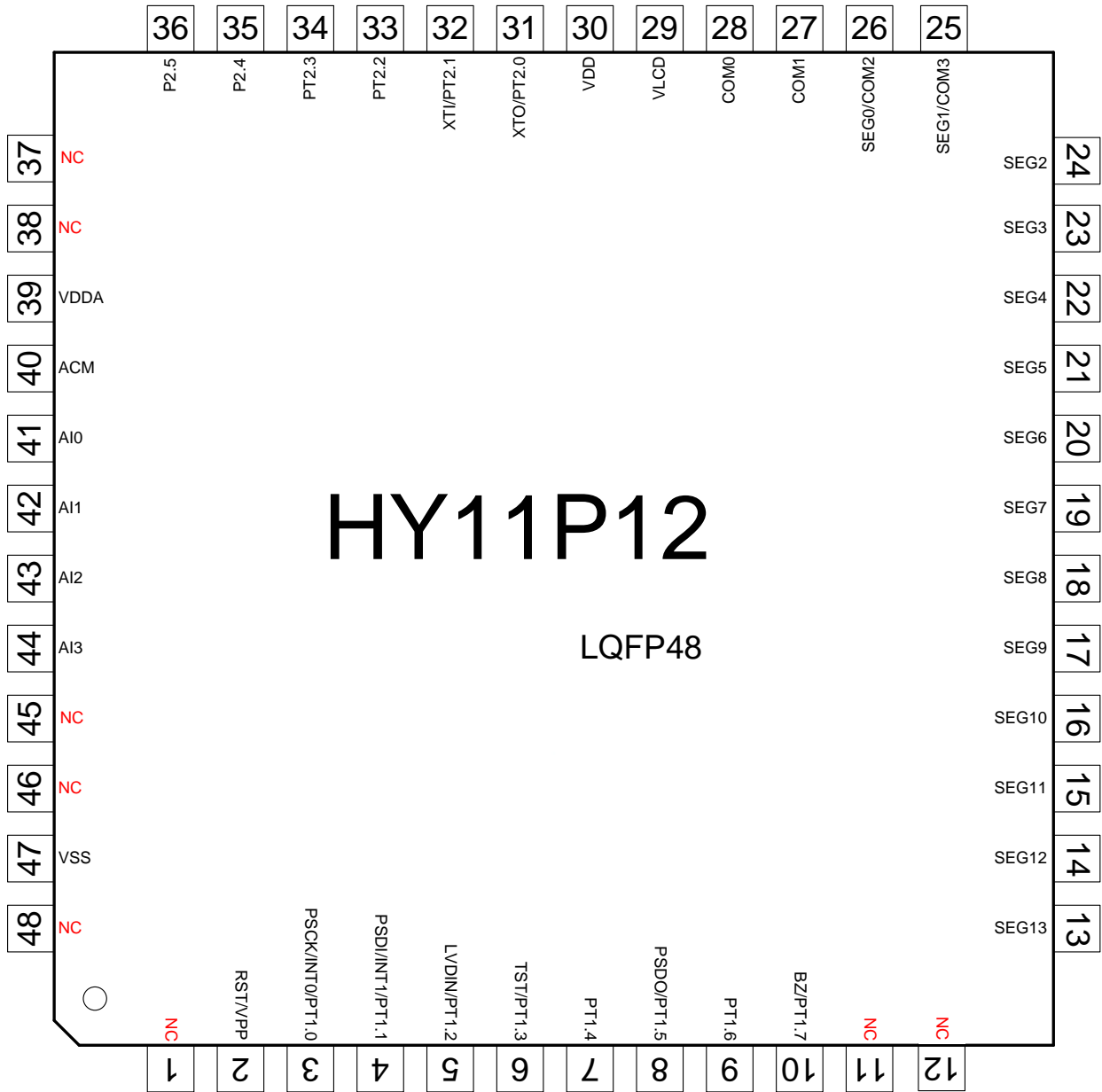


圖 2-2 HY11P12 LQFP48 引腳圖

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8-Bit RISC-like Mixed Signal Microcontroller

2.3 QFN48 引腳圖

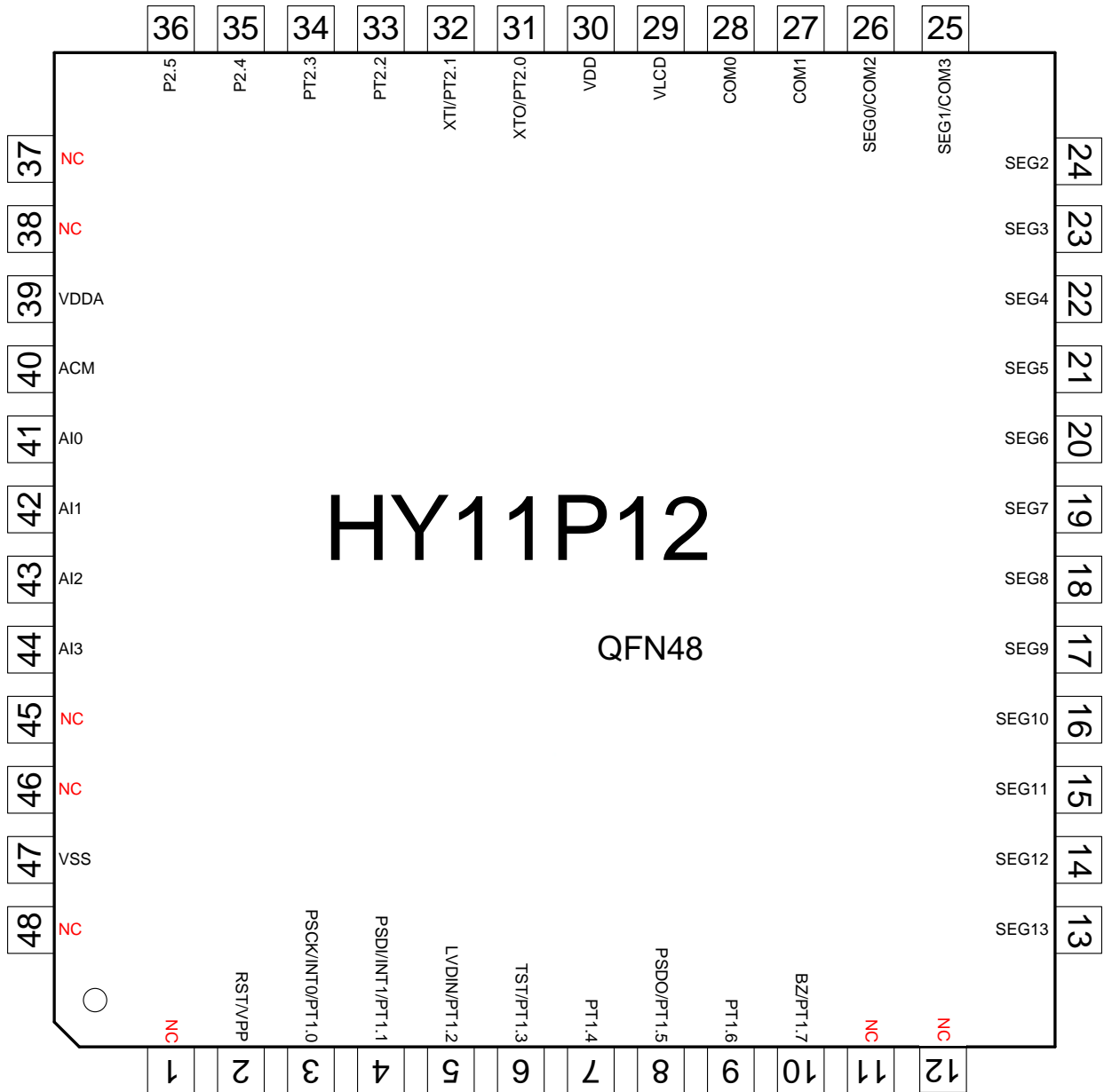


圖 2-3 HY11P12 QFN48 引腳圖

註 1：VPP與RST復用同一接口，非燒錄EPROM時禁止輸入電壓超過 5.8V

註 2：TST與PT1.3 復用同一接口，操作時禁止輸入電壓超過Vdd+0.3V

註 3：若不將 PT1.3 設定成外部引腳按鍵，可以提升抗干擾能力

2.4 I/O 定義與說明(LQFP44)

“I/O”輸入/輸出,“I”輸入,“O”輸出,“S”史密斯觸發,“C”CMOS 特性兼容輸出與輸入,“P”電壓源,“A”類比通道

| 編號 | 引腳名稱 | 引腳特性 | | 功能說明 | |
|----|-----------------|-----------------------|-------------|-------------|----------------------------------|
| | | 格式 | 緩衝 | | |
| 1 | RST/VPP | RST VPP | I P | S P | 復位晶片 EPROM讀/寫時的電壓源 |
| 2 | PT1.0/INT0/PSCK | PT1.0 INT0 PSCK | I I I | S S S | 數位輸入 中斷源INT0 OTP讀/寫介面SCK接口 |
| 3 | PT1.1/INT1/PSDI | PT1.1 INT1 PSDI | I I I | S S S | 數位輸入 中斷源INT1 OTP讀/寫介面SDI接口 |
| 4 | PT1.2/LVDIN | PT1.2 LVDIN | I A | S A | 數位輸入 LVD外部信號輸入接口 |
| 5 | PT1.3/TST | PT1.3 TST | I I | S S | 數位輸入 測試模式致能輸入（未開放） |
| 6 | PT1.4 | | I/O | S | 數位輸入/輸出 |
| 7 | PT1.5/PSDO | PT1.5 PSDO | I/O O | S C | 數位輸入/輸出 OTP讀/寫介面SDO接口 |
| 8 | PT1.6 | | I/O | S | 數位輸入/輸出 |
| 9 | PT1.7/BZ | PT1.7 BZ | I/O O | S C | 數位輸入/輸出 蜂鳴器輸出端 |
| 10 | NC | | - | - | 未使用 |
| 11 | SEG13 | | O | A | LCD的Segment輸出 |
| 12 | SEG12 | | O | A | LCD的Segment輸出 |
| 13 | SEG11 | | O | A | LCD的Segment輸出 |
| 14 | SEG10 | | O | A | LCD的Segment輸出 |
| 15 | SEG9 | | O | A | LCD的Segment輸出 |
| 16 | SEG8 | | O | A | LCD的Segment輸出 |
| 17 | SEG7 | | O | A | LCD的Segment輸出 |

| | | | | |
|----|-----------|-----|---|---------------------|
| 18 | SEG6 | O | A | LCD的Segment輸出 |
| 19 | SEG5 | O | A | LCD的Segment輸出 |
| 20 | SEG4 | O | A | LCD的Segment輸出 |
| 21 | SEG3 | O | A | LCD的Segment輸出 |
| 22 | SEG2 | O | A | LCD的Segment輸出 |
| 23 | COM3/SEG1 | O | A | LCD的COM與Segment共用輸出 |
| 24 | COM2/SEG0 | O | A | LCD的COM與Segment共用輸出 |
| 25 | COM1 | O | A | LCD的COM輸出 |
| 26 | COM0 | O | A | LCD的COM輸出 |
| 27 | VLCD | P | P | LCD的電壓源 |
| 28 | NC | - | - | 未使用 |
| 29 | VDD | P | P | 晶片工作電壓源 |
| 30 | PT2.0/XTO | I/O | S | 數位輸入/輸出 |
| | | | A | 外接振盪器輸出端 |
| 31 | PT2.1/XTI | I/O | S | 數位輸入/輸出 |
| | | | A | 外接振盪器輸入端 |
| 32 | PT2.2 | I/O | C | 數位輸入/輸出 |
| 33 | PT2.3 | I/O | S | 數位輸入/輸出 |
| 34 | PT2.4 | I/O | S | 數位輸入/輸出 |
| 35 | PT2.5 | I/O | S | 數位輸入/輸出 |
| 36 | VDDA | P | P | 穩壓器輸出，類比電路電壓源 |
| 37 | ACM | P | P | 內部類比電路共地引腳 |
| 38 | AI0 | A | A | 類比輸入通道 |
| 39 | AI1 | A | A | 類比輸入通道 |
| 40 | AI2 | A | A | 類比輸入通道 |
| 41 | AI3 | A | A | 類比輸入通道 |
| 42 | NC | - | - | 未使用 |
| 43 | NC | - | - | 未使用 |
| 44 | VSS | P | P | 晶片工作電壓源接地端 |

表 2-1 LQFP44 引腳定義與功能說明

2.5 I/O 定義與說明(LQFP48/QFN48)

“I/O”輸入/輸出,“I”輸入,“O”輸出,“S”史密斯觸發,“C”CMOS 特性兼容輸出與輸入,“P”電壓源,“A”類比通道

| 編號 | 引腳名稱 | 引腳特性 | | 功能說明 | |
|----|-----------------|-------|-----|---------------|---------------|
| | | 格式 | 緩衝 | | |
| 1 | NC | - | - | 未使用 | |
| 2 | RST/VPP | RST | I | S | 復位晶片 |
| | | VPP | P | P | EPROM讀/寫時的電壓源 |
| 3 | PT1.0/INT0/PSCK | PT1.0 | I | S | 數位輸入 |
| | | INT0 | I | S | 中斷源INT0 |
| | | PSCK | I | S | OTP讀/寫介面SCK接口 |
| 4 | PT1.1/INT1/PSDI | PT1.1 | I | S | 數位輸入 |
| | | INT1 | I | S | 中斷源INT1 |
| | | PSDI | I | S | OTP讀/寫介面SDI接口 |
| 5 | PT1.2/LVDIN | PT1.2 | I | S | 數位輸入 |
| | | LVDIN | A | A | LVD外部信號輸入接口 |
| 6 | PT1.3/TST | PT1.3 | I | S | 數位輸入 |
| | | TST | I | S | 測試模式致能輸入（未開放） |
| 7 | PT1.4 | I/O | S | 數位輸入/輸出 | |
| 8 | PT1.5/PSDO | PT1.5 | I/O | S | 數位輸入/輸出 |
| | | PSDO | O | C | OTP讀/寫介面SDO接口 |
| 9 | PT1.6 | I/O | S | 數位輸入/輸出 | |
| 10 | PT1.7/BZ | PT1.7 | I/O | S | 數位輸入/輸出 |
| | | BZ | O | C | 蜂鳴器輸出端 |
| 11 | NC | - | - | 未使用 | |
| 12 | NC | - | - | 未使用 | |
| 13 | SEG13 | O | A | LCD的Segment輸出 | |
| 14 | SEG12 | O | A | LCD的Segment輸出 | |
| 15 | SEG11 | O | A | LCD的Segment輸出 | |
| 16 | SEG10 | O | A | LCD的Segment輸出 | |
| 17 | SEG9 | O | A | LCD的Segment輸出 | |

| | | | | | |
|----|-----------|-------|-----|---|---------------------|
| 18 | SEG8 | | O | A | LCD的Segment輸出 |
| 19 | SEG7 | | O | A | LCD的Segment輸出 |
| 20 | SEG6 | | O | A | LCD的Segment輸出 |
| 21 | SEG5 | | O | A | LCD的Segment輸出 |
| 22 | SEG4 | | O | A | LCD的Segment輸出 |
| 23 | SEG3 | | O | A | LCD的Segment輸出 |
| 24 | SEG2 | | O | A | LCD的Segment輸出 |
| 25 | COM3/SEG1 | | O | A | LCD的COM與Segment共用輸出 |
| 26 | COM2/SEG0 | | O | A | LCD的COM與Segment共用輸出 |
| 27 | COM1 | | O | A | LCD的COM輸出 |
| 28 | COM0 | | O | A | LCD的COM輸出 |
| 29 | VLCD | | P | P | LCD的電壓源 |
| 30 | VDD | | P | P | 晶片工作電壓源 |
| 31 | PT2.0/XTO | PT2.0 | I/O | S | 數位輸入/輸出 |
| | | XTO | A | A | 外接振盪器輸出端 |
| 32 | PT2.1/XTI | PT2.1 | I/O | S | 數位輸入/輸出 |
| | | XTI | A | A | 外接振盪器輸入端 |
| 33 | PT2.2 | | I/O | C | 數位輸入/輸出 |
| 34 | PT2.3 | | I/O | S | 數位輸入/輸出 |
| 35 | PT2.4 | | I/O | S | 數位輸入/輸出 |
| 36 | PT2.5 | | I/O | S | 數位輸入/輸出 |
| 37 | NC | | - | - | 未使用 |
| 38 | NC | | - | - | 未使用 |
| 39 | VDDA | | P | P | 穩壓器輸出，類比電路電壓源 |
| 40 | ACM | | P | P | 內部類比電路共地引腳 |
| 41 | AI0 | | A | A | 類比輸入通道 |
| 42 | AI1 | | A | A | 類比輸入通道 |
| 43 | AI2 | | A | A | 類比輸入通道 |
| 44 | AI3 | | A | A | 類比輸入通道 |
| 45 | NC | | - | - | 未使用 |
| 46 | NC | | - | - | 未使用 |
| 47 | VSS | | P | P | 晶片工作電壓源接地端 |
| 48 | NC | | - | - | 未使用 |

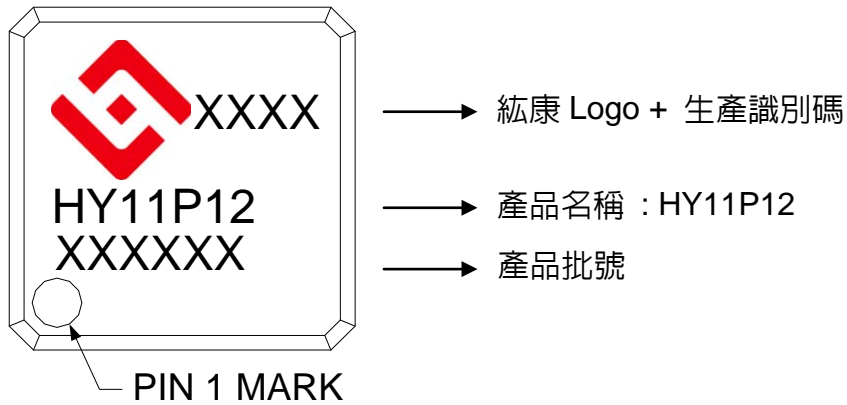
表 2-2 LQFP48/QFN48 引腳定義與功能說明

HY11P12

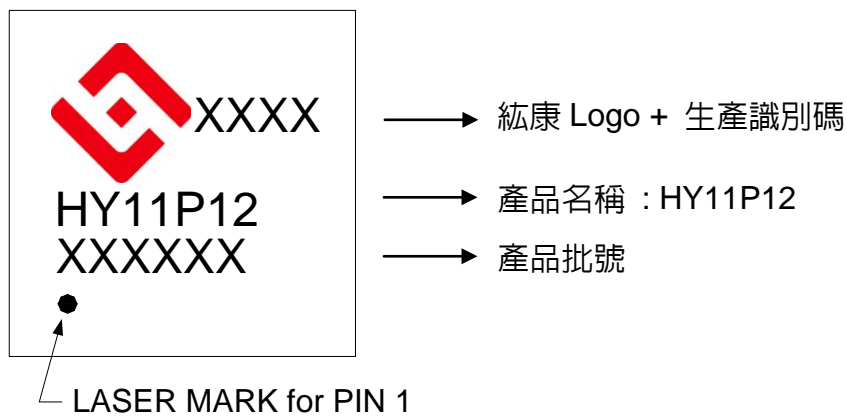
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8-Bit RISC-like Mixed Signal Microcontroller

2.5.1 LQFP 封裝片標記信息



2.5.2 QFN 封裝片標記信息



3. 應用電路

3.1 橋式感測器 I

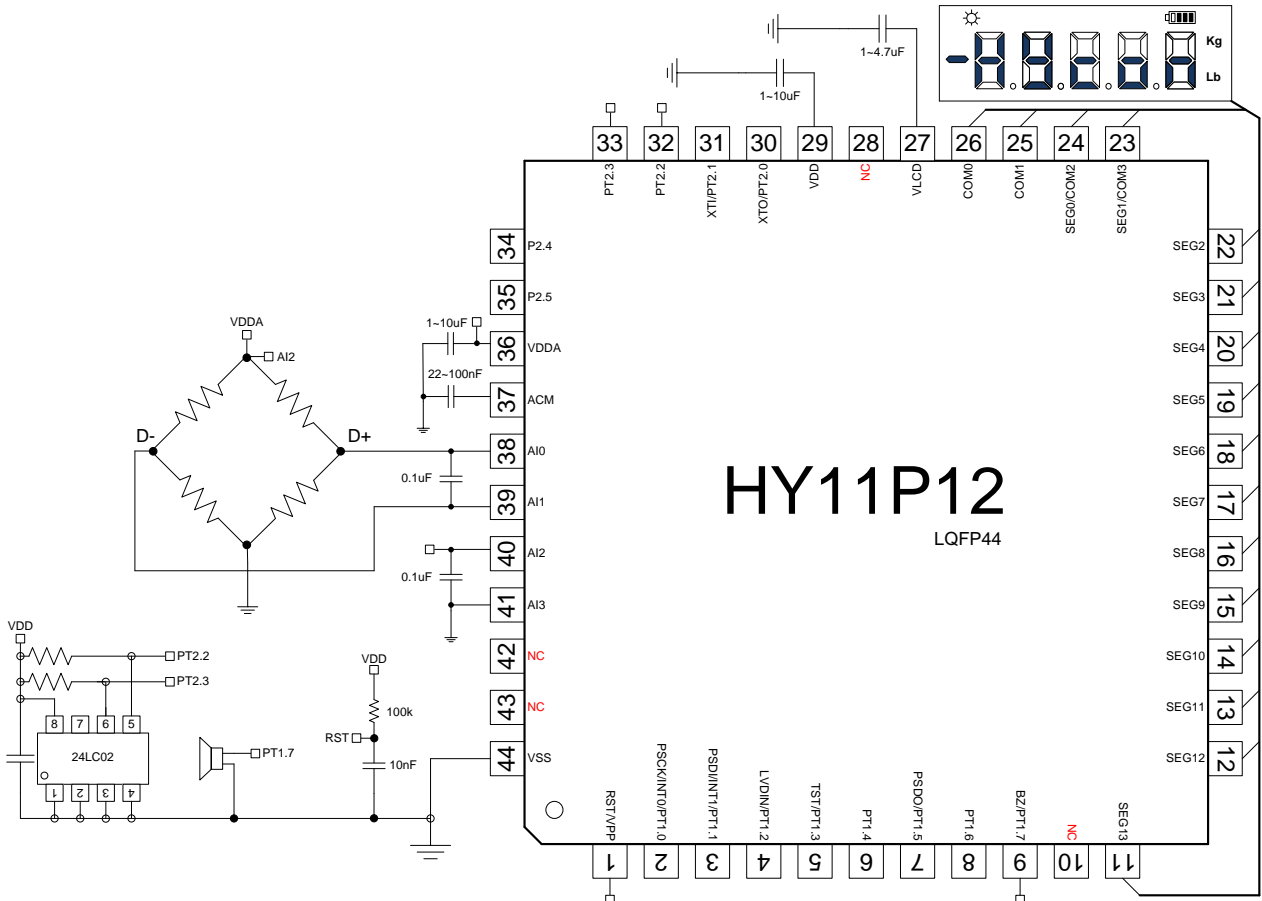


圖 3-1 橋式感測器應用電路

註：Load Cell 零點電壓位置可透過 DCSET[2:0] 進行偏壓調整。

3.2 橋式感測器 II

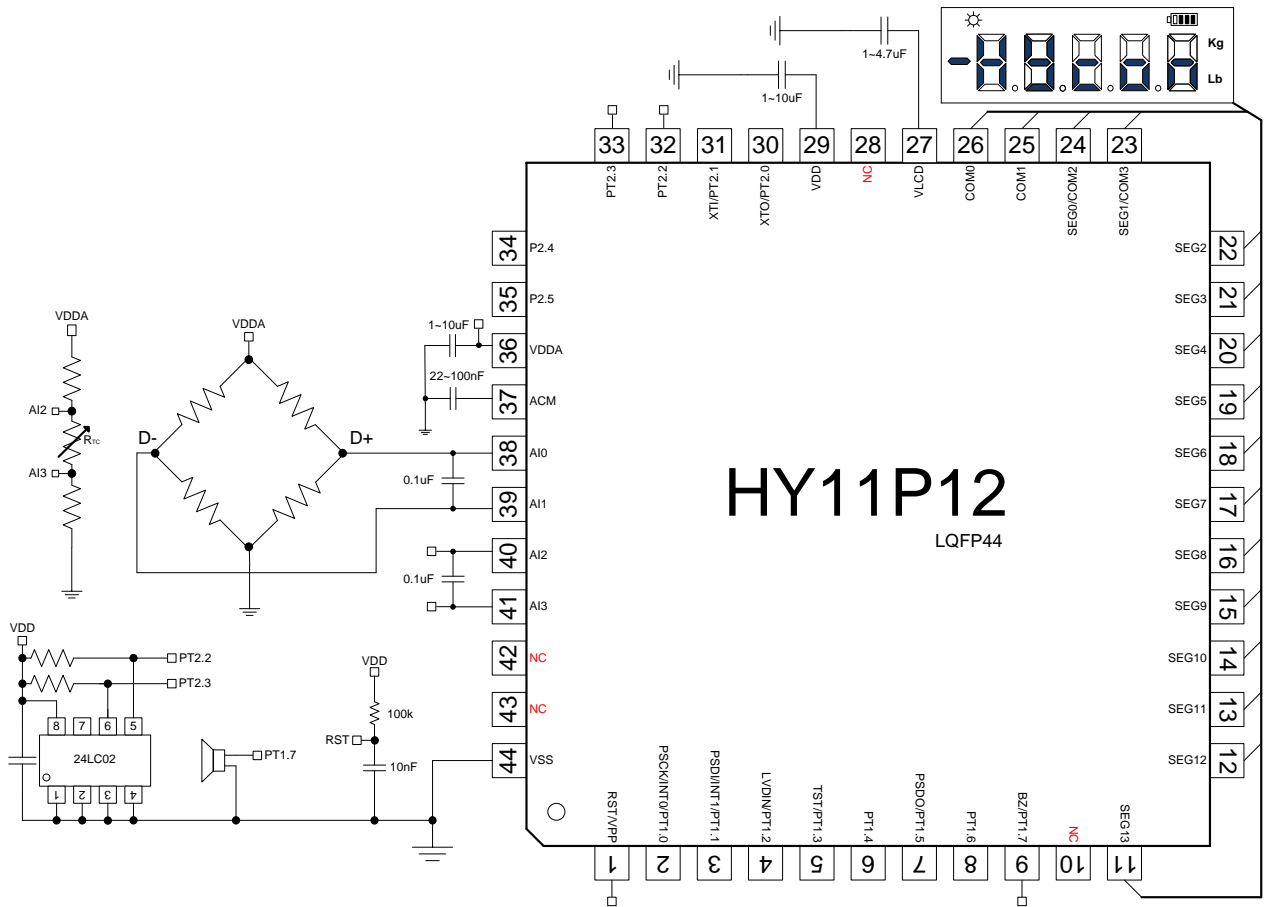


圖 3-2 具溫度補償的橋式感測器應用電路

註：使用外部參考電壓並設計溫度補償電阻 NTC基本線路

註：關於Load Cell 零點電壓位置可透過 DCSET[2:0] 進行偏壓調整。

4. 功能概述

4.1 内部方块图

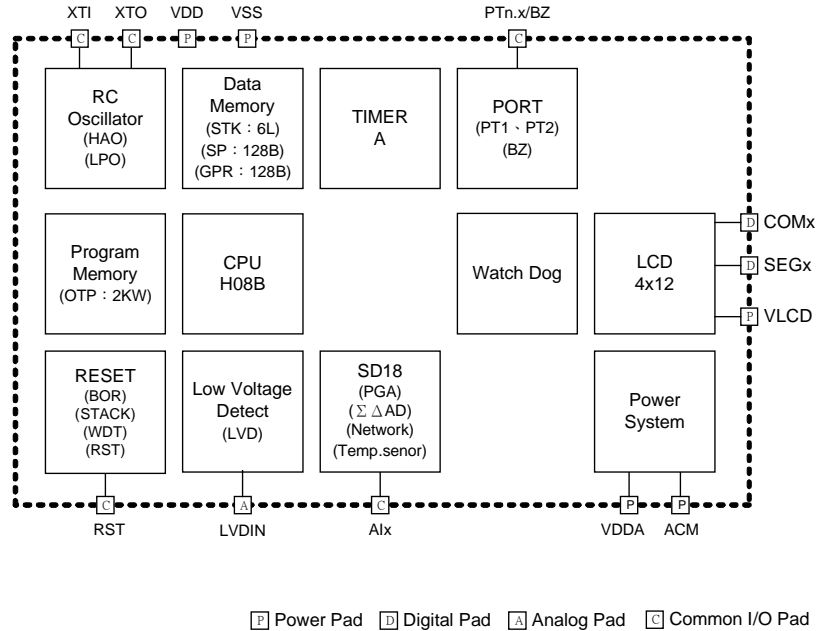


圖 4-1 HY11P12 内部方块图

4.2 相關說明與支援文件

晶片功能相關使用說明書

| | |
|-----------------|-----------------|
| DS-HY11P12-Vxx | HY11P12 說明書 |
| UG-HY11S14-Vxx | HY11Pxx 系列使用說明書 |
| APD-CORE003-Vxx | H08B 指令說明書 |

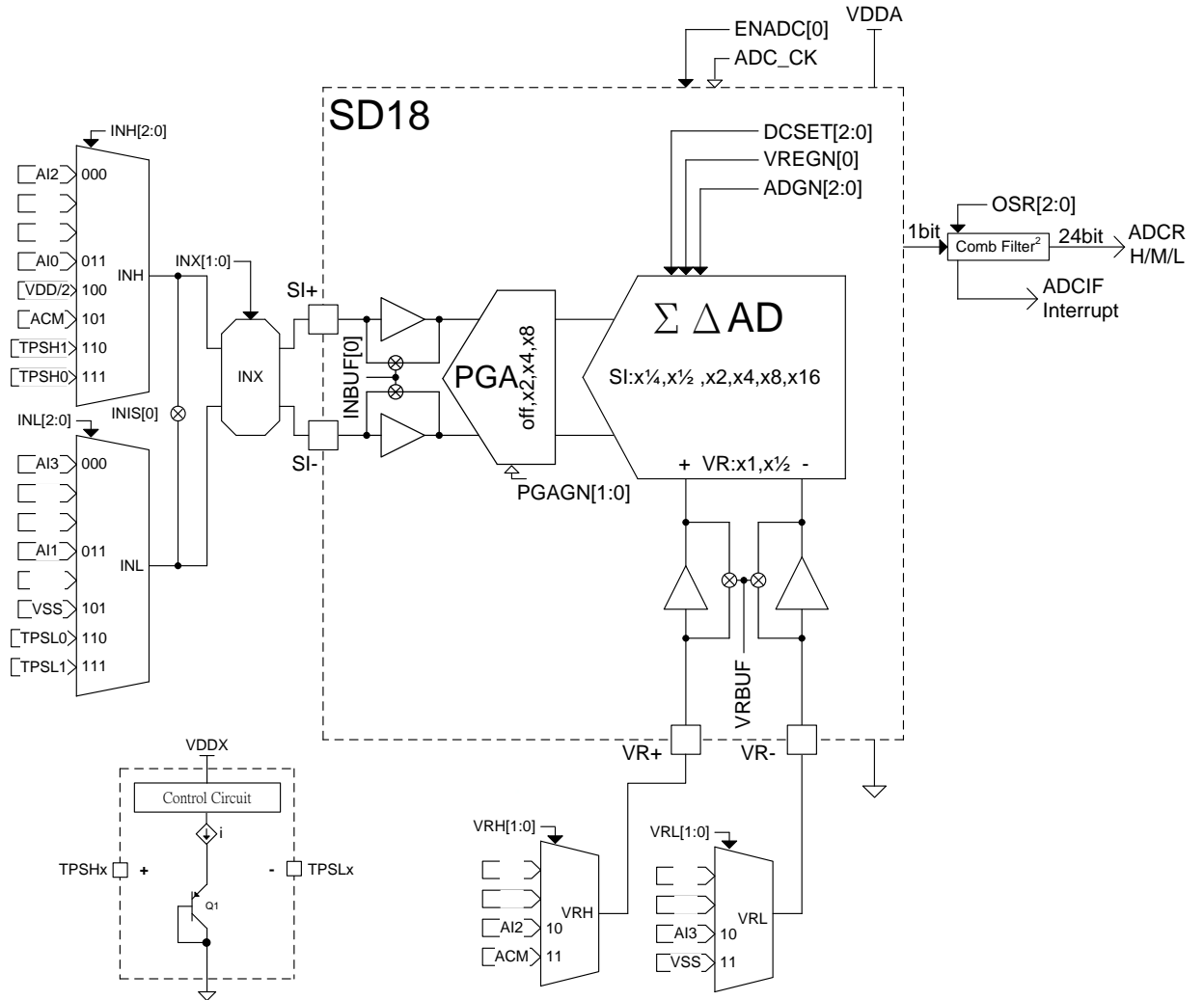
開發工具相關使用說明書

| | |
|------------------|-----------------------|
| APD-HYIDE006-Vxx | HY11xxx 系列開發工具軟體使用說明書 |
| APD-HYIDE005-Vxx | HY11xxx 系列開發工具硬體使用說明書 |
| APD-OTP001-Vxx | OTP 產品燒錄引腳說明書 |

產品生產相關使用說明書

| | |
|------------------|-----------------------|
| APD-HYIDE004-Vxx | HY1xxxx 系列生產線專用燒錄器說明書 |
| BDI-HY11P12-Vxx | HY11P12 個別產品的裸片打線資訊 |

4.3 SD18 Network



4-2 SD18 Network

5. 暫存器列表

| “-”no use, “*”read/write, “w”write, “r”read, “r0”only read 0, “r1”only read 1, “w0”only write 0, “w1”only write 1 | | | | | | | | | | | | | |
|---|-----------|---|-------------|------------|------------|-------------|-------------|-------|-------|-------------|-----------|-----------|----------------------------------|
| “.”unimplemented bit, “x”unknown, “u”unchanged, “d”depends on condition | | | | | | | | | | | | | |
| Address | File Name | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | A-RESET | i-RESET | R/W | |
| 00H | INDF0 | Contents of FSR0 to address data memory value of FSR0 not changed | | | | | | | | | N/A | N/A | ***** |
| 05H | INDF1 | Contents of FSR1 to address data memory value of FSR0 not changed | | | | | | | | | N/A | N/A | ***** |
| 10H | FSR0L | Indirect Data Memory Address Pointer 0 Low Byte, FSR0[7:0] | | | | | | | | | xxxx xxxx | uuuu uuuu | ***** |
| 12H | FSR1L | Indirect Data Memory Address Pointer 1 Low Byte, FSR1[7:0] | | | | | | | | | xxxx xxxx | uuuu uuuu | ***** |
| 18H | STKPTR | STKFL | STKUN | STKOV | | | | | | STKPRT[2:0] | 000. .000 | 000. .000 | r, rw0, rw0, -, r, r, f |
| 1AH | PCLATH | | | | | | PC[10] | PC[9] | PC[8] | |000 |000 | -,-,-,-,-,-,-,-,-,- |
| 1BH | PCLATL | PC Low Byte for PC<7:0> | | | | | | | | | 0000 0000 | 0000 0000 | ***** |
| 23H | INTE1 | GIE | ADCIE | | | TMAIE | WDTIE | E1IE | E0IE | | 00.. 0000 | 00.. 0000 | *,-,-,-,-,-,-,-,-,- |
| 26H | INTF1 | | ADCIF | | | TMAIF | WDTIF | E1IF | E0IF | | .0.. 0000 | .0.. 0000 | *,-,-,-,-,-,-,-,-,- |
| 29H | WREG | Working Register | | | | | | | | | xxxx xxxx | uuuu uuuu | ***** |
| 2BH | STATUS | | | | C | | | | | Z | ...X ...X | ...U ...U | -,-,-,-,-,-,-,-,-,- |
| 2CH | PSTATUS | PD | TO | IDLEB | BOR | | SKERR | | | | 000d .0.. | uduu .d.. | rw0, rw0, rw0, rw0, -, rw0, -, - |
| 2DH | LVDCN | | LVDFG | LVD | LVDON | | | | | VLDX[3:0] | .000 0000 | .000 uuuu | -,-,-,-,-,-,-,-,-,- |
| 30H | PWRCN | ENVDDA | VDDAX[1:0] | ENACM | | | | | | | 0000 | 0000 | ***** |
| 31H | MCKCN1 | | ADCS[2:0] | ADCCK | XTHSP | XTSP | ENXT | ENHAO | | | 0000 0001 | 0000 0001 | ***** |
| 32H | MCKCN2 | | | LSCK | HSCK | HSS[1:0] | CPUCK[1:0] | | | | .00 0000 | .00 0000 | -,-,-,-,-,-,-,-,-,- |
| 33H | MCKCN3 | | LCDS[2:0] | | PERCK | | BZS[2:0] | | | | 000. 0000 | 000. 0000 | ***** |
| 39H | ADCRH | ADC conversion memory HighByte | | | | | | | | | xxxx xxxx | uuuu uuuu | r, r, r, r, r, r, r, f |
| 3AH | ADCRM | ADC conversion memory Middle Byte | | | | | | | | | xxxx xxxx | uuuu uuuu | r, r, r, r, r, r, r, f |
| 3BH | ADCRL | ADC conversion memory Low Byte | | | | | | | | | xxxx xxxx | uuuu uuuu | r, r, r, r, r, r, r, f |
| 3CH | ADCCN1 | ENADC | ENHIGN | ENCHP | PGAGN[1:0] | | ADGN[2:0] | | | | 0000 0000 | 0000 0000 | ***** |
| 3DH | ADCCN2 | | | INBUF | VRBUF | VREGN | DCSET[2:0] | | | | .00 0000 | .00 0000 | -,-,-,-,-,-,-,-,-,- |
| 3EH | ADCCN3 | | OSR[2:0] | | | | | | | | 000. | 000. | ***** |
| 3FH | AINET1 | | INH[2:0] | | | INL[2:0] | | INIS | | | 0000 000. | 0000 000. | ***** |
| 40H | AINET2 | | VRH[1:0] | | INX[1:0] | | VRL[1:0] | | | | .000 000. | .000 000. | -,-,-,-,-,-,-,-,-,- |
| 41H | TMACN | ENTMA | TMACK | TMAS[1:0] | ENWDT | | WDTS[2:0] | | | | 0000 0000 | 0000 0000 | ***** w1, **** |
| 42H | TMAR | TimerA data register | | | | | | | | | xxxx xxxx | uuuu uuuu | r, r, r, r, r, r, r, f |
| 52H | LCDCN1 | ENLCD | LC DPR | VLCDX[1:0] | LCDBF | LCDBI[1:0] | | | | | 0000 000. | 0000 000. | ***** |
| 53H | LCDCN2 | LCDBL | LC DMX[1:0] | | | | | | | | 000. | 000. | ***** |
| 54H | LCD0 | Segment SEG2@[3:0] and SEG3@[7:4] data register of LCD | | | | | | | | | xxxx xxxx | uuuu uuuu | ***** |
| 55H | LCD1 | Segment SEG4@[3:0] and SEG5@[7:4] data register of LCD | | | | | | | | | xxxx xxxx | uuuu uuuu | ***** |
| 56H | LCD2 | Segment SEG6@[3:0] and SEG7@[7:4] data register of LCD | | | | | | | | | xxxx xxxx | uuuu uuuu | ***** |
| 57H | LCD3 | Segment SEG8@[3:0] and SEG9@[7:4] data register of LCD | | | | | | | | | xxxx xxxx | uuuu uuuu | ***** |
| 58H | LCD4 | Segment SEG10@[3:0] and SEG11@[7:4] data register of LCD | | | | | | | | | xxxx xxxx | uuuu uuuu | ***** |
| 59H | LCD5 | Segment SEG12@[3:0] and SEG13@[7:4] data register of LCD | | | | | | | | | xxxx xxxx | uuuu uuuu | ***** |
| 6DH | PT1 | PT1.7 | PT1.6 | PT1.5 | PT1.4 | PT1.3 | PT1.2 | PT1.1 | PT1.0 | | xxxx xxxx | uuuu uuuu | ***** r, r, r, f |
| 6EH | TRISC1 | TC1.7 | TC1.6 | TC1.5 | TC1.4 | | | | | | 0000 | 0000 | ***** |
| 6FH | PT1DA | | | | | | DA1.2 | | | |0.. |0.. | -,-,-,-,-,-,-,-,-,- |
| 70H | PT1PU | PU1.7 | PU1.6 | PU1.5 | PU1.4 | PU1.3 | PU1.2 | PU1.1 | PU1.0 | | 0000 0000 | 0000 0000 | ***** |
| 71H | PT1M1 | | | | | INTEG1[1:0] | INTEG0[1:0] | | | | 0000 | 0000 | -,-,-,-,-,-,-,-,-,- |
| 72H | PT1M2 | | PM1.7[0] | | | | | | | | .0. | .0. | -,-,-,-,-,-,-,-,-,- |
| 74H | PT2 | | | PT2.5 | PT2.4 | PT2.3 | PT2.2 | PT2.1 | PT2.0 | | ..xx xxxx | ..uu uuuu | -,-,-,-,-,-,-,-,-,- |
| 75H | TRISC2 | | | TC2.5 | TC2.4 | TC2.3 | TC2.2 | TC2.1 | TC2.0 | | .00 0000 | .00 0000 | -,-,-,-,-,-,-,-,-,- |
| 77H | PT2PU | | | PU2.5 | PU2.4 | PU2.3 | PU2.2 | PU2.1 | PU2.0 | | .00 0000 | .00 0000 | -,-,-,-,-,-,-,-,-,- |
| 80H ~ FFH | GPR0 | General Purpose Register as 128Byte | | | | | | | | | xxxx xxxx | uuuu uuuu | ***** |

圖 5-1 HY11P12 暫存器列表

6. 電氣特性

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

| | |
|--|-----------------------------------|
| Voltage applied at V _{DD} to V _{SS} | -0.2 V to 4.0V |
| Voltage applied to any pin | -0.2 V to V _{DD} + 0.3 V |
| Voltage applied to RST/VPP pin | -0.2 V to 6.9 V |
| Voltage applied to TST/PT1.3 pin | -0.2 V to V _{DD} + 1 V |
| Diode current at any device terminal | ±2 mA |
| Storage temperature, Tstg: (unprogrammed device) | -55°C to 150°C |
| (programmed device) | -40°C to 85°C |
| Total power dissipation. | 0.5w |
| Maximum output current sink by any PORT1 to PORT3 I/O pin. | .25mA |

6.1 Recommended operating conditions

T_A = -40°C ~ 85°C, unless otherwise noted

| Sym. | Parameter | | Test Conditions | Min. | Typ. | Max. | unit |
|-----------------|----------------|-------------------|--------------------------------------|-----------------------|------|---------|------|
| V _{DD} | Supply Voltage | | All digital peripherals and CPU | 2.2 | | 3.6 | V |
| | | | Analog peripherals | 2.4 | | 3.6 | |
| V _{SS} | Supply Voltage | | | 0 | | 0 | |
| XT | External | Watch crystal | V _{DD} = 2.2V, ENXT[0]=1 | XTSP[0]=0, XTHSP[0]=0 | | 32.768K | Hz |
| | Oscillator | Ceramic resonator | | XTSP[0]=1, XTHSP[0]=0 | | 450K 8M | |
| | Frequency | Crystal | | XTSP[0]=1, XTHSP[0]=0 | | 1M 8M | |

6.2 Internal RC Oscillator

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

| Sym. | Parameter | Test Conditions | Min. | Typ. | Max. | unit |
|------|---------------------------------|---------------------------------------|------|------|------|------|
| HAO | High Speed Oscillator frequency | ENHAO[0]=1 | 1.8 | 2.0 | 2.2 | MHz |
| LPO | Low Power Oscillator frequency | V_{DD} supply voltage be enable LPO | 22 | 28 | 35 | KHz |

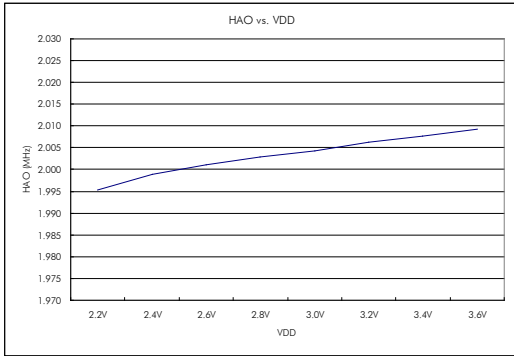


Figure 6.2-1 HAO vs. VDD

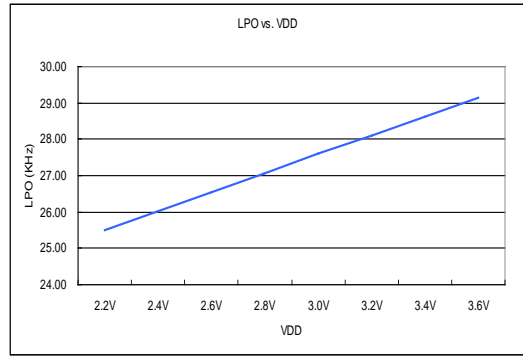


Figure 6.2-2 LPO vs. VDD

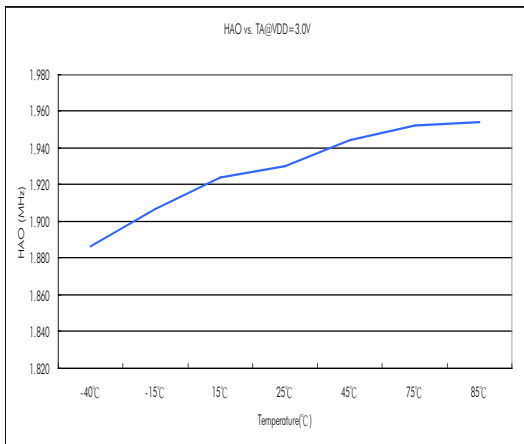


Figure 6.2-3 HAO vs. Temperature

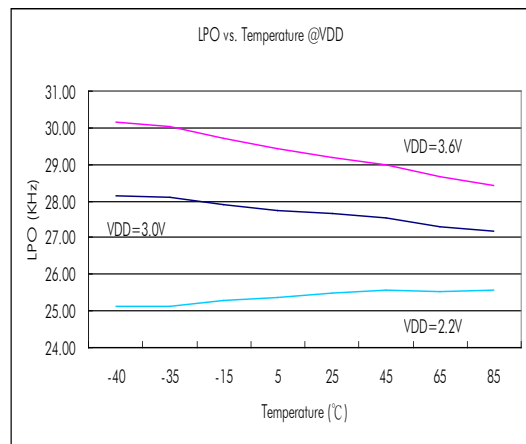


Figure 6.2-4 LPO vs. Temperature

6.3 Supply current into VDD excluding peripherals current

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, \text{OSC_LPO} = 28\text{KHz}$, unless otherwise noted

| Sym. | Parameter | Test Conditions | Min. | Typ. | Max. | unit |
|-----------|---------------|--|------|-------|------|------|
| I_{AM1} | Active mode 1 | OSC_CY = 8MHz, OSC_HAO = off, CPU_CK = 8MHz | | 1 | 2 | mA |
| I_{AM2} | Active mode 2 | OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 2MHz | | 0.28 | 0.55 | mA |
| I_{AM3} | Active mode 3 | OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 1MHz | | 0.165 | 0.3 | mA |
| I_{LP1} | Low Power 1 | OSC_CY = 32768Hz, OSC_HAO = off, CPU_CK = 16384Hz | | 7 | 12 | uA |
| I_{LP2} | Low Power 2 | OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state | | 1.65 | 3 | uA |
| I_{LP3} | Low Power 3 | OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state | | 0.65 | 1.2 | uA |

OSC_CY : External Oscillator frequency.

OSC_HAO : Internal High Accuracy Oscillator frequency.

CPU_CK : CPU core work frequency.

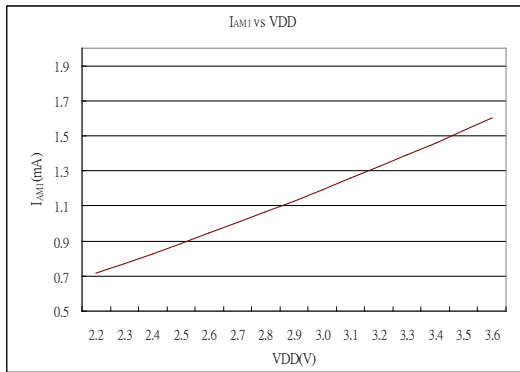


Figure 6.3-1 I_{AM1} vs. VDD

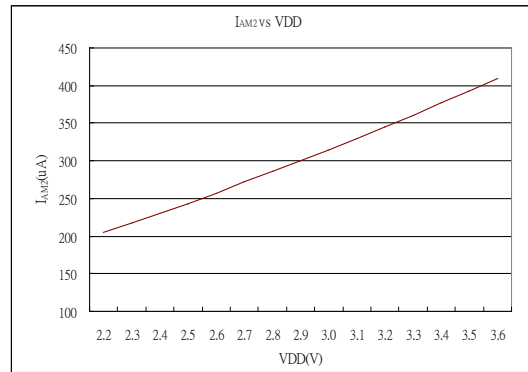


Figure 6.3-2 I_{AM2} vs. VDD

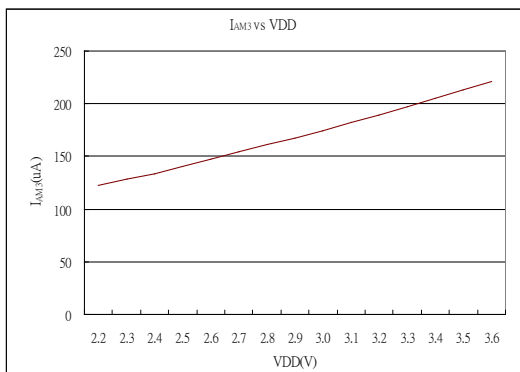


Figure 6.3-3 I_{AM3} vs. VDD

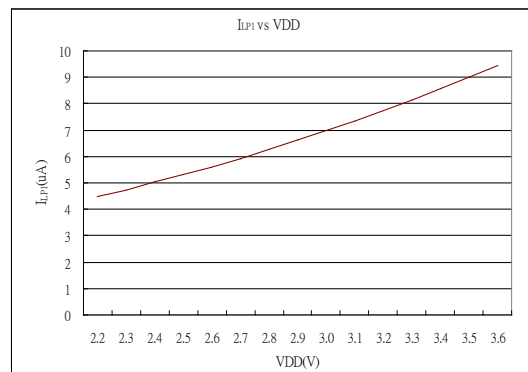


Figure 6.3-4 I_{LP1} vs. VDD

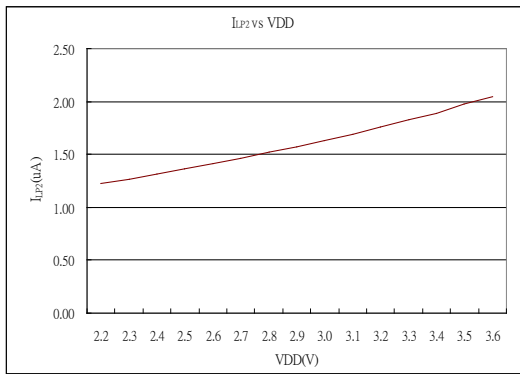


Figure 6.3-5 I_{LP2} vs. VDD

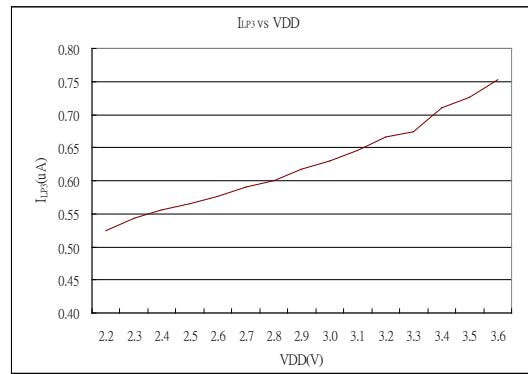


Figure 6.3-6 I_{LP3} vs. VDD

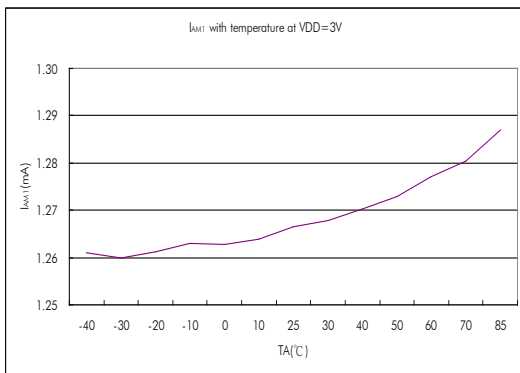


Figure 6.3-7 I_{AM1} vs. Temperature

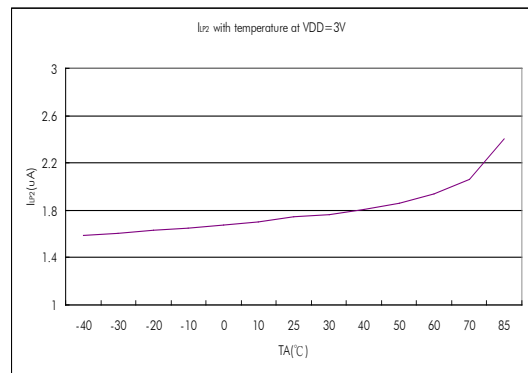


Figure 6.3-8 I_{LP2} vs. Temperature

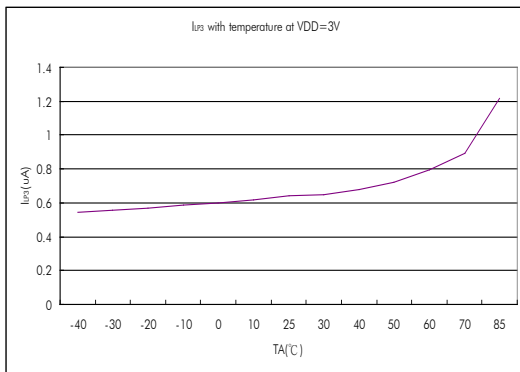


Figure 6.3-9 I_{LP3} vs. Temperature

6.4 Port1~2

$T_A = 25^{\circ}\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

| Sym. | Parameter | Test Conditions | Min. | Typ. | Max. | unit |
|---|---|-----------------------|----------------|------|----------------|------------------|
| Input voltage and Schmitt trigger and leakage current and timing | | | | | | |
| V_{IH} | High-Level input voltage | | | | 2.1 | V |
| V_{IL} | Low-Level input voltage | | 0.9 | | | |
| V_{hys} | Input Voltage hysteresis($V_{IH} - V_{IL}$) | | | 0.8 | | V |
| I_{LKG} | Leakage Current | | | | 0.1 | μA |
| R_{PU} | Port pull high resistance | | | 180 | | $\text{k}\Omega$ |
| Output voltage and current and frequency | | | | | | |
| V_{OH} | High-level output voltage | $I_{OH}=10\text{mA}$ | $V_{DD} - 0.3$ | | | V |
| V_{OL} | Low-level output voltage | $I_{OL}=-10\text{mA}$ | | | $V_{SS} + 0.3$ | |

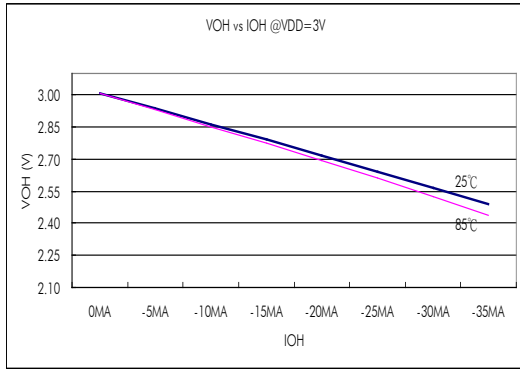


Figure 6.4-1 V_{OH} vs. I_{OH} @ $V_{DD}=3.0\text{V}$

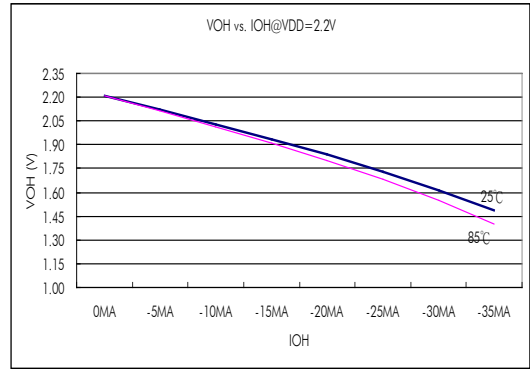


Figure 6.4-2 V_{OH} vs. I_{OH} @ $V_{DD}=2.2\text{V}$

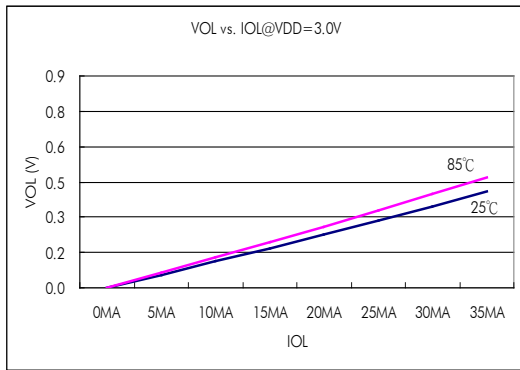


Figure 6.4-3 V_{OL} vs. I_{OL} @ $V_{DD}=3.0\text{V}$

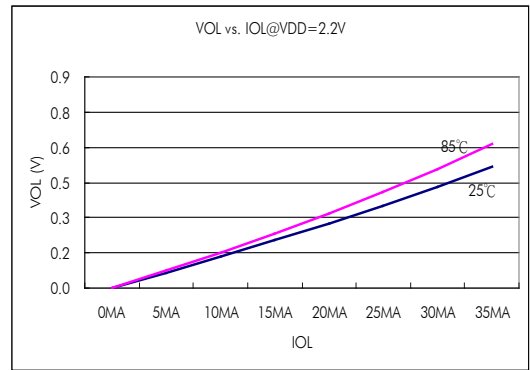


Figure 6.4-4 V_{OL} vs. I_{OL} @ $V_{DD}=2.2\text{V}$

6.5 Reset(Brownout, External RST pin, Low Voltage Detect)

$T_A = 25^{\circ}\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

| Sym. | Parameter | Test Conditions | Min. | Typ. | Max. | unit | |
|--|--|---|------|------|------|-------------------------|--|
| BOR | Pulse length needed to accepted reset internally, t_{d-LVR} | | 2 | | | us | |
| | V_{DD} Start Voltage to accepted reset internally (L→H), V_{LVR} | | 1.6 | 1.85 | 2.1 | V | |
| | Hysteresis, $V_{HYS-LVR}$ | | | 70 | | mV | |
| RST | Pulse length needed as RST/VPP pin to accepted reset internally, t_{d-RST} | | 2 | | | us | |
| | Input Voltage to accepted reset internally | | 0.9 | | | V | |
| | Hysteresis, $V_{HYS-RST}$ | | | 0.8 | | V | |
| LVD | Operation current, I_{LVD} | | | 10 | 15 | uA | |
| | External input voltage to compare reference voltage | | | 1.2 | | V | |
| | Compare reference voltage temperature drift | $T_A = -40^{\circ}\text{C} \sim 85^{\circ}\text{C}$ | | 100 | | ppm/ $^{\circ}\text{C}$ | |
| | Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1110b | | | 3.3 | | V | |
| | Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1101b | | | 3.2 | | | |
| | Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1100b | | | 3.1 | | | |
| | Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1011b | | | 3.0 | | | |
| | Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1010b | | | 2.9 | | | |
| | Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1001b | | | 2.8 | | | |
| | Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=1000b | | | 2.7 | | | |
| | Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0111b | | | 2.6 | | | |
| | Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0110b | | | 2.5 | | | |
| | Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0101b | | | 2.4 | | | |
| | Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0100b | | | 2.3 | | | |
| | Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0011b | | | 2.2 | | | |
| | Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0010b | | | 2.1 | | | |
| Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0001b | | | 2.0 | | | | |
| BOR : Brownout Reset LVR : Low Voltage Reset of BOR LVD : Low Voltage Detect RST : External Reset pin | | | | | | | |

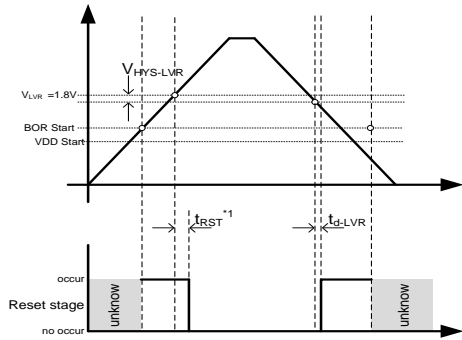


Figure6.5-1 BOR reset diagram

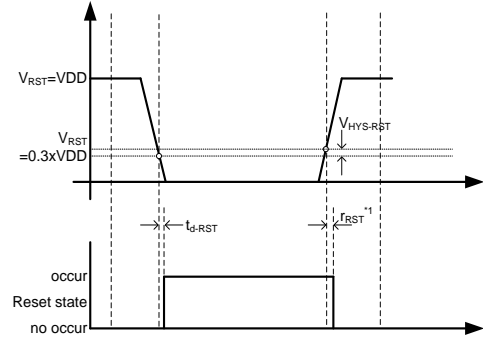


Figure6.5-2 RST reset diagram

*1 t_{RST} : Please see BOR Introduce of HY11Pxx series User's Guide (UG-HY11S14-Vxx).

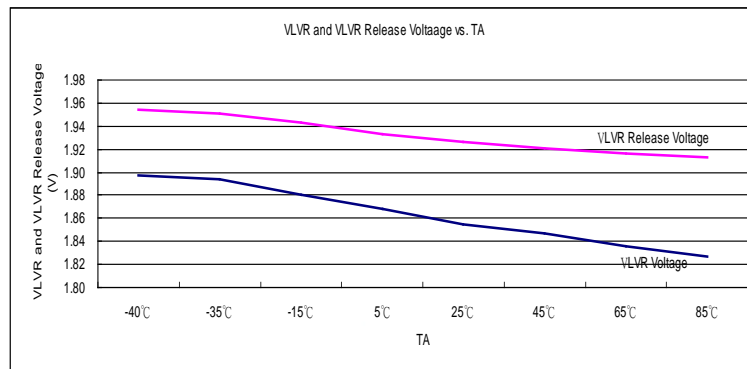


Figure6.5-3 LVR vs. Temperature

6.6 Power System

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

| Sym. | Parameter | Test Conditions | | Min. | Typ. | Max. | unit |
|------------------------|------------------------------------|---|---|-----------|------|------|------------------------|
| VDDA | VDDA operation current, I_{VDDA} | $I_L = 0\text{mA}$ | VDDAX[1:0]=00b | | 22 | | μA |
| | Select VDDA output voltage | $I_L = 0.1\text{mA}$, $V_{DD} \geq V_{DDA} + 0.2\text{V}$ | VDDAX [1:0]=00b | | 3.3 | | V |
| | | | VDDAX [1:0]=01b | | 2.9 | | V |
| | | | VDDAX [1:0]=10b | | 2.6 | | V |
| | | | VDDAX [1:0]=11b | | 2.4 | | V |
| | Dropout voltage | $I_L = 10\text{mA}$ | VDDAX [1:0]=00b | | 135 | | mV |
| | | | VDDAX [1:0]=01b | | 150 | | mV |
| | | | VDDAX [1:0]=10b | | 165 | | mV |
| | | | VDDAX [1:0]=11b | | 180 | | mV |
| | Temperature drift | VDDAX [1:0]=11b | $T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$ | | 50 | | ppm/ $^\circ\text{C}$ |
| V_{DD} Voltage drift | $I_L = 0.1\text{mA}$ | $V_{DD} = 2.5\text{V} \sim 3.6\text{V}$ | | ± 0.2 | | %/V | |
| ACM | ACM operation current, I_{ACM} | $I_L = 0\text{mA}$ | | | 20 | | μA |
| | Output voltage, V_{ACM} | ENACM[0]=1 | $I_L = 0\mu\text{A}$ | | 1.0 | | V |
| | Output voltage with Load | | $I_L = \pm 200\mu\text{A}$ | 0.98 | | 1.02 | V_{ACM} |
| | Temperature drift | ENACM[0]=1, | $T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$ | | 50 | | ppm/ $^\circ\text{C}$ |
| | VDDA Voltage drift | $I_L = 10\mu\text{A}$ | | | 100 | | $\mu\text{V}/\text{V}$ |

VDDA : Adjust Voltage Regulator
 ACM : Analog Common Mode Voltage

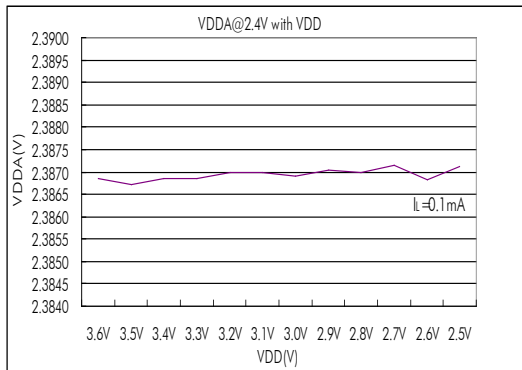


Figure6.6-1 VDDA $I_L=0.1\text{mA}$ vs. VDD

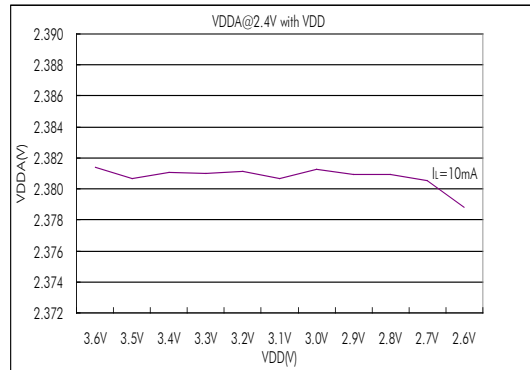


Figure6.6-2 VDDA $I_L=10\text{mA}$ vs. VDD

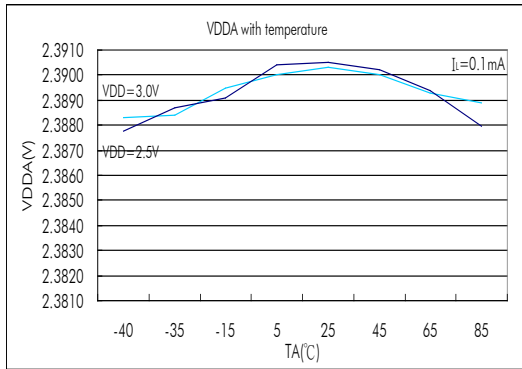


Figure6.6-3 VDDA $I_L=0.1\text{mA}$ vs. Temperature

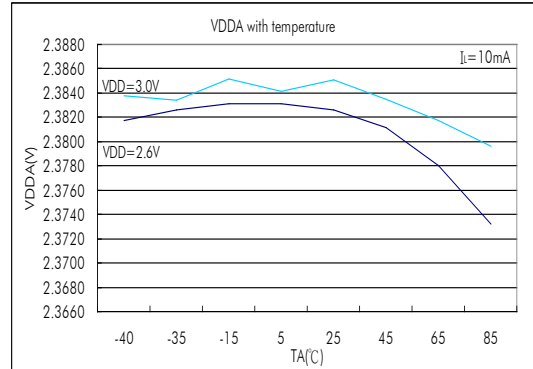


Figure6.6-4 VDDA $I_L=10\text{mA}$ vs. Temperature

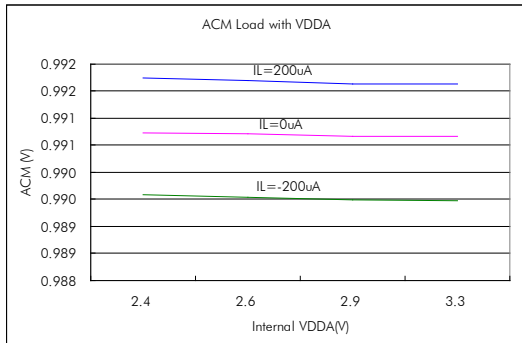


Figure6.6-5 ACM Load vs. VDDA

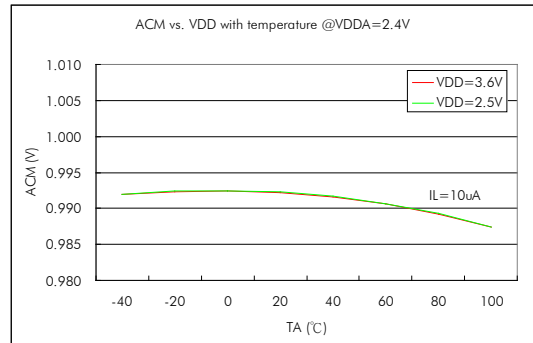


Figure6.6-6 ACM vs. Temperature

6.7 LCD

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, C_{VLCD} = 4.7\mu\text{F}$, unless otherwise noted.

| Sym. | Parameter | Test Conditions | Min. | Typ. | Max. | unit | |
|----------------|--|--|------------------------|-------|------|------------|---|
| I_{LCD} | Operation supply current without output buffer.(all segment turn on) | LCDPR[0]=1 | $V_{DD} = 2.2\text{V}$ | 10 | | uA | |
| | | | $V_{DD} = 3.0\text{V}$ | | | | |
| VLCD | Supply Voltage at VLCD pin | LCDPR[0]=0 | 2.2 | | 3.6 | V | |
| | Embedded Charge Pump output voltage at VLCD pin | $V_{DD} = 2.2\text{V}$, LCDPR[0]=1, $C_{VLCD} = 4.7\mu\text{F}$ | VLCDX[1:0]=11b | 2.295 | 2.55 | 2.805 | V |
| | | | VLCDX[1:0]=10b | 2.52 | 2.8 | 3.08 | |
| | | | VLCDX[1:0]=01b | 2.745 | 3.05 | 3.355 | |
| VLCDX[1:0]=00b | 2.97 | 3.3 | 3.63 | | | | |
| Z_{LCD} | Output impedance with LCD buffer | $f_{LCD} = 128\text{Hz}, VLCD = 3.05\text{V}$ | | 10 | | k Ω | |

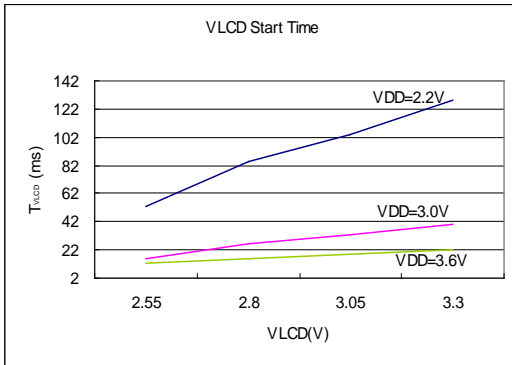


Figure6.7-1 LCD start time

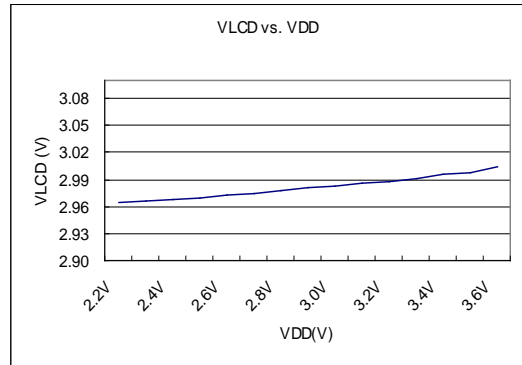


Figure6.7-2 VLCD vs. VDD

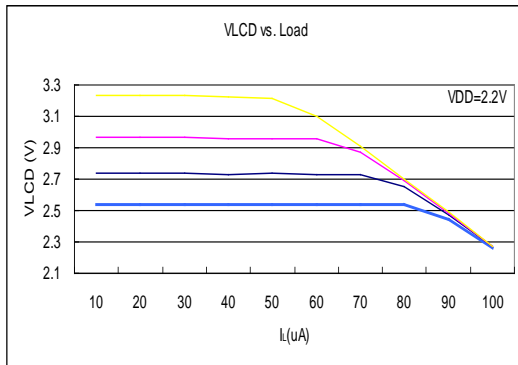


Figure6.7-3 VLCD vs. I_L @VDD=2.2V

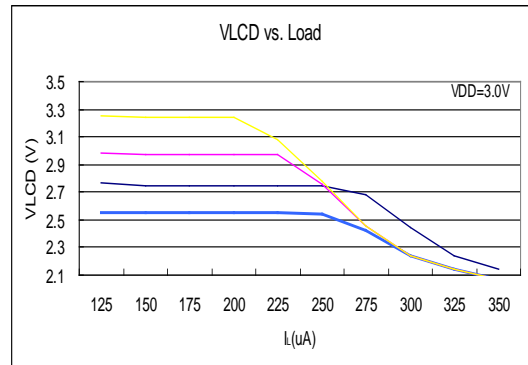


Figure6.7-4 VLCD vs. I_L @VDD=3.0V

6.8 SD18, Power Supply and recommended operating conditions

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA} = 2.4\text{V}$, unless otherwise noted

| Sym. | Parameter | Test Conditions | | Min. | Typ. | Max. | unit |
|------------|--------------------------------------|--------------------------------------|---------------------------|------|------|-------|------|
| V_{SD18} | Supply Voltage at VDDA | ENVDDA[0]=0 | | 2.4 | | 3.6 | V |
| f_{SD18} | Modulator sample frequency, ADC_CK | | | 25 | 250 | 300 | KHz |
| | Over Sample Ratio, OSR | | | 256 | | 32768 | |
| I_{SD18} | Operation supply current without PGA | ENADC[0]=1 INBUF[0]=1, VRBUF[0]=0 | GAIN =4, ADC_CK=250KHz | | | 168 | uA |
| | | ENADC[0]=1 INBUF[0]=0, VRBUF[0]=1 | | | | 150 | |
| | | ENADC[0]=1 INBUF[0]=0, VRBUF[0]=0 | | | | 120 | |

6.8.1 PGA, Power Supply and recommended operating conditions

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA} = 2.4\text{V}$, unless otherwise noted

| Sym. | Parameter | Test Conditions | | Min. | Typ. | Max. | unit |
|-----------|--------------------------|---|----------|------|------|------|--------|
| V_{PGA} | Supply Voltage at VDDA | ENVDDA[0]=0 | | 2.4 | | 3.6 | V |
| I_{PGA} | Operation supply current | PGAGN[1:0]=<01> or <1x> | | | | 320 | uA |
| G_{PGA} | Gain temperature drift | $T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$ | GAIN=128 | | | 5 | ppm/°C |

6.8.2 SD18, performance II ($f_{SD18} = 250\text{KHz}$)

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA} = 2.9\text{V}, V_{VR} = 1.0\text{V}, \text{GAIN} = 1$ without PGA, unless otherwise noted

| Sym. | Parameter | Test Conditions | | Min. | Typ. | Max. | unit |
|------------|---|---|---|------|------|-------------|--------|
| INL | Integral Nonlinearity(INL) | $V_{DDA} = 2.4\text{V}, V_{VR} = 1.0\text{V}, \Delta\text{SI} = \pm 200\text{mV}$ | | | | ± 0.003 | %FSR |
| | | $V_{DDA} = 2.4\text{V}, V_{VR} = 1.0\text{V}, \Delta\text{SI} = \pm 450\text{mV}$ | | | | ± 0.01 | |
| | No Missing Codes ³ | ADC_CK=250KHz, OSR[2:0]=010b | | 23 | | | Bits |
| G_{SD18} | Temperature drift Gain 1~x16 (INBUF[0]=0b,) Gain 1~x4 (INBUF[0]=1b,) | INBUF[0]=0b, VRBUF[0]=0b | $T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$ | | | 2 | ppm/°C |
| | | INBUF[0]=1b, VRBUF[0]=0b | | | | | |
| | | INBUF[0]=0b, VRBUF[0]=1b | | | | | |
| | | INBUF[0]=1b, VRBUF[0]=1b | | | | | |
| E_{OS} | Offset error of Full Scale Rang input voltage range with Chopper and Buffer(INBUF, VRBUF) without PGA | $\Delta\text{AI} = 0\text{V}$ $\Delta\text{VR} = 0.9\text{V}$ | Gain=2 | | | 1 | %FSR |
| | Offset error of Full Scale Rang input voltage range with Chopper without PGA and Buffer(INBUF, VRBUF) | DCSET[2:0]=<000> * ΔAI is external short | Gain=2 | | | 1 | |

HY11P12

Embedded 18-Bit $\Sigma\Delta$ ADC

8-Bit RISC-like Mixed Signal Microcontroller

| | | | | | | | | | |
|---------------------------|---|--|-------------------|-----------------------|-------|--|---------------------------------|----|----|
| CM _{SD18} | Offset temperature drift with chopper without PGA and Buffer (INBUF,VRBUF). | | GAIN=1 | 2 | uV/°C | | | | |
| | | | GAIN=2 | 1 | | | | | |
| | | | GAIN=4 | 0.5 | | | | | |
| | Offset temperature drift with chopper and Buffer (INBUF,VRBUF) without PGA. | GAIN=1 | 2 | | | | | | |
| | | GAIN=2 | 1 | | | | | | |
| | | GAIN=4 | 0.5 | | | | | | |
| | Offset temperature drift with chopper without Buffer (INBUF,VRBUF). | | | GAIN=128 | | 0.02 | | | |
| | | | | Common-mode rejection | | V _{CM} =0.7V to 1.7V, V _{VR} =1.0V, without PGA | V _{SI} =0V, GAIN=1 | 90 | dB |
| | | | | | | V _{CM} =0.7V to 1.7V, V _{VR} =1.0V, without PGA | V _{SI} =0V, GAIN=16 | 75 | |
| DC power supply rejection | | V _D DA=3.0V, Δ V _D DA=±100mV, V _{VR} =1.0V, V _{SI} =1.2V, V _{SI} =1.2V, | GAIN=1 PGA=off | 75 | dB | | | | |
| | | | GAIN=16 PGA=8 | | | | | | |

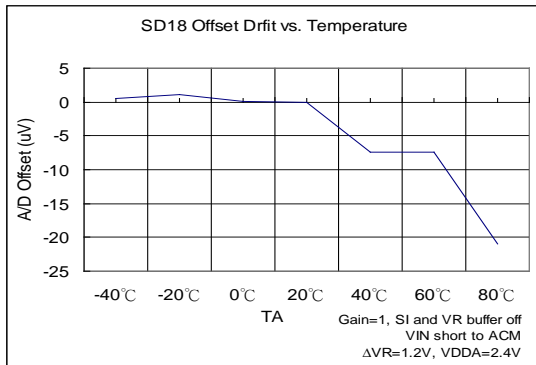


Figure 6.8-1(a) SD18 Offset Temperature drift

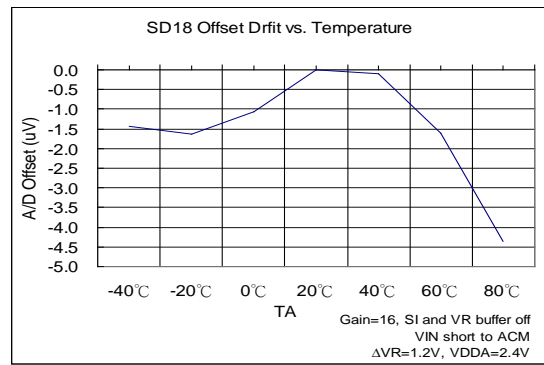


Figure 6.8-1(b) SD18 Offset Temperature drift

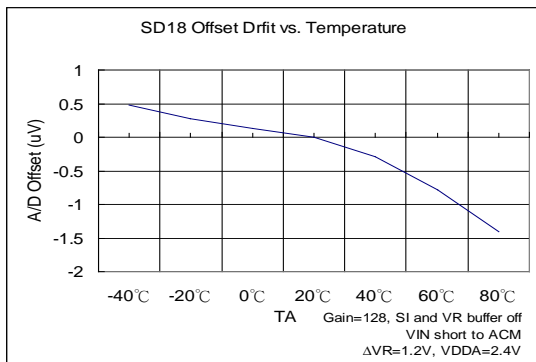


Figure 6.8-1(c) SD18 Offset Temperature drift

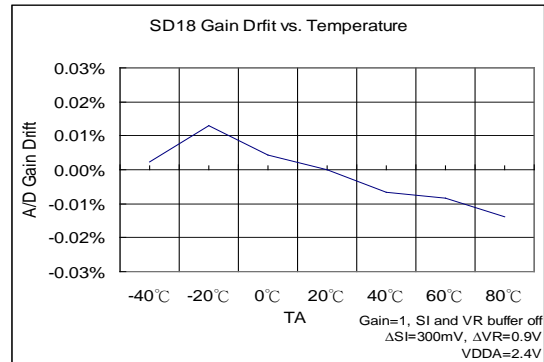


Figure 6.8-2(a) SD18 Gain drift with temperature

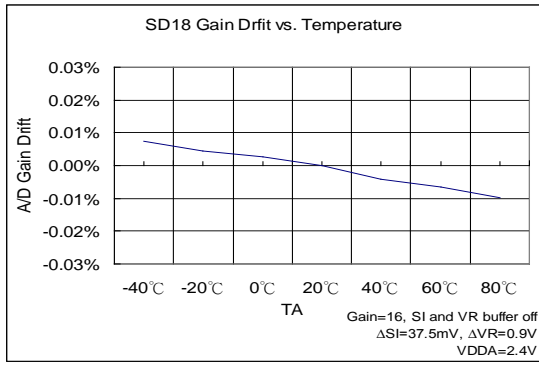


Figure6.8-2(b) SD18 Gain drift with temperature

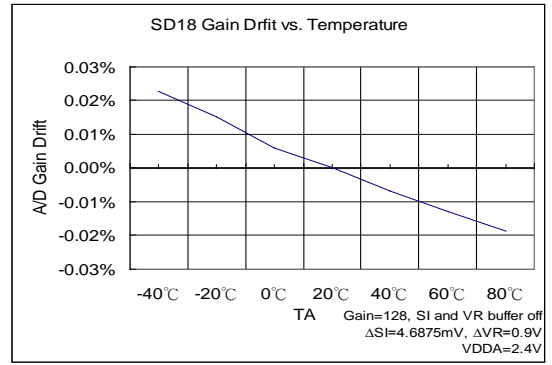


Figure6.8-2(c) SD18 Gain drift with temperature

6.8.3 SD18, Temperature sensor

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA} = 2.4\text{V}$, unless otherwise noted

| Sym. | Parameter | Test Conditions | Min. | Typ. | Max. | unit |
|-------------------|--|--|------|---------|------|------------------------------|
| TC _S | Sensor temperature drift | $\Delta V_R = 2.4\text{V}, V_{RGN}[0] = 1,$ | | 178 | | $\mu\text{V}/^\circ\text{C}$ |
| KT | Absolute Temperature Scale 0°K | INBUF[0]=1 | | -289 | | $^\circ\text{C}$ |
| TC _{ERR} | One point calibrate error temperature | Calibration at 25°C of $-40^\circ\text{C} \sim 85^\circ\text{C}$ | | ± 2 | | $^\circ\text{C}$ |

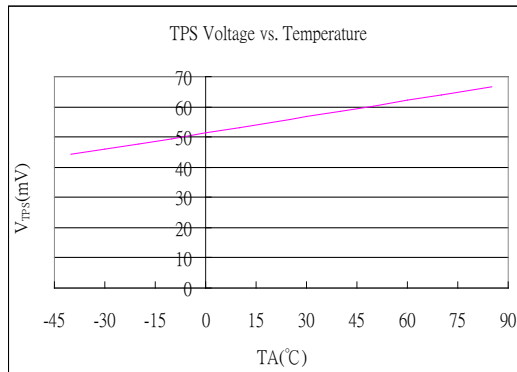


Figure 6.8-3 TPS output voltage vs. temperature drift

6.8.4 SD18 Noise Performance

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA} = 2.4\text{V}$, unless otherwise noted

HY11P12 針對 SD18 提供了重要的輸入雜訊規格。Table6.8-4(a), Table6.8-4(b) 列出典型的雜訊規格表與 Gain, Output rate, 及單端最大輸入電壓等關係。測試條件設定在外部輸入訊號短路，參考電壓為 1.2V，取樣 1024 筆資料。

| ENOB(RMS) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V | | | | | | | | | | | | | |
|--|-----------------|---|-----|---|------|------|------|------|------|------|------|-------|-------|
| Max. Vin(mV) =0.9*VREF ⁽¹⁾ | OSR | | | | | 256 | 512 | 1024 | 2048 | 4096 | 8192 | 16384 | 32768 |
| | Output rate(HZ) | | | | | 977 | 488 | 244 | 122 | 61 | 31 | 15 | 8 |
| | Gain | = | PGA | x | ADGN | | | | | | | | |
| ±2400 | 0.25 | = | 1 | x | 0.25 | 16.3 | 17.4 | 17.9 | 18.5 | 19.0 | 19.5 | 20.0 | 20.4 |
| ±2160 | 0.5 | = | 1 | x | 0.5 | 16.3 | 17.3 | 17.9 | 18.4 | 18.9 | 19.4 | 19.8 | 20.2 |
| ±1080 | 1 | = | 1 | x | 1 | 16.2 | 17.2 | 17.8 | 18.3 | 18.8 | 19.3 | 19.7 | 20.1 |
| ±540 | 2 | = | 1 | x | 2 | 16.1 | 17.1 | 17.6 | 18.2 | 18.7 | 19.2 | 19.6 | 20.0 |
| ±270 | 4 | = | 1 | x | 4 | 16.0 | 16.9 | 17.5 | 18.0 | 18.5 | 18.9 | 19.4 | 19.8 |
| ±135 | 8 | = | 1 | x | 8 | 15.9 | 16.6 | 17.2 | 17.7 | 18.2 | 18.7 | 19.2 | 19.6 |
| ±68 | 16 | = | 1 | x | 16 | 15.6 | 16.3 | 16.8 | 17.3 | 17.7 | 18.3 | 18.8 | 19.3 |
| ±34 | 32 | = | 2 | x | 16 | 14.8 | 15.3 | 15.9 | 16.4 | 16.9 | 17.4 | 17.8 | 18.3 |
| ±17 | 64 | = | 4 | x | 16 | 14.5 | 15.0 | 15.5 | 16.0 | 16.5 | 17.0 | 17.5 | 18.0 |
| ±8 | 128 | = | 8 | x | 16 | 14.0 | 14.6 | 15.1 | 15.6 | 16.0 | 16.6 | 17.0 | 17.5 |

(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).

Table6.8-4(a) SD18 ENOB Table

| RMS Noise(uV) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V | | | | | | | | | | | | | |
|--|-----------------|---|-----|---|------|--------|-------|-------|-------|-------|-------|-------|-------|
| Max. Vin(mV) =0.9*VREF | OSR | | | | | 256 | 512 | 1024 | 2048 | 4096 | 8192 | 16384 | 32768 |
| | Output rate(HZ) | | | | | 977 | 488 | 244 | 122 | 61 | 31 | 15 | 8 |
| | Gain | = | PGA | x | ADGN | | | | | | | | |
| ±2400 | 0.25 | = | 1 | x | 0.25 | 121.08 | 57.40 | 38.74 | 26.66 | 18.39 | 13.21 | 9.49 | 6.98 |
| ±2160 | 0.5 | = | 1 | x | 0.5 | 61.63 | 29.23 | 19.21 | 13.51 | 9.78 | 7.02 | 5.12 | 3.91 |
| ±1080 | 1 | = | 1 | x | 1 | 32.21 | 15.70 | 10.25 | 7.31 | 5.19 | 3.77 | 2.80 | 2.13 |
| ±540 | 2 | = | 1 | x | 2 | 16.59 | 8.54 | 5.91 | 4.06 | 2.86 | 2.06 | 1.48 | 1.12 |
| ±270 | 4 | = | 1 | x | 4 | 9.00 | 4.84 | 3.33 | 2.37 | 1.67 | 1.19 | 0.87 | 0.65 |
| ±135 | 8 | = | 1 | x | 8 | 5.04 | 2.97 | 2.02 | 1.44 | 1.01 | 0.73 | 0.51 | 0.39 |
| ±68 | 16 | = | 1 | x | 16 | 3.03 | 1.84 | 1.29 | 0.92 | 0.70 | 0.46 | 0.33 | 0.24 |
| ±34 | 32 | = | 2 | x | 16 | 2.61 | 1.81 | 1.27 | 0.89 | 0.62 | 0.45 | 0.32 | 0.23 |
| ±17 | 64 | = | 4 | x | 16 | 1.66 | 1.13 | 0.80 | 0.56 | 0.41 | 0.29 | 0.20 | 0.14 |
| ±8 | 128 | = | 8 | x | 16 | 1.13 | 0.77 | 0.55 | 0.38 | 0.28 | 0.19 | 0.14 | 0.10 |

Table6.8-4(b) SD18 RMS Noise Table

The RMS noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$\text{ENOB(RMS)} = \frac{\ln\left(\frac{\text{FSR}}{\text{RMS Noise}}\right)}{\ln(2)}$$

$$\text{RMS Noise} = \frac{\left(2 \times \text{VREF} \times \sqrt{\sum_{k=1}^{1024} (\text{ADO}[k] - \text{Average})^2}\right)}{2^{23}}$$

Where FSR (Full - Scale Range) = $2 \times \text{VREF}/\text{Gain}$.

$$\text{Average} = \frac{\sum_{k=1}^{1024} (\text{ADO}[k])}{1024}$$

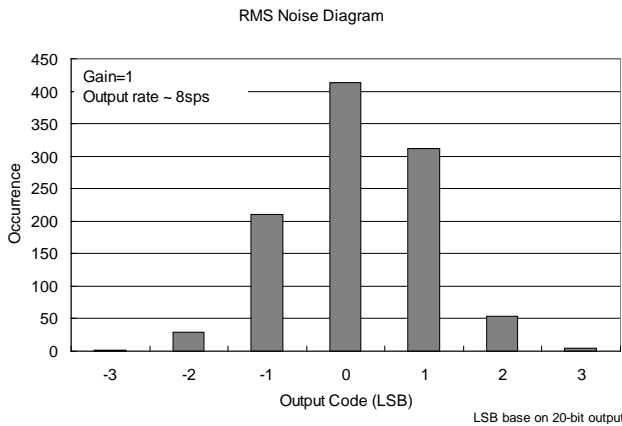


Figure6.8-4(a) RMS Noise Diagram

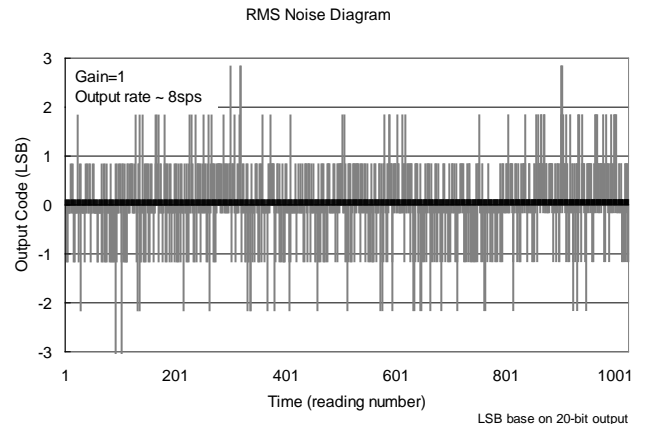


Figure6.8-4(b) Output Code Diagram

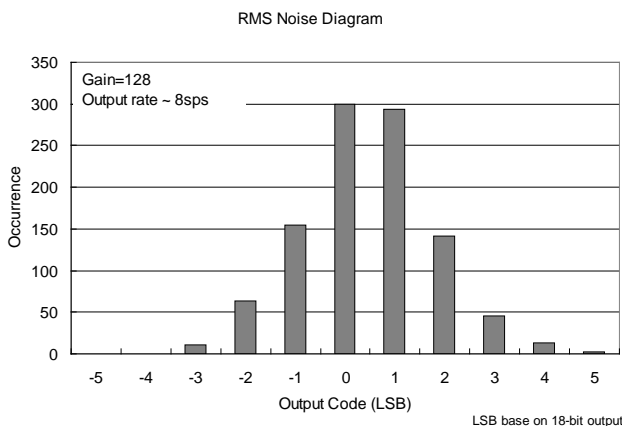


Figure6.8-4(c) RMS Noise Diagram

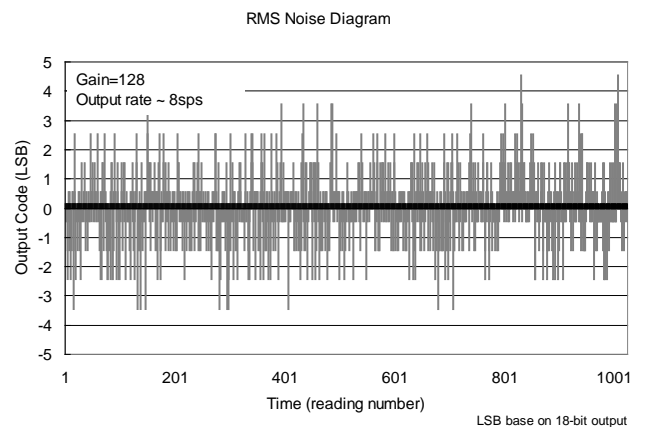


Figure6.8-4(d) Output Code Diagram

7. 訂貨資訊

| 下單品名 ¹ | 封裝型式 | 引腳數 | 封裝型式 | | 程式碼 編號 ² | 出貨包裝 形式 | 個裝 數量 | 材料 組成 | MSL ³ |
|-------------------|------|-----|------|-----|------------------------|-------------|----------|--------------------|------------------|
| | | | 描述方式 | | | | | | |
| HY11P12-D000 | Die | - | D | 000 | 000 | - | 200 | Green ⁴ | - |
| HY11P12-L044 | LQFP | 44 | L | 044 | 000 | Tray | 160 | Green ⁴ | MSL-3 |
| HY11P12-L048 | LQFP | 48 | L | 048 | 000 | Tray | 250 | Green ⁴ | MSL-3 |
| HY11P12-N048 | QFN | 48 | N | 048 | 000 | Tape & Reel | 3000 | Green ⁴ | MSL-3 |

¹ 產品名稱 – 封裝型式描述方式 – 程式碼編號（空白片 / 標準品 / 代客燒錄碼）

例如：您的代客燒錄服務申請的程式碼編號為 008，且需要的產品是裸片出貨。則下單品名為 HY11P12-D000-008

例如：您的需求是不帶程式碼的空白片且需要的產品是裸片出貨。則下單品名為 HY11P12-D000

例如：您的需求是不帶程式碼的空白片且需要的產品是封裝片LQFP44 出貨，則下單品名為HY11P12-L044，且需以 Tray出貨，則除下單品名外，請特別註明出貨包裝形式為 Tray

例如：您的代客燒錄服務申請的程式碼編號為 009，而需求的產品是封裝片LQFP48 出貨，則下單品名為HY11P12-L048-009，且需以 Tray出貨，則除下單品名外，請特別註明出貨包裝形式為 Tray

² 程式碼編號

“001”~“999” 為標準品或代客燒錄申請的程式碼編號，而空白晶片不帶此碼。

³ MSL:

濕度敏感性等級係依據 IPC/JEDEC J-STD-020 的規範加以試驗分級，並參考 IPC/JEDEC J-STD-033 的標準處理、包裝、運輸與使用。

⁴ Green (RoHS & no Cl/Br):

HYCON 產品皆為 Green Product，符合 RoHS 指令，REACH 高關注物質(SVHC) 以及無鹵素相關規定。

HY11P12

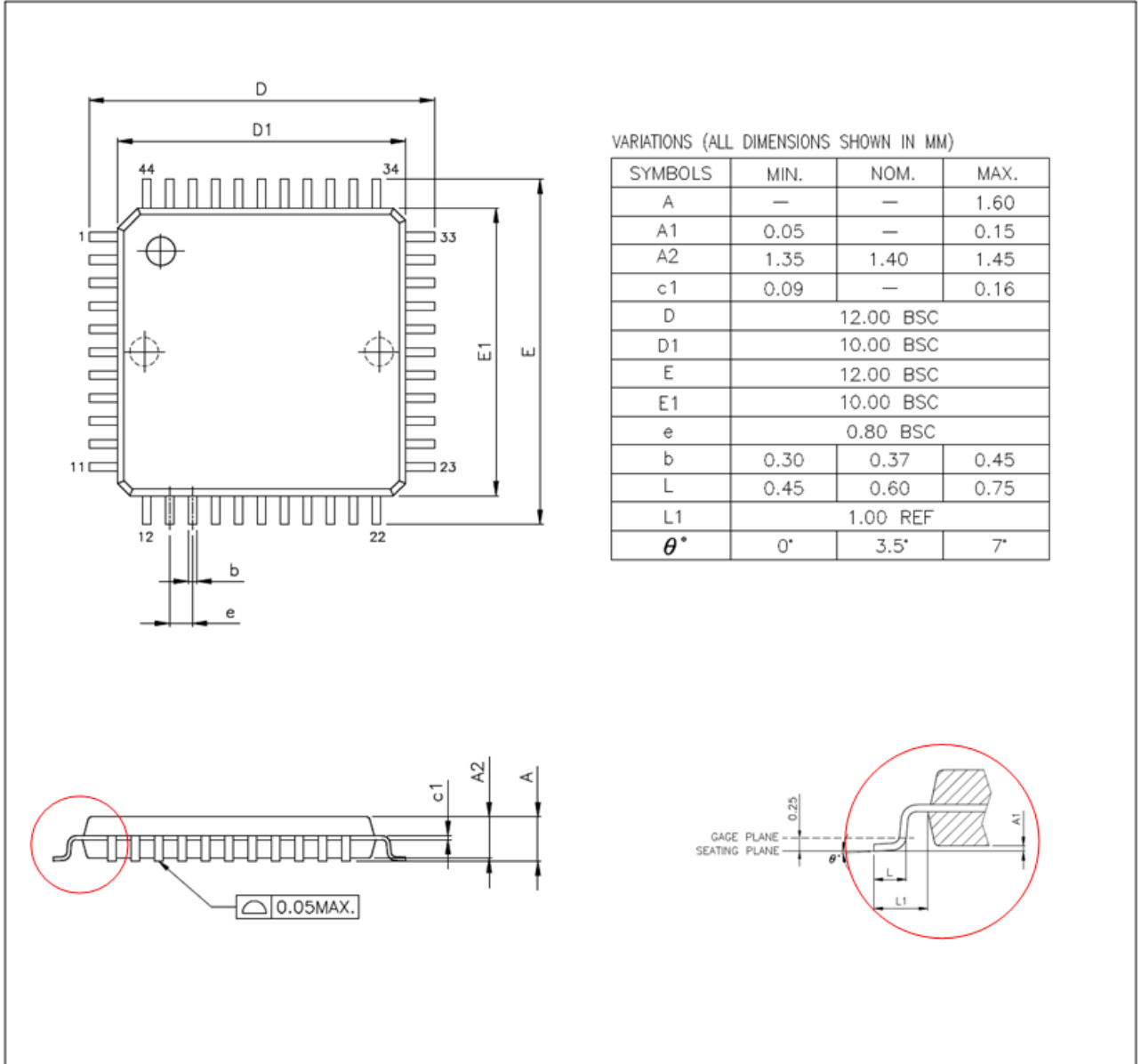
Embedded 18-Bit $\Sigma\Delta$ ADC

8-Bit RISC-like Mixed Signal Microcontroller

8. 封裝型式資訊

8.1 LQFP44(L044)

8.1.1 Package Dimensions



JEDEC MS-026 compliant

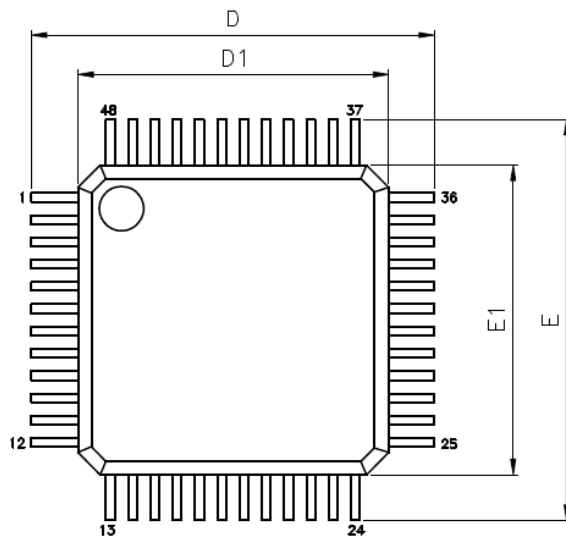
HY11P12

Embedded 18-Bit $\Sigma\Delta$ ADC

8-Bit RISC-like Mixed Signal Microcontroller

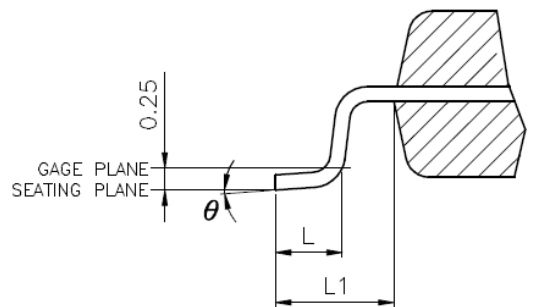
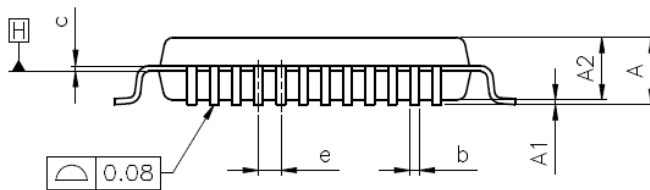
8.2 LQFP48(L048)

8.2.1 Package Dimensions



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

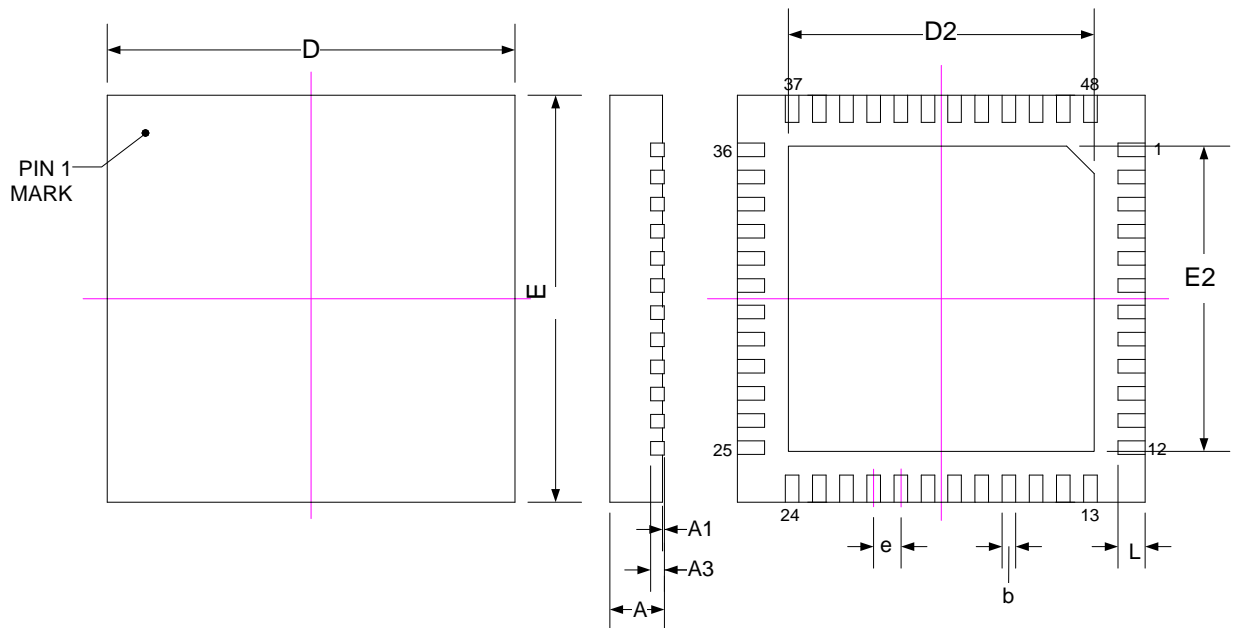
| SYMBOLS | MIN. | NOM. | MAX. |
|----------|----------|------|------|
| A | -- | -- | 1.60 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.09 | -- | 0.20 |
| D | 9.00 BSC | | |
| D1 | 7.00 BSC | | |
| E | 9.00 BSC | | |
| E1 | 7.00 BSC | | |
| e | 0.50 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF | | |
| θ | 0° | 3.5° | 7° |



JEDEC MS-026 compliant

8.3 QFN48(N048)

8.3.1 Package Dimensions



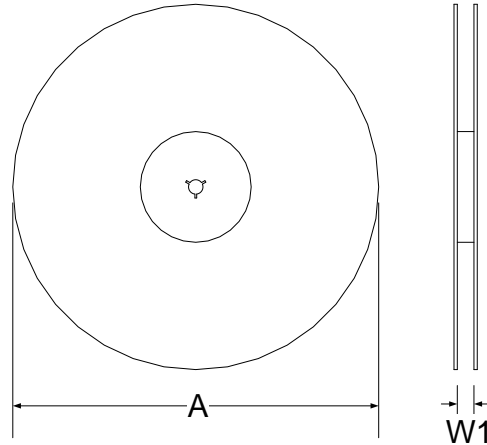
| SYMBOLS | MIN | NOM | MAX |
|---------|-----------|------|------|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.20 REF. | | |
| b | 0.15 | 0.20 | 0.25 |
| D | 6.00 BSC | | |
| E | 6.00 BSC | | |
| D2 | 4.40 | 4.50 | 4.55 |
| E2 | 4.40 | 4.50 | 4.55 |
| L | 0.35 | 0.40 | 0.45 |
| e | 0.40 BSC | | |

Note: All dimensions refer to JEDEC OUTLINE MO-220.

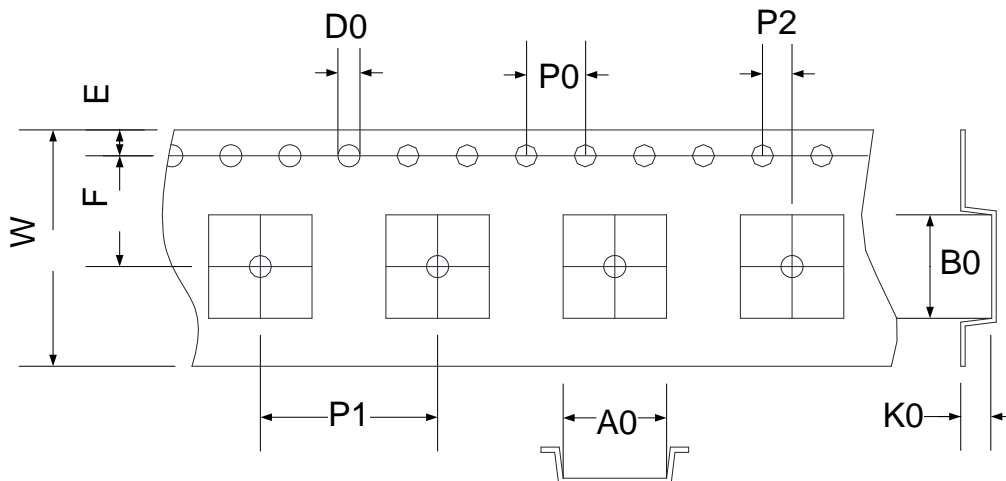
8.3.2 Tape & Reel Information

8.3.2.1 Reel Dimensions –Type1

Unit : mm



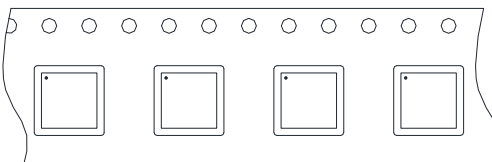
8.3.2.2 Carrier Tape Dimensions



| SYMBOLS | Reel Dimensions | | Carrier Tape Dimensions | | | | | | | | | |
|-----------|-----------------|---------|-------------------------|------------|------------|------------|------------|------------|------------|------------|---------|------------|
| | A | W1 | A0 | B0 | K0 | P0 | P1 | P2 | E | F | D0 | W |
| Spec. | 330 | 16.5 | 6.30 | 6.30 | 1.10 | 4.00 | 12.00 | 2.00 | 1.75 | 7.50 | 1.50 | 16.00 |
| Tolerance | +6/-3 | +1.5/-0 | ± 0.10 | ± 0.10 | ± 0.10 | ± 0.10 | ± 0.10 | ± 0.10 | ± 0.10 | ± 0.10 | +0.1/-0 | ± 0.30 |

Note: 10 Sprocket hole pitch cumulative tolerance is ± 0.20 mm.

8.3.2.3 Pin1 direction



9. 修訂記錄

以下描述本文件差異較大的地方，而標點符號與字形的改變不在此描述範圍。

| 版本 | 頁次 | 變更摘要 |
|-----|-------|--|
| V01 | ALL | 初版發行 |
| V02 | ALL | 全面變更內容 |
| V03 | 5~10 | 第 2、3、4 章節順序調整 |
| | 17 | 修訂 6.5 章節；移除關於 LVD 描述外部輸入比較電壓的規格以符合實際產品功能。 |
| | 24 | 修訂 7 章節；轉為中文資訊且編修欄位與內容 |
| | 26 | 新增 9 章節；文件修訂記錄 |
| V04 | 4 | 修訂 48 個指令成 46 個指令，特點內容修改 |
| | 14 | 調整電流規格 |
| | 21 | 增加 G_{SD18} Temperature Drift 內容說明 |
| V05 | 4 | 修訂特點內容 |
| | 6 | 修訂 I/O 定義與說明內容 |
| | 10 | 修訂暫存器列表 |
| | 17 | 修訂 Reset 內容 |
| | 19 | 修訂 Power System 內容 |
| | 20 | 修訂 Figure6.6-5, Figure6.6-6 ACM Chart |
| V06 | 6~7 | 修訂章節內容 |
| | 8~9 | 修訂電路圖 |
| | 22~24 | 修訂章節內容 |
| V07 | 11 | 修訂章節內容 |
| V08 | 1 | 修訂標題文字 |
| | 5 | 修訂引腳圖，增加 LVDIN 引腳 |
| | 8~9 | 修訂應用電路圖，增加 LVDIN 引腳 |
| V09 | 4 | 修訂特點內容，刪除 1/2bias 說明 |
| | 5 | 增加註 3 內容說明 |
| | 8~9 | 修訂應用電路圖，增加 RST 的 RC 電路 |
| | 10 | 增加內部方塊圖中 LVDIN 引腳 |
| V10 | 11 | 增加 SD18 Network 章節 |
| | 20 | 修訂 Power System 溫飄規格 |
| | 26~27 | 增加 SD18 Noise Performance 章節 |
| V11 | 5 | 修改 1.特點內容 |
| | 9 | 修改圖 3-2 內容 |
| | 14 | 修改 6.電氣特性內容 |
| | 28 | 修改 RMS Noise Diagram |

HY11P12

Embedded 18-Bit Σ ADC

8-Bit RISC-like Mixed Signal Microcontroller

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| V12 | 3 | 刪除空白頁 |
| | 22 | 修改I _{LCD} 電流規格 |
| V13 | 6 | 增加 LQFP48 引腳圖 |
| | 12 | 修改圖 4-2 INH/INL |
| | 30 | 增加訂貨資訊 |
| | 32 | 增加封裝型式資料 |
| V14 | 11 | 修改開發工具相關使用說明書編號 |
| | 30 | 增加訂貨資訊內容 |
| V15 | 8 | 增加 QFN48 引腳圖 |
| | 11~12 | 增加 I/O 定義與說明(LQFP48/QFN48) |
| | 34 | 增加訂貨資訊 |
| | 37 | 增加封裝型式資訊 |
| V16 | 13 | 新增封裝型式與正印說明 |
| | 35 | 更新 Green (RoHS & no Cl/Br) |
| | 39 | 新增 Tape & Reel Information |