HYCON TECHNOLOGY

50/60Hz Rejection Solution

For HY11P Series

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1. Brief Introduction

For high accuracy products that use AC power, the 50/60 Hz power noise will be measured due to the equal quantity noise is inputted to the signal end. If 50/60 Hz Normal Mode Rejection of the measuring system is not good, it will cause the measuring result not stable. To solve such a problem, except enhance the filter capacity of the power line for general products, it is also a common method to make the digital filter by software.

For HY11P series ADC, the built-in digital filter is the $SINC^2$ COMB Filter that uses the internal RC oscillator as its clock rate and the OSR=32768 (approximately 8 SPS output rate) so that its 50/60 Hz Normal Mode Rejection is possible only 50~60 dB. It can only reach 80dB even if makes 8 times average by software. Comparing to TI ADS1230 that uses the $SINC^4$ COMB Filter, which may achieve 100dB in 10 SPS output rate, it has the obvious difference for 50/60 Hz Normal Mode Rejection of HY11P series ADC.

This article provides the digital filter by software that enables HY11P series ADC to reach correspondingly 100 dB 50/60 Hz Normal Mode Rejection to solve the problem of AC power noise for our customers' use.

2. Theory Description

The following figure is the spectrum of SINC^4 COMB Filter in 10 sps output rate. For the COMB Filter, 10, 20, 30, 40, 50, 60Hz and so on signals will be filtered, and it reaches the signal attenuation over 95dB at least in 50~60Hz. However, if use the SINC^2 COMB Filter, although it can also filter 50/60 Hz, its signal attenuation is only 50dB in 50~60Hz.

Since HY11P can enhance ADC output rate by changing ADC OSR setup, we can make the advanced COMB Filter by software to increase ADC normal mode Rejection.

In following we realize the SINC^3/ SINC^4 COMB Filter by software and compare their 50/60Hz normal mode Rejection capacity with the original SINC^2 by hardware. We compared with approximately 1 s' output stable time (it needs 3 records for SINC^3, and 4 for SINC^4). Except the original SINC^2 OSR=32768 output, we average 8 records (SINC^1).

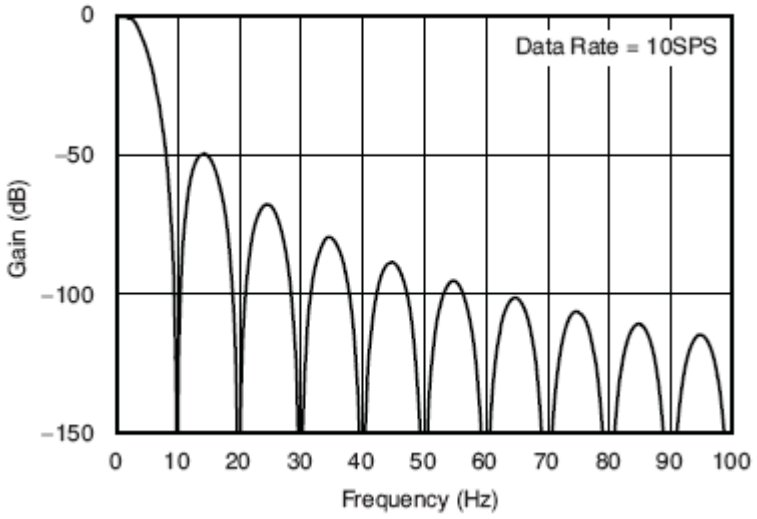


Figure 2-1

2.1. Software SINC^4 Theory

SINC^4 is composed of 4 accumulators and 4 substraters that can be regarded as 4 integrators and 4 differentiators.

Because the integrator must accumulate the average 32 times (2^5), 1 integrator needs 5 more bits Registers so that 4 integrators need 20 more bits Registers. ADC has 24 bit output, so each integrator needs 44 bits Registers. After calculating 32 records, we take Bit 20~43 output to proceed the differentiation, and each differentiator needs only 24 bits Registers, so it needs 272 bits (34 bytes) Registers at least to process the SINC^4 COMB Filter by software.

Due to the result of SINC^4 COMB Filter is obtained after 4 times of calculation, the input signal is delay for 4 records output. Therefore, if ADC Output Rate is 122Hz, it is about 3.8Hz after averaging 32 records, however, the signal is delay for 4 records, it takes 1.05 seconds from the signal input to the stable output.

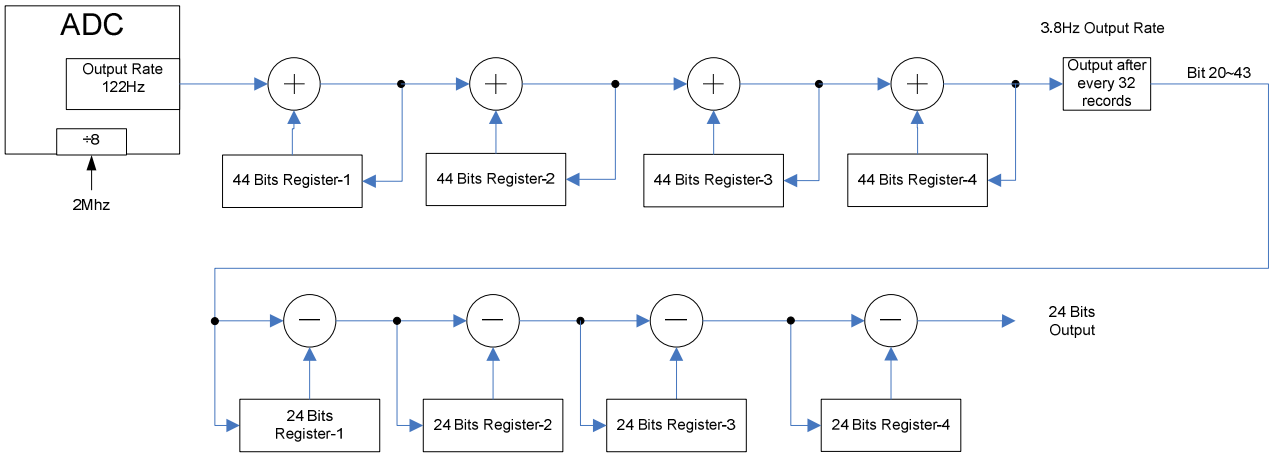


Figure 2-2 Software SINC^4 COMB Filter Diagram

2.2. Software SINC^3 Theory

SINC^3 is composed of 3 accumulators and 3 substraters that can be regarded as 3 integrators and 3 differentiators.

Because the integrator must accumulate the average 32 times (2^5), 1 integrator needs 5 more bits Registers so that 3 integrators need 15 more bits Registers. ADC has 24 bit output, so each integrator needs 39 bits Registers. After calculating 32 records, we take Bit 15~38 output to proceed the differentiation, and each differentiator needs only 24 bits Registers, so it needs 189 bits (23.6 bytes) Registers at least to process the SINC^3 COMB Filter by software.

Due to the result of SINC^3 COMB Filter is obtained after 3 times of calculation, the input signal is delay for 3 records output. Therefore, if ADC Output Rate is 122Hz, it is about 3.8Hz after averaging 32 records, however, the signal is delay for 3 records, it takes 0.79 seconds form the signal input to the stable output.

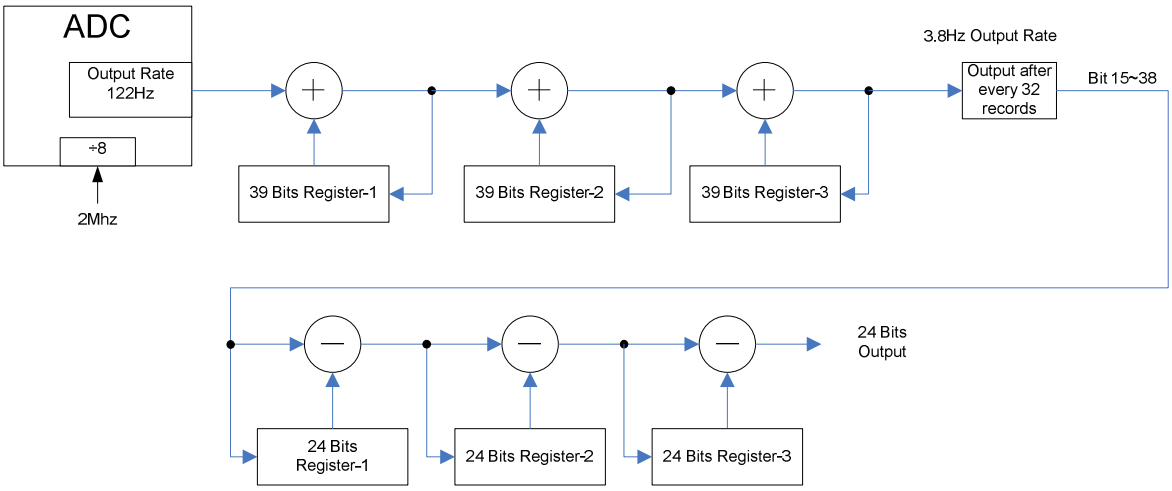


Figure 2-3 Software SINC^3 COMB Filter Diagram

3. The Difference of 50/60Hz Normal Mode Rejection in Software Average (SINC^1), Software SINC^3 and Software SINC^4

Considering the shift of the internal RC oscillating frequency in HY11P series, we test the frequency from 40~70Hz to compare the normal mode Rejection capacity by different ways.

3.1. The Comparison of The Normal Mode Rejection for SINC^1, SINC^3 and SINC^4 under Different Input Frequency

PGA Gain = 1，ADC Gain = 8

VDD=3.3V，VDDA = 2.93V

Input Signal = 50mV$_{RMS}$ @ 40~70Hz，DC offset 70.7mV

Hz / dB	40	41	42	44	45	46	47	48	49	50	51	52	54	55
SINC^1	-72.55	-84.87	-78.7	-97.54	-99.76	-93.41	-82.46	-80.55	-85.85	-95.4	-95.02	-85.37	-89.41	-113.4
SINC^3	-115.8	-109.3	-99.22	-113.5	-106.8	-98.9	-113.8	-115.1	-118	-113.8	-116.5	-115.3	-108.1	-118
SINC^4	-120.5	-117.1	-117.6	-118.9	-117.3	-114.9	-117.4	-118.7	-118.2	-117.3	-116.4	-120.3	-116.6	-118.4

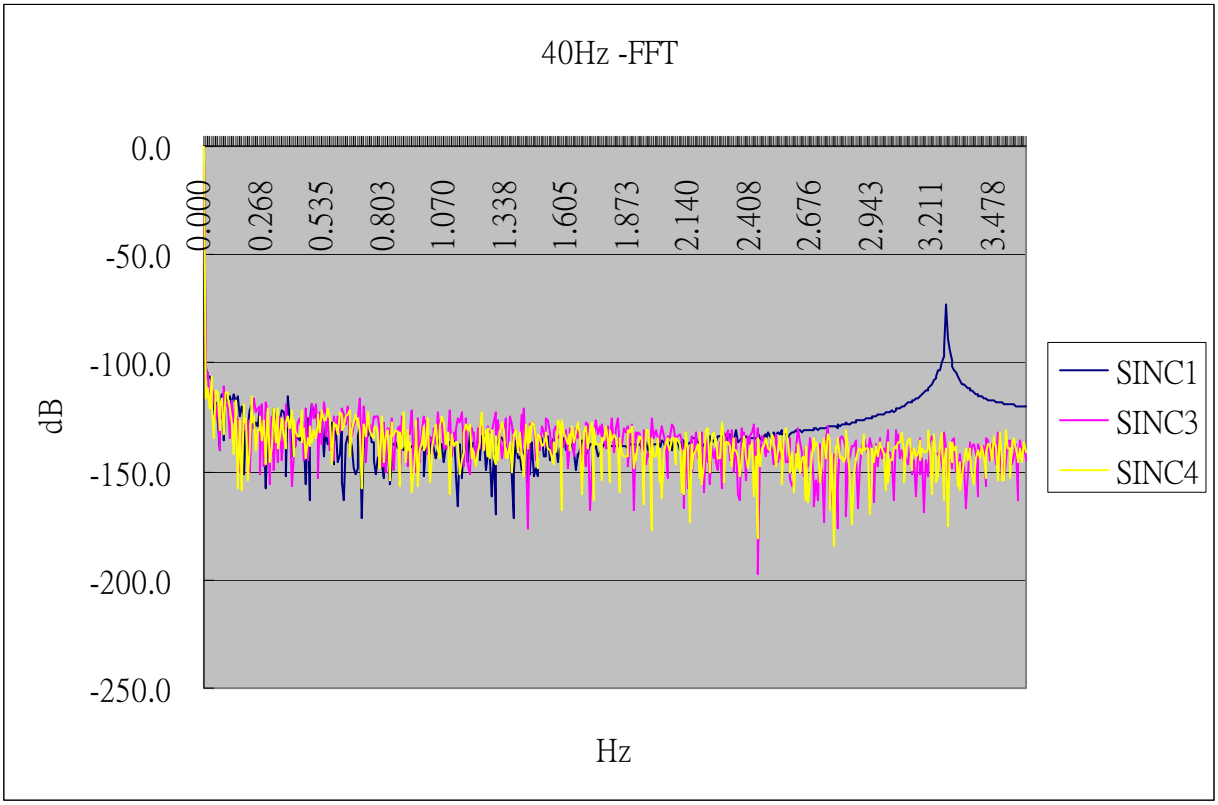
Hz / dB	56	57	58	59	60	61	62	63	64	66	68	69	70
SINC^1	-106.7	-97.01	-95.64	-85.44	-105	-84.92	-85.06	-114.8	-115	-100.4	-96.17	-82.87	-102
SINC^3	-111.1	-108.5	-117.1	-116.5	-105.1	-109.8	-113.8	-114.3	-105	-117.1	-115.9	-116.5	-118.3
SINC^4	-118.1	-118.8	-116.4	-116	-115.7	-115.8	-117.8	-117.5	-114.4	-115.8	-115.9	-117.9	-117.9

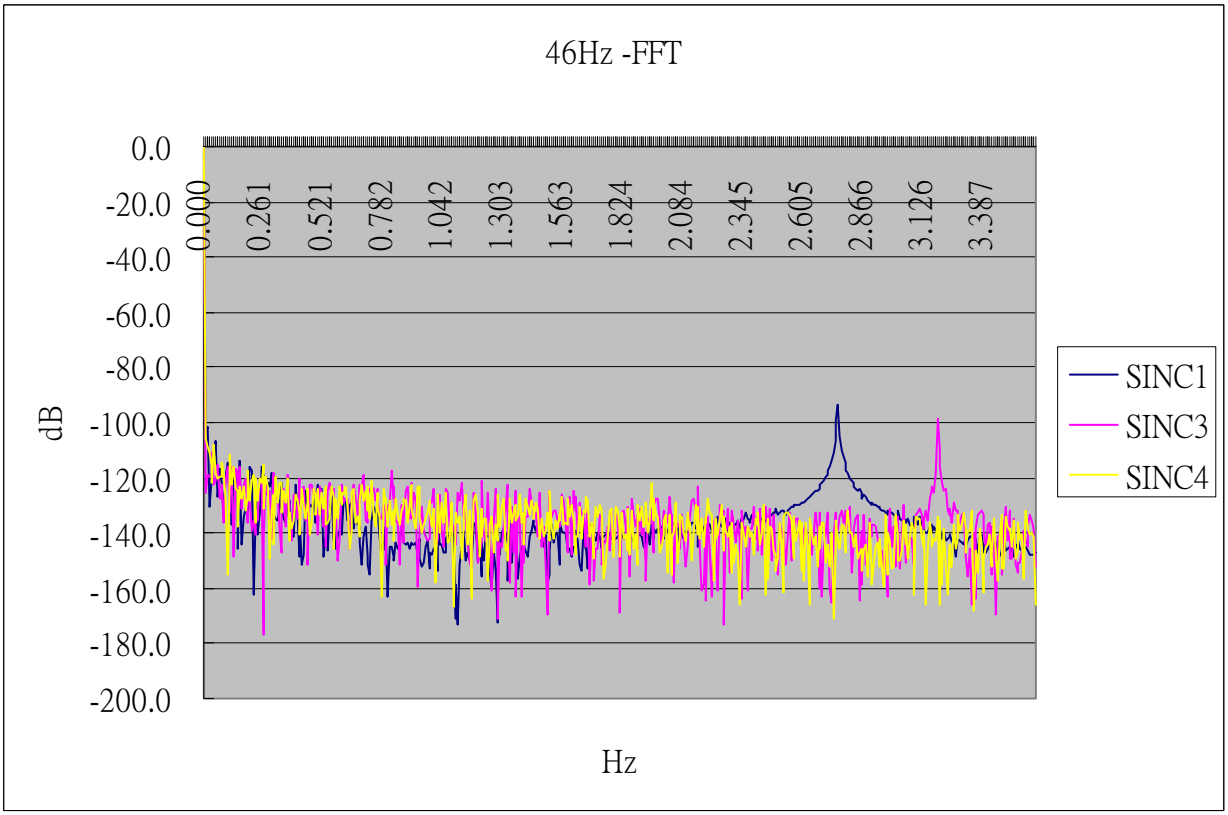
Table 3-1

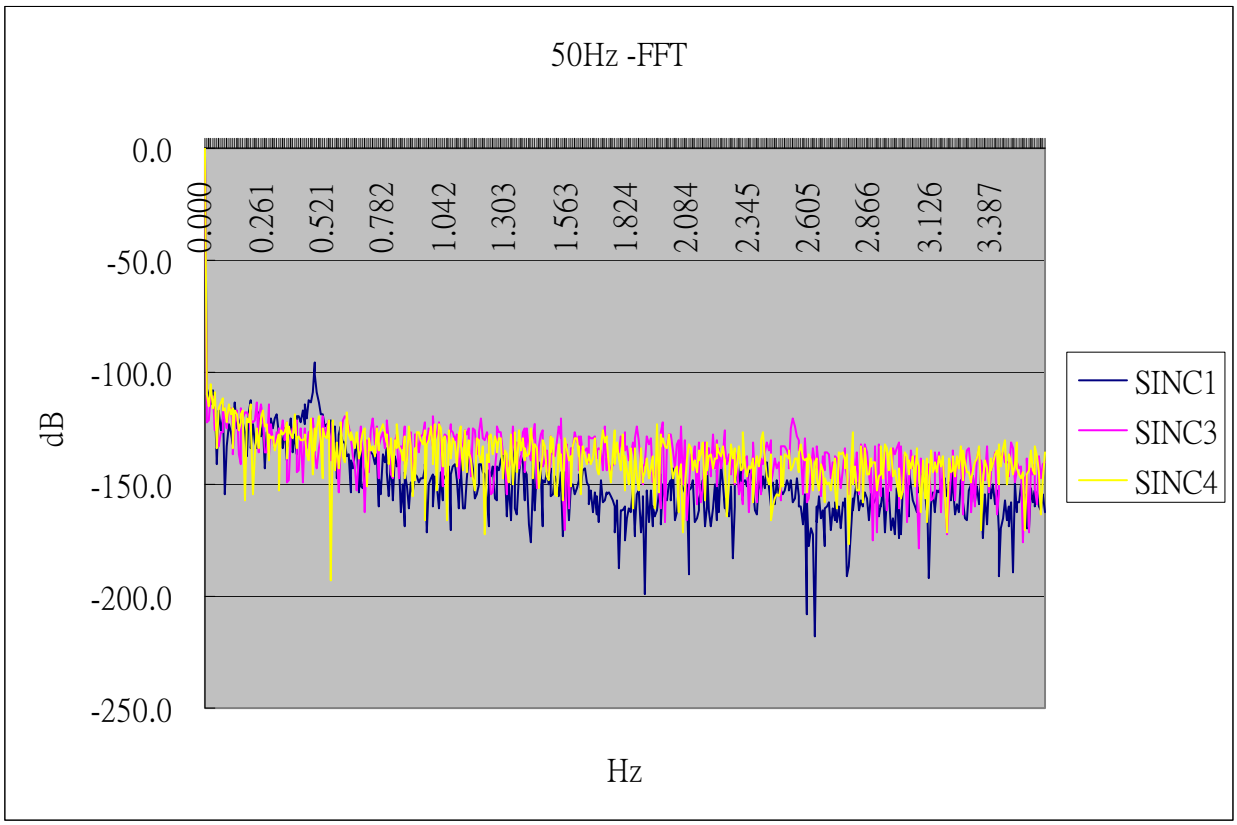
錯誤! 找不到參照來源。 shows the comparison of the Rejection effect for the Average (SINC^1), Software SINC^3 and Software SINC^4 under input 40~70Hz signals in Common mode. SINC^3 is above 98dB at least and has peaks in some input frequency; SINC^4 does not have any peaks and is above 114dB at least; the effect of SINC^1 Rejection can reach only 72dB.

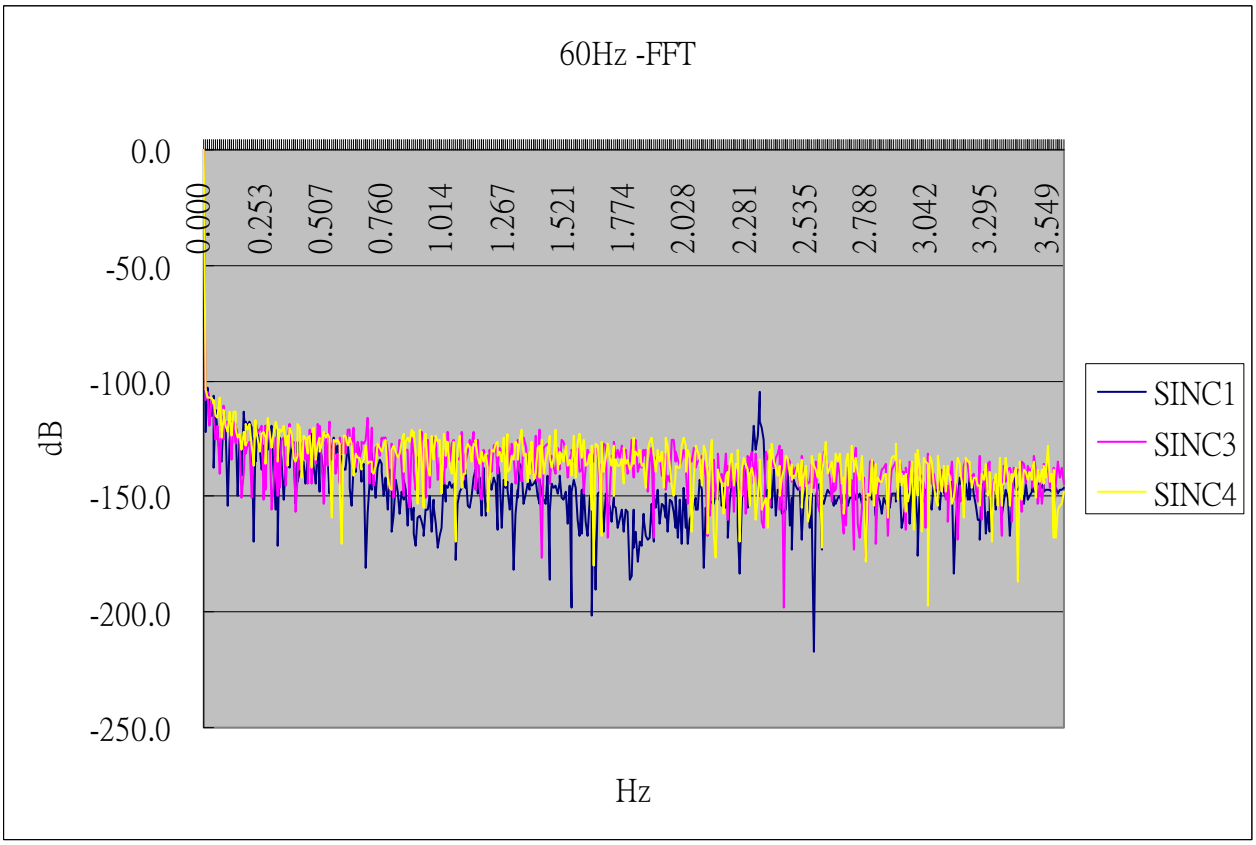
3.2. The FFT Comparison for Average(SINC^1), SINC^3 and SINC^4 under Different Frequency

Although we can see directly the different rolling status for different frequency input signals by using the Average simply in Time domain, however, SINC^3 and SINC^4 do not have any rolling nearly. For more imperceptible differences, we took 1024 records for FFT that we could observe the quantified results on the spectrum. The following figures are the FFT results in different frequency. We can see that the signals in 40~70 Hz are hardly influenced for SINC^4, it cannot filter completely in some frequency (such as 46Hz) for SINC^3, and the simple average is the worst one.






50Hz -FFT
0.0
-50.0
-100.0
-150.0
-200.0
-250.0
dB
0.000
0.261
0.521
0.782
1.042
1.303
1.563
1.824
2.084
2.345
2.605
2.866
3.126
3.387
Hz
SINC1
SINC3
SINC4


60Hz -FFT
0.0
-50.0
-100.0
-150.0
-200.0
-250.0
dB
0.000
0.253
0.507
0.760
1.014
1.267
1.521
1.774
2.028
2.281
2.535
2.788
3.042
3.295
3.549
Hz
SINC1
SINC3
SINC4

4. Software Compiling for SINC^4

```
;================================================================================
; ADC output about 122 Hz
; Output 32 records to do SINC4 average    about 3.8hz ouput
; Integrator bit 0 ~ bit 43
; Differentiator bit 20 ~ bit 43
; IZAL、IZAM、IZAH、IZAU、IZAY  、IZAX   =   Integral Buffer 1
; IZBL、IZBM、IZBH、IZBU、IBAY  、IBAX   =   Integral Buffer 2
; IZCL、IZCM、IZCH、IZCU、ICAY  、ICAX   =   Integral Buffer 3
; IZDL、IZDM、IZDH、IZDU、IDAY  、IDAX   =   Integral Buffer 4
; DZAL、DZAM、DZAH ' Differential Buffer 1
; DZBL、DZBM、DZBH ' Differential Buffer 2
; DZCL、DZCM、DZCH ' Differential Buffer 3
; DZDL、DZDM、DZDH ' Differential Buffer 4
;================================================================================
    btss    INTF1,ADCIF,ACCE
    jmp     Inter_3_out
    bcf     INTF1,ADCIF,ACCE

    lbsr    IZAL
    mvf     ADC0RL,W,ACCE       ;Integrator 1 + ADC --> Integrator 1
    addf    IZAL,F,BANK
    mvf     ADC0RM,W,ACCE
    addc    IZAM,F,BANK
    mvf     ADC0RH,W,ACCE
    addc    IZAH,F,BANK
    mvl     0
    btsz    ADC0RH,7,ACCE
    mvl     0FFh
    addc    IZAU,F,BANK
    addc    IZAY,F,BANK
    addc    IZAX,F,BANK

    mvf     IZAL,W,BANK         ;Integrator 1 + Integrator 2 --> Integrator 2
    addf    IZBL,F,BANK
    mvf     IZAM,W,BANK
    addc    IZBM,F,BANK
    mvf     IZAH,W,BANK
    addc    IZBH,F,BANK
    mvf     IZAU,W,BANK
    addc    IZBU,F,BANK
    mvf     IZAY,W,BANK
    addc    IZBY,F,BANK
    mvf     IZAX,W,BANK
    addc    IZBX,F,BANK

    mvf     IZBL,W,BANK         ;Integrator 2 + Integrator 3 --> Integrator 3
    addf    IZCL,F,BANK
    mvf     IZBM,W,BANK
    addc    IZCM,F,BANK
    mvf     IZBH,W,BANK
    addc    IZCH,F,BANK
    mvf     IZBU,W,BANK
    addc    IZCU,F,BANK
    mvf     IZBY,W,BANK
    addc    IZCY,F,BANK
    mvf     IZBX,W,BANK
    addc    IZCX,F,BANK

    mvf     IZCL,W,BANK         ;Integrator 3 + Integrator 4 --> Integrator 4
    addf    IZDL,F,BANK
    mvf     IZCM,W,BANK
    addc    IZDM,F,BANK
    mvf     IZCH,W,BANK
    addc    IZDH,F,BANK
    mvf     IZCU,W,BANK
    addc    IZDU,F,BANK
    mvf     IZCY,W,BANK
    addc    IZDY,F,BANK
```

```
        mvf     IZCX,W,BANK
        addc    IZDX,F,BANK

        inf     ADCCnter,W,ACCE
        mvl     31                      ; Accumulate 32 times
        cpsl    ADCCnter,ACCE
        jmp     INTER_DVIN
        inf     ADCCnter,F,ACCE
        jmp     Inter_3_out
    ;================================
    INTER_DVIN:
        mvl     0C0h
        andf    ADCCnter,F,ACCE
        inf     WECNT,F,ACCE
    INTER_DVOU:
        mvff    IZDL,BIOUL          ;Integrator 4   --> Buffer
        mvff    IZDM,BIOUM
        mvff    IZDH,BIOUH
        mvff    IZDU,BIOUU
        mvff    IZDY,BIOUY
        mvff    IZDX,BIOUX

        bsf     ADCFg,b_ADCint,ACCE
        bsf     Flag,b_ADCPCOK,ACCE
        lbsr    DZAL
        mvl     4                       ; Take Bit 20 ~ 44 in Buffer
    LINTER_DVOULOOP:
        bcf     Status,C,ACCE
        rrfc    BIOUX,F,BANK
        rrfc    BIOUY,F,BANK
        rrfc    BIOUU,F,BANK
        rrfc    BIOUH,F,BANK
        rrfc    BIOUM,F,BANK
        rrfc    BIOUL,F,BANK
        dcsz    WREG,F,ACCE
        jmp     LINTER_DVOULOOP

        mvf     DZAL,W,BANK             ;Buffer - Differentiator 1 --> BufferA
        subf    BIOUH,W,BANK
        mvf     BADCOL,F,BANK
        mvf     DZAM,W,BANK
        subc    BIOUU,W,BANK
        mvf     BADCOM,F,BANK
        mvf     DZAH,W,BANK
        subc    BIOUY,W,BANK
        mvf     BADCOH,F,BANK
        mvff    BIOUH,DZAL              ; Buffer --> Differentiator 1
        mvff    BIOUU,DZAM
        mvff    BIOUY,DZAH

        mvf     DZBL,W,BANK             ; BufferA - Differentiator 2 --> BufferB
        subf    BADCOL,W,BANK
        mvf     BBBADNEWL,F,BANK
        mvf     DZBM,W,BANK
        subc    BADCOM,W,BANK
        mvf     BBBADNEWM,F,BANK
        mvf     DZBH,W,BANK
        subc    BADCOH,W,BANK
        mvf     BBBADNEWH,F,BANK
        mvff    BADCOL,DZBL             ; BufferA --> Differentiator 2
        mvff    BADCOM,DZBM
        mvff    BADCOH,DZBH

        mvf     DZCL,W,BANK             ; BufferB - Differentiator 2 --> BufferA
        subf    BBBADNEWL,W,BANK
        mvf     BADCOL,F,BANK
        mvf     DZCM,W,BANK
        subc    BBBADNEWM,W,BANK
        mvf     BADCOM,F,BANK
        mvf     DZCH,W,BANK
        subc    BBBADNEWH,W,BANK
```

```
        mvf     BADCOH,F,BANK
        mvff    BBBADNEWL,DZCL          ; BufferB --> Differentiator 3
        mvff    BBBADNEWM,DZCM
        mvff    BBBADNEWH,DZCH


        mvf     DZDL,W,BANK             ; BufferA - Differentiator 4 --> BufferB
        subf    BADCOL,W,BANK
        mvf     BBBADNEWL,F,BANK
        mvf     DZDM,W,BANK
        subc    BADCOM,W,BANK
        mvf     BBBADNEWM,F,BANK
        mvf     DZDH,W,BANK
        subc    BADCOH,W,BANK
        mvf     BBBADNEWH,F,BANK
        mvff    BADCOL,DZDL             ; BufferA --> Differentiator 4
        mvff    BADCOM,DZDM
        mvff    BADCOH,DZDH

        mvff    BBBADNEWH,BADNEWH   ; BufferA output to ADC Output
        mvff    BBBADNEWM,BADNEWM
        mvff    BBBADNEWL,BADNEWL
;=============================================================================================
Inter_3_out:
```

5. Software Compiling for SINC^3

```
;================================================================================
; ADC output about 122 Hz
; Output 32 records to do SINC3 average    about 3.8hz output
; Integrator bit 0 ~ bit 38
; Differentiator bit 15 ~ bit 38
; IZAL、IZAM、IZAH、IZAU、IZAY → Integral Buffer 1
; IZBL、IZBM、IZBH、IZBU、IBAY → Integral Buffer 2
; IZCL、IZCM、IZCH、IZCU、ICAY → Integral Buffer 3
; DZAL、DZAM、DZAH → Differential Buffer 1
; DZBL、DZBM、DZBH → Differential Buffer 2
; DZCL、DZCM、DZCH → Differential Buffer 3
;================================================================================
    btss    INTF1,ADCIF,ACCE
    jmp     Inter_3_out
    bcf     INTF1,ADCIF,ACCE

    lbsr    IZAL
    mvf     ADC0RL,W,ACCE          ;Integrator 1 + ADC --> Integrator 1
    addf    IZAL,F,BANK
    mvf     ADC0RM,W,ACCE
    addc    IZAM,F,BANK
    mvf     ADC0RH,W,ACCE
    addc    IZAH,F,BANK
    mvl     0
    btsz    ADC0RH,7,ACCE
    mvl     0FFh
    addc    IZAU,F,BANK
    addc    IZAY,F,BANK

    mvf     IZAL,W,BANK            ;Integrator 1 + Integrator 2 --> Integrator 2
    addf    IZBL,F,BANK
    mvf     IZAM,W,BANK
    addc    IZBM,F,BANK
    mvf     IZAH,W,BANK
    addc    IZBH,F,BANK
    mvf     IZAU,W,BANK
    addc    IZBU,F,BANK
    mvf     IZAY,W,BANK
    addc    IZBY,F,BANK

    mvf     IZBL,W,BANK                ;Integrator 2 + Integrator 3 --> Integrator 3
    addf    IZCL,F,BANK
    mvf     IZBM,W,BANK
    addc    IZCM,F,BANK
    mvf     IZBH,W,BANK
    addc    IZCH,F,BANK
    mvf     IZBU,W,BANK
    addc    IZCU,F,BANK
    mvf     IZBY,W,BANK
    addc    IZCY,F,BANK

    inf     ADCCnter,W,ACCE            ; Accumulate 32 times
    mvl     31
    cpsl    ADCCnter,ACCE
    jmp     INTER_DVIN
    inf     ADCCnter,F,ACCE
    jmp     Inter_3_out
;================================
INTER_DVIN:
    mvl     0C0h
    andf    ADCCnter,F,ACCE
INTER_DVOU:
    mvff    IZCL,BIOUL                 ;Integrator 3   --> Buffer
    mvff    IZCM,BIOUM
    mvff    IZCH,BIOUH
    mvff    IZCU,BIOUU
    mvff    IZCY,BIOUY
```

```
        bsf     ADCFg,b_ADCint,ACCE
        bsf     Flag,b_ADCPCOK,ACCE
        lbsr    DZAL
        mvl     7                               ; Take Bit 15 ~ 38 in Buffer
LINTER_DVOULOOP:
        bcf     Status,C,ACCE
        rrfc    BIOUY,F,BANK
        rrfc    BIOUU,F,BANK
        rrfc    BIOUH,F,BANK
        rrfc    BIOUM,F,BANK
        rrfc    BIOUL,F,BANK
        dcsz    WREG,F,ACCE
        jmp     LINTER_DVOULOOP

        mvf     DZAL,W,BANK                     ; Buffer - Differentiator 1 --> BufferA
        subf    BIOUM,W,BANK
        mvf     BADCOL,F,BANK
        mvf     DZAM,W,BANK
        subc    BIOUH,W,BANK
        mvf     BADCOM,F,BANK
        mvf     DZAH,W,BANK
        subc    BIOUU,W,BANK
        mvf     BADCOH,F,BANK
        mvff    BIOUM,DZAL                      ; Buffer --> Differentiator 1
        mvff    BIOUH,DZAM
        mvff    BIOUU,DZAH

        mvf     DZBL,W,BANK                     ; BufferA - Differentiator 2 --> BufferB
        subf    BADCOL,W,BANK
        mvf     BBBADNEWL,F,BANK
        mvf     DZBM,W,BANK
        subc    BADCOM,W,BANK
        mvf     BBBADNEWM,F,BANK
        mvf     DZBH,W,BANK
        subc    BADCOH,W,BANK
        mvf     BBBADNEWH,F,BANK
        mvff    BADCOL,DZB                      ; BufferA --> Differentiator 2
        mvff    BADCOM,DZBM
        mvff    BADCOH,DZBH

        mvf     DZCL,W,BANK                     ; BufferB - Differentiator 2 --> BufferA
        subf    BBBADNEWL,W,BANK
        mvf     BADCOL,F,BANK
        mvf     DZCM,W,BANK
        subc    BBBADNEWM,W,BANK
        mvf     BADCOM,F,BANK
        mvf     DZCH,W,BANK
        subc    BBBADNEWH,W,BANK
        mvf     BADCOH,F,BANK
        mvff    BBBADNEWL,DZCL                  ; BufferB --> Differentiator 3
        mvff    BBBADNEWM,DZCM
        mvff    BBBADNEWH,DZCH

        mvff    BADCOH,BADNEWH                  ; BufferB output to ADC Output
        mvff    BADCOM,BADNEWM
        mvff    BADCOL,BADNEWL
Inter_3_out:
```

6. Demo Code

Chip Select: HY11P14

Function Select: Only provide to display the code.

HY11P14-SINC3.rar

HY11P14-SINC4.rar