



HY12P65 ENOB Test Tool User Manual

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1. HY12P65 ENOB Test

1.1 Software Introduction

The main function of HY12P65 ENOB Kit is to test ADC performance of HY12P65 and to test basic DMM ranges on its software.

1.2 Software Installation

1.2.1 Installation

System Requirements of **operating HY12P65 ENOB Test kit:**

- PC Hardware Request
 - Compatible PC with PENTIUM® CPU
 - 128 MB Memory (256MB is recommended)
 - 10 GB Hard Disk Space
- OS
 - Windows 98SE/Windows 2000/Windows XP/Windows Vista/Windows 7
 - Supporting x86, 32bit system; 64bit system is not supported.
- Applicable Interface
 - USB Port
- Supporting Software Version
 - DMMENOBTEST V1.1
- Model number in support:
 - HY12P65
- Function items:
 - ENOB Test
 - Testing basic ranges of DMM

Note: For some Windows OS, it may require to have administrator identity to install the Hex Loader to the computer.

- Insert the HYCON-IDE CD into the CD ROM drive and find the file in the CD ROM or file to execute Setup.exe.
- Following the instruction window dialogs step by step to continue setup procedures. As shown in Figure 1-1.

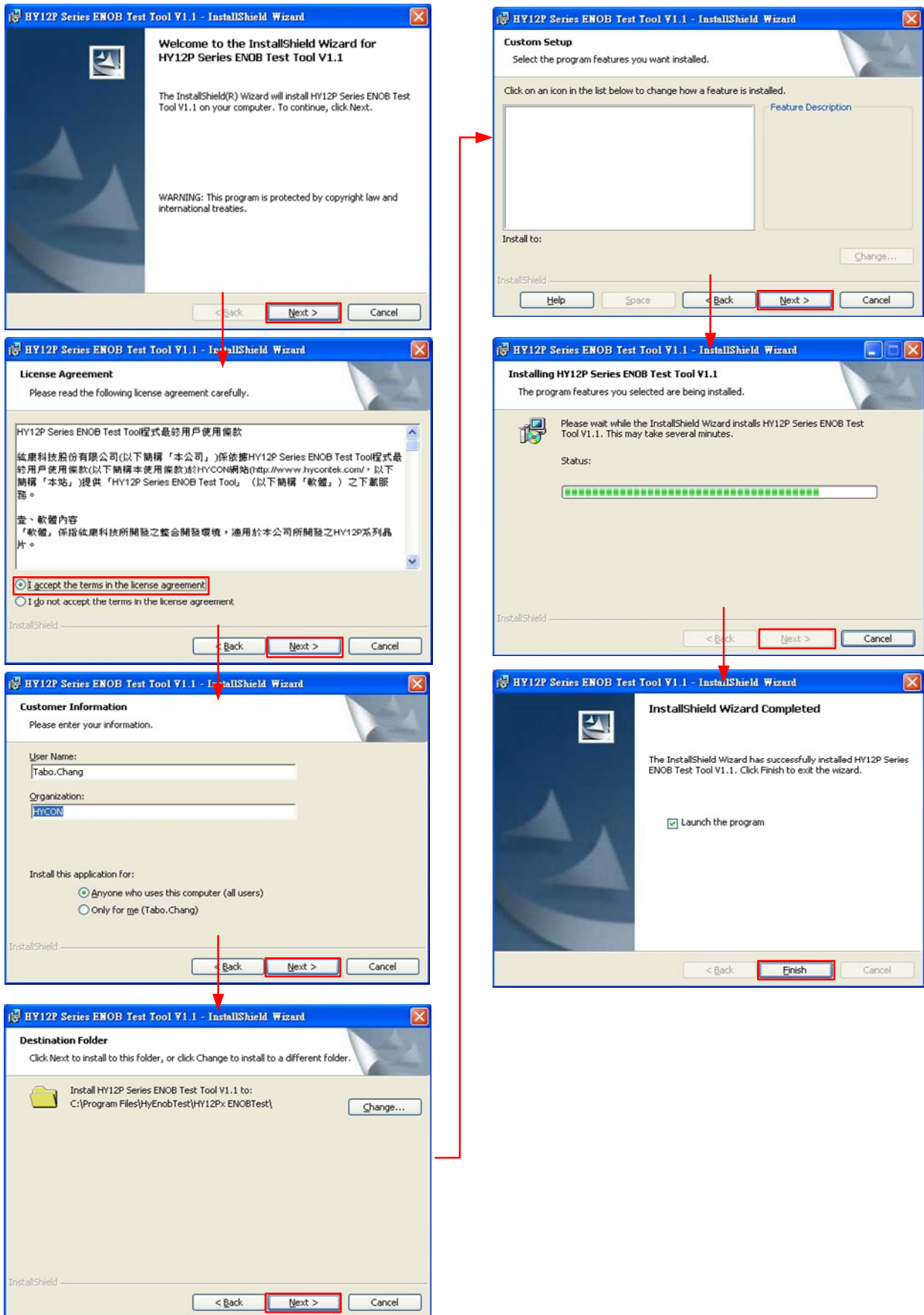


Figure 1- 1

1.2.2 Uninstall

Please remove the file of “HY12P Series ENOB Test Tool V1.1” in “Add/Remove Program” under Control Panel.

1.3 ENOB and Noise Free Description

$$\text{ENOB} = \text{Log}_2\left(\frac{\text{FSR}}{\text{RMS Noise}}\right) = \frac{\text{In}\left(\frac{\text{FSR}}{\text{RMS Noise}}\right)}{\text{In}(2)} \quad \text{Equation 1}$$

$$\text{Noise Free Bits} = \text{Log}_2\left(\frac{\text{FSR}}{\text{Peak - to - Peak Noise}}\right) = \frac{\text{In}\left(\frac{\text{FSR}}{\text{Peak - to - Peak Noise}}\right)}{\text{In}(2)} \quad \text{Equation 2}$$

RMS Noise that generated from Sigma Delta ADC is the minimum voltage value of distinguishable sampling signal. Hence, ENOB (Effective Number of Bits) is calculated by RMS Noise and Full Scale Range ratio. However, RMS Noise must be calculated by many average times. Insufficient sampling times can only represent RMS Noise for a specific period of time instead of the RMS Noise of the entire ADC operation. Therefore, RMS Noise operation times cannot be less than 1024 times.

However, Noise Free Bit represents that ADC output value count is not rolling. Noise Free Bits are stable ADC output performance. Bit operation is defined as Peak-to-Peak Noise and Full Scale Range ratio.

RMS Noise Calculation:

$$\text{Average Counts} \rightarrow \text{Average} = \frac{\sum_{k=1}^n \text{ADC}[k]}{n} \quad \text{Equation 3}$$

n = Total ADC sampling times.

$$\text{RMS Noise} = \frac{V_{\text{REF}} \times \sqrt{\frac{\sum_{k=1}^n (\text{ADC}[k] - \text{Average})^2}{n}}}{2^{\text{Scale}}} \quad \text{Equation 4}$$

Scale = Total ADC Output Bits

Peak-to-Peak Noise Calculation:

$$\text{Peak - to - Peak Noise} = \frac{V_{\text{REF}} \times (\text{ADC}_{\text{Max}} - \text{ADC}_{\text{Min}})}{2^{\text{Scale}}} \quad \text{Equation 5}$$

ADCMax = Maximum ADC value of total sample

ADCMin = Minimum ADC value of total sample

1.4 Window Interface

When the software is opened, the window in below will pop up, as Figure 1- 2:

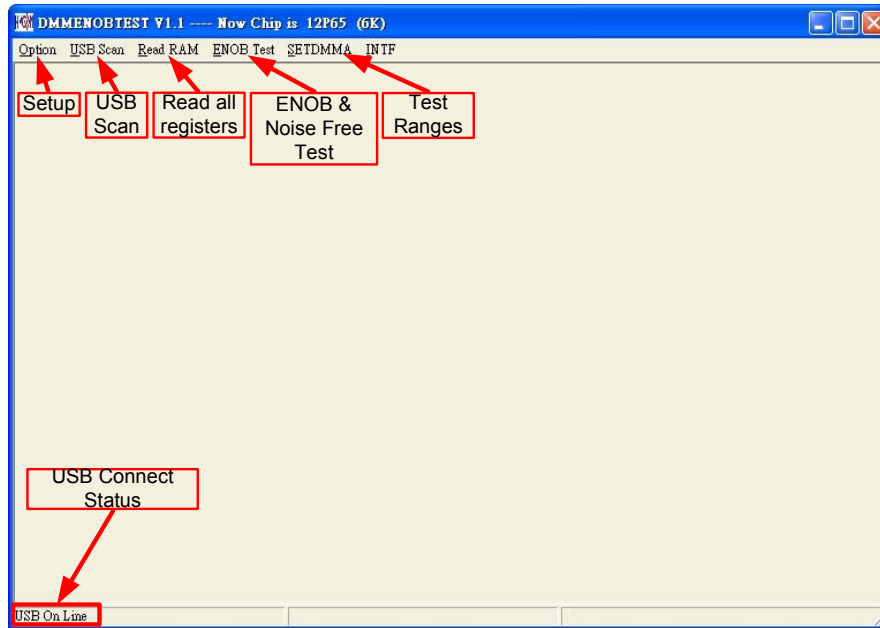


Figure 1- 2

1.4.1 Option

Choose Option, the window will display as shown in Figure 1- 3.

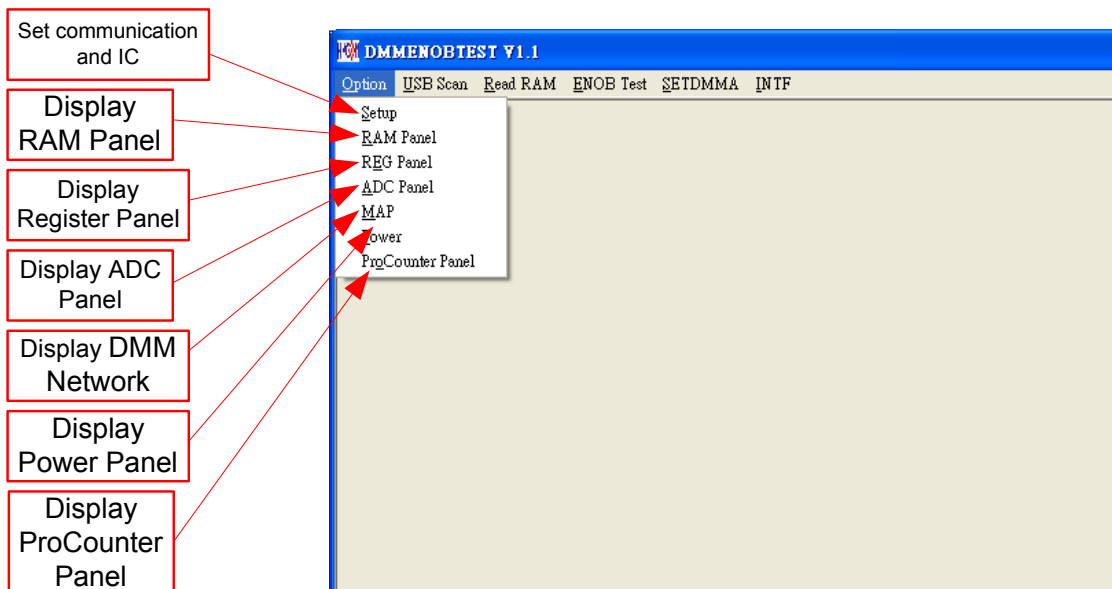


Figure 1- 3

1.4.1.1 Setup

When selecting Option→Setup, a window will show as Figure 1- 4:

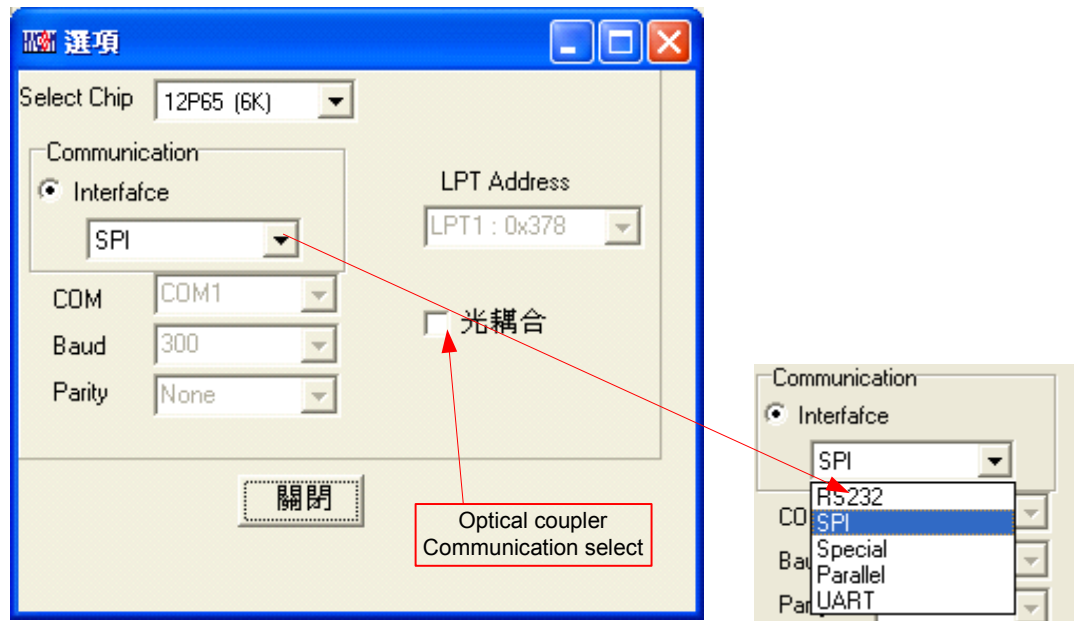


Figure 1- 4

Function	Description
Select Chip	Select OTP IC, OTP IC program needs to burn SPI or Special communication procedures.
Communication	Only SPI or Special can be selected, other interfaces are not supportive.
Optical Coupler	When communication interface selects optical coupler to isolate channels.

1.4.1.2 RAM Panel

When selecting Option→RAM Panel, a window will show as Figure 1- 5:

Figure 1- 5

Please refer to Chapter 3.2, RAM window operation of HY12P-IDE software user manual.

1.4.1.2 REG Panel

When selecting Option→REG Panel, a window will show Figure 1- 6:

PAGE1		PAGE2		PAGE3	
STKPTR	STKPL	STKUN	STKOV	-	-
INTE1	GE	-	TMCIE	-	TMAIE
INTE2	TXIE	RCIE	RMSIE	LPFIE	AD1IE
INTE3	E27IE	ES2IE	ES2IE	ES2IE	ES2IE
INTF1	-	ADCIF	TMCIF	TMBIF	TMAIF
INTF2	TXIF	RCIF	RMSIF	LPFIF	AD1IF
INTF3	E27IF	E26IF	E25IF	E24IF	E23IF
STATUS	-	-	-	C	DC
PSTATUS	PD	TO	IDLEB	BOR	-
LVDEN1	ENLYD	LVD	V1	V2	VLDX3
LVDEN2	V1	SVN3	SVN2	SVN1	SVN0
SBMSET1	SKRST	-	HAOTR5	HAOTR4	HAOTR3
MCKCN1	HS_SEL	CPUCK1	CPUCK0	HS1	HS0
MCKCN2	LCDS2	LCDS1	LCDS0	ADOCK	PERCK
TMACN	ENTMA	TMACK	TMA61	TMA50	ENWDT
TMCN	ENTMC	TMOCK1	TMOCK0	TMC512	TMC511
PWMCN	ENPWM	ENPF0	PWMR1	PWMR0	-
LCDCN1	ENLCD	LCDFR	VLCDX1	VLCDX0	LCDFB
LCDCN2	LCDBL	LCDMX1	LCDMX0	-	-

Figure 1- 6

Please refer to Chapter 3.3, REG window operation of HY12P-IDE software user manual.

1.4.1.3 ADC Panel

When selecting Option→ADC Panel, a window will show Figure 1- 7:

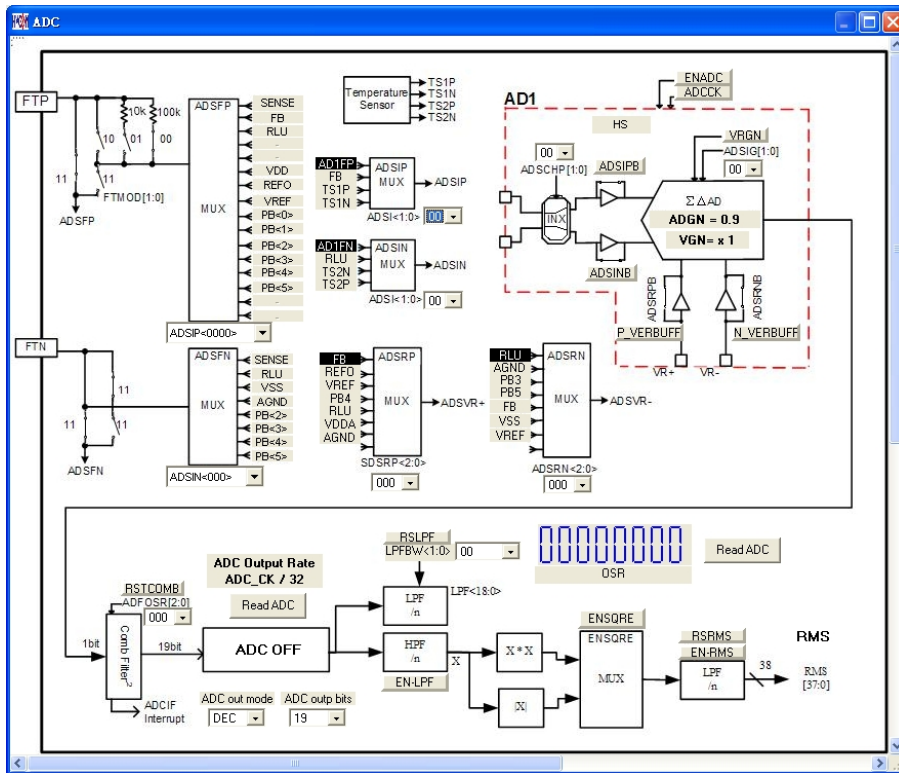


Figure 1- 7

Please refer to Chapter 3.6, ADC window operation of HY12P-IDE software user manual.

1.4.1.4 MPN Panel

When selecting Option→MPN Panel, a window will show Figure 1- 8:

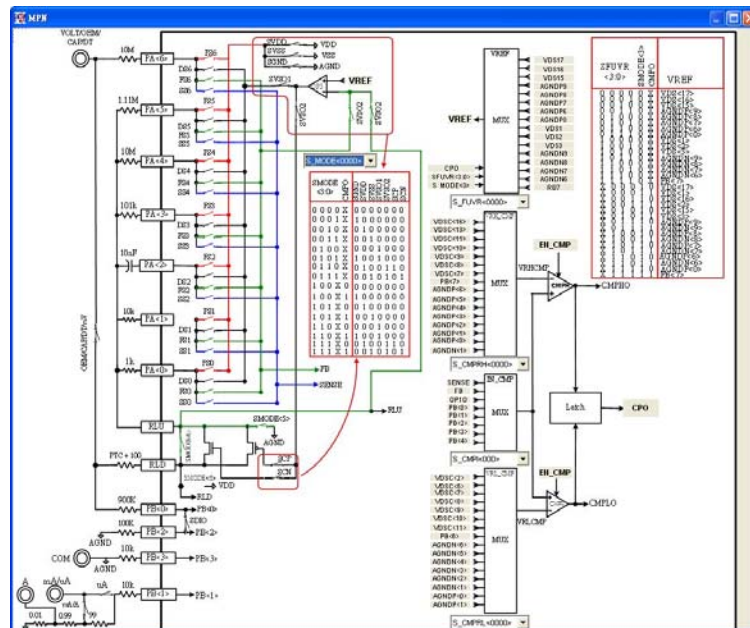


Figure 1- 8

Please refer to Chapter 3.8, ADC window operation of HY12P-IDE software user manual.

1.4.1.5 Power Panel

When selecting Option→Power Panel, a window will show Figure 1- 9:

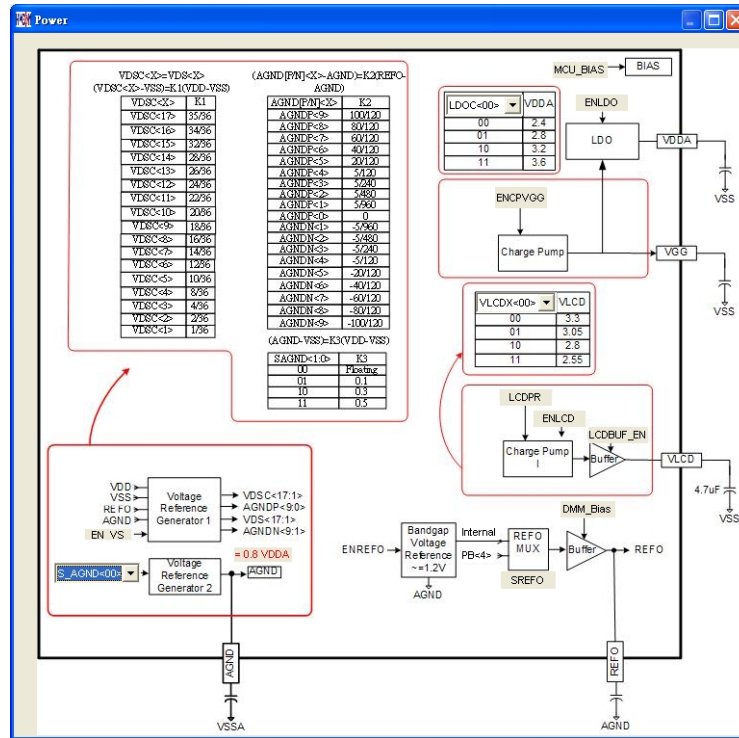


Figure 1- 9

Please refer to Chapter 3.7, ADC window operation of HY12P-IDE software user manual.

1.4.1.6 ProCounter Panel

When selecting Option→ProCounter Panel, a window will show Figure 1- 10:

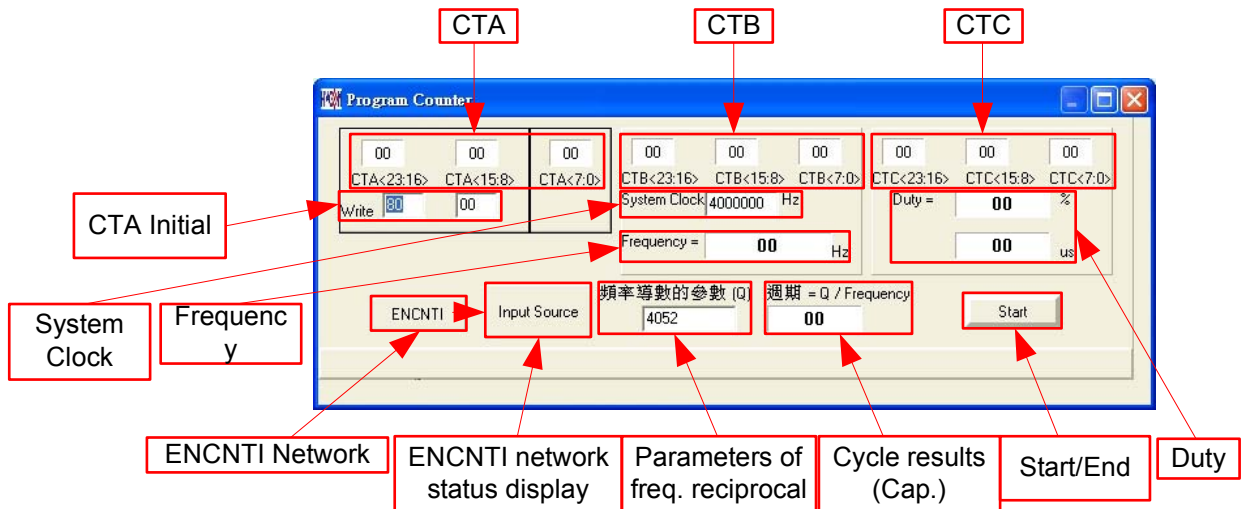
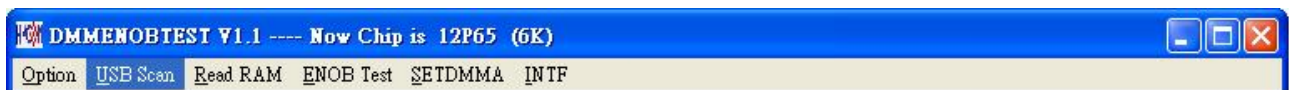


Figure 1- 10

Function	Description
CTA	CTA value display
CTB	CTB value display
CTC	CTC value display
CTA Initial	CTA Initial value setup
System Clock	Main frequency of System
ENCNTI Network	Signal input network; OFF=CMPO · ON=CNTI
ENCNTI Network Status Display	Display input source in accordance with "ENCNTI" setup
Parameters of Freq. Reciprocal	Reciprocal of input frequency
Start/End	Start/End measurement
Frequency	Display freq. result
Cycle results (Cap.)	Display cycle result for capacitor range measurement
Duty	Display duty cycle result

1.4.2 USB Scan



USB scan function help to detect whether USB scan communication port is connected to HY12P65 ENOB Test Tool. If it is connected, the status, USB On Line, will be shown in left corner, as Figure 1- 11 displayed.

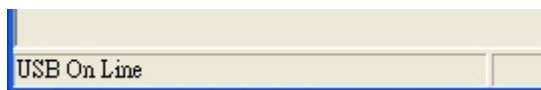


Figure 1- 11

If not connected, "USB not Connect!!!" will show up as Figure 1- 12:

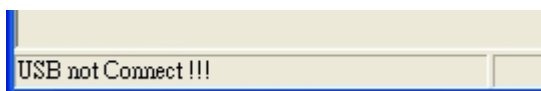
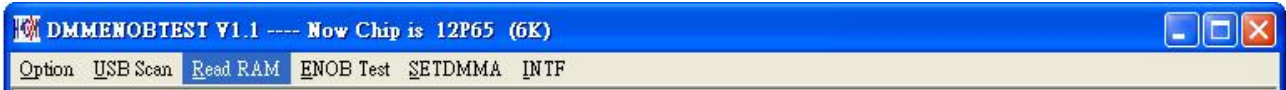


Figure 1- 12

※Note :

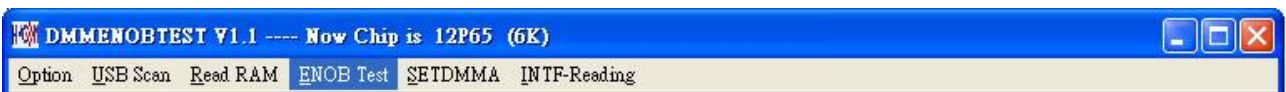
1. If using USB to supply power, connecting USB Line to USB ENOB Test Board (T09011 V02) can click USB Scan on the interface.
2. If using external power supply, please connect the external power to HY12P65 ENOB Test Tool first then connecting USB Line to USB ENOB Test Board (T09011 V02) and click USB Scan on the interface.
3. When using external power supply, please open USB ENOB Test Board (T09011 V02) J5 & J8 Jump to avoid power collide.

1.4.3 Read Ram



When USB port connects to HY12P65 ENOB Test Tool and "USB On Line" is confirmed, please select Read Ram on the interface. This function will read the current RAM and register of HY12P65 to PC buffer, influencing RMS Noise & Vp-p Noise operation of ENOB Test.

1.4.4 ENOB Test



After clicking ENOB Test, ENOB Test Panel will show up as Figure 1- 13:

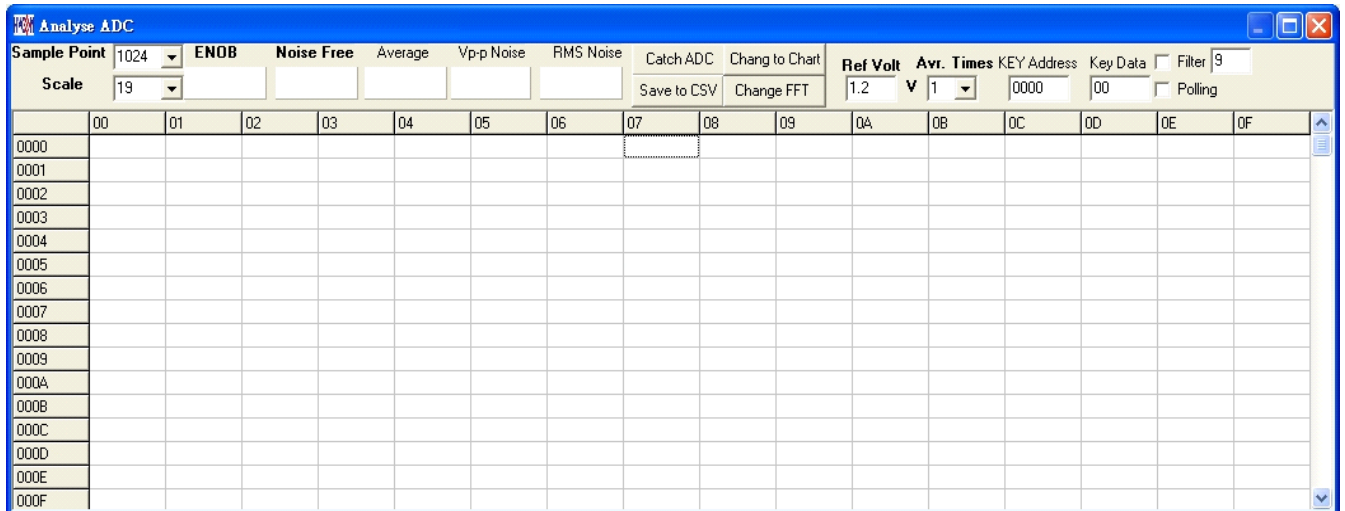
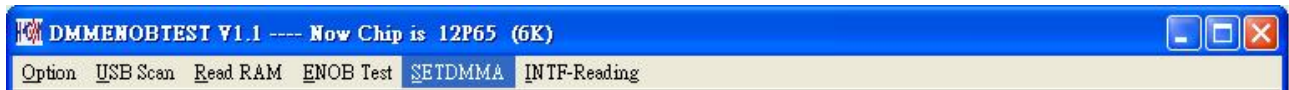


Figure 1- 13

Function	Description
Sample Point	"Catch ADC" of ADC sample number, min. 32, max. 131072. It is suggested to keep as 1024.
Scale	Captured bit of every ADC output. Min. 8Bits, Max.19Bits
ENOB	Display ENOB(Effective Number of Bits), please refer to equation 1 for calculation, unit is Bit.
Noise Free	Display Noise Free Bits, please refer to equation 2 for calculation, unit is Bit.
Average	Display average of ADC sample, please refer to equation 3 for calculation, unit is Count.
Vp-p Noise	Display Peak-to-Peak Noise, please refer to equation 5 for calculation, unit is nV.
RMS Noise	Display RMS Noise, please refer to equation 4 for calculation, unit is nV.

Catch ADC	Real time capture and sequencing display ADC value to display zone.
Save to CSV	Store the value in display zone to HyADC.CSV file, including ENOB, Noise Free, Average & RMS Noise.
Change to Chart	Switch the value in display zone to chart
Change FFT	Switch chart to display "frequency domain/time domain".
Ref Volt	Input Reference Voltage value, unit is V.
Avr. Time	Select software average, value of the display zone will be averaged according to the time set, then display to the zone again.

1.4.5 SETDMMA



After clicking SETDMMA, the window will show up as Figure 1- 14:

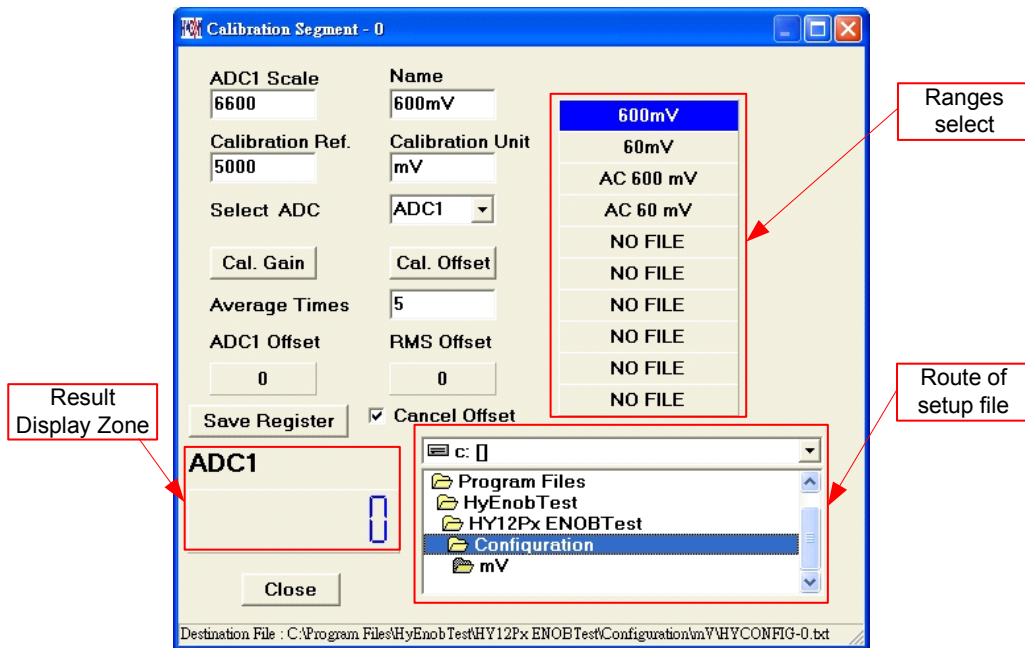


Figure 1- 14

Function	Description
Setup file route	Select the save route of setup file
Range selection	After the setup is done, different ranges can be tested by this function
Name	Pure character format, the input character will be the range name of "range select"
Calibration Unit	Pure character format
ADC1 Scale	Max value (full scale) after calibration

Calibration Ref.	Calibrate current ADC1 or RMS value as the input value (calibration point)
Select ADC	Select ADC1 or RMS Output as output
Cal. Gain	After pressing Cal. Gain, the current ADC1 or RMS output value will be calibrated as "Calibration Ref." setup
Cal. Offset	After pressing Cal. Offset, the current ADC1 or RMS output value will be deemed as Offset
Average Times	Average ADC1 or RMS output value according to the input times
ADC1 Offset	Display ADC1 Offset value
RMS Offset	Display RMS Offset value
Save Register	Store all register status. If "NO FILE" is selected and store is clicked, a new record will be added to this menu, utmost 10 setup files.
Cancel Offset	When ticking "Cancel Offset", ADC1 will deduct Offset value and multiple Gain. RMS will deduct Offset first, then root and multiple Gain
Result Display Zone	Display results after calculation
Close	Close the window

1.5 SETDMMA Operation Procedures

This function can simulate all basic ranges of DMM, excluding frequency that must be measured by ProCounter. Below SETDMMA software operation procedures demonstrate the measurement of DC 600mV

Step 1: Click USB Scan on the interface of HY12P65 ENOB Test Tool. "USB On line" will show up when the connection is successful, as Figure 1- 15. If not, please make sure the hardware connection or power supply is correct.

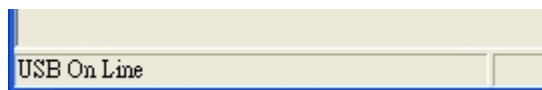


Figure 1- 15

※Note:

1. If using USB to supply power, connecting USB Line to USB ENOB Test Board (T09011 V02) can click USB Scan on the interface.
2. If using external power supply, please connect the external power to HY12P65 ENOB Test Tool first then connecting USB Line to USB ENOB Test Board (T09011 V02) and click USB Scan on the interface.
3. When using external power supply, please open USB ENOB Test Board (T09011 V02) J5 & J8 Jump to avoid power collide.

Step 2: Click Read Ram on the interface when "USB On Line" was shown, loading all registers of HY12P65 to PC buffer.

Step 3: Click SETDMMA on the interface, a window as like Figure 1- 16 will pop up.

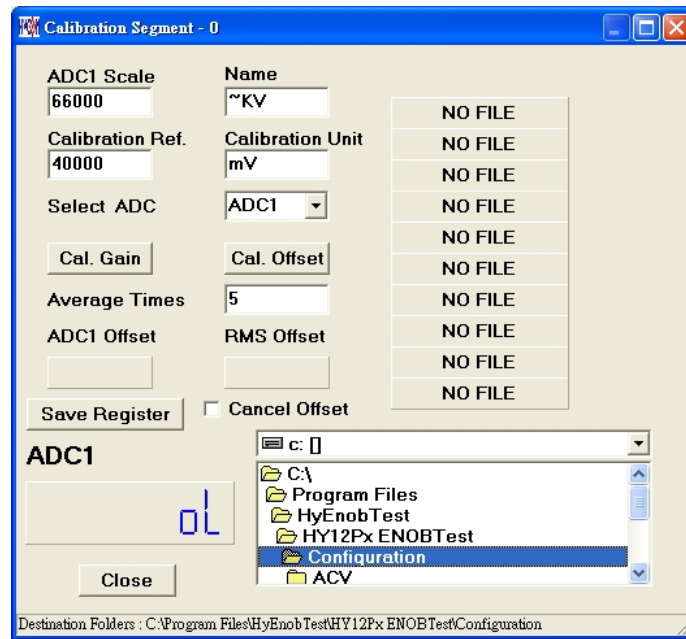


Figure 1- 16

Step 4: Select setup file reserve route. This program provides demo configurations for users, the default route is: <C:\Program Files\HyEnobTest\HY12Px ENOBTest\Configuration>

Step 5: The route of DC 600mV is C:\Program Files\HyEnobTest\HY12Px ENOBTest\Configuration\mV, clicking 600mV of the range select tag will make the information marked in blue, as shown in Figure 1- 17. At this time, the registers of HY12P65 ENOB Test Tool will be set as the configurations of DC 600mV range. And the assumed full scale of DC 600mV (ADC1 Scale) is 6600 Count, calibration Ref. is 5000 Count.

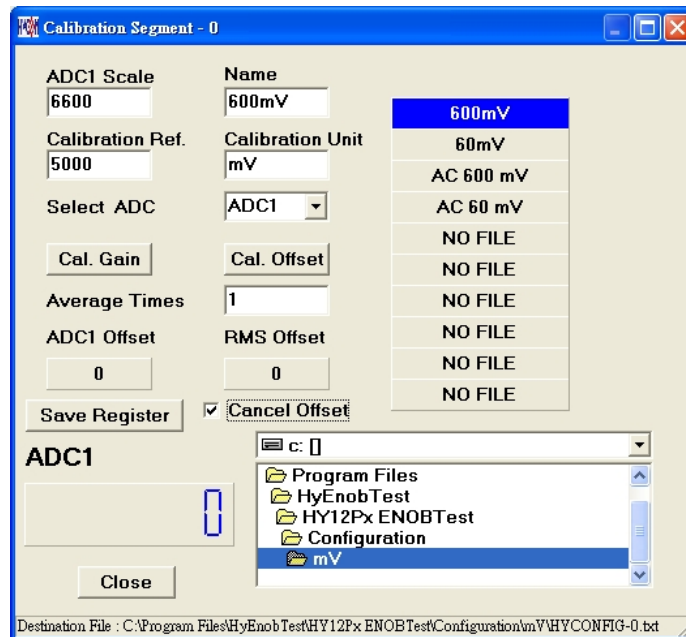


Figure 1- 17

Step 6: Calibration started. Input 0mV first, then click Cal. Offset and tick Cancel Offset. This time, the result zone should display 0. After input DC 500mV, click Cal. Gain. This time, the result zone should display 5000, as shown in Figure 1- 18 to finish calibration.

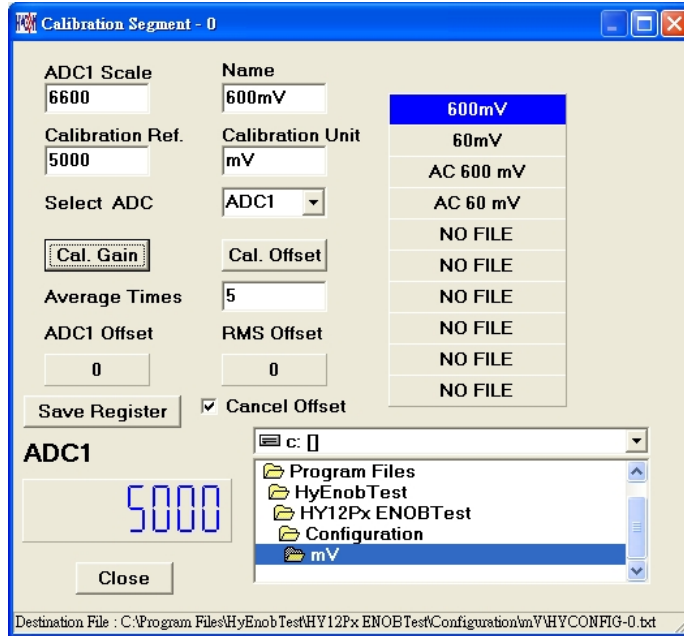


Figure 1- 18

Step 7: Save Configuration. Clicking Save Register after selecting the route, to store the register data as Configuration file, as shown in Figure 1- 19.

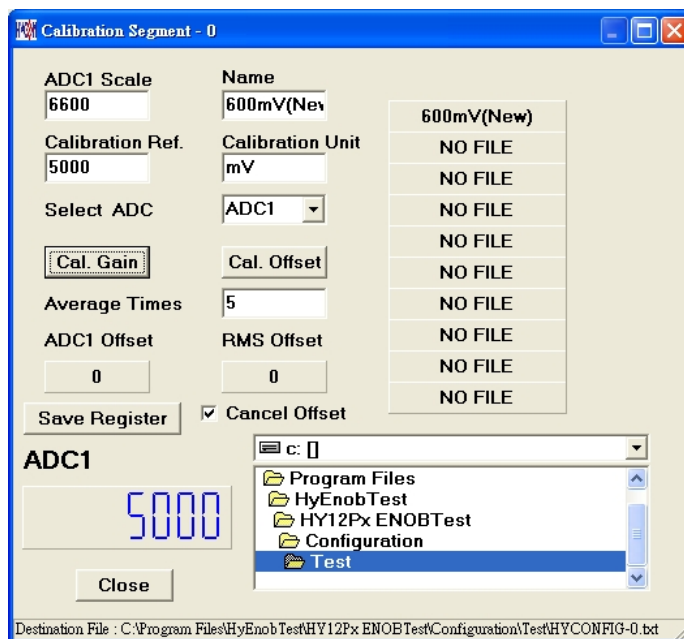


Figure 1- 19

Step 8: Revise Configuration. Clicking Save Register after selecting the file to-be-covered.

Then click Yes to cover the origin file, as shown in Figure 1- 20.

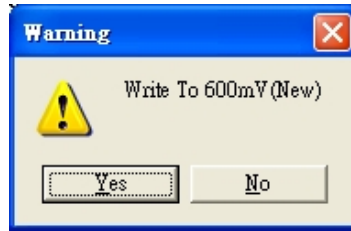


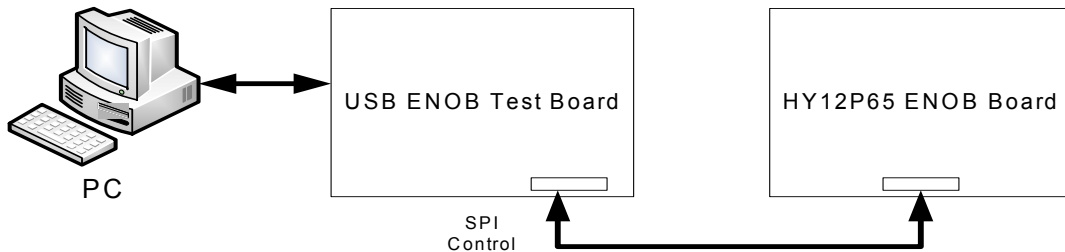
Figure 1- 20

Configure Jump on HY12P65 Target Board based on different measurement functions:

Function	J4	J6 & J9	J7	J3
ACV	Short	Open	Open	Open
DCV				
AC mV	Open	Short	Open	Open
DC mV				
Thermocouple				
AC Current	Open	Open	Open	A(Open) mA(1-2) uA(2-3)
DC Current				
Resistor	Open	Short	Open	Open
Continuity				
Diode				
Capacitor				
Frequency(CNT Input)	Open	Short	Short	Open

2. Hardware Description

2.1 Communication Structure



PC sent Command or Data to USB ENOB Test Board and USB ENOB Test Board read/write SRAM Data of HYCON OTP or read/write Flash Memory.

2.2 USB ENOB Test Board

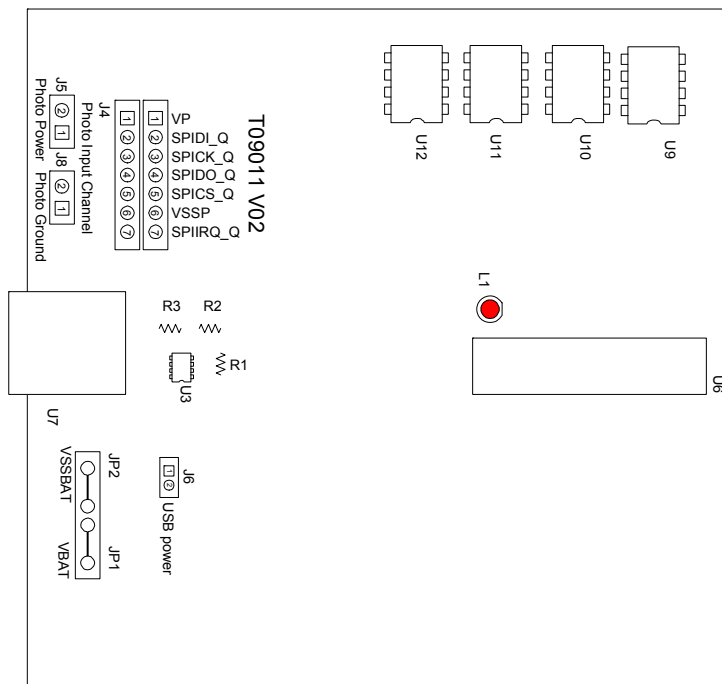


Figure 2- 1

1. J2, J3: SPI communication Port

J2 Description:

PIN 1 → VDDIN supply power to U1. If OTP external power supplies to J3, then J3 is open. If the power was supplied by USB ENOB Test Board, then J3 short.

PIN 2 → ICESDI_Q , DI signal line of SPI

PIN 3 → ICESCK_Q , CK signal line of SPI

PIN 4 → ICESDO_Q, DO signal line of SPI

PIN 5 → ICECS_Q, CS signal line of CS

PIN 6 → VSS

PIN 7 → ICEIRQ_Q, signal line of detecting whether the write of HYCON OTP to Flash Memory is finished.

2. J4, J5, J8 : Optical coupler communication port

J4 description

PIN 1 → VP, supply power to Optical coupler IC(U9~U13). To isolate the power completely, then J5 & J8 must be opened; for common power, J5 & J8 must be short circuit.

PIN 2 → SPIDI_Q, DI signal line of optical coupler.

PIN 3 → SPICK_Q, CK signal line of optical coupler.

PIN 4 → SPIDO_Q, DO signal line of optical coupler.

PIN 5 → SPICS_Q, CS signal line of optical coupler.

PIN 6 → VSSP, Ground of optical coupler.

PIN 7 → SPIIRQ_Q, signal line (optical coupler) of detecting whether the write of HYCON OTP to Flash Memory is finished.

3. J9, J10, J11 & U8

U8 is 512K byte Flash Memory

J10 & J11 is power source of Flash Memory. Using optical coupler to isolate power, then PIN1-2 of J10 & J11 must be short circuit; If no need to isolate power, then PIN2-3 of J10 & J11 must be short circuit.

J9 description :

PIN 1 → VDD_X, supply power to U8.

PIN 2 → FLDI, control DI signal line of U8.

PIN 3 → FLCK, control CK signal line of U8.

PIN 4 → FLDO, control DO signal line of U8.

PIN 5 → FLCS, control CS signal line of U8.

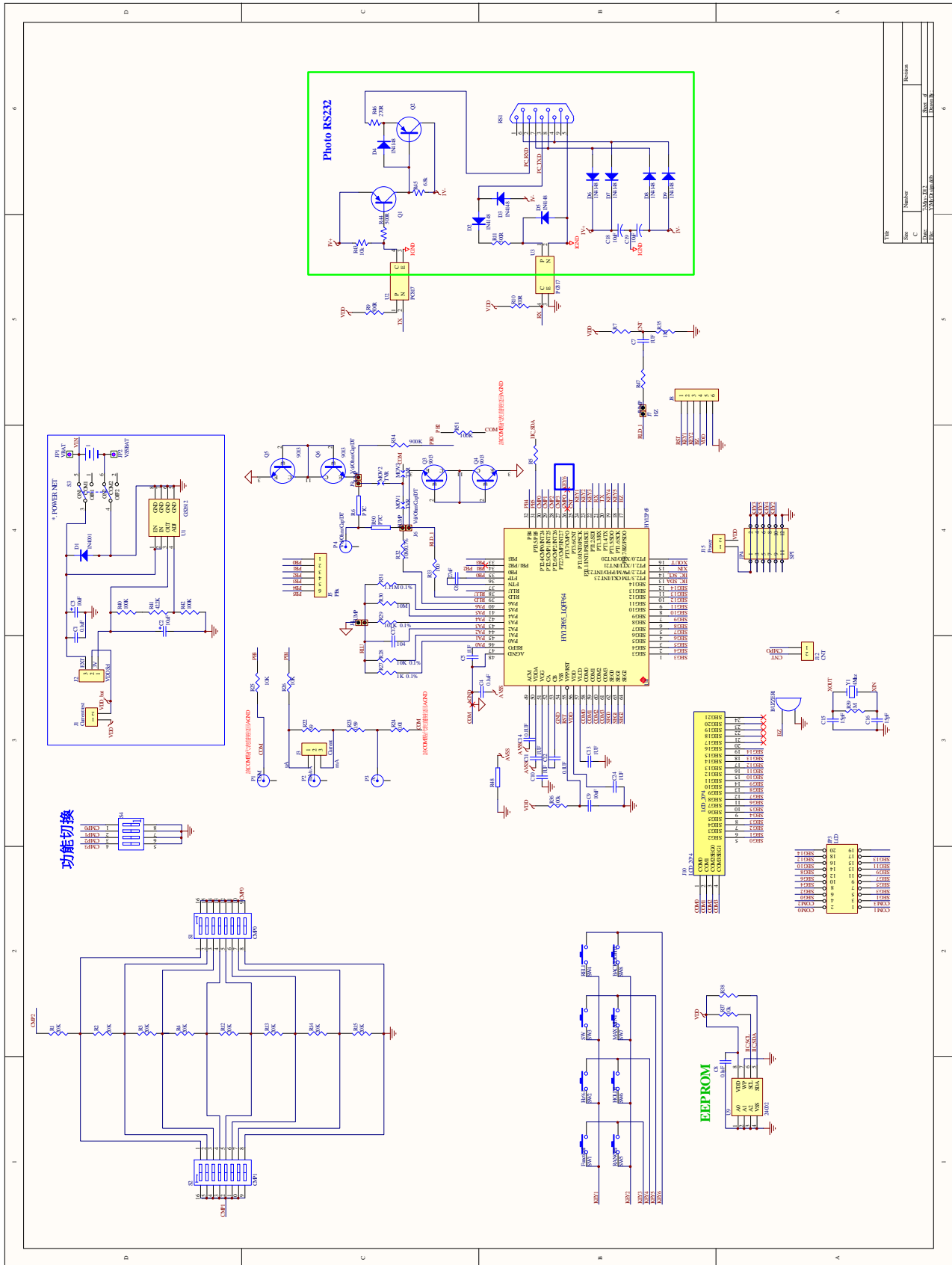
PIN 6 → VSS_X, Ground of U8.

4. JP1, JP2, J6 & U3

JP1 & JP2 are external input power of U3, to generate VDD power. If using USB power then J6 is short circuit. Using external Power (5V), then JP1 & JP2 is input and J6 is open. U3, R1, R2 & R3 consist of a Regulator, to generate VDD power. To change output voltage, R1, R2 & R3 can be changed, its relation is given:

$$VDD = 1.240V \times \left(1 + \frac{R1 + R2}{R3}\right)$$

2.3 HY12P65 ENOB Board Circuitry



3. Revision History

Version	Page	Summary
V01	ALL	First Edition
V02	17	Add in the Table of Target Board Jump of different measurement functions.