HY14E10/HY14E10M

User's Guide

Digital Pressure Sensor Platform

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1.1. Terms and Definition

1.1.1. Glossary

1MW	1MegaWord
1KB	1KiloByte
ADC	Analog to Digital Converter
Bit	bit
BOR	Brown-Out Reset
BSR	Bank Select Register
Byte	Byte
CCP	Capture and Compare
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DM	Data Memory
ECAP	Enhance Comparator
FSR	File Select Register
GPR	General Purpose Register
HAO	High Accuracy Oscillator
LNOP	Low Noise OP AMP
LPO	Low Power Oscillator
LSB	Least Significant Bit
MEM	Memory
MPM	Main Program Memory
MSB	Most Significant Bit
OTP	One Time Program-EPROM
PC	Program Counter
PPF	PWM and PFD
ΣΔADC	Sigma-Delta ADC
SR	Special Register
SRAM	Static Random Access Memory
STK	Stack
WDT	Watch Dog Timer
WREG	Work Register

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1.1.2. Register Related Glossary

[ ]	Register length
< >	Register value
ABC[7:0]	ABC register had 0 to 7bit
ABC<111>	ABC register had 3bit and value had 111 of binary
ABC<11x>	x：can be neglected, it can be set as 1 or 0

rw	Read/Write
r	Read only
r0	Read as 0
r1	Read as 1
w	Write only
w0	Write as 0
w1	Write as 1
h0	cleared by Hardware
h1	set by Hardware
u0	cleared by User
u1	set by User
-	Not use
!	users are forbidden to change
u	unchanged
x	unknown
d	depends on condition

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2. Central Processing Unit (CPU)

2.1. CPU Core

CPU Core (H08) adopts Harvard architecture concept in order to enhance execution efficiency. Separate program memory and data memory incorporated in program memory address increases user convenience of program writing.

CPU features include :

- Isolated design frame of program memory and data memory upgrades instruction execution speed and CPU efficiency.
- Max 46 operation instructions include block switching and stacking control of data memory.
- One instruction accomplished utmost 16-bit FSR register data movement and address 1MW program memory look-up-table instruction.
- Data memory operation includes Program Counter (PC), Status Register (Status) and Stack Register (Stack) data movement.
- The CPU core is H08B core of starter edition.

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2.2. Memory

Memory is composed by program memory (EEPROM) and data memory (SRAM).Memory size differs from diverse part number; hence product data sheets should be read with extra caution.

Program Memory :

Main Program Memory (MPM)

Program Counter (PC)

Stack (STK)

Data Memory :

Special Register (SR)

General Purpose Register (GPR)

Memory Related Registers : (x : Means it constitutes several registers)

PC[10:0]	PCHSR[2:0],PCLATH[2:0],PCLATL[7:0]
TOS[10:0]	TOSH[2:0],TOSL[7:0]
FSR0[7:0]	FSR0L[7:0]
INDF0	INDF0[7:0]
STKCN	STKFL,STKOV,STKUN,STKPRT[2:0]
PSTATUS	SKERR

2.2.1. Program Memory

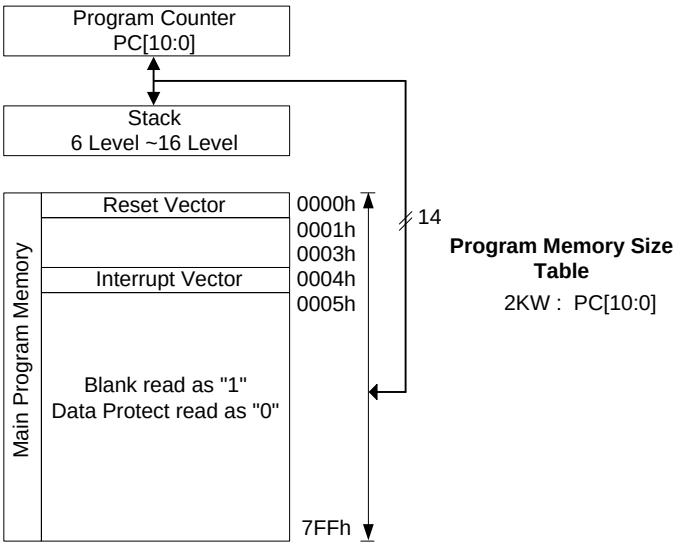

Figure 2-1 Program Memory Flame

2.2.1.1. Main Program Memory, MPM

The frame of main program memory is as follows :

- Interrupt Vector Position
- Reset Vector Position

Addressing capability is from 0x00000h to 0x7FFh, with a total capacity of 2048 Word.

When the chip is not taken program writing, data type of all addresses is 1. After writing, the addresses will be 1 or 0 according to the written data type. Note: in program development, if the

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assemble option of simulation software (HYIDE) has burn protection function setting, the data type of chip is 0 at the addresses that burning can be read.

2.2.1.2. Program Counter (PC)

Program Counter (PC) is composed of shift register PCSR and buffer register PCLAT. Se Figure 2-2。

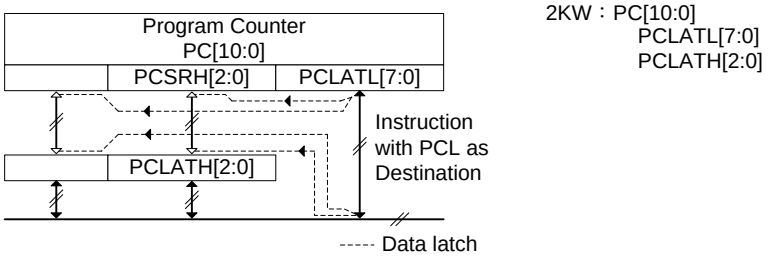

Figure 2-2 PC Architecture

Chip used in tool development of PC [10:0] has 11-bit data length. It is composed of two special registers, PCSRH [2:0] and PCLATL [7:0]. PCLATL [7:0] and PCLATH [2:0] can be read / written directly, while PCSRH [2:0] cannot be read / written directly and it must use buffer register PCLATH [2:0] as indirect reading /writing.

Before reading PC [10:0], it must read PCLATL [7:0] first and then read PCLATH [2:0] before reading correct data. Reverse order will not read correct data.

Before writing PC [10:0], it must write PCLATH [2:0] and then PCLATL [7:0] finally. Reverse order will not write correct data.

2.2.1.3. Stack (STK)

Stack, STK is mainly composed by Stack Index Control Register (STKCN), Top-of-Stack Register (TOSx), Stack Layer Register (STKn), Stack Error Flag Bit (SKERR) and Stack Error Reset Controller (SKRST).

When the stack appears overflow and underflow, it may lead to unexpected execution results for program. When necessary, it can restart chip via setting. In program development process, it can set stack reset control bit SKRST[0][1] as <1> via software setting. When stack appears underflow or overflow, it may generate reset signal and shall restart chip after the SKERR [0] is set as <1>.

- Stack Full: Configure STKFL[0] as <1>, PC[10:0] is not influenced.
- Stack Underflow: Configure STKUN[0] as <1>, PC[10:0] moves to 0x00000h, STKPRT points to 0 Level. If SKRST[0] is set as <1>, reset signal will be aroused after stack underflow and SKERR[0] may be configured as <1>, STKUN[0] will be <0>

[1] SKRST[0] is the generated reset signal control bit of stack error. Instead of direct read or write, it only can be set by developing software at the program development stage. That is to say, whether to generate stack error reset signal must be determined at program developing stage. If reset is chosen, after IC enpowered, SKRST [0] is set as 1, the opposite situation is set as 0.

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after reset.

- Stack Overflow: Configure STKOV[0] as <1>, PC[10:0] is not influened but STKPRT remains at the last layer and new values may be written in. That is to say, the lastest written-in data may be safed after stack full. If SKRST[0] is configured as <1>, reset signal may be generated after stack overflow and SKERR[0] may be set as <1>. STKOV[0] will be set as <0> after reset.
- Errot: Configure SKERR[0] as <1>, stack error occurred. If SKRST[0] is configured <1>, reset signal will be generated after stack overflow and SKERR[0] will be placed <1>. STKUN[0] and STKOV[0] will be configured as <0> after reset.

2.2.1.4. Register Description-Program Memory Controller

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1											
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition											
Address	**File Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**A-RESET**	**R/W**
018h	SKCN	SKFL	SKUN	SKOV	-	-	SKPRT[2:0]			000. .000	u$$. .$$$
01Ah	PCLATH	-	-	-	-	-	PC[10]	PC[9]	PC[8]	.... .0000	 0000
01Bh	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000
02Ch	PSTATUS	POR	PD	TO	IDL	RST	SKERR	-	-	$000 $00.	uu$u u$u.

Table 2-1Program Memory Control Register

STKPTR : Stack Controller Register

Bit	Name	Description
Bit7	STKFL	Stack Full Flag <1> Occurred. <0> Not Occurred.
Bit6	STKUN	Stack Underflow Flag <1> Occurred. <0> Not Occurred.
Bit5	STKOV	Stack Overflow Flag <1> Occurred. <0> Not Occurred.
Bit2~0	STKPRT[2:0]	Stack Pointer Register <111> 7th layer <110> 6th layer ⋮ <000> 0 layer，TOS[10:0]=0x0000h

PCLATH : Program Counter High Byte, PC[10:8]

PCLATL : Program Counter Low Byte, PC[7:0]

PSTATUS : Status Register

Bit	Name	Description
Bit2	SKERR	Stack Error Generated Reset Flag

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		<1> Occurred. <0> Not Occurred.

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2.2.2. Data Memory (DM)

Data Memory (DM) is composed of Specially Register (SR) and General Purpose Register (GPR). Furthermore, it takes every 256byte as a block. 128byte Specially Register and 128 byte General Purpose Register is as in Figure 2-3.

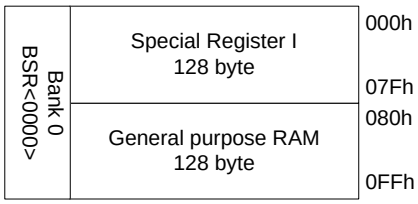

Figure 2-3 Data Memory (DM) Architecture

2.2.2.1. Memory and Instruction

H08 instruction set can be divided A and B two version, which have great difference in memory application, such as addressing capability, hardware multiplier, table look-up instruction, support functions and parameters definition. Here just illustrate definition of instruction memory parameters. See Instruction part of Instruction Set on detailed instruction parameter illustration.

Instructions with address computation function in instruction set have three parameters at most, i.e. "f", "d" and "a".

"f" refers to Data or Data Memory Address.

"d" refers to data storage place after computation. If d=0, it is stored in WREG register. If d=1, it is stored in Data Memory Register.

"a" is memory operation block appointing. If a=0, it is operated in block 0. If a=1, it is operated in BSR [3:0] appointed block.

2.2.2.2. Special Register (SR)

Special Register (SR) includes CPU Core peripheral function related registers. It mainly has control function register and data return register. If it takes reading for address which is not defined in data register or address used bit, read data is 0.

In SR, it also has several registers dedicated in instruction collocation. It just introduces two kinds of commonly used registers. One is working register WREG and the other is indirect addressing register FSR. The rest special registers, which are not introduced here, will be taken detailed illustration in each chapter.

2.2.2.2.1. Working Register (WREG)

Working register is shortened as W. It is the most frequently used register for instruction collocation, ranging from data movement, computation and judgment etc.

2.2.2.2.2. General Purpose Register (GPR)

General Purpose Register (GPR) takes data storage, computation, flag setting and other free planning area for the users.

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2.2.2.3. Register Description-Data Memory Controller

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1											
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition											
位址	名稱	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST
029H	WREG	Working Register								xxxx xxxx	*,*,*,* *,*,*,*

Table 2-2 Data Memory Control Register

WREG: Working Register

WREG[7:0]: See 2.2.2.2.1 Working Register, WREG Description in detail.

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2.2.3. Register List-Data Memory

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1											
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition											
Address	**File Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**A-RESET**	**R/W**
00H	INDF0	Contents of FSR0 to address data memoryvalue of FSR0 not changed								N/A	*,*,*,*,*,*,*,*
0FH	FSR0H									x	-,-,-,- -,-,-,*
10H	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	*,*,*,*,*,*,*,*
18H	STKPTR	STKFL	STKUN	STKOV	-	-	STKPRT[2:0]			000. .000	r,rw0,rw0,- -,r,r,r
1AH	PCLATH	-	-	-	-	-	PC[10]	PC[9]	PC[8]	 0000	-,-,-,- *,*,*,*
1BH	PCLATL	PC Low Byte for PC<7:0>								0000 0000	*,*,*,*,*,*,*,*
1DH	TBLPTRH	TBLW+	TBLW	TBLR+	TBLR	TBLPTR[11]	TBLPTR[10]	TBLPTR[9]	TBLPTR[8]	 0000	-,-,-,- *,*,*,*
1EH	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								0000 0000	*,*,*,*,*,*,*,*
20H	TBLDL	Program Memory Table Latch Low Byte								0000 0000	*,*,*,*,*,*,*,*
23H	INTE0	GIE	ADCIE	TMBIE	TMAIE	LVD_BE	LVDE	E1IE	E0IE	000. 0000	*,*,*,*,*,*,*,*
24H	INTE1	I2CW7IE	I2CW6IE	I2CW5IE	I2CW4IE	I2CW3IE	I2CW2IE	I2CW1IE	I2CW0IE	000. 0000	*,*,*,*,*,*,*,*
25H	INTE2	-	-	-	-	-	I2CW10IE	I2CW9IE	I2CW8IE	000. 0000	*,*,*,*,*,*,*,*
26H	INTF0	-	ADCIF	TMBIF	TMAIF	LVD_BF	LVDF	E1IF	E0IF	000. 0000	w0
27H	INTF1	I2CW7IF	I2CW6IF	I2CW5IF	I2CW4IF	I2CW3IF	I2CW2IF	I2CW1IF	I2CW0IF	000. 0000	w0
28H	INTF2	-	-	-	-	-	I2CW10IF	I2CW9IF	I2CW8IF	000. 0000	w0
29H	WREG	Working Register								xxxx xxxx	*,*,*,*,*,*,*,*
2BH	STATUS	-	-	-	C	-	-	-	Z	...x xxxx	-,-,-,* *,*,*,*
2CH	PSTATUS	BOR	PD	-	IDLE	Crst	SKERR	I2C_RST	I2C_GC_RST	000d .0..	rw0,rw0,rw0,rw0 -,rw0,-,-
2DH	ADCR0H	ADC[19:12]								xxxx xxxx	*,*,*,*,*,*,*,*
2EH	ADCR0M	ADC[11:4]								xxxx xxxx	*,*,*,*,*,*,*,*
2FH	ADCR0L	ADC[3:0]				0	0	0	0	xxxx xxxx	*,*,*,*,*,*,*,*
30H	ADCR1H	ADC[19]	ADC[19]	ADC[19]	ADC[19]	ADC[19]	ADC[18]	ADC[17]	ADC[16]	xxxx xxxx	*,*,*,*,*,*,*,*
31H	ADCR1M	ADC[15:8]								xxxx xxxx	*,*,*,*,*,*,*,*
32H	ADCR1L	ADC[7:0]								xxxx xxxx	*,*,*,*,*,*,*,*
33H	PWRCN0	ENBGR	ENTPS	ENSDR	INIS	TPSLCN	ENLDO	ENLVD	ENADC	000. 0000	*,*,*,*,*,*,*,*
34H	PWRCN1	ADHV	SDRV[1:0]		LVDV[1:0]		LDOV[1:0]		LVDO	000. 0000	*,*,*,*,*,*,*,*
35H	ADCCN0	OSR[2:0]			VREGN	ADG[1:0]		SACM[1:0]		000. 0000	*,*,*,*,*,*,*,*
36H	ADCCN1	INL[2:0]			INH[2:0]			VRI[1:0]		000. 0000	*,*,*,*,*,*,*,*
37H	ADCCN2	DCSET[2:0]			TCR[1:0]		-	-	ADRST	000. 0000	*,*,*,*,*,*,*,*
38H	CLKCN	-	-	-	HAOM[1:0]		CPUCKS	ENHAO	ENLPO	000. 0011	*,*,*,*,*,*,*,*
39H	AL_MO0	LSB for multiplexer input A / LSB for multiplexer output								xxxx xxxx	*,*,*,*,*,*,*,*
3AH	AH_MO1	MSB for multiplexer input A / 15-8 bit multiplexer output								xxxx xxxx	*,*,*,*,*,*,*,*
3BH	BL_MO2	LSB for multiplexer input B / 23-16 bit multiplexer output								xxxx xxxx	*,*,*,*,*,*,*,*
3CH	BH_MO3	MSB for multiplexer input B / MSB for multiplexer output								xxxx xxxx	*,*,*,*,*,*,*,*
3DH	PT0	-	-	PT0EG[1:0]		ENPWM1O	PU0	TC0	PT0IO	000. 0000	*,*,*,*,*,*,*,*
3EH	PT1	-	-	PT1EG[1:0]		ENPWM0O	PU1	TC1	PT1IO	000. 0000	*,*,*,*,*,*,*,*
3FH	PT2	-	-	-	-	ENPWM1O	PU2	TC2	PT2IO	000. 0000	*,*,*,*,*,*,*,*
40H	PT3	-	-	-	-	ENPWM0O	PU3	TC3	PT3IO	000. 0000	*,*,*,*,*,*,*,*

Table 2-3 Data Memory List

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"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1											
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition											
Address	**File Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**A-RESET**	**R/W**
41H	LSB_SEL	SEL_FLAG[7:0]								0000 0000	********
42H	I2C_CMD	TIP	scu_L3	SP	0	0	0	0	EN_SCLO	0000 0000	RRRRRRRW
43H	I2C_O0	I2C Data Output Buffer 0								xxxx xxxx	w
44H	I2C_O1	I2C Data Output Buffer 1								xxxx xxxx	w
45H	I2C_O2	I2C Data Output Buffer 2								xxxx xxxx	w
46H	I2C_O3	I2C Data Output Buffer 3								xxxx xxxx	w
47H	I2C_O4	I2C Data Output Buffer 4								xxxx xxxx	w
48H	I2C_O5	I2C Data Output Buffer 5								xxxx xxxx	w
49H	I2C_O6	I2C Data Output Buffer 6								xxxx xxxx	w
4AH	I2C_O7	I2C Data Output Buffer 7								xxxx xxxx	w
4BH	I2C_I0	I2C Data Intput Buffer 0								xxxx xxxx	r
4CH	I2C_I1	I2C Data Intput Buffer 1								xxxx xxxx	r
4DH	I2C_I2	I2C Data Intput Buffer 2								xxxx xxxx	r
4EH	I2C_I3	I2C Data Intput Buffer 3								xxxx xxxx	r
4FH	I2C_I4	I2C Data Intput Buffer 4								xxxx xxxx	r
50H	I2C_I5	I2C Data Intput Buffer 5								xxxx xxxx	r
51H	I2C_I6	I2C Data Intput Buffer 6								xxxx xxxx	r
52H	I2C_I7	I2C Data Intput Buffer 7								xxxx xxxx	r
53H	I2C_I8	I2C Data Intput Buffer 8								xxxx xxxx	r
54H	I2C_I9	I2C Data Intput Buffer 9								xxxx xxxx	r
55H	I2C_I10	I2C Data Intput Buffer 10								xxxx xxxx	r
56H	TMACN	ENTMA	TMACL	TMAS	DTMA[2:0]			-	-	0000 $000	*,*,*,* rw1,*,*,*
57H	TMAR	TMAR[7:0]								0000 0000	r,r,r,r r,r,r,r
58H	TB1CN0	ENTMB	TB1M[1:0]		DTMB[1:0]		-	-	TMBCL	0000 0000	*,*,*,*,*,*,*,*
59H	TB1C0L	TimerB1 counter Condition Register0 [7:0]								xxxx xxxx	*,*,*,*,*,*,*,*
5AH	TB1C0H	TimerB1 counter Condition Register0 [15:8]								xxxx xxxx	*,*,*,*,*,*,*,*
5BH	TB1C1L	TimerB1 counter Condition Register1 [7:0]								xxxx xxxx	*,*,*,*,*,*,*,*
5CH	TB1C1H	TimerB1 counter Condition Register1 [15:8]								xxxx xxxx	*,*,*,*,*,*,*,*
5EH	EE_CTRL	EN_TBL	PGM	0	0	0	0	0	0		0,1,1,1,1,1,0,0
80H ~ FFH	GPR0	General Purpose Register as 128Byte								xxxx xxxx	

Table 2-4 Data Memory List (Continued)

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3. Oscillator, Clock Source and Power Consumption Management

HY14E10x have two clock sources, ie HAO and LPO, as in Table 3-1. It can distribute and manage CPU and peripheral operation frequency feasibly through clock controller register. Furthermore, it can adjust power consumption of chip properly to reach the energy saving purpose.

Abstract of Clock Control Register :

CLKCN HAOM[1:0], CPUCKS ,ENHAO,ENLPO

Symbol	Frequency	Frequency Controller CLKCN[7:0] Configuration		Instruction Execution Status	
		ENHAO[0]	HAOM[1:0]	SLP	IDLE
HAOM[1:0]	8MHz	1	11	Stop	Oscillation
	8MHz	1	10	Stop	Oscillation
	4MHz	1	01	Stop	Oscillation
	2MHz	1	00	Stop	Oscillation
ENLPO	32KHz	Oscillation is started after the chip is power on.		Stop	Oscillation

Table 3-1Internal RC Oscillator Parameter, Frequency Controller Configuration and Instruction Status

3.1. Oscillator

3.1.1. HAO Oscillator

HAO is internal high speed RC oscillator. Typical output frequency is 2.0~8.0MHz.

When CPU of HY14E10x products uses other oscillators as operation clock source, it can shut off the HAO oscillator via ENHAO[0] setting.

Note : SD18 sampling frequency regardless of how the choice of HAO, will be fixed frequency division to 1MHz. However, when the ADC is turned on, the HAO frequency source must select 4MHz, the ADC will be the best effect.

3.1.2. LPO Oscillator

LPO is internal low speed RC oscillator. Typical output frequency is 32KHz. it is mainly applied to low speed and power saving CPU operation mode clock source.

After HY14E10x of products execute Sleep instructions, LPO oscillator is shut off. LPO will be started oscillation automatically when the chip is awakened.

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3.2. CPU and Peripheral Circuit Clock Source

3.2.1. Clock Source Configuration

Two groups of oscillators output (HS_CK、LS_CK) will be started /stopped, switched and pre-scaled frequency via pre-set operation clock distributor, and then enter CPU and all peripheral circuits of chip, as in Figure 3-1.

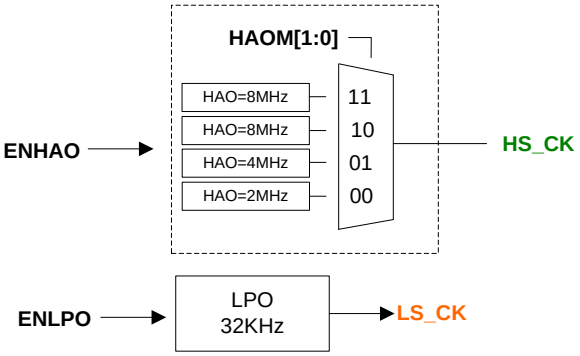

Figure 3-1 Pre-set operation Clock Distributor

3.2.2. CPU Clock Source

CPU has several operation frequency for option. Via CPUCKS[0], optional operation frequency is from HS_CK or DHS_CK.

Instruction operation frequency adopts 1/4 CPU_CK design and frequency is divided to frequency source of INTR_CK.

- When operating ΣΔADC, it is suggested to divide current operation frequency after using HAO=4M for CPU to obtain better performance.
- When CPU_CK frequency and instruction execute cycle, it is as in Figure 3-2. Table 3-2 lists the relation between CPU operation frequency and instruction cycle briefly.

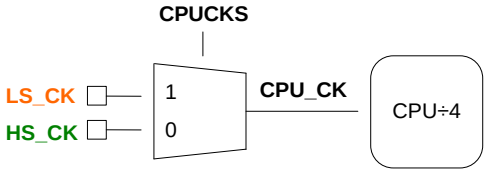

Figure 3-2 CPU and Peripheral Operation Clock

Operation Frequency / CPU_CK	CPU	Instruction	
	Frequency	Frequency	Cycle
8MHZ	8MHZ	2MHz	0.5us
4MHz	4MHz	1MHz	1us
2MHz	2MHz	500kHz	2us
32KHz	32KHz	8KHz	125us

Table 3-2 CPU Operation Frequency and Instruction Execution Cycle

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3.2.3. CPU Peripheral Circuit Clock Source

Operation clock of HY14E10x peripheral circuits is configured by different configuration controller and frequency pre-scaler. The configuration will make detailed illustration in peripheral units, so peripheral operation clock configuration diagram is just attached here, as in Figure 3-3.

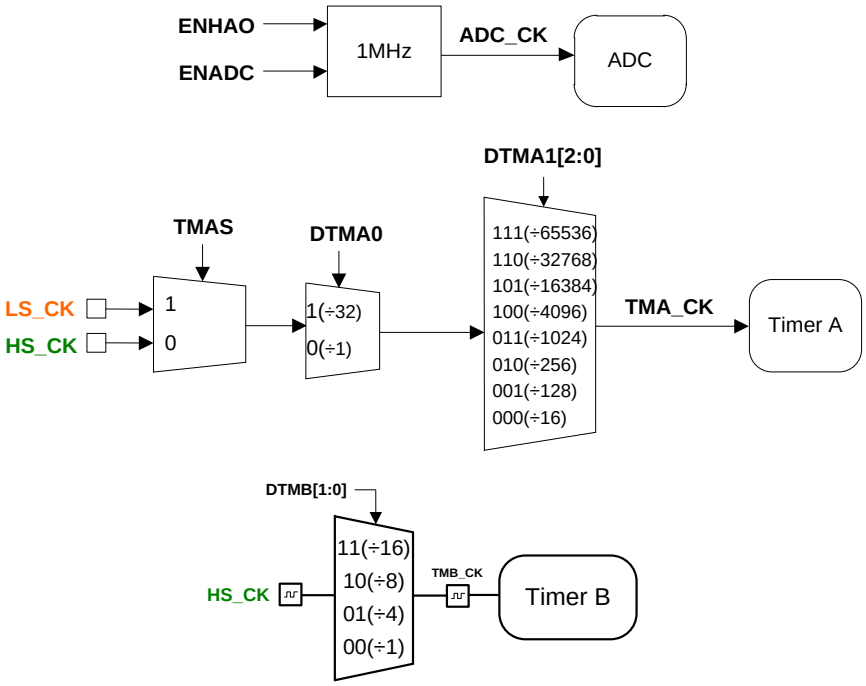

Figure 3-3 Peripheral Operation Clock Configuration Diagram

3.3. Register Description-Operation Clock Source Controller

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1											
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition											
Address	**File Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**A-RESET**	**R/W**
38H	CLKCN	-	-	-	HAOM1	HAOM0	CPUCKS	ENHAO	ENLPO	000. 0011	*,*,*,*,*,*,*,*

Table 3-3 Operation Clock Source Control Register

CLKCN[7:0] : Chip Operation Frequency Control Register

Bit	Name	Description
Bit4~3	HAOM[1:0]	Internal Oscillator HAO Oscillation Frequency Selection <11> 8MHz <10> 8MHz <01> 4MHz <00> 2MHz
Bit2	CPUCKS	CPU Clock Source Selection <1> Selection LS, Internal low frequency oscillator(LPO) <0> Selection HS, Internal high-frequency oscillator(HAO) (ADC operating frequency fixed 1MHz, HS must enable.)
Bit1	ENHAO	Internal HAO Oscillator Control Bit Sleep is invalid, ineffective BOR voltage VDD is lower than the rest are free to switch. <1> Enable HAO <0> Disable HAO
Bit0	ENLPO	Internal LPO Oscillator Control Bit Sleep is invalid, ineffective BOR voltage VDD is lower than the rest are free to switch. <1> Enable LPO <0> Disable LPO

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4. RESET

HY14E10x reset line contains the following events to trigger a reset signal, Reset block diagram is as Figure 4-1.

- **BOR** Power interference reset
- **SKERR** Stack error reset (determined by the user)

Abstract of Operation Status Register :

PSTATUS BOR, PD, IDLE, SKERR

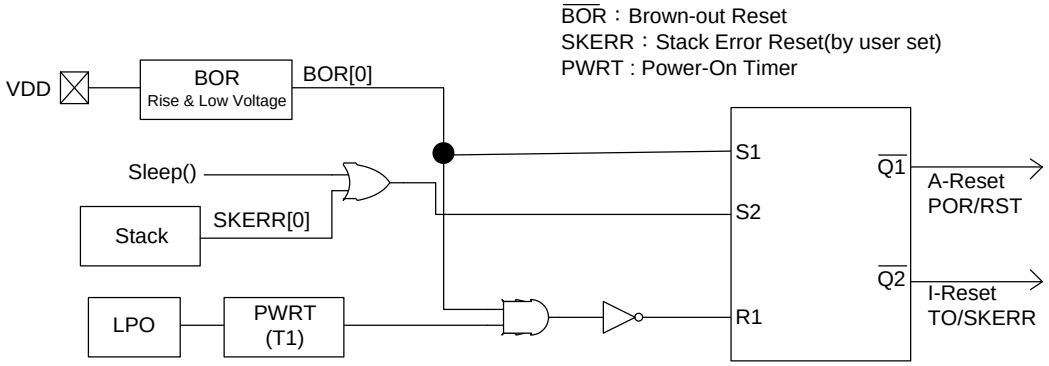

Figure 4-1 Reset Block Diagram

These reset events can be divided into software reset and hardware reset, as in Table 4-1. CPU reset program is started by 0x0000h.

Reset Type	Event	Sym.	Description
Hardware Reset	BOR	A-RESET	CPU restart needs internal oscillator completes counter starting before entering normal operation status.
Low Tier Reset	SKERR	I-RESET	It only clears partial register. CPU is back to normal operation status rapidly.

Table 4-1 Reset Rank List

4.1. Reset Event Description

4.1.1. BOR Power Interference Reset

When CPU is suffered from external interference during powering on process or the power is suffered from external interference, CPU will enter into normal operation voltage from abnormal operation and low operation voltage. Therefore, if CPU cannot be in reset status when the operation voltage is too low, it may cause crash of CPU and make the operation of peripheral circuits abnormal. Therefore, it must rely on BOR circuit function. When it detects that operation voltage is suffered from interference and voltage level is lower than the designed value, it may generate reset signal and make chip enter restart status, until the operation voltage is recovered. Then it will relieve reset signal and make chip enter normal operation mode.

When BOR reset occurs, BOR[0] flag in PSTATUS[7:0] register is set as <1> to record the occurred event.

HY14E10x of BOR circuits will generate about 0.6uA power consumption. It cannot be closed via

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program or other setting method.

4.1.2. SKERR Stack Error Reset

When the program occurs stack overflow or underflow, it may generate reset signal and make chip enter rapid start status. When SKERR stack error reset occurs, SKERR[0] flag in PSTATUS[7:0] register is set as <1> to record the occurred event. See ***Memory*** Section on detailed operation description.

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4.2. Status Register

Chip operation status is displayed in PSTATUS[7:0] reset register. Mutual relation is as in Table 4-2。

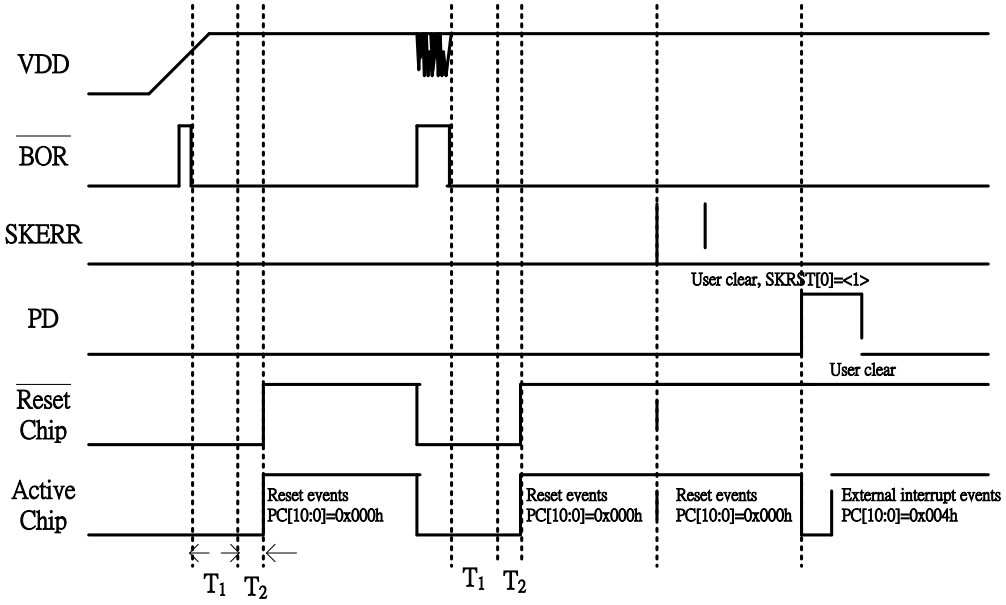
"0": Not Occured,"1": Occurred, "u": Not Changed,"-": Not Used

Name/Status	Address	7	6	5	4	3	2	1	0
PSTATUS	02CH	BOR	PD	-	IDLE	-	SKERR	-	-
Hardware Reset (A-RESET)	BOR	1	0		0		0		
Software Reset (I-RESET)	SKERR	u	u		u		1		

Table 4-2 Reset Status Flags Relation Table

4.2.1. Sequence Diagram of Reset Status

Figure 4-2 presents the time frame from hardware reset signal happened to IC accesses into operating status.



T_1：2048 LPO delay times,T_2：1024 HAO delay times.

Figure 4-2 Sequence Diagram of Reset & Operation Mode and Status Flags

"-" : no definition

Reset Signal	Delay Time			Operating Status		
	Symbol	T1	T2	Run	Idle	Sleep
BOR	t_{RST}	T1＋T2		Valid	Valid	Valid
SKERR	-	-		Valid	Invalid	Invalid

Table 4-3 Interrelation of Reset Status Delay Time and Operating Status

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4.2.2. Register Description-Reset Status

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition											
Address	**File Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**A-RESET**	**R/W**
2CH	PSTATUS	BOR	PD	-	IDLE	ICP_Crst	SKERR	I2C_RST	I2C_GC_RST	000d .0..	rw0,rw0,rw0,rw0 -,rw0,-,-

Table 4-4 Reset Register

PSTATUS : Status Register

Bit	Name	Description
Bit7	BOR	BOR reset event flag <1> Power interference reset has been occurred. It shall use RST or instruction for clearing. <0>Not occurred interference reset
Bit6	PD	SLEEP event flag <1> Sleep event has been occurred. It shall use BOR, RST or instruction for clearing. <0> Not occurred sleep event
Bit4	IDLE	Standby IDLE event flag <1> IDLE event has been occurred. It shall use BOR or instruction for clearing. <0> Not occurred IDLE event
Bit2	SKERR	Stack error reset flag <1> Stack error. It shall use BOR or instruction for clearing. <0> No stack error

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5. Interrupt

Interrupt is composed of interrupt start controller INTE and interrupt event flag INTF. When Interrupt service is established, if it appears interrupt event, program counter (PC) will jump to interrupt address 0x0004h in PM to execute interrupt service program.

Abstract of Interrupt Control Register :

INTE0	GIE, ADCIE, TMBIE, TMAIE, LVD_BE,L VDE, E1IE, E0IE
INTE1	I2CW7IE, I2CW6IE, I2CW5IE, I2CW4IE, I2CW3IE, I2CW2IE, I2CW1IE, I2CW0IE
INTE2	I2CW10, I2CW9, I2CW8IE
INTF0	ADCIF, TMBIF, TMAIF, LVD_BF, LVDF, E1IF, E0IF
INTF1	I2CW7IF, I2CW6IF, I2CW5IF, I2CW4IF, I2CW3IF, I2CW2IF, I2CW1IF, I2CW0IF
INTF2	I2CW10, I2CW9, I2CW8IF

Interrupt service event governor has two layers totally. The higher layer is interrupt service event controller GIE [0] and the lower layer is interrupt event start control bit.

- To start interrupt event, it only needs to set the controller of corresponding interrupt event start controller INTEx [7:0] as <1>. On the contrary, it will close the interrupt event when it is set as <0>.
- To start interrupt service, it only needs to set the interrupt service controller GIE[0] of interrupt control register INTE0[7:0] as <1>. On the contrary, it will close the interrupt service when it is set as <0>.

When entering into interrupt service vector, GIE [0] will be set as <0> automatically. When it is going to return interrupt occurrence address after completing interrupt service program execution, it can execute interrupt return instruction RETI directly. At the moment, GIE [0] will be set as <1> automatically. Or it executes return instruction RET, and GIE [0] status maintains at 0 at the moment.

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5.1. Register Description-Interrupt

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1											
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition											
Address	File Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A-RESET	R/W
23H	INTE0	GIE	ADCIE	TMBIE	TMAIE	LVD_BE	LVDE	E1IE	E0IE	000. 0000	*,*,*,*,*,*,*,*
24H	INTE1	I2CW7IE	I2CW6IE	I2CW5IE	I2CW4IE	I2CW3IE	I2CW2IE	I2CW1IE	I2CW0IE	000. 0000	*,*,*,*,*,*,*,*
25H	INTE2	-	-	-	-	-	I2CW10IE	I2CW9IE	I2CW8IE	000. 0000	*,*,*,*,*,*,*,*
26H	INTF0	-	ADCIF	TMBIF	TMAIF	LVD_BF	LVDF	E1IF	E0IF	000. 0000	w 0
27H	INTF1	I2CW7IF	I2CW6IF	I2CW5IF	I2CW4IF	I2CW3IF	I2CW2IF	I2CW1IF	I2CW0IF	000. 0000	w 0
28H	INTF2	-	-	-	-	-	I2CW10IF	I2CW9IF	I2CW8IF	000. 0000	w 0

Table5-1 Interrupt Register

INTE0 : Interrupt Enable Control Register 0

Bit	Name	Description
Bit7	GIE	Global Interrupt Enable Controller <1> Enable GIE <0> Disable GIE
Bit6	ADCIE	ADC Interrupt Event Enable Controller <1> Enable (Analog Digital Converter, ΣΔADC) <0> Disable
Bit5	TMBIE	Timer-B Interrupt Event Enable Controller <1> Enable (Timing/ Timer B, TMB) <0> Disable
Bit4	TMAIE	Timer-A Interrupt Event Enable Controller <1> Enable (Timing/ Timer A, TMA) <0> Disable
Bit3	LVD_BE	VDD Voltage Recovery Detection Interrupt Enable Controller <1> Enable (VDD>LVD Interrupt) <0> Disable
Bit2	LVDE	VDD Low Voltage Detection Interrupt Enable Controller <1> Enable (VDD<LVD Interrupt) <0> Disable
Bit1	E1IE	Input Pin 0 Interrupt Event Enable Controller <1> Enable (External Input Pin, PT1) <0> Disable
Bit0	E0IE	Input Pin 0 Interrupt Event Enable Controller <1> Enable (External Input Pin, PT0) <0> Disable

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INTE1 : Interrupt Enable Control Register 1

Bit	Name	Description
Bit7	I2CW7IE	I^2C data written to the interrupt controller to enable event <1> Enable,(Data written to allow I^2C master Buffer 7 generate an interrupt event) <0> Disable
Bit6	I2CW6IE	I^2C data written to the interrupt controller to enable event <1> Enable,(Data written to allow I^2C master Buffer 6 generate an interrupt event) <0> Disable
Bit5	I2CW5IE	I^2C data written to the interrupt controller to enable event <1> Enable,(Data written to allow I^2C master Buffer 5 generate an interrupt event) <0> Disable
Bit4	I2CW4IE	I^2C data written to the interrupt controller to enable event <1> Enable,(Data written to allow I^2C master Buffer 4 generate an interrupt event) <0> Disable
Bit3	I2CW3IE	I^2C data written to the interrupt controller to enable event <1> Enable,(Data written to allow I^2C master Buffer 3 generate an interrupt event) <0> Disable
Bit2	I2CW2IE	I^2C data written to the interrupt controller to enable event <1> Enable,(Data written to allow I^2C master Buffer 2 generate an interrupt event) <0> Disable
Bit1	I2CW1IE	I^2C data written to the interrupt controller to enable event <1> Enable,(Data written to allow I^2C master Buffer 1 generate an interrupt event) <0> Disable
Bit0	I2CW0IE	I^2C data written to the interrupt controller to enable event <1> Enable,(Data written to allow I^2C master Buffer 0 generate an interrupt event) <0> Disable

INTE2 : Interrupt Enable Control Register 2

Bit	Name	Description
Bit2	I2CW10IE	I^2C data written to the interrupt controller to enable event <1> Enable,(Data written to allow I^2C master Buffer 10 generate an interrupt event) <0> Disable
Bit1	I2CW9IE	I^2C data written to the interrupt controller to enable event <1> Enable,(Data written to allow I^2C master Buffer 9 generate an interrupt event) <0> Disable
Bit0	I2CW8IE	I^2C data written to the interrupt controller to enable event <1> Enable,(Data written to allow I^2C master Buffer 8 generate an interrupt event) <0> Disable

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INTF0 : Interrupt Event Flag Register 0

Bit	Name	Description
Bit6	ADCIF	ADC interrupt event flag <1> Happened (Analog-to-digital converter, ΣΔADC) <0> Not happened
Bit5	TMBIF	Timer-B interrupt event flag <1> Happened (Time B, TMB) <0> Not happened
Bit4	TMAIF	Timer-A interrupt event flag <1> Happened (Time A, TMA) <0> Not happened
Bit3	LVD_BF	VDD voltage recovery detection interrupt event flag <1> Happened (Response VDD>LVD) <0> Not happened
Bit2	LVDF	VDD Low voltage detect interrupt event flag <1> Happened (Response VDD<LVD) <0> Not happened
Bit1	E1IF	Interrupt event flag of input pin 1 <1> Happened (External input pin, PT1) <0> Not happened
Bit0	E0IF	Interrupt event flag of input pin 0 <1> Happened (External input pin, PT0) <0> Not happened

INTF1 : Interrupt Event Flag Register 1

Bit	Name	Description
Bit7	I2CW7IF	I^2C data write interrupt event flag <1> Happened (I^2C host write data Buffer 7) <0> Not happened
Bit6	I2CW6IF	I^2C data write interrupt event flag <1> Happened (I^2C host write data Buffer 6) <0> Not happened
Bit5	I2CW5IF	I^2C data write interrupt event flag <1> Happened (I^2C host write data Buffer 5) <0> Not happened
Bit4	I2CW4IF	I^2C data write interrupt event flag <1> Happened (I^2C host write data Buffer 4) <0> Not happened

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Bit	Name	Description
Bit3	I2CW3IF	I^2C data write interrupt event flag <1> Happened (I^2C host write data Buffer 3) <0> Not happened
Bit2	I2CW2IF	I^2C data write interrupt event flag <1> Happened (I^2C host write data Buffer 2) <0> Not happened
Bit1	I2CW1IF	I^2C data write interrupt event flag <1> Happened (I^2C host write data Buffer 1) <0> Not happened
Bit0	I2CW0IF	I^2C data write interrupt event flag <1> Happened (I^2C host write data Buffer 0) <0> Not happened

INTF2 : Interrupt Event Flag Register 2

Bit	Name	Description
Bit2	I2CW10IF	I^2C data write interrupt event flag <1> Happened (I^2C host write data Buffer 10) <0> Not happened
Bit1	I2CW9IF	I^2C data write interrupt event flag <1> Happened (I^2C host write data Buffer 9) <0> Not happened
Bit0	I2CW8IF	I^2C data write interrupt event flag <1> Happened (I^2C host write data Buffer 8) <0> Not happened

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6. Input/ Output Port (I/O)

Every pins of Input/ Output Port (I/O) are one port. It can be taken as digital input and output and analog signal measuring channel. Each port is controlled by a group of registers.

Abstract of I/O related register :

PT0 PT0GE[1:0], ENPWM0O, PU0, TC0, PT0IO

PT1 PT1GE[1:0], ENPWM1O, PU1, TC1, PT1IO

PT2 ENPWM2O, PU2, TC2, PT2IO

PT3 ENPWM3O, PU3, TC3, PT3IO

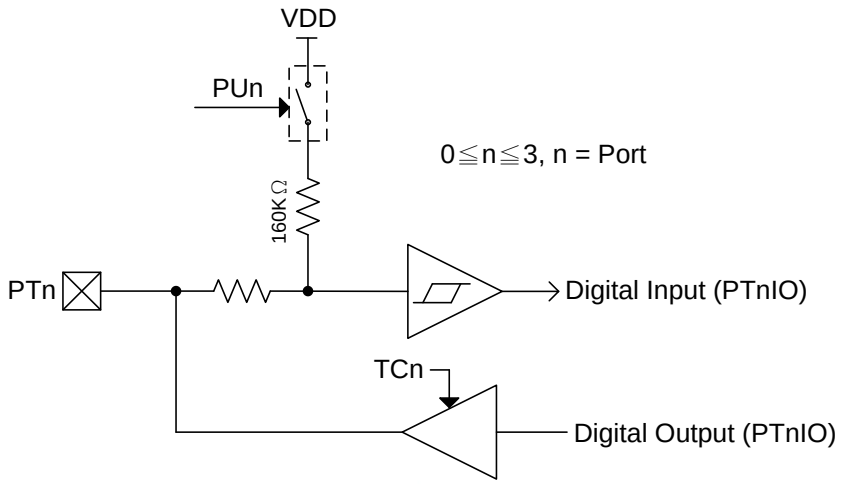

Figure 6-1 I/O Architecture Block Diagram

6.1. PORT Related Register Introduction

PORT mainly offers digital or analog signal I/O pin.

6.1.1. PTEG Interrupt Signal Generated Conditions

When I/O external input potential belongs to certain changes, it may cause interrupt signal. Potential changes can be divided into rising edge (0→1) change, falling edge (1→0) change and potential transition (0→1or 1→0).

6.1.2. PTPU Pull-Up Resistor Control Register

When I/O is set as whether pull-up resistor function is started. Set <1> as I/O starting and set <0> as disconnection. Before the chip enters into sleep mode, if I/O is set as digital input status and external circuit connection way may cause floating phenomena of I/O, it can start pull-up resistor to avoid I.O floating and causing the chip entering into sleep mode and producing current leakage.

6.1.3. TC Input/Output Control Register

When I/O is selected as input or output, set <1>I/O as output status and <0> as input status. When I/O is set as input status, it must give definite input potential when the chip enters into sleep status. Don't make I/O in floating status to avoid causing power leakage phenomena of chip.

6.1.4. PTIO Status Control Register

When I/O is set as input, it can read current I/O status at corresponding register position. I/O

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input is high potential when the reading is 1 at the moment, and low potential when is 0.

When I/O is set as output, it can control output status at corresponding register position. I/O output is high potential when it is set as <1> at the moment, and low potential when is<0>.

6.2. Register Description-PORT

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1											
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition											
Address	**File Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**A-RESET**	**R/W**
3DH	PT0	-	-	PT0EG[1:0]		ENPWM1O	PU0	TC0	PT0IO	000. 0000	*,*,*,* *,*,*,*
3EH	PT1	-	-	PT1EG[1:0]		ENPWM0O	PU1	TC1	PT1IO	000. 0000	*,*,*,* *,*,*,*
3FH	PT2	-	-	-	-	ENPWM1O	PU2	TC2	PT2IO	000. 0000	*,*,*,* *,*,*,*
40H	PT3	-	-	-	-	ENPWM0O	PU3	TC3	PT3IO	000. 0000	*,*,*,* *,*,*,*

Table 6-1 PORT Control Register

INTE0/INTF0 : Please refer to *Interrupt* Chapter

PT0/ PT1/PT2/PT3 : PORT Control Register

Bit	Name	Description
Bit5~4	PTnGE[1:0]	Pin PTn interrupt way controller (n=0~1) <11> When the next CPU instruction read I/O status, when external changes to the I/O status interrupt occurs. <10> potential transition (0→1 or 1→0),i.e. Producing interrupt event; interrupt event will be occurred so long as potential transition. <01> rising edge (0→1) <00> falling edge (1→0)
Bit3	ENPWMnO	PWM Output control bit (0≦n≦1) <1> Enable <0> Disable
Bit2	PUn	External pin pull-up resistor control bit (0≦n≦3) <1> Enable <0> Disable
Bit1	TCn	External pin input /output control bit (0≦n≦3) <1> Enable Output Mode <0> Input Mode Only
Bit0	PTnIO	External pin control bit (0≦n≦3) <1> High potential <0> Low potential

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7. Timer-A (TMA)

Timer-A (hereinafter referred to as TMA) is designed in 8-bit frame. TMA can function in Run Mode and Idle Mode.

- Ascending counter
- 4-step overflow value select
- Overflow generated interrupt event
- Counter value is readable

TMA Registers :

TMACN	ENTMA, TMACL, TMAS, DTMA1[2:0]
TMAR	TMAR[7:0]
INTE0	TMAIE
INTF0	TMAIF

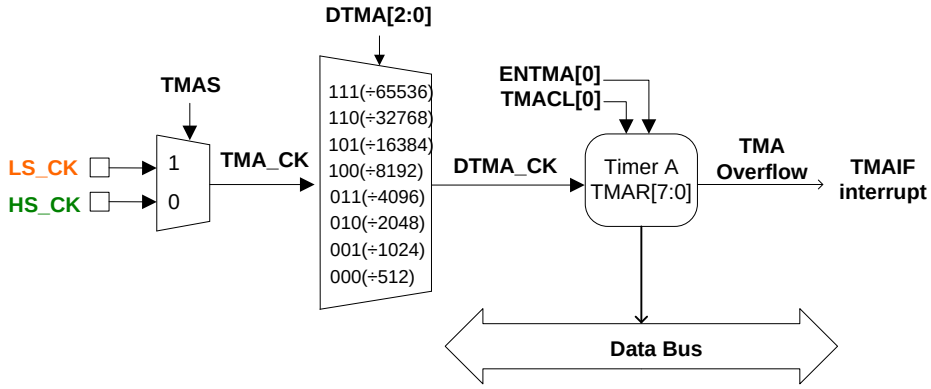

Figure 7-1 Timer-A Block Diagram

- Operation Instructions :

  Set ENTMA[0] as <1> to start TMA; on the contrary, set as<0> to close and clear TMAR[7:0].

  When DTMA[2:0] timing condition is established, it may produce interrupt event and make TMAR[7:0] progressively increase 1.

  TMA interrupt event TMAIF[0] must have interrupt service when TMAIE[0] is set as <1> and GIE[0] is set as <1>. TMA interruption in Debug Mode, the interrupt flag TMAI always 0. But interrupt function still exists, the user still needs to be cleared in the interrupt subroutine interrupt flag TMAIF.

  Reading TMAR[7:0] will not make TMA timer zeroed.

  After the user sets TMACL[0] as <1> and clear all timers of TMA, TMACL[0]will be set as <0> automatically.

  TMAR[7:0] can read TMA progressively increased value of the timer, and can write motion to clear the timing value of TMAR[7:0].

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7.1. Register Description-TMA

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1											
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition											
Address	**File Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**A-RESET**	**R/W**
23H	INTE0	GIE	ADCIE	TMBIE	TMAIE	LVD_BE	LVDE	EUIE		000. 0000	*,*,*,*,*,*,*,*
26H	INTF0	-			TMAIF					000. 0000	w 0
56H	TMACN	ENTMA	TMACL	TMAS	TMA[2:0]			-		0000 $000	*,*,*,* rw 1,*,*,*
57H	TMAR	TMAR[7:0]								0000 0000	r,r,r,r r,r,r,r

Table 7-1 TMA Control Register

INTE0/INTF0 : Please refer to *Interrupt* Chapter

TMACN : Timer-A Control Register

Bit	Name	Description
Bit7	ENTMA	Timer-A enable controller <1> Enable <0> Shutoff ; Zero counters
Bit6	TMACL	TMA clear of counter <1> TMA clear of counter, When writing "1" clear TMAR[7: 0] and Pre-counter, automatically returns to "0" <0> TMA Counting.
Bit5	TMAS	TMA Operation Frequency Selector <1>TMA clock=LS <0>TMA clock=HS(default)
Bit4~2	DTMA1[2:0]	TMA Pre-Counter Selector, Also Timer A interrupt frequency <111> TMAR clock = TMA clock/65536 <110> TMAR clock = TMA clock/32768 <101> TMAR clock = TMA clock/16384 <100> TMAR clock = TMA clock/8192 <011> TMAR clock = TMA clock/4096 <010> TMAR clock = TMA clock/2048 <001> TMAR clock = TMA clock/1024 <000> TMAR clock = TMA clock/512

TMAR : TMA ascending counter, readable but not writable

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8. 16-bit TimerB (TMB)

Timer B (hereinafter referred to as TMB) has 2 PWM output, which is PWMA0/1 respectively. Each TMB has 4 types of operation mode. All timers of each mode have special function design to satisfy different application method.

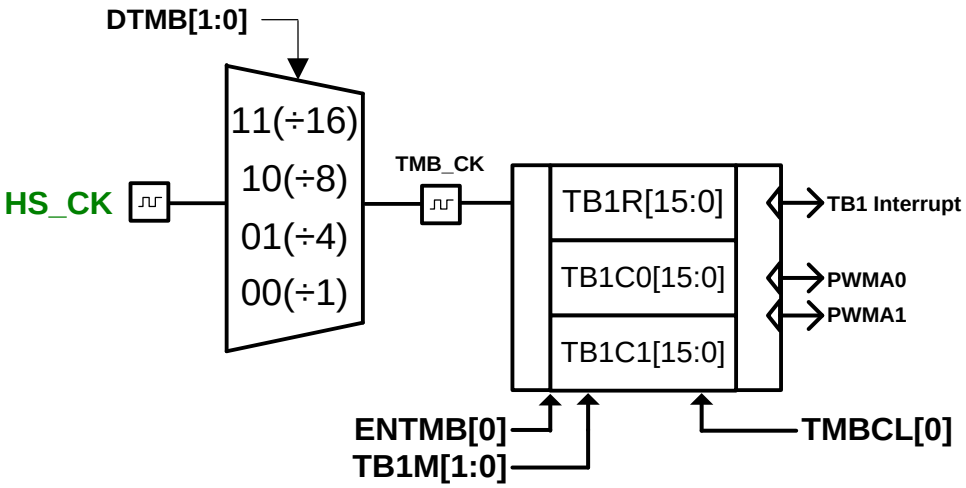

Figure 8-1 Timer-B Block Diagram

◆ Timer Registers of TMB are

Increment / decrement timer TB1R[15:0] (this is a hardware counter and can not be read or written)

Overflow event condition controller TB1C0[15:0]

PWMA condition controller TB1C1[15:0]

Enable controller ENTMB[0]

Mode controller TB1M[1:0]

Zeroing controller TB1CL[0]

Operation frequency pre-eliminator DTMB[1:0]

◆ 4 types of counting modes of TMB

16-bit counting

16 bit pulse generator mode

Dual 8-bit PWM mode

8+8bit PWM mode

◆ System power consumption operation of TMB

Operation Mode

Idle Mode

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◆ TB1R[15:0] Zeroing and Re-counting Condition

Read TMB related register, and it will not make TB1R[15:0] zero and re-count.

Writing TB1C0[15:0] and TB1C1[15:0] will not make TB1R[15:0] zero and re-count.

Writing TB1CN0 control register will not make TB1R[15:0] zero and re-count.

When TB1R[15:0] progressive counting is up to more than TB1C0[15:0], it will make TB1R[15:0] zero and re-count.

After user set TB1CL[0] as <1> and clear TB1R[15:0] timer, TB1CL[0] is set as<0> automatically.

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8.1. 4 types of counting modes of TMB

8.1.1. 16-bit counting

Set the counting mode selector TB1M[1:0] as <00> to make TMB operate under 16-bit counting mode. Under this mode, it has the following features:

- When TB1R[15:0] progressive counting is equal to TB1C0[15:0], it generator overflow event TB1IF[0] and zero and re-count TB1R[15:0].

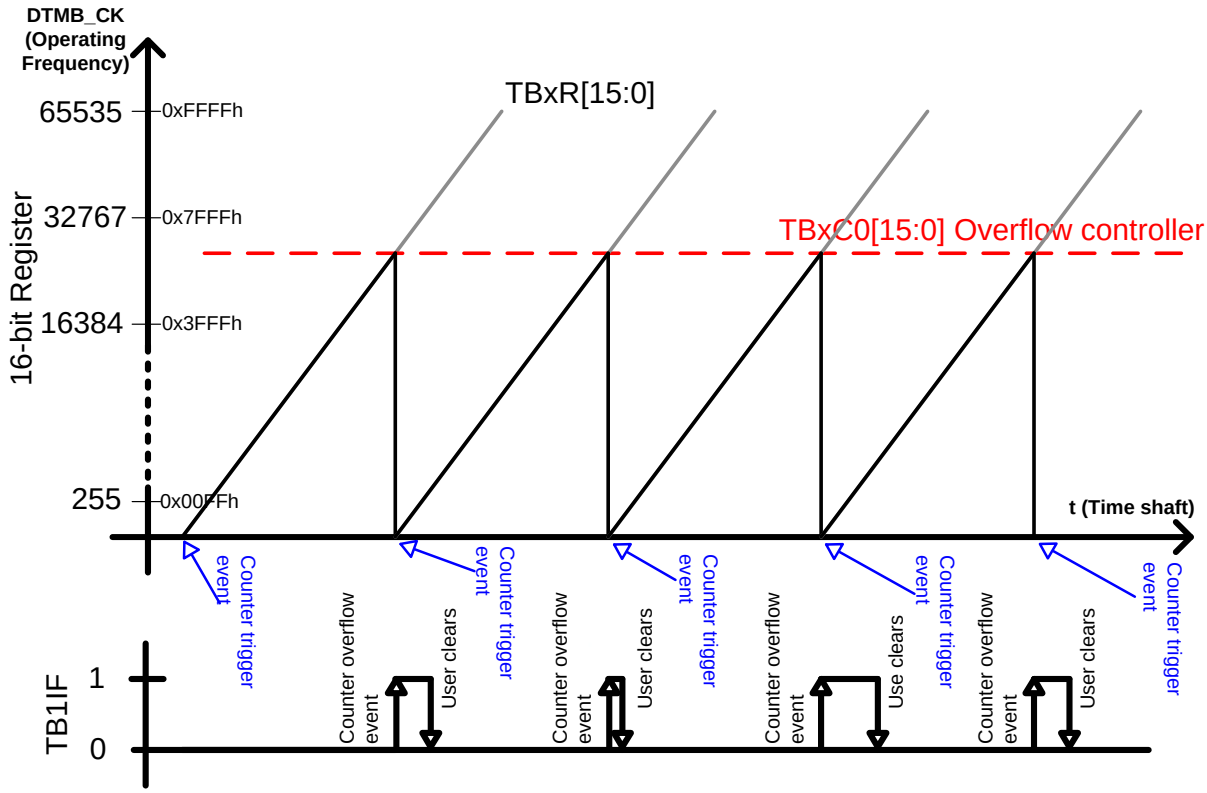

Figure 8-2 16-bit Timer Waveform and Using Schematic Diagram

- Operation Instructions of 16-bit Counting Mode
  - Initial Configuration
    - TMB source operating frequency is fixed at HAO Set DTMB[1:0] to determine TMB operation frequency.
    - TB1M[1:0 is set as<00>. Plan TMB1 as 16-bit timer.
    - Write data to TB1C0[15:0]. (TB1C0H*256+TB1C0L)
  - Trigger counting signal as Always Enable status, i.e. cycle count.
  - Set ENTMB[0] as <1> to start timer.
    - When TB1R[15:0] counting value is equal to TB1C0[15:0], it will produce overflow event and make TB1IF[0] set as <1>, and it is zeroed and re-taken increment counting. At the moment, it will produce interrupt event service when GIE[0]、TB1IE[0] is set as <1>.
    - During counting process, the user can set counting zeroing controller TB1CL[0] as <1> to recount, and TB1CL[0] will be set as <0> automatically.
  - Set ENTMB[0] as <0> to close the timer.

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- Operation Instructions of 16-bit PWM Mode
  - Initialization Configuration (PWM Frequency and Duty Cycle Setting)
    - TMB source operating frequency is fixed at HAO Set DTMB[1:0] to determine TMB operation frequency.
    - TB1M[1:0] is set as <00>. Plan TMB1 as 16-bit timer.
    - Trigger counting signal as Always Enable, i.e. cycle count.
    - Write data to TB1C0[15:0] (TB1C0H*256+TB1C0L)to determine the frequency of PWM.
    - Write data to TB1C1[15:0] (TB1C1H*256+TB1C1L) to determine the Duty Cycle of PWM.
    - Set ENTMB[0] as <1> to start timer.
  - Generator PWM0 Waveform
    - When TB1R[15:0] counting value is equal to TB1C1[15:0], it makes the status of PWM0 be 0➔1.
    - When TB1R[15:0] recounting value is equal to TB1C0[15:0], it makes the status of PWM0 be 1➔0. Furthermore, it generator overflow event and makes TMBIF[0] set as <1> and zero and retake increment counting. At the moment, it will produce interrupt event service when GIE[0]、TMBIE[0] is set as <1>.
  - PWM Output Control
    - Set the pin output PWM waveform status as output status, and set ENPWM0[0] as <1>to start output as PWM function. Confirm whether the pin related setting is correct.
  - When ENTMB[0] is set as <0>, it will close timer and PWM output.
  - Calculation equation of PWM1 frequency Duty Cycle is:

$$\text{PWM0 Frequency} = \frac{\text{DTMB\_CK}}{\text{TB1C0}[15:0]+1}$$

$$\text{PWM0 Duty Cycle} = \frac{(\text{TB1C0}[15:0]+1) - \text{TB1C1}[15:0]}{\text{TB1C0}[15:0]+1}$$

8.1.2. 16 bit pulse generator mode

The counting mode selector TB1M[1: 0] settings <01> so TMB operates in 16-bit mode pulse generator, which generates a pulse wave number is (TB1C1H * 256 + TB1C1L).

After the pulse generator, TMB will automatically shut down. To the end of the pulse generator issues an interrupt, set (TB1C0H * 256 + TB1C0L) settings (TB1C1H * 256 + TB1C1L) the same.

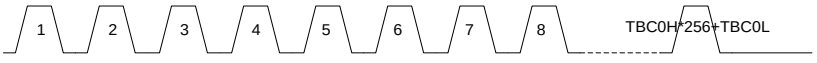
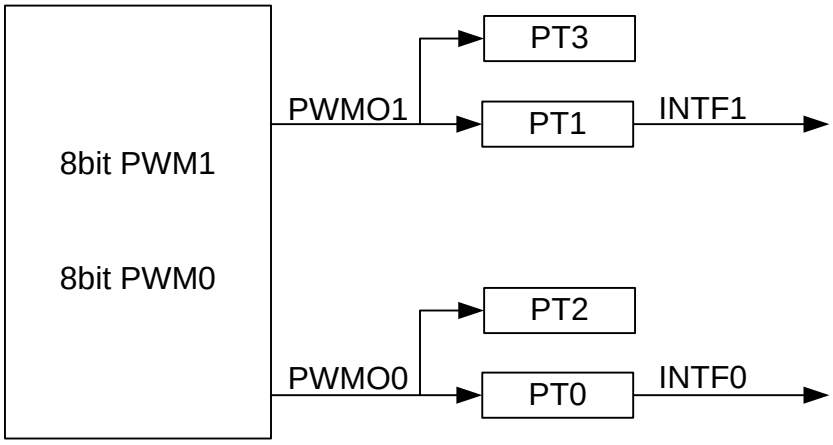


Figure 8-3 16 bit pulse generator Waveform and Using Schematic Diagram

8.1.3. Dual 8-bit PWM mode



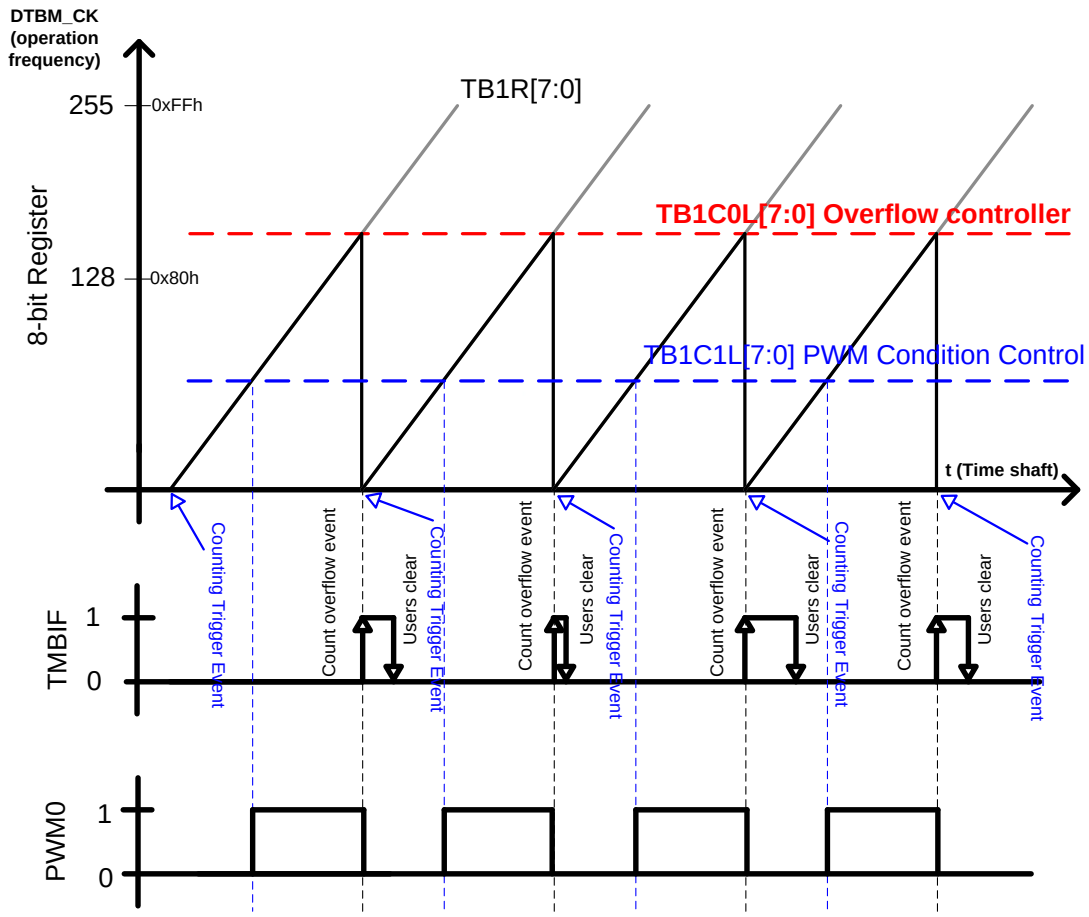


Figure 8-4 PWM1 Waveform and Using Schematic Diagram

- PWM0 Output Operation Instructions
  - Initialization Configuration (PWM Frequency and Duty Cycle Setting)
    - TMB source operating frequency is fixed at HAO Set DTMB[1:0] to determine TMB operation frequency.
    - TB1M[1:0] is set as <10>. Plan TMB1 as Dual 8-bit count.
    - Trigger counting signal as Always Enable, i.e. cycle count.
    - Write data to TB1C0L[7:0] to determine the frequency of PWM.
    - Write data to TB1C1L[7:0] to determine the Duty Cycle of PWM.

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- Set ENTMB [0] as <1> to start timer.

- Generator PWM0 Waveform
  - When TB1R[7:0] counting value is equal to TB1C1L[7:0], it makes the status of PWM0 be 0➔1.
  - When TB1R[7:0] recounting value is equal to TB1C0L[7:0], it makes the status of PWM0 be 1➔0. Furthermore, it generator overflow event and makes TMBIF[0] set as <1> and zero and retake increment counting. At the moment, it will produce interrupt event service when GIE[0]、TMBIE[0] is set as <1>.
- PWM Output Control
  - Set the pin output PWM waveform status as output status, and set ENPWM0[0] as <1>to start output as PWM function. Confirm whether the pin related setting is correct.
- When ENTMB[0] is set as <0>, it will close timer and PWM output.
- Calculation equation of PWM0 frequency Duty Cycle is:

$$\text{PWM0 Frequency} = \frac{\text{DTMB\_CK}}{\text{TB1C0L}[7:0]+1}$$

$$\text{PWM0 Duty Cycle} = \frac{(\text{TB1C0L}[7:0]+1) - \text{TB1C1L}[7:0]}{\text{TB1C0L}[7:0]+1}$$

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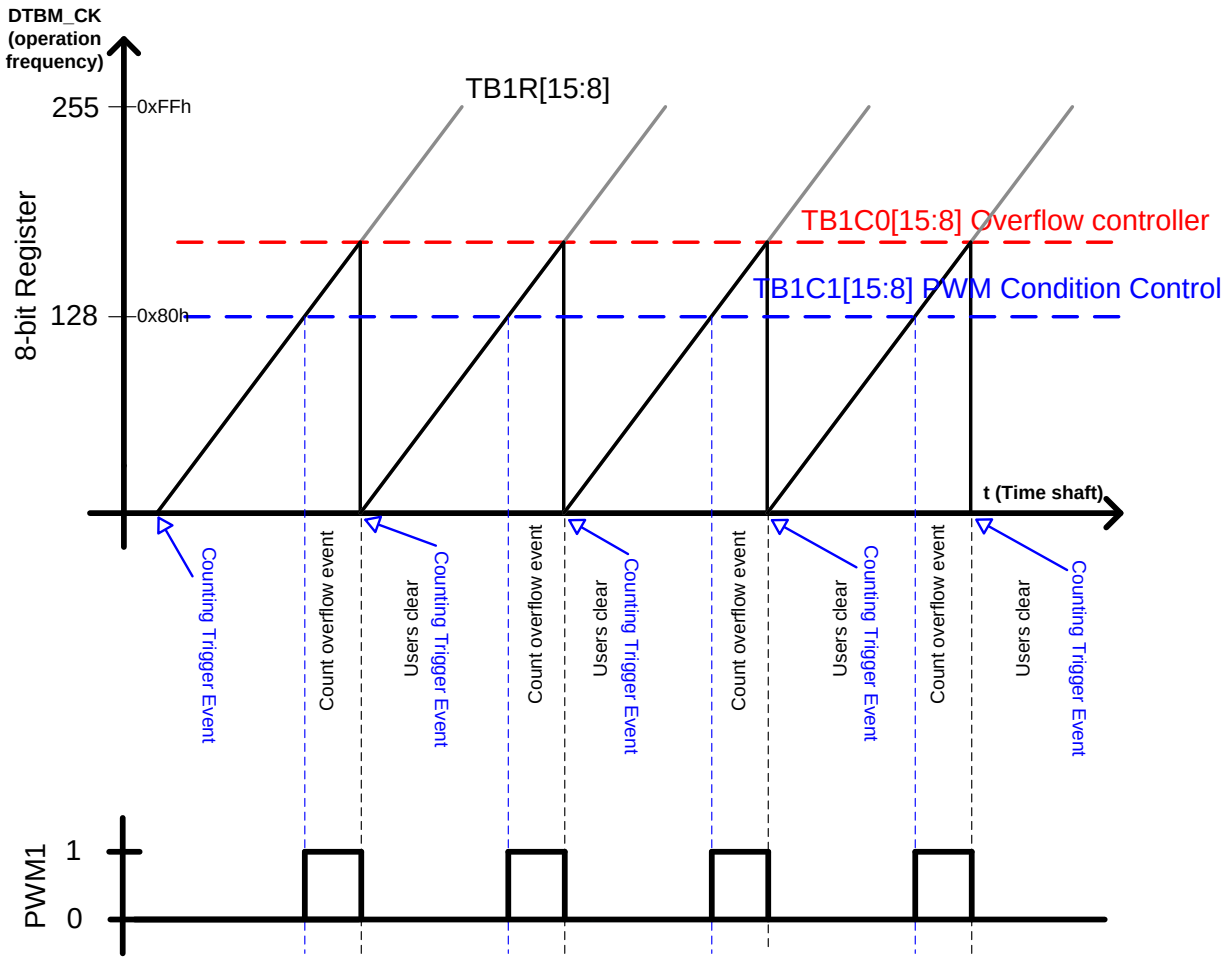

Figure 8-5 PWM1 Waveform and Using Schematic Diagram

- PWM1 Output Operation Instructions
  - Initialization Configuration (PWM Frequency and Duty Cycle Setting)
    - TMB source operating frequency is fixed at HAO Set DTMB[1:0] to determine TMB operation frequency.
    - TB1M[1:0] is set as <10>. Plan TMB1 as Dual 8-bit count.
    - Trigger counting signal as Always Enable, i.e. cycle count.
    - Write data to TB1C0H[7:0] to determine the frequency of PWM.
    - Write data to TB1C1H[7:0] to determine the Duty Cycle of PWM.
    - Set ENTMB[0] as <1> to start timer.
  - Generator PWM1 Waveform
    - When TB1R[15:8] counting value is equal to TB1C1H[15:8], it makes the status of PWM0 be 0➔1.
    - When TB1R[15:8] recounting value is equal to TB1C0H[15:8], it makes the status of PWM0 be 1➔0. Furthermore, it generator overflow event and makes TMBIF[0] set as <1> and zero and retake increment counting. At the moment, it will produce interrupt event service when GIE[0]、TMBIE[0] is set as <1>.
  - PWM Output Control

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- Set the pin output PWM waveform status as output status, and set ENPWM1[0] as <1>to start output as PWM function. Confirm whether the pin related setting is correct.

- When ENTMB[0] is set as <0>, it will close timer and PWM output.
- Calculation equation of PWM0 frequency Duty Cycle is:

$$\text{PWM1 Frequency} = \frac{\text{DTMB\_CK}}{\text{TB1C0H}[15:8]+1}$$

$$\text{PWM1 Duty Cycle} = \frac{(\text{TB1C0H}[15:8]+1) - \text{TB1C1H}[15:8]}{\text{TB1C0H}[15:8]+1}$$

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8.1.4. 8+8-bit PWM

When TMB is set as 8+8-bit mode and PWM output waveform is selected as PWM5, it can produce 8+8bit PWM output.

8+8-bit PWM is composed of TB1R[7:0], TB1C0L[15:8], TB1C1L[7:0] and TB1C1H[15:8] control registers and internal digital circuit. TB1C0[7:0] is PWM frequency controller, TB1C1L[7:0] is PWM duty cycle controller, and TB1C1H[15:8] is 8+8-bit PWM duty cycle trimmer.

Setting and instruction of 8+8-bit PWM duty cycle spinne TB1C1H[15:8] are as in the following table.

Setting / Weighted Quantity	TB1C1H[15:8]							
	80h	40h	20h	10h	08h	04h	02h	01h
Fine tuning of PWM duty cycle	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256
Description	2 times of TMB overflow, one half N+1and one half N	4 times of TMB overflow，one half N+1and one half N	8 times of TMB overflow，one half N+1and one half N	16 times of TMB overflow，one half N+1and one half N	32 times of TMB overflow，one half N+1and one half N	64 times of TMB overflow，one half N+1and one half N	128 times of TMB overflow，one half N+1and one half N	256 times of TMB overflow，one half N+1and one half N

Table 8-1 Duty Cycle Trimmer Setting Table

- Description of duty cycle trimmer TB1C1H[15:8], in which N is the width of duty cycle, (*Note: N = TB1C1[7:0]*)
  - Basic Type
    - TB1C1H[15:8] is set as 80h, and it makes waveform of PWM duty cycle occur N+1 and N output, i.e. it generator waveform taking 2 output periods as a group--- one is N+1 and the other is N.
    - TB1C1H[15:8] is set as 40h, and it makes waveform of PWM duty cycle occur N+1 and N output, i.e. it generator waveform taking 4 output periods as a group--- 2 continuous output is N+1 and the other 2 is N.
    - TB1C1H[15:8] is set as 20h, and it makes waveform of PWM duty cycle occur N+1 and N output, i.e. it generator waveform taking 8 output periods as a group--- 4 continuous output is N+1 and the other 4 is N.

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- TB1C1H[15:8] is set as 10h, and it makes waveform of PWM duty cycle occur N+1 and N output, i.e. it generator waveform taking 16 output periods as a group--- 8 continuous output is N+1 and the other 8 is N.
- TB1C1H[15:8] is set as 08h, and it makes waveform of PWM duty cycle occur N+1 and N output, i.e. it generator waveform taking 32 output periods as a group---16 continuous output is N+1 and the other 16 is N.
- TB1C1H[15:8] is set as 04h, and it makes waveform of PWM duty cycle occur N+1 and N output, i.e. it produces waveform taking 64 output periods as a group--- 32 continuous output is N+1 and the other 32 is N.
- TB1C1H[15:8] is set as 02h, and it makes waveform of PWM duty cycle occur N+1 and N output, i.e. it generator waveform taking 128 output periods as a group--- 64 continuous output is N+1 and the other 64 is N.
- TB1C1H[15:8] is set as 01h, and it makes waveform of PWM duty cycle occur N+1 and N output, i.e. it generator waveform taking 256 output periods as a group--- 128 continuous output is N+1 and the other 128 is N.

■ Logic Computation OR Superimposition Type

(only takes 1/2+1/4,1/2+1/8,~,1/2+1/4+1/8+1/16+1/32+1/64+1/128,1/2+1/4+1/8+1/16+1/32+1/64+1/256 as description and demonstration)

- TB1C1H[15:8] is set as C0h(1/2+1/4), and it makes waveform of PWM duty cycle occur N+1 and N output, i.e. it generator waveform taking 4 output periods as a group--- 1 output is N+1 and the other 3 is N.
- TB1C1H[15:8] is set as A0h(1/2+1/8), and it makes waveform of PWM duty cycle occur N+1 and N output, i.e. it generator waveform taking 8 output periods as a group--- 2 output is N+1 and the other 6 is N.
- TB1C1H[15:8] is set as 90h(1/2+1/16), and it makes waveform of PWM duty cycle occur N+1 and N output, i.e. it generator waveform taking 16 output periods as a group--- 4 output is N+1 and the other 12 is N.
- TB1C1H[15:8] is set as 88h(1/2+1/32), and it makes waveform of PWM duty cycle occur N+1 and N output, i.e. it generator waveform taking 32 output periods as a group--- 8 output is N+1 and the other 24 is N.
- TB1C1H[15:8] is set as 84h(1/2+1/64), and it makes waveform of PWM duty cycle occur N+1 and N output, i.e. it generator waveform taking 64 output periods as a group--- 16 output is N+1 and the other 40 is N.
- TB1C1H[15:8] is set as 90h(1/2+1/128), and it makes waveform of PWM duty cycle occur N+1 and N output, i.e. it generator waveform taking 128 output periods as a group--- 32 output is N+1 and the other 96 is N.
- TB1C1H[15:8] is set as 90h(1/2+1/256), and it makes waveform of PWM duty cycle occur N+1 and N output, i.e. it generator waveform taking 256 output periods as a group---64 output is N+1 and the other 192 is N.

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- TB1C1H[15:8] is set as C0h(1/2+1/4+1/8), and it makes waveform of PWM duty cycle occur N+1 and N output, i.e. it generator waveform taking 8 output periods as a group--- 1 output is N+1 and the other 7 is N.
- TB1C1H[15:8] is set as C0h(1/2+1/4+1/8), and it makes waveform of PWM duty cycle occur N+1 and N output, i.e. it generator waveform taking 8 output periods as a group--- 1 output is N+1 and the other 7 is N.
- TB1C1H[15:8] is set as C0h(1/2+1/4+1/8+1/16), and it makes waveform of PWM duty cycle occur N+1 and N output, i.e. it generator waveform taking 16 output periods as a group--- 1 output is N+1 and the other 15 is N.
- TB1C1H[15:8] is set as C0h(1/2+1/4+1/8+1/16+1/32), and it makes waveform of PWM duty cycle occur N+1 and N output, i.e. it generator waveform taking 32 output periods as a group--- 1 output is N+1 and the other 31 is N.
- TB1C1H[15:8] is set as C0h(1/2+1/4+1/8+1/16+1/32+1/64), and it makes waveform of PWM duty cycle occur N+1 and N output, i.e. it generator waveform taking 64 output periods as a group--- 1 output is N+1 and the other 63 is N.
- TB1C1H[15:8] is set as C0h(1/2+1/4+1/8+1/16+1/32+1/64+1/128), and it makes waveform of PWM duty cycle occur N+1 and N output, i.e. it generator waveform taking 128 output periods as a group--- 1 output is N+1 and the other 127 is N.
- TB1C1H[15:8] is set as C0h(1/2+1/4+1/8+1/16+1/32+1/64+1/128+1/256), and it makes waveform of PWM duty cycle occur N+1 and N output, i.e. it generator waveform taking 256 output periods as a group--- 1 output is N+1 and the other 255 is N.

◆ Following Table 8 -2 and Figure 8-6 sections list 8+8-bit PWM waveform changing of TB1C1H[15:8] under different setting for user's reference.

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8+8bit PWM			TBN Overflow Times																	
Type	TB1C1H [15:8]	Logic Computation	0	1	2	3	4	5	6	7	8	9	10	~	127	128	~	252	253	254	255
Basic Waveform	80h	1/2	N	N+1	N	N+1	N	N+1	N	N+1	N	N+1	N	~	N+1	N	~	N	N+1	N	N+1
	40h	1/4	N	N	N+1	N	N	N	N+1	N	N	N	N+1	~	N	N	~	N	N	N+1	N
	20h	1/8	N	N	N	N	N+1	N	N	N	N	N	N	~	N	N	~	N+1	N	N	N
	10h	1/16	N	N	N	N	N	N	N	N	N+1	N	N	~	N	N	~	N	N	N	N
	08h	1/32	N	N	N	N	N	N	N	N	N	N	N	~	N	N	~	N	N	N	N
	04h	1/64	N	N	N	N	N	N	N	N	N	N	N	~	N	N	~	N	N	N	N
	02h	1/128	N	N	N	N	N	N	N	N	N	N	N	~	N	N	~	N	N	N	N
	01h	1/256	N	N	N	N	N	N	N	N	N	N	N	~	N	N+1	~	N	N	N	N
Logic Computation Superimposition Type	C0h	3/4	N	N+1	N+1	N+1	N	N+1	N+1	N+1	N	N+1	N+1	~	N+1	N	~	N	N+1	N+1	N+1
	A0h	5/8	N	N+1	N	N+1	N+1	N+1	N	N+1	N	N+1	N	~	N+1	N	~	N+1	N+1	N	N+1
	E0h	7/8	N	N+1	N+1	N+1	N+1	N+1	N+1	N+1	N	N+1	N	~	N+1	N	~	N+1	N+1	N+1	N+1
	F0h	15/16	N	N+1	N+1	N+1	N+1	N+1	N+1	N+1	N+1	N+1	N	~	N+1	N	~	N+1	N+1	N+1	N+1
	A1h	161/256	N	N+1	N	N+1	N+1	N+1	N	N+1	N	N+1	N	~	N+1	N+1	~	N+1	N+1	N	N+1
	F1h	241/256	N	N+1	N+1	N+1	N+1	N+1	N+1	N+1	N+1	N+1	N	~	N+1	N+1	~	N+1	N+1	N+1	N+1
	FFh	255/256	N	N+1	N+1	N+1	N+1	N+1	N+1	N+1	N+1	N+1	N+1	~	N+1	N+1	~	N+1	N+1	N+1	N+1

Table 8 -2 8+8-bit PWM Output Waveform and Using Schematic Table

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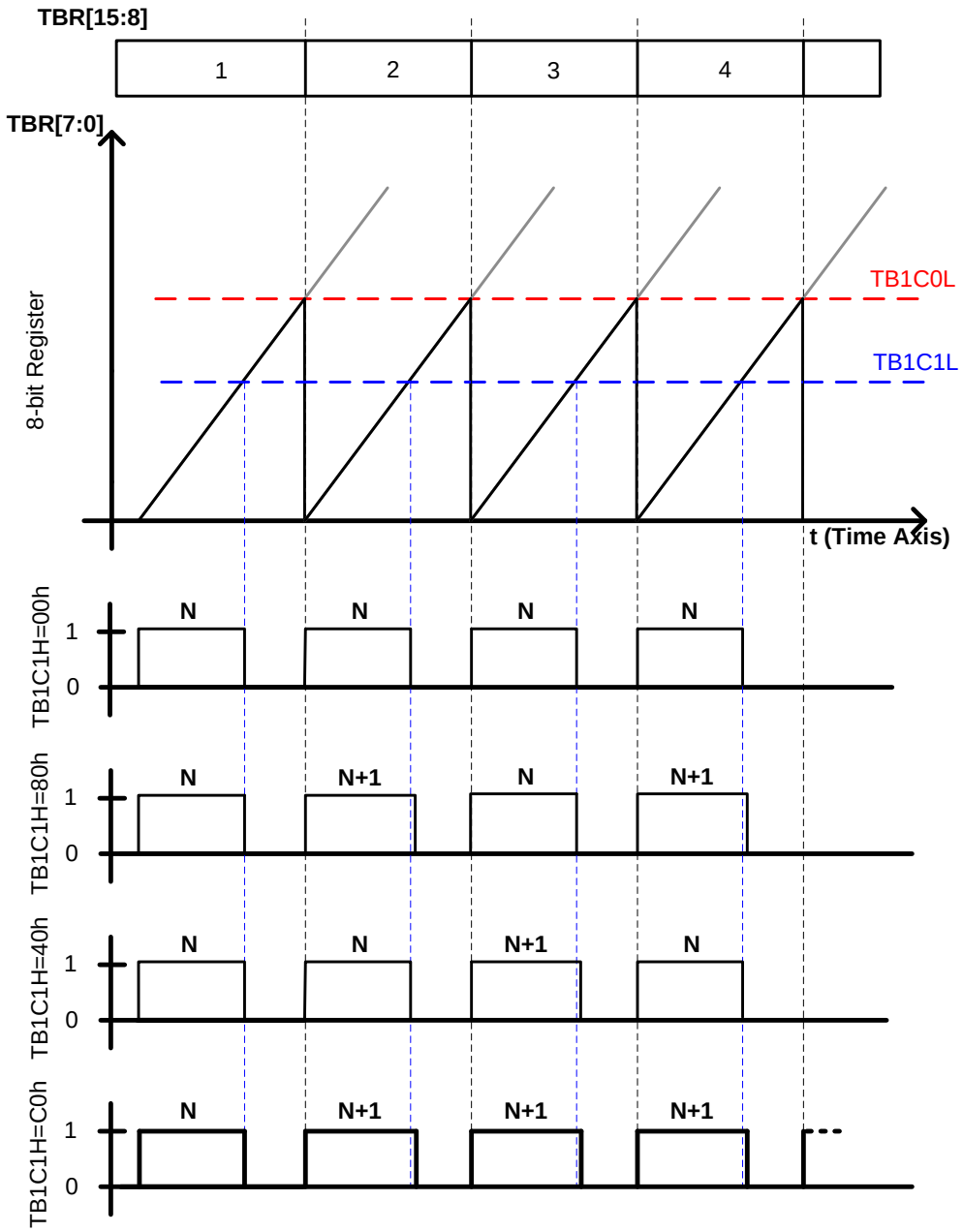

Figure 8-6 8+8-bit PWM Output Waveform Schematic Diagram

- 8+8-bit PWM Output Operation Instructions
  - Initialization Configuration (PWM Frequency and Duty Cycle Setting)
    - TMB source operating frequency is fixed at HAO Set DTMB[1:0] to determine TMB operation frequency.
    - TB1M[1:0] is set as <11>. Plan TMB1 as 8+8-bit count.
    - Trigger counting signal as Always Enable, i.e. cycle count.
    - Write data to TB1C0L[7:0] to determine the frequency of PWM.
    - Write data to TB1C1H[15:8] to determine the Duty Cycle of PWM.
    - Set ENTMB[0] as <1> to start timer.

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- Generator 8+8-BIT PWM Waveform
  - When TB1R[7:0] counting value is equal to TB1C0L[7:0], it makes the status of 8+8-Bit PWM be 0➔1.
  - When TB1R[7:0] recounting value is equal to TB1C1L[7:0], it makes the status of 8+8-Bit PWM be 1➔0.
    - ✓ Furthermore, it produces overflow event and makes TB1IF[0] set as <1> and zero and retake increment counting. At the moment, it will produce interrupt event service when GIE[0]、TB1IE[0] is set as <1>.
    - ✓ At the moment, all TB1C1H[7:0] set data is adjust 8+8-Bit PWM output as N+1 and N. As in Table 8-1, N＝TB1C1L[7:0].
- PWM Output Control
  - Set the pin output PWM waveform status as output status, and set ENPWM0[0] as <1>to start output as PWM function. Confirm whether the pin related setting is correct.
- When ENTMB[0] is set as <0>, it will close timer and PWM output.
- Calculation equation of 8+8-Bit PWM frequency Duty Cycle is:

$$\text{PWM Frequency} = \frac{\text{DTMB\_CK}}{\text{TB1C0L}[7:0]+1}$$

$$\text{PWM Duty Cycle} = \frac{(\text{TB1C1L}[7:0]+1)+\frac{\text{TB1C1H}[15:8]}{256}}{\text{TB1C0L}[7:0]+1}$$

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8.2. TMB1 Control Register List and Instructions :

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1											
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition											
Address	**File Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**A-RESET**	**R/W**
58H	TB1CN0	ENTMB	TB1M[1:0]		DTMB[1:0]		-	-	TMBCL	0000 0000	*,*,*,*,*,*,*,*
59H	TB1C0L	TimerB1 counter Condition Register0 [7:0]								xxxx xxxx	*,*,*,*,*,*,*,*
5AH	TB1C0H	TimerB1 counter Condition Register0 [15:8]								xxxx xxxx	*,*,*,*,*,*,*,*
5BH	TB1C1L	TimerB1 counter Condition Register1 [7:0]								xxxx xxxx	*,*,*,*,*,*,*,*
5CH	TB1C1H	TimerB1 counter Condition Register1 [15:8]								xxxx xxxx	*,*,*,*,*,*,*,*

Table 8-3 TMB1 Related Register

INTE0/INTF0 : Please refer to *Interrupt* Chapter

TB1CN0 : Timer-B Control Register

Bit	Name	Description
Bit7	ENTMB	Timer-B enable controller <1> Enable count <0> Disable Count ; Zero counters
Bit6~5	TB1M[1:0]	TMB Operation Mode Selector <00> 16bit counter mode.TMB_CLK/(TBC0H*256+TBC0L)發生週期性的中斷 <01> 16bit pulse generator mode. Pulse generation quantity (TB1C1H*256+TB1C1L) <10> Dual 8-bit PWM mode. PWMO0 Duty 為 TB1C1L/TB1C0L PWMO1 Duty 為 TB1C1H/TB1C0H <11> 8+8bit PWM mode. Output Duty is TB1C1L/TB1C0L+TB1C1H/256
Bit4~3	DTMB[1:0]	Timer-B operating frequency prescaler <00> TMB clock=HS(default) <01> TMB clock=HS/4 <10> TMB clock=HS/8 <11> TMB clock=HS/16
Bit0	TMBCL	TMB clear of counter <1> TMB clear of counter, When writing "1" clear TMBR and Pre-counter, automatically returns to "0" <0> TMB Counting

TB1C0H : TMB1 Count condition register TB1C0[15:8]

TB1C0L : TMB1 Count condition register TB1C0 [7:0]

TB1C1H : TMB1 Count condition register TB1C1[15:8]

TB1C1L : TMB1 Count condition register TB1C1 [7:0]

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9. Power System(PWR)

The power supply system includes a linear power supply(VDDA) and analog circuit common ground power supply ACM, which provides chip analog peripheral circuits can be properly used to drive an external circuit.

- ◆ VDDA Linear Regulator Power
  - 4-segment voltage adjustment design, Output Voltage 1.8V, 2.3V, 3V and 3.95V
  - Low temperature drift coefficient
- ◆ SDR(Sensor Driver) Linear regulated power supply
  - To Thermistor use a voltage 2.4V
  - Low temperature drift coefficient
- ◆ ACM Internal Analog Circuit Ground Power
  - Output Voltage 0.9V、1.2V、1.4V、2.4V
  - Low temperature drift coefficient

Abstract of PWR Register :

PWRCN0 ENBGR, ENSDR , INIS, TPSL, ENLVD

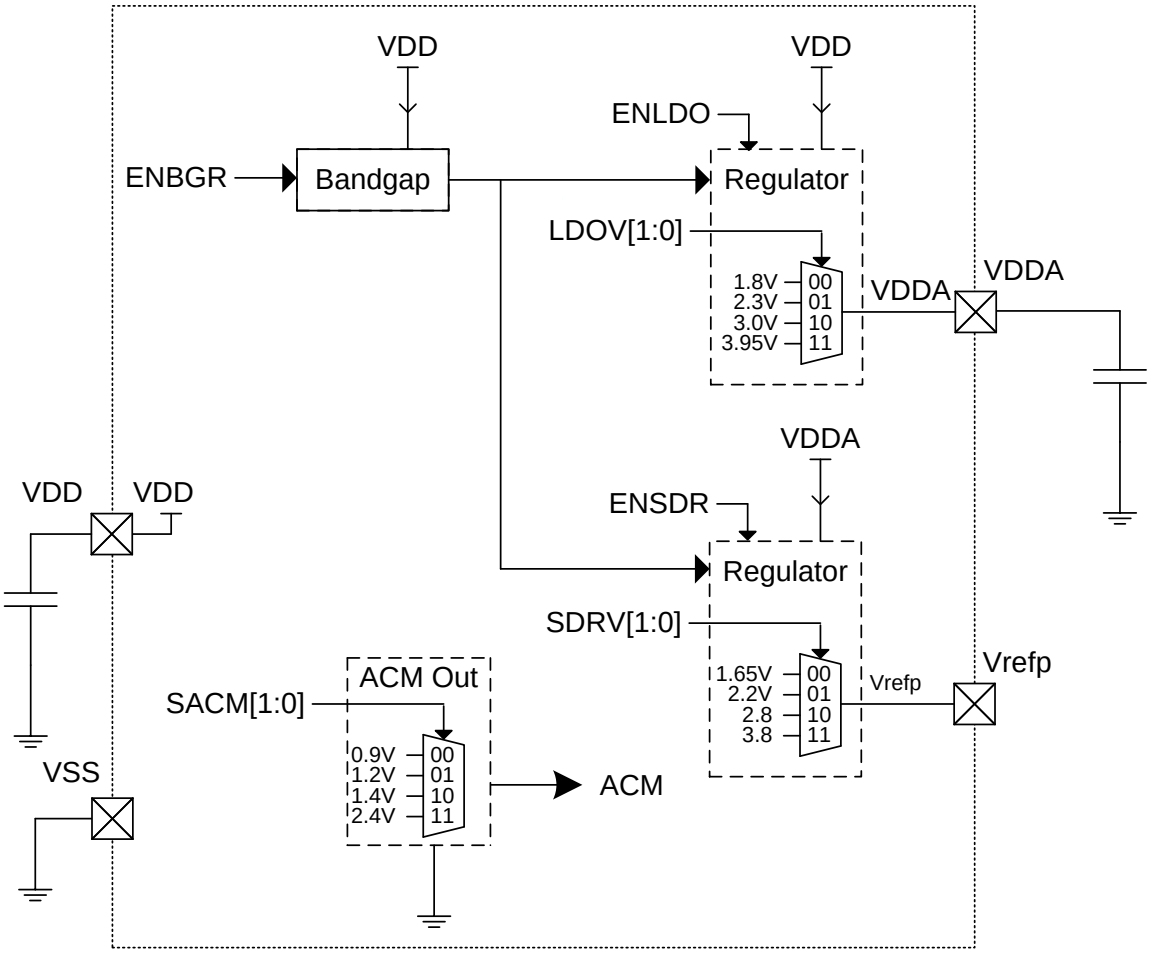

Figure 9-1 Power System Block Diagram

9.1. Bandgap Manual

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9.1.1. Bandgap Initial Configuration :

Bandgap addition to HS / LS OSC, all analog components are required to open it, IDLE / SLP mode must be closed.

9.2. VDDA Manual

9.2.1. VDDA Initial Configuration :

Regulators selector LDOV [1: 0] can be set VDDA pin output voltage 1.8V, 2.3V, 3V and 3.95V. Since VDDA is a linear regulated power supply, care must be taken when using the operating voltage VDD voltage value is lower than the set value of the output voltage VDDA and Bandgap is turned on in order to avoid unexpected circuit malfunction.

9.2.2. VDDA using external input :

VDDA can be designed by external input voltage, if users would like to provide alternative voltage sources, the voltage must input from VDDA pin. Using this method, VDDA must be closed, which means ENLDO[0] must be configured as 0. Moreover, this method may impact analog circuit performance, so it should be dealt with extra caution.

9.2.3. VDDA Initiation :

Configure ENLDO[0] as <1> to initiate VDDA regulator. Oppositely, if ENLDO[0] is configured as <0>, VDDA will be shut off. To start VDDA, ΣΔADC cannot in enabled status. It must wait after VDDA voltage is stabilized then to startΣΔADC. When external 1uF(10uF) regulated capacitor is connected, it requires 500uS(5mS) to stabilize.

9.3. Sensor Driver Manual

9.3.1. Sensor Driver Initial Configuration :

When the SDR(Sensor Driver) use, must pay attention to VDDA voltage is lower than the set value of the SDR and Bandgap output voltage is turned on in order to avoid unexpected circuit malfunction.

When you enable ENSDR[0] internally generated voltage V24 can provide 2.4V to Thermistor use

9.4. ACM Manual

9.4.1. ACM Initial Configuration :

When using the internal analog circuit common ground power supply ACM, you must first enable VDDA. ACM internally generated output voltage of 0.9V, 1.2V, 1.4V, 2.4V.

9.5. LVD Manual

9.5.1. LVD Initial Configuration :

ENLVD Setting <1> LVD will be enabled. LVD voltage selector LVDV [1: 0] can be set to a point of comparison LVD 1.7V, 2.3V, 2.95V, 3.95V.

When VDD is greater than the set voltage LVD, LVDO automatically to <1>, want to interrupt you need to set the LVD_BE <1> and with GIE opening to generate an interrupt.

When VDD is below LVD set voltage, LVDO will automatically <0>, you need to want to interrupt the LVDE set <1> and with GIE opening to generate an interrupt.

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9.6. Register Description-PWR

Address	File Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A-RESET	R/W
33H	PWRCN0	ENBGR	ENTPS	ENSDR	INIS	TPSL	ENLDO	ENLVD	ENADC	0000 0000	*,*,*,* *,*,*,*
34H	PWRCN1	ADHV	SDRV[1:0]		LVDS[1:0]		LDOV[1:0]		LVDO	0000. 0000	*,*,*,* *,*,*,*

Table 9-1 PWR Register

PWRCN0 : Power System Control Register 0

Bit	Name	Description
Bit7	ENBGR	Bandgap Enable Control <1> Enable <0> Disable
Bit6	ENTPS	Internal TPS Enable Control <1> Enable, Network to be set relative ADC <0> Disable
Bit5	ENSDR	SDR Enable Control <1> Enable <0> Disable
Bit4	INIS	**SI±** input signal short selector <1> Short <0> Not short
Bit3	TPSL	TPS output voltage reverse control <1> Reverse <0> Normal
Bit2	ENLDO	LDO(VDDA) Enable Control <1> Enable <0> Disable
Bit1	ENLVD	VDD Low Voltage Detection Enable Control <1> Enable <0> Disable
Bit0	ENADC	ADC Enable Control <1> Enable <0> Disable

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PWRCN1 : Power System Control Register 1

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>Bit7</td><td>ADHV</td><td>When an application on VDDA=VDD and greater than 3.6V, the need to set this bit, if you use ENLDO is not an issue.</td></tr>
<tr><td>Bit6~5</td><td>SDRV[1:0]</td><td>Sensor Driver(SDR) voltage selection control
<table>
<tr><th>SDRV[1:0]</th><th>Vrefp Output Voltage</th></tr>
<tr><td>00</td><td>1.65V</td></tr>
<tr><td>01</td><td>2.2V</td></tr>
<tr><td>10</td><td>2.8V</td></tr>
<tr><td>11</td><td>3.8V</td></tr>
</table></td></tr>
<tr><td>Bit4~3</td><td>LVDV[1:0]</td><td>LVD(Low Voltage Detection) voltage selection control
<table>
<tr><th>LVDV[1:0]</th><th>LVD Monitor Voltage</th></tr>
<tr><td>00</td><td>1.7V</td></tr>
<tr><td>01</td><td>2.3V</td></tr>
<tr><td>10</td><td>2.95V</td></tr>
<tr><td>11</td><td>3.95V</td></tr>
</table></td></tr>
<tr><td>Bit2~1</td><td>LDOV[1:0]</td><td>LDO(Low Dropout Regulator) voltage selection control
<table>
<tr><th>LDOV[1:0]</th><th>VDDA Output Voltage</th></tr>
<tr><td>00</td><td>1.8V</td></tr>
<tr><td>01</td><td>2.3V</td></tr>
<tr><td>10</td><td>3V</td></tr>
<tr><td>11</td><td>3.95V</td></tr>
</table></td></tr>
<tr><td>Bit0</td><td>LVDO</td><td>Low Voltage Detection Status
<1> VDD>LVD
<0> VDD<LVD</td></tr>
</table>

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10. Sigma Delta Analog-to-Digital Converter (ΣΔADC)

ΣΔADC is a high resolution over sampling sigma delta analog-to-digital converter that equips with multi-channel 20 bit output. ΣΔADC consists of four main categories, multi-functional input multiplexer, input buffer and pre-low noise programmable gain amplifier (PGA), Sigma Delta Modulator(ΣΔADC) and comb filter.

- Multi-Functional Input Multiplexer

  Can switch to diversified set of input channels, single IC can execute several measurements

  Input channel can conduct reserve and short, eliminating ADC zero point drift

  Built-in temperature sensor circuit voltage output

- ΣΔ Modulator

  Adjustable input voltage amplification: 1, 2, 4 and 8 amplifications

  Note : Voltage amplifier ratio x1 / x2 / x4 as reservations and recommend the use of amplifiers ratio x8.

  Selectable reference voltage amplification: 1 or 1/2

  3 bit direct current input bias configuration

- Comb Filter

  Can adjust OSR(Over Sampling Ratio)= 128~16384

  Can produce interrupt event

Abstract of ΣΔADC Register :

ADCR0[23:0]	ADCRH[7:0], ADCRM[7:0], ADCRL[7:4],
ADCR1[23:0]	ADCRH[3:0], ADCRM[7:0], ADCRL[7:0],
PWRCN0	ENBGR, ENTPS, ENSDR, INIS, TPSL, ENLDO, ENLVD, ENADC
ADCCN0	OSR[2:0], VREGN, ADGN[1:0]
ADCCN1	INH[2:0], INL[2:0], VRI[1:0]
ADCCN2	DCSET[2:0], OSM,ADRST

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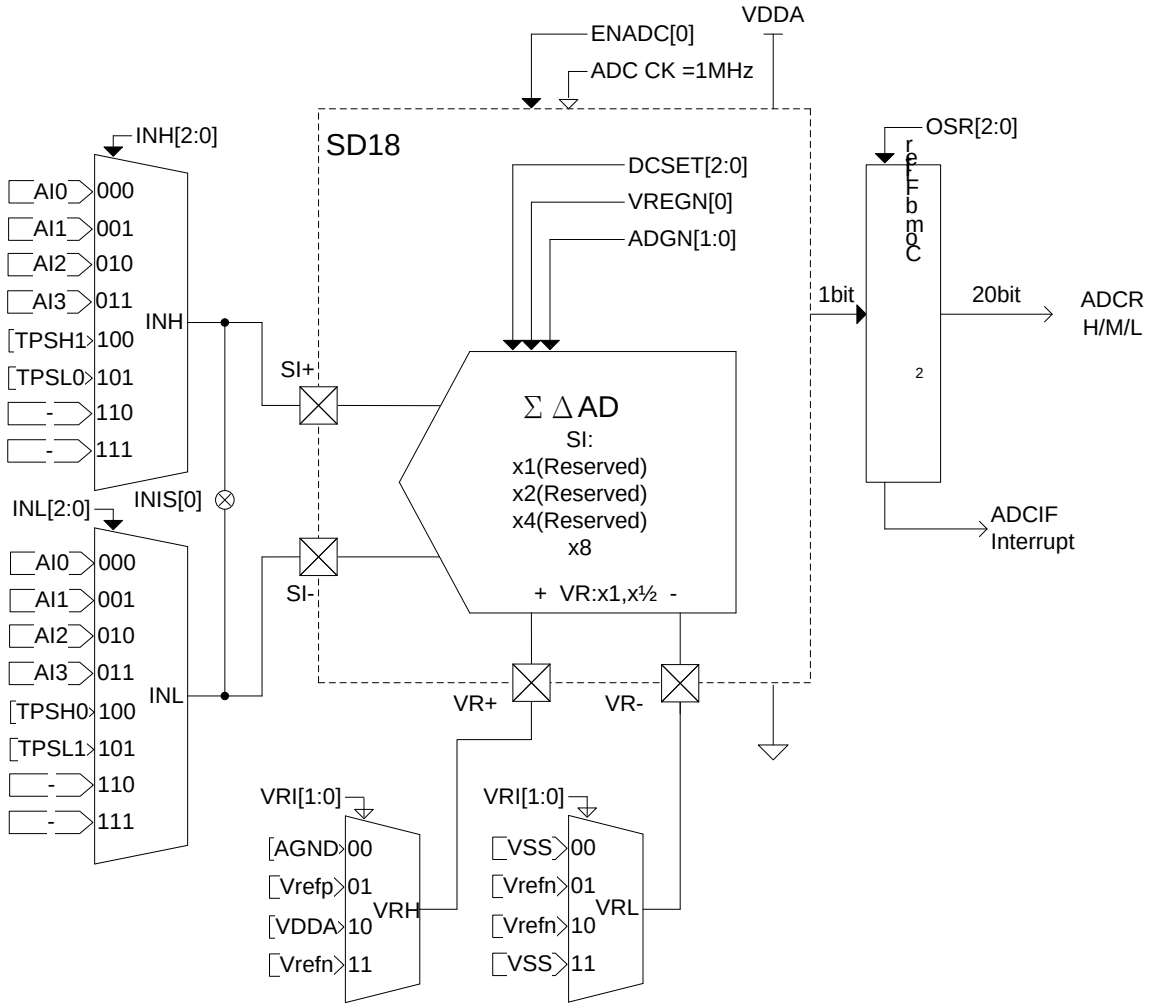

圖 10-1 ΣΔADC Block Diagram

10.1. ΣΔADC Manual

10.1.1. ΣΔADC Initial Configuration

10.1.1.1. Operating Frequency Configuration

ΣΔ ADC sampling frequency regardless of HAO independent of the choice, all will be in addition to the fixed frequency to 1MHz. It suggested the use 4MHz ΣΔADC can get better results.

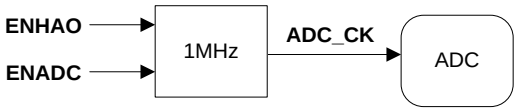

Figure 10-2 ΣΔADC Operating Frequency Block Diagram

10.1.1.2. Configuration of Multi-Functional Input Multiplexer

Multi-functional input multiplexer can generate two sets of differential input signals, unmeasured signal **SI+** and **SI-** and voltage reference **VR+** and **VR-**.

- **SI±** input signal selector INH[2:0] and INL[2:0] can send the input signals to **SI+** or **SI-** end via the following paths, such as Table 10-2(a)；
- **VR±** voltage signal selectors VRH[1:0] and VRL[1:0] can determine ΣΔADC reference voltage is sent to **VR+** or **VR-** end via the following paths, as in Table 10-2(b).
- When **SI±** input signal short circuit INIS[0] is set as <1>, it can make INH and INL channels short circuits. On the contrary, when it is set as <0>, INH and INL channels are not short circuits.

Configuration / Unmeasured Signal	INH[2:0],INL[2:0]							
	000	001	010	011	100	101	110	111
SI+	AI0	AI1	AI2	AI3	TPSH1	TPSL0	-	-
SI-	AI0	AI1	AI2	AI3	TPSH0	TPSL1	-	-

Table 10-2 (a) SI± Input Selector

Configuration / Input	VRI[1:0]			
	00	01	10	11
VRI+	AGND	Vrefp	VDDA	Vrefn
VRI-	VSS	Vrefn	Vrefn	VSS

Table 10-2 (b) VR± Input Selector

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10.1.1.3. ΣΔ Modulation Configuration

Σ Δ ADC is adopted second order ΣΔ modulator. The signal for testing and reference voltage can be taken magnification and bias adjustment via the following settings.

- When ΔVR± magnification adjuster VREGN[0] is set as <1>, it will take 1/2 magnification adjustment for reference voltage signal, and also change the ratio of input signals ΔSI± = (SI+ − SI-) and ΔVR± = (VR+ − VR-). When it is set as <0>, it takes 1 time of adjustment.
- Via the setting of magnification adjuster ADGN[1:0], input signal can be up to max 8 times of signal magnification, as in Table 10-3(a).
- Input signal SI± can adjust the input signal zero position to increase measurement range via DC input bias adjuster DCSET[4:0]. Bias method is adopted magnification value of weighted reference signal VR±, as in Table 10-3(b).
- When taking signal measuring, it shall note the matching problem of external input signal impedance and ADC. See Analog Channel Input Characteristics

Configuration / Input	ADGN[1:0]			
	00	01	10	11
AD Gain	x1	x2	x4	x8

Note : Voltage amplifier ratio x1 / x2 / x4 as reservations and recommend the use of amplifiers ratio x8.

Table 10-3 (a)ADGN[2:0] Amplification Configuration

Configuration / Input	DCSET[4:0]									
	00000	00001	00010	…	01111	10000	10001	10010	…	11111
SI±	+0	1/64 * Vref	2/64 * Vref	…	15/64 * Vref	+0	-1/64 * Vref	-2/64* Vref	…	-15/64 * Vref

unit : VR±

Table 10-3 (b) SI± Input Signal Weighted Voltage Reference Chart

After ΣΔ modulator takes pre-PGA and modulator magnification bias adjustment, the calculation equation of equivalent signal for testing ΔSI_I and equivalent reference voltage ΔVR_I are as the following respectively:

Equation 10-1

$$\Delta SI\_I = PGAGN \times ADGN \times \Delta SI \pm + (DCSET \times \Delta VR\pm)$$

Equation 10 -2

$$\Delta VR\_I = VREGN \times VR\pm$$

Notes: To ensure ΣΔ modulator output get higher resolution and degree of linearity, equivalent reference voltage ΔVR_I is suggested as 在ΔVR_I=0.8V~1.2V , and equivalent signal for testing ΔSI_I is operated at ΔSI_I=±0.9 x ΔVR_I.

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10.1.1.4. Comb Filter Configuration

ΣΔ Modulator output1-bit data is sent to second order Comb Filter, then it is covered into 20-bit value via Comb Filter and stored in ADCR[19:0] register. The update speed of ADCR[19:0] data is the output speed of ΣΔADC, and the calculation mode is the ratio of ΣΔADC sampling frequency to ΣΔADC output speed. ΣΔADC output speed frequency is also called OSR (Over Sampling Ratio).

Thus, ΣΔADC output rate is ADC_CK÷OSR. However, OSR value can be set by OSR[2:0] in order to generate different ΣΔADC output conversion frequency, as Table 10-3 (c).

Configuration / ADC_CK	OSR[2:0]							
	000	001	010	011	100	101	110	111
1M Hz	16384	8192	4096	2048	1024	512	256	128

Table 10-3 (c) ΣΔADC Over-Sampling Rate Configuration

ADCR[19:0] is constituted by ADCRH[3:0] , ADCRM[7:0] and ADCRL[7:0] where 20-bit Comb Filter outputted data is stored. Comb Filter data format is presented in Figure 10-3.

+FSR/-FSR : Optimum positive and negative measurement range

	Equivalent unmeasured signal	ADCR[19:0]	
		Hexadecimal	Binary
The output format is two complement	ΔVR_I	7FFFF	0111 1111-1111 1111-1111
	$\Delta VR\_I \times \frac{1}{2^{19}}$	00001	0000-0000-0000-0000-0001
	0	00000	0000 0000-0000 0000-0000
	$-\Delta VR\_I \times \frac{1}{2^{19}}$	FFFFF	1111 1111-1111 1111-1111
	$-\Delta VR\_I$	80000	1000 0000 0000 0000 0000

Table 10-4 ADCR[19:0] and Input Signal Correlation

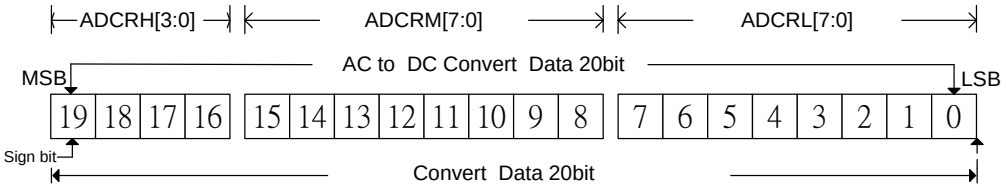

Figure 10-3 ADCR[19:0] Resolution Chart

10.1.2. Interrupt Service Configuration

After comb filter converted the value, it will be stroed in register, ADCR[19:0]. At this time, interrupt event signal will be generated and ADCIF[0] will be placed as <1>. Configuring ADCIE[0] and GIE[0] as <1> can cease interrupt event service .

10.1.3. ΣΔADC Initiation

Configuring ENADC[0] as <1> enables ΣΔADC to carry out analog to digital conversion. On the other hand, when ENADC[0] is set as <0>, ΣΔADC is disabled. VDDA supplies ΣΔADC power and uses V12 as the internal common mode reference voltage point. Thus, VDDA and V12 must be initiated first before starting ΣΔADC.

ΣΔADC operating voltage source comes from VDDA and the voltage of Aix input pin can not exceed VDDA voltage. When VDDA power turns off (neither from internal initiate nor external input), voltage exists in ΣΔADC input signal network SI± and voltage reference network VR± may bring about power leakge and may indirectly damage the chip and enlarge power consumption. Thus, before truning off VDDA power, ΣΔADC input signal network or voltage reference network must be properly selected. To avoid power leakage caused by external voltage, the network switch must be turend to internal V12 or VSS.

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10.2. Analog Channel Input Characteristics

ΣΔADC adopts switched capacitor circuit to process analog signals. When input buffer is not used, in order to acquire accurate sampling capacitor voltage value, the highest output impedance of input signal must be confined. Moreover, it will have impeditive interrelation between ΣΔADC sampling frequency and signal amplification.

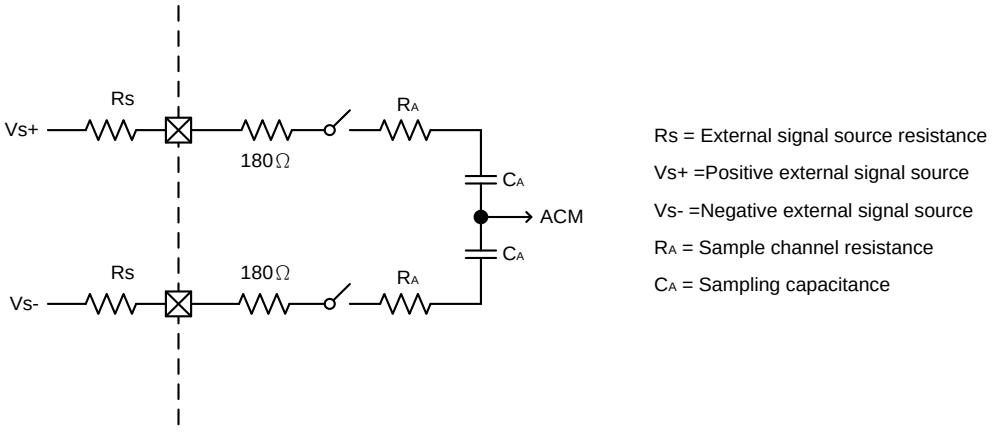

Figure 10-4 AIx Input Capatitor and Impedance Module

As Figure 10-4 illustrated, if input signal does not pass through buffer, further consideration of input signal impedance, Rs and ΣΔADC sampling frequency, ADC_CK and parasitical resistor R_A, capacitor C_A effect must also been taken into account.Related calculation is given by :

Equation 10-3

$$t_s > (R_s + R_A + 180\Omega) \times C_A \times [\ln(2^{ENOB} \times Gain) + 2]$$

t_s : ΣΔADCshortest sampling time

ENOB : Expected ΣΔADC effective bit

Gain : (ΣΔAD Gain)

Equation 10 -4

$$F_s = \frac{1}{2 \times t_s}$$

Fs : ΣΔADC shortest sampling frequency

ΣΔADC is composed by PGA and ΣΔAD, these two parts have separate R_A and C_A value in design. The shortest sampling time, t_s are calculated by direct and input signal matching consideration.

ΣΔAD Gain	C_A	R_A
x1	1.5pF	10KΩ
x2	3pF	10KΩ
x4	6pF	10KΩ
x8	12pF	5KΩ

Table 10-5(a) ΣΔADC Gaifn and R_A and C_A Relation

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VR Gain	C_A	R_A
x1/2	0.75pF	10KΩ
X1	1.5pF	10KΩ

Table 10-5(b) VR Gain and R_A and C_A Relation

ΣΔADC is mainly applied to low frequency signal measurement. Nevertheless, unmeasured signal includes much more high frequency noise in the real world. Based on signal sampling theory, any high frequency noise that exceeds sampling frequency will produce zero point drift and low frequency noise. Furthermore, it will cause measurement deviation.

Hence, it is suggested to add on 10nF~100nF filter capacitor in IC differential unmeasured signal and voltage reference end to strengthen measurement accuracy.

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10.3. Absolute Temperature Sensor (TPS)

Absolute temperature sensor is composed by diode (BJT). Its voltage signal to temperature change is a curve that passes through 0°K that equips with the following features.

- Temperature sensor in ambient temperature 0°K, its output voltage: $V_{TPS@0K}$ =0V.
- Through measurement method, ADC bias ($V_{ADC-OFFSET}$) and BJT asymmetry ($I_{S1} \neq I_{S2}$) can be offset automatically.
- Single point temperature calibration.

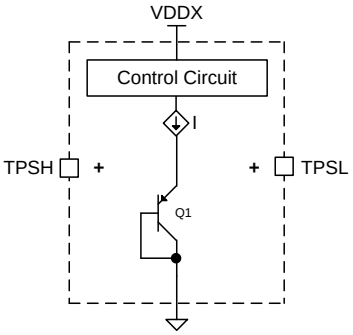

Figure 10-5 Block Diagram of Absolute Temperature Sensor Application

10.3.1. TPS Initial Configuration and Calculation

When ΣΔADC enabled, TPS function does not automatically enable, if necessary using the TPS function needs to ENTPS set to 1.

Configuring input signal selector, INH[2:0] and INL[2:0] as INH=[110]、INL=[111] to measure voltage signal, V_{TPS0}. Configuring INH=[111]、INL=[110] to measure voltage signal, V_{TPS1}. Recommend removal of offset when doing chopper,, TPSLCN control bit must be different, such as when measuring V_{TPS0} TPSLCN = 1, when the measurement V_{TPS1} TPSLCN = 0.

Under the same temperature TA(°C), after ΣΔADC measured the value of V_{TPS0} and V_{TPS1}, add the value together and get the mean, TPS corresponding voltage value, $V_{TPS@TA}$ can be acquired.

The response of TPS output voltage V_{TPS} to temperature change is a linear curve, thus, the gain, G_{TPS}(or called as slope) is derived.

Equation 10 -5 TPS Gain

$$G_{TPS} = \frac{V_{TPS@T_A} - V_{TPS@0K}}{(273.15 + T_{offset} + T_A) - (0)} = \frac{V_{TPS@T_A}}{289.15 + T_A}$$

10.3.2. TPS Example Description

(1) Set INH=[110]、INL=[111]、TPSLCN=1，ADC measured a digital code,V_{TPS0}Code。

(2) Set INH=[111]、INL=[110]、TPSLCN=0，ADC measured a digital code,V_{TPS1}Code。

(3) Calculate V_{TPS}Code=(V_{TPS0}Code + V_{TPS1}Code)/2, this move can erase Temperature Sensor Offset.

(4) Supposed that one point was calculated at 25℃, and then V_{TPS}Code@25℃ can be obtained. Due to the fact that there is a level shift, an offset will be added. Temperature curve slope, G can be gained as follows:

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$$G = \frac{V_{TPS}Code@25^{o}C}{25 + 273.15 + T_{OS}}$$, T_{OS} is offset, about 32K。

(5) Supposed that the temperature-to-be-measured is T_X℃, then we can gained:

$$T_X = \frac{V_{TPS}Code@T_X{}^{o}C}{G} - \left[273.15 + T_{Offset}\right] \quad {}^{o}C$$

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10.4. Register Description-ΣΔADC

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1											
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition											
Address	**File Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**A-RESET**	**R/W**
23H	INTE0	GIE	ADCIE	TMBIE	TMAIE	LVD_BE	LVDE	E1IE	E0IE	000. 0000	*,*,*,*,*,*,*,*
26H	INTF0	-	ADCIF							000. 0000	w0
2DH	ADCR0H	ADC[19:12]								xxxx xxxx	*,*,*,*,*,*,*,*
2EH	ADCR0M	ADC[11:4]								xxxx xxxx	*,*,*,*,*,*,*,*
2FH	ADCR0L	ADC[3:0]				0	0	0	0	xxxx xxxx	*,*,*,*,*,*,*,*
30H	ADCR1H	ADC[19]	ADC[19]	ADC[19]	ADC[19]	ADC[19]	ADC[18]	ADC[17]	ADC[16]	xxxx xxxx	*,*,*,*,*,*,*,*
31H	ADCR1M	ADC[15:8]								xxxx xxxx	*,*,*,*,*,*,*,*
32H	ADCR1L	ADC[7:0]								xxxx xxxx	*,*,*,*,*,*,*,*
33H	PWRCN0	ENBGR	ENTPS	ENSDR	INIS	TPSLCN	ENLDO	ENLVD	ENADC	000. 0000	*,*,*,*,*,*,*,*
34H	PWRCN1	ADHV	SDRV[1:0]		LVDV[1:0]		LDOV[1:0]		LVDO	000. 0000	*,*,*,*,*,*,*,*
35H	ADCCN0	OSR[2:0]			VREGN	ADG[1:0]		SACM[1:0]		000. 0000	*,*,*,*,*,*,*,*
36H	ADCCN1	INL[2:0]			INH[2:0]			VRI[1:0]		000. 0000	*,*,*,*,*,*,*,*
37H	ADCCN2	DCSET[2:0]			TCR[1:0]				ADRST	000. 0000	*,*,*,*,*,*,*,*

Table 10-6 ΣΔADC Register

INTE0/INTF0 : Please refer to *Interrupt* Chapter

PWRCN0 : Power System Control Register0

Bit	Name	Description
Bit7	ENBGR	Bandgap Enable Control <1> Enable <0> Disable
Bit6	ENTPS	Internal TPS Enable Control <1> Enable, Network to be set relative ADC <0> Disable
Bit4	INIS	**SI±** input signal short selector <1> Short <0> Not short
Bit3	TPSL	TPS Output Voltage Reverse Control <1> Reverse <0> Normal
Bit0	ENADC	ADC Enable Control <1> Enable <0> Disable

PWRCN1：Power System Control Register 1

Bit	Name	Description
Bit7	ADHV	When an application on VDDA=VDD and greater than 3.6V, the need to set this bit, if you use ENLDO is not an issue.

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ADCCN0 : ΣΔADC Control Register 0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>Bit7~5</td><td>OSR[2:0]</td><td>ADC Over-sampling rate frequency eliminator
<111> OSR=128
<110> OSR=256
<101> OSR=512
<100> OSR=1024
<011> OSR=2048
<010> OSR=4096
<001> OSR=8192
<000> OSR=16384</td></tr>
<tr><td>Bit4</td><td>VRGN</td><td>ADC Reference Gain Setting
<0> x1
<1> x1/2</td></tr>
<tr><td>Bit3~2</td><td>ADGN[1:0]</td><td>ADC Input Gain Setting
<table>
<tr><th>ADGN[1:0]</th><th>ADC Input Gain</th></tr>
<tr><td>00</td><td>X1(Reserved)</td></tr>
<tr><td>01</td><td>X2(Reserved)</td></tr>
<tr><td>10</td><td>X4(Reserved)</td></tr>
<tr><td>11</td><td>X8</td></tr>
</table></td></tr>
<tr><td>Bit1~0</td><td>SACM[1:0]</td><td>ADC Analog Ground Voltage Setting
<table>
<tr><th>SACM[1:0]</th><th>Analog Ground Voltage</th></tr>
<tr><td>00</td><td>0.9V (when ADC supply voltage is 2.4-1.8V)</td></tr>
<tr><td>01</td><td>1.2V (when ADC supply voltage is 2.8-2.3V)</td></tr>
<tr><td>10</td><td>1.4V (when ADC supply voltage is 3.8-2.6V)</td></tr>
<tr><td>11</td><td>2.4V (when ADC supply voltage is 5.5-3.8V)</td></tr>
</table></td></tr>
</table>

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ADCCN1 : ΣΔADC Control Register 1

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>Bit7～5</td><td>INL[2:0]</td><td>ADC Negative Input Signal Selector
<table>
<tr><th>INL[2:0]</th><th>ADC- INL</th></tr>
<tr><td>000</td><td>AI0</td></tr>
<tr><td>001</td><td>AI1</td></tr>
<tr><td>010</td><td>AI2</td></tr>
<tr><td>011</td><td>AI3</td></tr>
<tr><td>100</td><td>TPSH0</td></tr>
<tr><td>101</td><td>TPSL1</td></tr>
<tr><td>110</td><td>Floating</td></tr>
<tr><td>111</td><td>Floating</td></tr>
</table></td></tr>
<tr><td>Bit4~2</td><td>INH[2:0]</td><td>ADC Positive Input Signal Selector
<table>
<tr><th>INH[2:0]</th><th>ADC-INH</th></tr>
<tr><td>000</td><td>AI0</td></tr>
<tr><td>001</td><td>AI1</td></tr>
<tr><td>010</td><td>AI2</td></tr>
<tr><td>011</td><td>AI3</td></tr>
<tr><td>100</td><td>TPSH1</td></tr>
<tr><td>101</td><td>TPSL0</td></tr>
<tr><td>110</td><td>Floating</td></tr>
<tr><td>111</td><td>Floating</td></tr>
</table></td></tr>
<tr><td>Bit1~0</td><td>VRI[1:0]</td><td>ADC Reference Voltage Input Selection
<table>
<tr><th>VRI[1:0]</th><th>VRI+</th><th>VRI-</th></tr>
<tr><td>00</td><td>AGND</td><td>VSS</td></tr>
<tr><td>01</td><td>Vrefp</td><td>Vrefn</td></tr>
<tr><td>10</td><td>VDDA</td><td>Vrefn</td></tr>
<tr><td>11</td><td>Vrefn</td><td>VSS</td></tr>
</table></td></tr>
</table>

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ADCCN2 : ΣΔADC Control Register 2

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>Bit7~5</td><td>DCSET[2:0]</td><td>SI± Bias Adjuster
<table>
<tr><th>DCSET[2:0]</th><th>ADC DC Offset</th></tr>
<tr><td>000</td><td>offset = 0</td></tr>
<tr><td>001</td><td>1/8 * Vref</td></tr>
<tr><td>010</td><td>2/8 * Vref</td></tr>
<tr><td>011</td><td>3/8 * Vref</td></tr>
<tr><td>100</td><td>offset = 0</td></tr>
<tr><td>101</td><td>-1/8 * Vref</td></tr>
<tr><td>110</td><td>-2/8 * Vref</td></tr>
<tr><td>111</td><td>-3/8 * Vref</td></tr>
</table></td></tr>
<tr><td>Bit4～3</td><td>TCR[1:0]</td><td>Set the input resistance value between Vrefn and VSS.
<11> R = 7.5K ohm
<10> R = 5K ohm
<01> R = 2.5K ohm
<00> R = 0</td></tr>
<tr><td>Bit0</td><td>ADRST</td><td>ΣΔADC and Comb Filter Reset Controller
<1> Reset; writing motion occurs.
<0> Not reset</td></tr>
</table>

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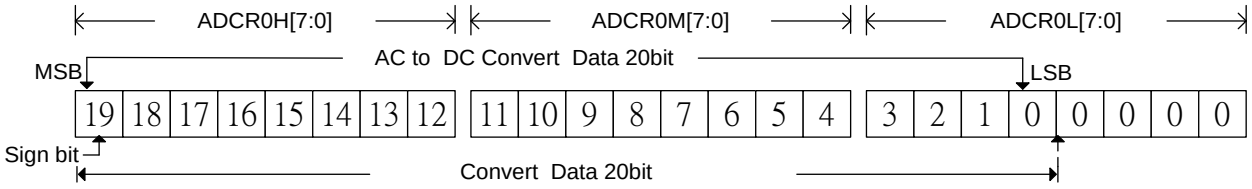
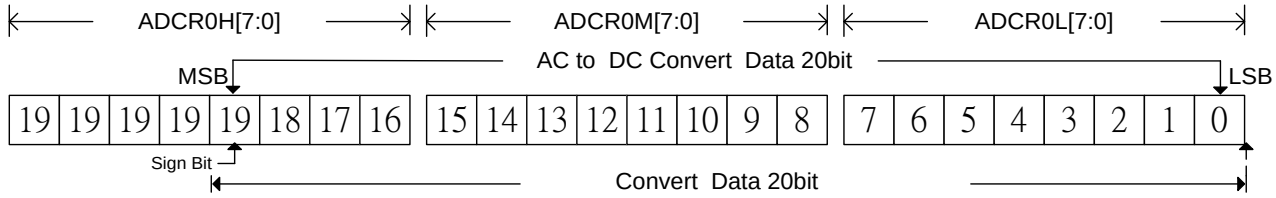
ADCR0H~ADCR0L : ADC Data Register 0(left-justified)

Address	Name	Description
2DH	ADCR0H	ADCR0H[7:0] represents ADC Data Bit19~Bit12
2EH	ADCR0M	ADCR0M[7:0] represents ADC Data Bit11~Bit4
2FH	ADCR0L	ADCR0L[7:4] represents ADC Data Bit3~Bit0, Bit3 ~ Bit0 represents ADC Data Bit0



ADCR1H~ADCR1L : ADC Data Register 1(right-justified)

Address	Name	Description
30H	ADCR1H	ADCR1H[3:0] represents ADC Data Bit19~Bit16, Bit7 ~ Bit4 Sign Extend ADC Data Bit19
31H	ADCR1M	ADCR1M[7:0] represents ADC Data Bit15~Bit8
32H	ADCR1L	ADCR1L[7:0] represents ADC Data Bit7~Bit0



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11. Hardware Multiplier

HY14E10x built-in 16bit * 16 bit signed hardware multiplier, the result is the number of a 32bit signal output, especially because there is no start and end of the flag, for an 16 CPU Clock (time four instructions).

The 16bit multiplier and multiplicand are written BH_MO3, BL_MO2, AH_MO1 register, automatically calculate after the last write AL_MO0 scratchpad. After 16 CPU Clock, the results back in the same address AL_MO0, AH_MO1, BL_MO2 and BH_MO3 register, the multiplier input and output settings exist.

11.1. Register Description-Hardware Multiplier

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1											
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition											
Address	**File Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**A-RESET**	**R/W**
39H	AL_MO0	LSB for multiplexer input A / LSB for multiplexer output								xxxx xxxx	*,*,*,*,*,*,*,*
3AH	AH_MO1	MSB for multiplexer input A / 15-8 bit multiplexer output								xxxx xxxx	*,*,*,*,*,*,*,*
3BH	BL_MO2	LSB for multiplexer input B / 23-16 bit multiplexer output								xxxx xxxx	*,*,*,*,*,*,*,*
3CH	BH_MO3	MSB for multiplexer input B / MSB for multiplexer output								xxxx xxxx	*,*,*,*,*,*,*,*

Table 11-1 Hardware Multiplier Register

AL_MO0 : LSB(Bit7~0) for Multiplier input A / LSB(Bit7~0) for Multiplier output

AH_MO1 : MSB(Bit15~8) for Multiplier input A / Byte(Bit15~8) for Multiplier output

BL_MO2 : LSB(Bit7~0) for Multiplier input B / Byte(Bit23~16) for Multiplier output

BH_MO3 : MSB(Bit15~8) for Multiplier input A / MSB(Bit31~24) for Multiplier output

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12. Inter-Integrated Circuit Serial interface (I²C)

HY14E10x the I²C serial communication interface is slave mode of operation.

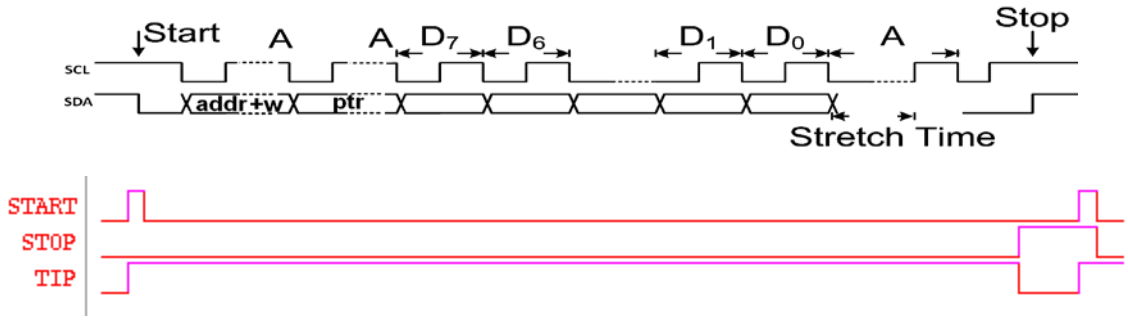
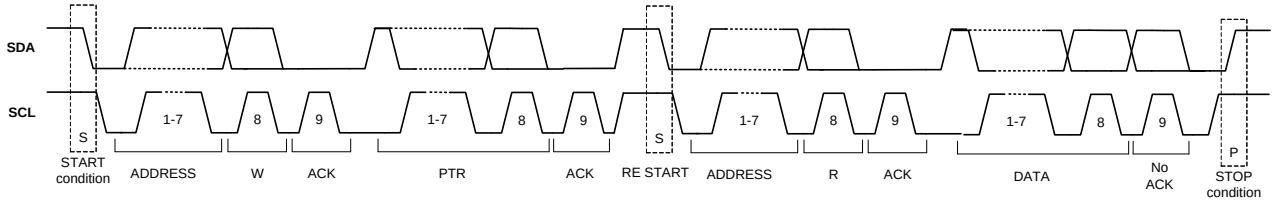


Figure 12-1 I²C Bus timing diagram

◆ I²C Operation Instructions

Slave address is 7bit thus receives little different with the general I²C transmission. Transmit data or information is not received from the address decision, but PTR.

■ Transmission



- When the Master sends Start, if the address and set the same, the hard experience of automatic replies ACK.
- After Master confirmation ACK, the transmission of information sent from the machine PTR (0x00 ~ 0x07), each PTR corresponding to different I²C Data Output Buffer. (Ex: Master sent PTR is 0x01, the value within the I²C Data Output Buffer 1 will receive correspondence)
- After receiving the Slave Master send data, after the response ACK, if not send Stop. Slave will continue to send out the same until Master Data sent Stop so far.
- To get a different I²C Data Output Buffer data to be re-sent Start, Address, PTR, Stop.
- Such as I²C Data Output Buffer data left to be read, to be updated in the I²C Data Output Buffer information from TIP [0] to know whether the information has been completed read. (Data for the 8bit)
- Such as I²C Data Output Buffer data after they are read, shall update the information in the I²C Data Output Buffer can be LSB_SEL[7:0] corresponding to the address is on, this time corresponding I²C Data Output Buffer lowest bit data is read Analyzing bit, I²C data Output Buffer regardless of what value is written, the lowest bit is automatically 1, when after the data is read, the lowest bit is automatically to 0. (Data for the 7bit). When new data is written I²C Data Output Buffer again, the lowest bit to 1 again automatically.
- For continuous reading I²C Data Output Buffer 0,1,2,3 ..... information can be made within a special PTR. When PTR highest bit is 1, continuous reading mode. (EX: PTR is 82, read

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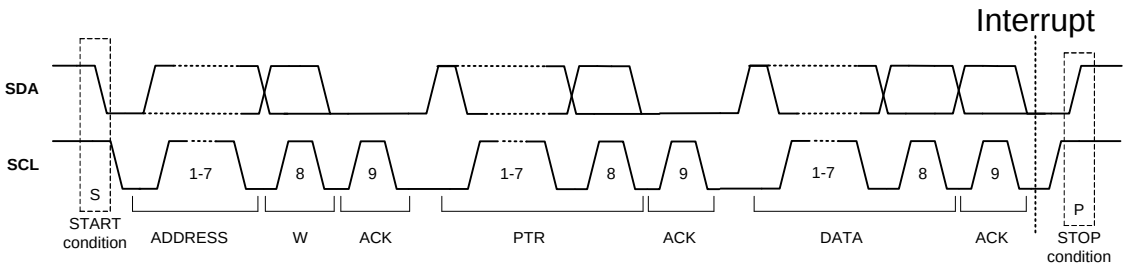
from the I2C Data Output Buffer 2 sequentially beginning to 3,4, ... continuous information.) but as sequential read over I2C Data Output Buffer after 7, Master still not sent back the Stop information received is not returned to I2C data Output Buffer 0, but unknow value.

- Receive



- When the Master sends Start, if the address and set the same, the hard experience of automatic replies ACK.
- After Master confirmation ACK, the transmission of information sent to Slave PTR (0x08 ~ 0x12), each PTR corresponding to different I^2C Data Input Buffer. (Ex: Master sent PTR is 0x08, Data to 0xFF and may, upon STOP in I^2C Data Intput Buffer 0 can be read to 0xFF)
- When turned on, the corresponding interrupt when the reception is completed Master the outgoing data that will interrupt.

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12.1. Register Description- I²C Serial communication interface

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1											
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition											
Address	**File Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**A-RESET**	**R/W**
23H	INTE0	GIE								000. 0000	*,*,*,*,*,*,*,*
24H	INTE1	I2CW7IE	I2CW6IE	I2CW5IE	I2CW4IE	I2CW3IE	I2CW2IE	I2CW1IE	I2CW0IE	000. 0000	*,*,*,*,*,*,*,*
25H	INTE2	-	-	-	-	-	I2CW10IE	I2CW9IE	I2CW8IE	000. 0000	*,*,*,*,*,*,*,*
27H	INTF1	I2CW7IF	I2CW6IF	I2CW5IF	I2CW4IF	I2CW3IF	I2CW2IF	I2CW1IF	I2CW0IF	000. 0000	w0
28H	INTF2	-	-	-	-	-	I2CW10IF	I2CW9IF	I2CW8IF	000. 0000	w0
41H	LSB_SEL	SEL_FLAG[7:0]								0000 0000	********
42H	I2C_CMD	TIP		SP	0	0	0	0	EN_SCLO	0000 0000	RRRRRRRW
43H	I2C_O0	I2C Data Output Buffer 0								xxxx xxxx	w
44H	I2C_O1	I2C Data Output Buffer 1								xxxx xxxx	w
45H	I2C_O2	I2C Data Output Buffer 2								xxxx xxxx	w
46H	I2C_O3	I2C Data Output Buffer 3								xxxx xxxx	w
47H	I2C_O4	I2C Data Output Buffer 4								xxxx xxxx	w
48H	I2C_O5	I2C Data Output Buffer 5								xxxx xxxx	w
49H	I2C_O6	I2C Data Output Buffer 6								xxxx xxxx	w
4AH	I2C_O7	I2C Data Output Buffer 7								xxxx xxxx	w
4BH	I2C_I0	I2C Data Intput Buffer 0								xxxx xxxx	r
4CH	I2C_I1	I2C Data Intput Buffer 1								xxxx xxxx	r
4DH	I2C_I2	I2C Data Intput Buffer 2								xxxx xxxx	r
4EH	I2C_I3	I2C Data Intput Buffer 3								xxxx xxxx	r
4FH	I2C_I4	I2C Data Intput Buffer 4								xxxx xxxx	r
50H	I2C_I5	I2C Data Intput Buffer 5								xxxx xxxx	r
51H	I2C_I6	I2C Data Intput Buffer 6								xxxx xxxx	r
52H	I2C_I7	I2C Data Intput Buffer 7								xxxx xxxx	r
53H	I2C_I8	I2C Data Intput Buffer 8								xxxx xxxx	r
54H	I2C_I9	I2C Data Intput Buffer 9								xxxx xxxx	r
55H	I2C_I10	I2C Data Intput Buffer 10								xxxx xxxx	r

Table 12-1 I²C Serial communication interface Register

INTE0/INTF0 : Please refer to *Interrupt* Chapter

LSB_SEL : I²C Status register

LSB_SEL Bit0~7 to map I²C output buffer0~7. When LSB_SEL this bit is set to 1, the mapped data transfer I²C output buffer will only bit7 ~ 1 valid. Data is updated LSB Flag is set to 1, the read data has been set to 0.

Example: LSB_SEL [7: 0] is set to 0x01, When I²C output buffer 0 write 0x0A, hard experience automatically LSB is set to 1; when that is the first time through the Master with PTR = 0x00 Slave to information, Slave will return 0x0B, and automatically I²C output buffer LSB set to 0 is 0; that is, if not re-do on the I²C output buffer 0 write operation, Master through PTR = 0x00 to the data will be as 0x0A.

It can be determined whether to go through the LSB value within the I²C output buffer has been updated.

Bit	Name	Description
Bit7	SEL_FLAGH[7]	<1> I²C output buffer 7 is 7bit applications, LSB for the Flag <0> I²C output buffer 7 is 8bit applications, LSB for the Data
Bit6	SEL_FLAGH[6]	<1> I²C output buffer 7 is 7bit applications, LSB for the Flag <0> I²C output buffer 7 is 8bit applications, LSB for the Data

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Bit	Name	Description
Bit5	SEL_FLAGH[5]	<1> I²C output buffer 7 is 7bit applications, LSB for the Flag <0> I²C output buffer 7 is 8bit applications, LSB for the Data
Bit4	SEL_FLAGH[4]	<1> I²C output buffer 7 is 7bit applications, LSB for the Flag <0> I²C output buffer 7 is 8bit applications, LSB for the Data
Bit3	SEL_FLAGH[3]	<1> I²C output buffer 7 is 7bit applications, LSB for the Flag <0> I²C output buffer 7 is 8bit applications, LSB for the Data
Bit2	SEL_FLAGH[2]	<1> I²C output buffer 7 is 7bit applications, LSB for the Flag <0> I²C output buffer 7 is 8bit applications, LSB for the Data
Bit1	SEL_FLAGH[1]	<1> I²C output buffer 7 is 7bit applications, LSB for the Flag <0> I²C output buffer 7 is 8bit applications, LSB for the Data
Bit0	SEL_FLAGH[0]	<1> I²C output buffer 7 is 7bit applications, LSB for the Flag <0> I²C output buffer 7 is 8bit applications, LSB for the Data

I2C_CMD :

Bit	Name	Description
Bit7	TIP	I²C Transfer in Process.
Bit5	SP	I²C STOP flag
Bit0	EN_SCLO	Enable auto SCL stretch time. I²C protocol does not specify the maximum time, but the CPU must clear the bit end of the work, I²C communication to work properly. This feature is mainly used when HY14E10x Master for reading, walking its first reading when Master know the desire to continue reading the second document data, but HY14E10x not yet ready, the first EN_SCLO set to <1> enable SCL to Low , to be prepared after completion of the second tranche of the information EN_SCLO set to <0>, Master data can be guaranteed to catch the second document data.

I2C_O0~I2C_O7 : I²C Slave transmission data buffer

I²C slave transmit buffer a total of 8 bytes, each occupying a PTR(PTR$_{7\text{-}0}$ = 0x00 ~ 0x01), can be used with LSB_SEL set I²C master data received from each of the LSB is data or update flag.

I2C_I0~I2C_I10 : I²C Slave receive data buffer

I²C Slave Receive buffer a total of 11 bytes, each occupying a PTR (PTR$_{7\text{-}0}$ = 0x08 ~ 0x12), each I²C master writes PTR7-0 = 0x08 ~ 0x12 (I2C_I0 ~ I2C_I10) when there will be relative I2C_INTFn, CPU can be set to allow for relative INTE interrupt.

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13. Information block

System Information Block has 111 bytes EEPROM using a custom tile. System Information Block can only be changed through the burn unit. Use the custom required by EEPROM look-up table reads / writes. Note: Before turning lookup functions, the first CPU to 2MHz switching frequency to ensure the proper functioning of EEPROM.

- Custom EEPROM Operating Instructions
  - Write Data
    - When the CPU clock is changed to the first HAO 2MHz frequency.
    - EN_TBL[0] is set as <1> and PGM[0] is set as <0>
    - Setting write data address TBLPTR [7: 0], TBLPTR [3: 0]. (EEPROM maximum address is 77H, so make sure TBLPTRH to <0000> when writing EEPROM)
    - The indicators point to burn here TBLPTR [7: 0], TBLPTR [3: 0]. (EEPROM maximum address is 77H, so make sure TBLPTRH to <0000> is burned into EEPROM.
    - Writes a value to be written to TBLDL[7: 0].
    - The TBLW or TBLW+ set to <1> write immediately.
    - After writing a NOP instruction to be added to ensure that written correctly.
  - Read Data
    - When the CPU clock is changed to the first HAO 2MHz frequency.
    - EN_TBL[0] is set as <1> and PGM[0] is set as <0>
    - Setting write data address TBLPTR [7: 0], TBLPTR [3: 0]. (EEPROM maximum address is 77H, so make sure TBLPTRH to <0000> read EEPROM)
    - The TBLR or TBLR+ set to <1> read immediately.
    - After reading a NOP instruction to be added to ensure that read correctly.
    - Read data will be placed in TBDL [7: 0].

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13.1. System Information Block Description

Address	File Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
77H		User Defined EEPROM							
…		…							
09H		User Defined EEPROM							
08H~00H	Rsv.	Reserved.							

Table 13-1 System Information Block configuration diagram

13.2. Use lookup function to read program memory

- Use lookup function to read program memory instruction
  - EN_TBL[0] and PGM[0] is set as <1>
  - Lookup function can only read one byte, Program memory address of a unit of a word. Therefore read Program memory, LSB for the selection or read High byte Low byte. When the LSB to read High byte 1; when LSB read Low byte is 0.
    Ex: Expected to read the address 7A0H High byte, TBLPTRL write 41H，TBLPTRH write 0FH
  - The TBLR or TBLR+ set to <1> read immediately. (Be sure to refer to the following example operational flow)
  - Read data will be placed in TBDL [7: 0].

Lookup process usage examples:

```
Expected to read the address 7A0H    High byte
MVL     0FH                 ;Set table look-up address
MVF     HiADD,F,A
MVL     40h
MVF     LoADD,F,A

INF     LoADD,F,A           ;Select the Word of High byte
MVF     LoADD,W,A
MVF     TBLPTRL,F,A
MVL     10H                 ;Table Read
IORF    HiADD,W,A
MVF     TBLPTRH,F,A         ;Give instruction to read table and store the
                             data to register, TBDL

ORG     7A0h
DW      2345H
```

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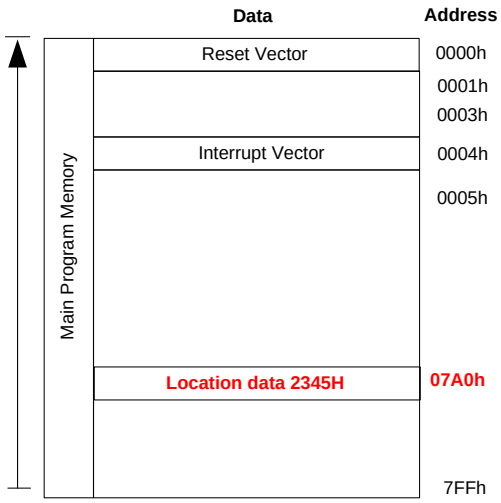
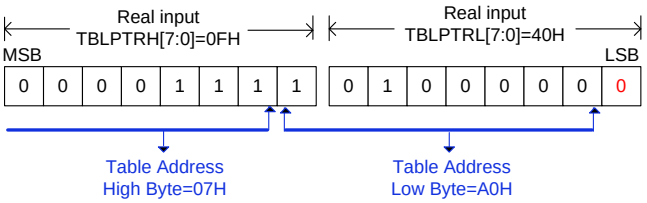
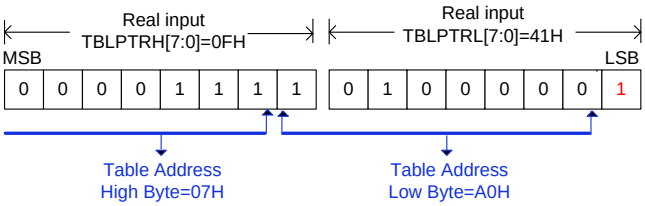


Program Memory Size Table
2KW : PC[10:0]

First 07A0h do shift left and LSB is set to 0, on behalf of program memory addresses to query the Low Byte data
You can TBLDL [7: 0] read 45H



First 07A0h do shift left and LSB is set to 1, on behalf of program memory addresses to query the High Byte data
You can TBLDL [7: 0] read 23H



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13.3. Register Description- System Information Block

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1											
"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition											
Address	**File Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**A-RESET**	**R/W**
1DH	TBLPTRH	TBLW+	TBLW	TBLR+	TBLR	TBLPTR[11]	TBLPTR[10]	TBLPTR[9]	TBLPTR[8]	 0000	-,-,-,- *,*,*,*
1EH	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								0000 0000	*,*,*,*,*,*,*,*
20H	TBLDL	Program Memory Table Latch Low Byte								0000 0000	*,*,*,*,*,*,*,*
5EH	EE_CTRL	EN_TBL	PGM	0	0	0	0	0	0		0,1,1,1,1,1,0,0

Table 13-2 Interrupt Register

TBLPTRH : Table read instruction pointer register High byte

Bit	Name	Description
Bit7	TBLW+	When writing bits <1>, TBDL data write TBLPTR specified address, TBLPTR automatically incremented.
Bit6	TBLW	When writing bits <1>, TBDL data write TBLPTR specified address.
Bit5	TBLR+	When writing bits <1>, TBLPTR specified address read data on TBLDL, TBLPTR automatically incremented.
Bit4	TBLR	When writing bits <1>, TBLPTR specified address read data on TBLDL.
Bit3~0	TBLPTR[11:8]	Table read instruction pointer register High byte

TBLPTRL : Table read instruction pointer register low byte

Bit	Name	Description
Bit7~0	TBLPTR[7:0]	Table read instruction pointer register low byte

Write EEPROM address setting operation:

Using Table Pointer (TBLPTR, TBL PRTL) table read, the look-up table unit BYTE (TBLDL), TBLPTR [11: 0] if an odd number (TBLPTRL [0] = 1) point to Program memory instruction of the High-Byte, TBLPTR [11: 0] if an even number (TBLPTRL [0] = 0) point to Program memory instruction of Low-Byte refer to the following table:

Program memory v.s. Table looking-up structure

	Instruction[15:0]	
PC[10:0]	**Instruction High byte**	**Instruction Low byte**
7FF	**TBLPTR**[11:0]=FFF	**TBLPTR**[11:0]=FFE
…		
2	**TBLPTR**[11:0]=5	**TBLPTR**[11:0]=4
1	**TBLPTR**[11:0]=3	**TBLPTR**[11:0]=2
0	**TBLPTR**[11:0]=1	**TBLPTR**[11:0]=0

TBLDL : Table read instruction data register

Bit	Name	Description
Bit7~0	TBLDL [7:0]	Table read instruction data register

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EE_CTRL : EEPROM Control Register

Bit	Name	Description
Bit7	EN_TBL	Lookup Table Function Enable Control <1> Enable. <0> Disable.
Bit6	PGM	EEPROM Lookup Table Block Selection <1> Lookup function TBLPTRL[11:0] point to Program memory. <0> Lookup function TBLPTRL[11:0] point to INFormation block.

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14. REVISION RECORD

Major differences are stated thereinafter.

Version	Page	Date	Revision Summary
V05	All	2016/03/17	First edition
V06	All	2016/12/10	Add in HY14E10M product model
	16	2016/12/10	Add in the note for the selection of HAO in section 3.1.1
	33~34	2016/12/10	Revised the TMB 及 TB1R[15:0] descriptions in chapter 8

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